Modeling and Control of a Hybrid Modular Multilevel Converter for High-AC/Low-DC Medium-Voltage Applications

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***Abstract*—Hybrid modular multilevel converters (HMMC) have emerged recently as an improvement over conventional MMCs due to their lower submodule capacitor sizing, smaller semiconductor count, and lower losses. HMMCs can achieve such advantages, while still maintaining modularity due to their intelligent use of line-frequency-switching medium-voltage switches in addition to the high-frequency low-voltage switch-based submodules. HMMC open-loop operation and performance are well elaborated in literature, but HMMC closed-loop submodule capacitor (SM-C) voltage control is not yet well demonstrated. Closed-loop balancing for HMMC SM-C is especially challenging as the operating mode changes every half-line cycle, making a unified continuous model and subsequent control development challenging. Furthermore, some HMMCs do not have a circulating current path to exchange energy among different arms/phases. This poses an additional challenge for energy transfer between HMMC SM-C. This article resolves these challenges by first proposing a converter model and then developing new control ideas. Novel methods to balance SM-C using midpoint-voltage and interphase circulating-currents are developed for HMMCs. Additionally, the model is utilized to explain power flows, elaborating on the fundamentals behind much lower SM-C size in HMMC compared to MMCs for the same operation. The developed model and controls are verified extensively on a medium-voltage 20 kW laboratory prototype.**

***Index Terms*—Converter control, converter modeling, hybrid converters, modular multilevel converters (MMCs).**

I. Introduction

MODULAR multilevel converters (MMCs) [1], [2] have gained popularity amongst high/medium voltage industries for use in high-voltage direct-current transmission [3], [4], static-Var compensators [5], [6], and motor drives [7], [8], [9], among others. MMCs are preferred for these applications due to MMC's inherent capability to circumvent the semiconductor rating limitations by allowing series stacking of smaller subconverters, called submodules (SMs). Additionally, the multilevel staircase-ac waveforms generated by MMCs have the advantage of reducing ac side filter size. The MMC modular structure is also preferable for scalability, redundancy, and ease of repair [10], [11], [12]. Despite their advantages, MMCs suffer from a wide array of practical challenges. The cost of MMCs is high due to the large number of semiconductors used. MMC power density is also limited due to the large capacitors required in each SM [13], [14]. These cost and density limitations have motivated research in new modular converters, a few of which are discussed in the following.

Merlin et al. in [15] and [16] combine two-level converters and MMCs to develop the alternate arm converter (AAC). AAC reduces the total switching devices and arm energy requirements but has high *di/dt* for operation except for its optimal modulation ratio or power factor. Three-phase multiplexing arm modular multilevel converter, introduced in [17], can also reduce the arm energy storage requirements and the number of required SMs, however, the topology is only discussed for high-dc/low-ac operation mode or $M \leq 1$. Here, M is the modulation ratio, defined as $M = 2V_{\mathrm{AC}}/V_{\mathrm{DC}}$, where V_{DC} is the dc voltage, and V_{AC} is the ac phase voltage. Additionally, it requires a full-bridge submodule (FB-SM) for $M \leq 1$ operation and has higher losses and device numbers than half-bridge SM (HB-SM) based MMC, which can also be used for $M \leq 1$ operation.

Vozikis et al. [18] propose mixed-cell MMC combining FB-SM and HB-SM with the advantage of slowing the fault currents, allowing for the use of slow and low-cost circuit breakers. Using a combination of FB-SM and HB-SM together for high-ac/low-dc operations has reported balancing challenges for high-ac/low-dc ($M > 1$) operations. As ac voltage is increased, only FB-SMs are inserted to generate negative arm voltage. This results in a difference in operation for HB-SM and FB-SM, which leads to different duty ratios for both within the same arm. With the increase in the ratio of ac and dc voltage, this difference in the duty ratio is further enlarged, leading to capacitor voltage imbalance issues, which can be challenging to control [19], [20]. Modular push–pull pulsewidth modulation (PWM) converter

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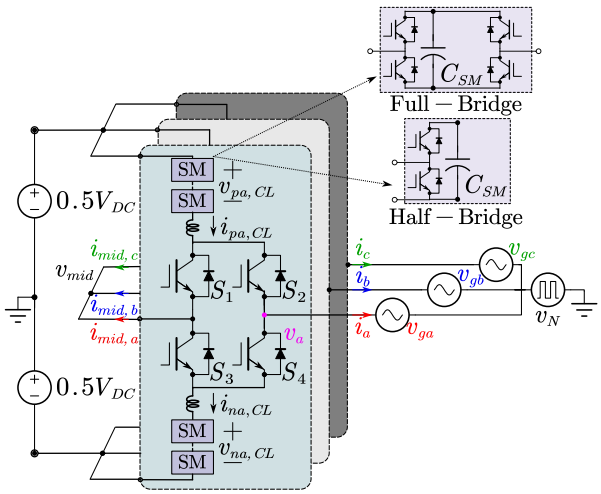

Fig. 1. High modulation-hybrid modular multilevel converter (HM-HMMC), also known as hybrid modular multilevel converter 3 ($HMMC_3$).

(MPC), discussed in [21], is also an excellent alternative for high-ac/low-dc operation due to its ability to operate at half the dc voltage compared to MMC. However, MPC requires a central transformer for its operation, which has its own power-density limitations as discussed later in this section. Moreover, MPC does not provide any critical advantage in terms of efficiency compared to MMC.

Hybrid MMCs (HMMCs) are a new breed of converters inspired by MMCs. Like MMCs, HMMCs use relatively low-voltage fast-switching-devices based SM chain-links (CLs) to generate multilevel waveforms. Here, CL refers to a series of multiple SMs, usually with an arm inductor. However, unlike MMCs, HMMCs use medium voltage (MV) switches, either as standalone or in series combination, referred to as medium voltage switching stacks (MVSSs) [22]. MVSS operates at line frequency and can use low-cost slow-switching devices. Three HMMCs, referred to as $HMMC_1$, $HMMC_2$, and $HMMC_3$, have been proposed earlier [22], [23]. Liu et al. [23] proposed HMMC usage for high-dc/low-ac ($M \leq 1$) operations. Motwani et al. [22] discussed modifications needed in terms of SMs and overall topology for high-ac/low-dc ($M > 1$) operations. Other variations like hybrid modular multilevel rectifiers [24], [25] have also been proposed inspired by HMMCs, primarily motivated toward cost/volume reduction, but they are limited in power flow direction and/or power factor.

Each HMMC has its own advantages, limitations, and recommended operation points. $HMMC_1$ is excellent for $M \leq 1$ application [26]. $HMMC_2$ has the advantage of a lower number of device requirements compared to other HMMCs for most high-M ($M > 1$) cases. $HMMC_3$, shown in Fig. 1, has four MVSSs, connected in a square as shown, with the two CL connected between the MVSS assembly and the dc rails. $HMMC_3$ is an excellent choice for device and volume reduction in *high-M* ($M > 1$) applications, hence, is commonly referred to as high-modulation HMMC (HM-HMMC) [26].

The HM-HMMC is designed primarily for MV applications with high-ac/low-dc voltage operation ($M>1$) like EV charging

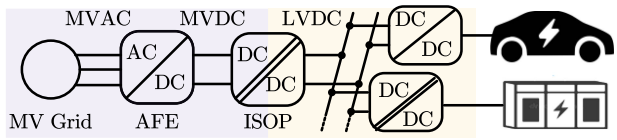

Fig. 2. Converter architecture for MVAC/LVDC conversion.

stations (EVCS), energy storage systems (ESS), and datacenters. The losses for providing such high-power systems operating at LV-DC (400 V to 1 kV) can be greatly reduced by interacting directly with MVAC grid (like 4.16, 13.8, or 30 kV). While low-frequency transformers (LFTs) have been traditionally used to step-down ac voltage for such systems, LFTs are bulky and voluminous, restricting power-density, especially if power-density critical applications like EVCS [27], [28], [29]. Moreover, LFTs are not ideal for pulsating power profile needed and have higher installation costs than other power electronics-based solutions [30].

A converter architecture without a central LFT is explored to connect high-ac (at MVAC grid) to low-dc (at EVCS/ESS/datacenter) in [22], [25], and [31] and is shown also in Fig. 2. It is a nonisolated MVAC-MVDC active-front end (AFE) converter, followed by galvanically isolated MVDC-LVDC converter. The MVDC-LVDC converter here is an input-series-output-parallel converter, with a collection of individual cells, each containing a lower power medium/high-frequency transformer (M/HFT). For this configuration, shown in Fig. 2, higher the intermediate MVDC voltage, higher the step-down ratio of second stage MVDC-LVDC, and higher the number of cells required. Consequently, the MVDC bus voltage is proposed to be decreased. This requires a first stage AFE that can operate for $M > 1$. HM-HMMC is an excellent candidate for such an operation.

The $M > 1$ operations require a negative CL voltage, even in conventional MMCs. Thus, such high-ac/low-dc operations cannot be completed with only HB-SM based MMC which produces unipolar voltage. Thus, MMCs require a few FB-SM in each CL. Additionally, while such high-ac/low-dc operating MMC can also be developed using a mix of FB-SM and HB-SM, such operation can be challenging for control [19], [20]. Consequently, mixed SM based MMC is not recommended for benchmarking, leaving only FB-SM based MMC to be used as benchmark for the analysis. A quantitative comparison was developed in paper [22] and is shown as Table I.

Two cases with changing dc voltage (V_{DC}) for fixed ac voltage (V_{AC}) are presented in Table I. Here, ac side has a phase-to-phase voltage of 13.8 kV RMS. The focus in Table I is on the cases with $M > 1$ and results are presented as per unit (p.u.) rating, comparing them to FB-MMC. As inferred from Table I, $HMMC_3$ is better suited for applications where the $M > 1$. $HMMC_3$ uses 27%–53% lower semiconductor devices, has 2%–38% smaller capacitance requirements, and incurs 53%–67% lower losses across the points under consideration. Moreover, $HMMC_3$ also has soft turn-ON and soft turn-OFF capabilities for MVSSs [22], making it ideal for series stacking devices for MVSSs as well as much lower switching losses.

TABLE I
SUMMARY OF COMPARISON STUDY [22]

13.8kVAC/12kVDC, M=1.88				
Topology	**FB-MMC**	**HMMC$_1$**	**HMMC$_2$**	**HMMC$_3$ (HM-HMMC)**
Device Number	1 p.u.	0.75 p.u.	0.52 p.u.	0.47 p.u.
E_{unit} (kJ/MVA at P.F.=1)	1 p.u.	1.46 p.u.	2.78 p.u.	0.98 p.u.
Device Losses (kW at P.F.=1, Power=1.8MVA)	1 p.u.	0.99 p.u.	0.81 p.u.	0.33 p.u.
13.8kVAC/6kVDC, M=3.76				
Topology	**FB-MMC**	**HMMC$_1$**	**HMMC$_2$**	**HMMC$_3$ (HM-HMMC)**
Device Number	1 p.u.	0.88 p.u.	0.60 p.u.	0.73 p.u.
E_{unit} (kJ/MVA at P.F.=1)	1 p.u.	1.85 p.u.	0.93 p.u.	0.62 p.u.
Device Losses (kW at P.F.=1, Power=1.8MVA)	1 p.u.	1.33 p.u.	0.66 p.u.	0.47 p.u.

Despite promising initial analysis, derivations, and verification proving HM-HMMC as an excellent candidate for $M > 1$ applications [22], HM-HMMC still faces a big challenge. It is not easy to actively control SM capacitor (SM-C) voltage in HM-HMMC. Unlike conventional MMCs, which use circulating currents to balance SM-Cs [32], [33], HM-HMMC has no real circulating current path among the two CLs in the same phase leg. Circulating current is used extensively in conventional MMCs to exchange energy among the two arms of the same phase leg as well as between phases [34], [35], [36]. In the absence of this circulating current, new SM-C balancing controls need to be developed. Development of such controls is made even more difficult by the changing converter operation every half-line cycle. Traditionally, converter controls are developed from converter models and the necessity of new controls in HM-HMMC forces the need for such models. Currently, such a model does not exist.

The continuous time average models of modular converters are also utilized to mathematically explain the power flow among SM-Cs and subsequent SM-C rating variation across different modular converters. Hsieh and Lee [37], [38] used an average mode model to explain such power flow in an MMC. Liu et al. [39] also developed HMMC$_1$ power flow model to explain the smaller SM-C sizing compared to MMC. However, such analysis cannot be directly extended for HM-HMMC because HM-HMMC operation is very different from HMMC$_1$ and MMC. The model may also be used to optimize the HM-HMMC modulation ratio with the objective to minimize the capacitor size like in papers [15], [16], [34], [37], and [38]. However, such analysis is hampered by the nonavailability of a converter model. This article develops this model and fills all the key research gaps. The major contributions of this research are listed as follows.

1) Develop a converter model for HM-HMMC.
2) Use the developed model to explain the lower arm energy requirements for HM-HMMC compared to MMC, arm energy variations with the modulation index (M) and explore M optimizations.
3) Use the developed HM-HMMC model to develop new closed-loop HM-HMMC controls.
4) Extensively experimentally verify developed analysis and controls.

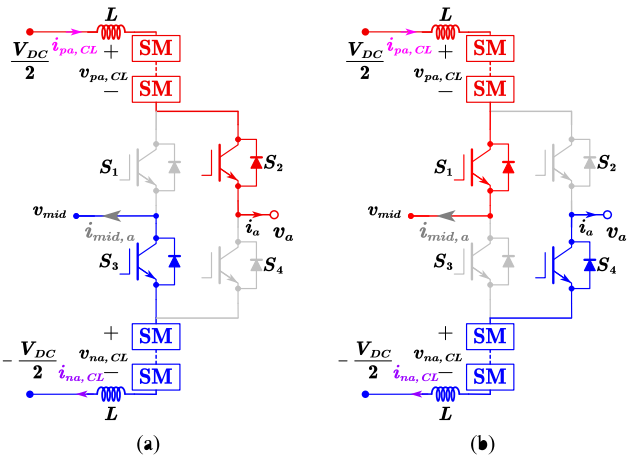

Fig. 3. Operating modes of HM-HMMC for (a) $v_a \geq 0$ and (b) $v_a < 0$.

The rest of this article is divided into five sections. Section II explains the HM-HMMC operation and develops its average model. This section also compares the developed model with that of MMC. Section III develops and explains the SM-C balancing controls to actively regulate SM-C voltage. Section IV demonstrates the developed MV laboratory prototype and presents experimental verifications. Section V concludes this article.

II. HM-HMMC Modeling, Optimization, and Comparison

A. HM-HMMC Topology and Operation

The three-phase HM-HMMC is shown in Fig. 1. As observed, for each phase, four MVSSs are used to interface the midpoint and ac node. The SMs are connected as CL between MVSSs and DC rails. Each CL also comprises an arm inductor, L like MMCs. The mid-points of all three phases are tied together at one point with voltage, $v_{\rm mid}$. The ac side voltage is denoted as $v_{x,\ x\ =\ a,b,c}$, and has current i_x. Each phase of HM-HMMC has two operating states, depending on the magnitude of v_x and converter switches between these two states every half-line cycle in balanced operation. The two states for phase-A are shown in Fig. 3.

The state shown in Fig. 3(a), referred to as the "P" state, is implemented when $v_a \geq 0$. The MVSS S_2 is turned ON here to connect the positive dc rail to the ac through upper CL. This is shown in red. The lower CL is inserted between the midpoint and negative dc rail by turning ON S_3, shown in blue. The operation shown in Fig. 3(b), referred to as the "N" state is used for $v_a < 0$. The MVSS S_4 is on here, shown in blue, to connect the negative dc bus to the ac node through lower CL. The upper arm CL, in this case, is inserted between the midpoint and positive dc rail by turning ON S_1, as shown in red. The commutation between "P" and "N" states does not require any deadtime for MVSS. The upper and lower arm currents are $i_{pa,\rm CL}$ and $i_{na,\rm CL}$, respectively. The CL voltages for the upper and lower arm are $v_{pa,\rm CL}$, and $v_{na,\rm CL}$, respectively. The current from phase leg to the midpoint is $i_{\rm mid,a}$.

As observed from Fig. 1, the ac side voltage, v_x for each phase comprises of a sinusoidal ac voltage, v_{gx} and common-mode/neutral-point voltage v_N, measured between the ac side neutral-point and the mid-point of the dc-link. v_N consists of high-frequency components due to SMs switching actions and a low-frequency component, typically from the third-order harmonic injection in control. If assuming zero third-order harmonic injection in control, and multiple SMs in each CL, v_N can be ignored for the average modeling and control development of HM-HMMC and v_x can be considered a pure sinusoid. It must be highlighted that v_N is different than converter mid-point voltage, v_{mid}. The voltage and current with phase shift, ϕ, are shown in (1). Based on Fig. 3, the upper and lower CL voltages for phase-A can be shown as (2) and (3). For ease of analysis, phase-A would be analyzed from hereon, but the other phases can be analyzed similarly

$$v_a = V_m \sin(\omega t), \quad i_a = I_m \sin(\omega t - \varphi), \tag{1}$$

$$v_{pa,\text{CL}} = \begin{cases} \frac{V_{\text{DC}}}{2} - v_a - L\frac{di_{pa,\text{CL}}}{dt} & 0 \le \omega t < \pi \text{ or } v_a \ge 0 \\ \frac{V_{\text{DC}}}{2} - L\frac{di_{pa,\text{CL}}}{dt} - v_{\text{mid}} & \pi \le \omega t < 2\pi \text{ or } v_a < 0 \end{cases} \tag{2}$$

$$v_{na,\text{CL}} = \begin{cases} \frac{V_{\text{DC}}}{2} - L\frac{di_{na,\text{CL}}}{dt} + v_{\text{mid}} & 0 \le \omega t < \pi \text{ or } v_a \ge 0 \\ \frac{V_{\text{DC}}}{2} + v_a - L\frac{di_{na,\text{CL}}}{dt} & \pi \le \omega t < 2\pi \text{ or } v_a < 0 \end{cases}. \tag{3}$$

V_m and I_m are the ac line-neutral voltage and current amplitudes, respectively. As observed, HM-HMMC CL voltages are dependent on ac voltage polarity, thus resulting in two different definitions for each half of the line cycle. However, to develop a unified converter model, it is preferable to have only one single operation definition per variable. Considering this, (2) and (3) are transformed to represent respective CL voltages as shown in (4). Here, the ac voltage polarity is masked by a new definition, "sgn," which considers the sign of v_a as is shown in (5)

$$\begin{cases} v_{pa,\text{CL}} = \frac{V_{\text{DC}}}{2} - L\frac{di_{pa,\text{CL}}}{dt} - v_{\text{mid}}\frac{(1-\text{sgn})}{2} - v_a\frac{(1+\text{sgn})}{2} \\ v_{na,\text{CL}} = \frac{V_{\text{DC}}}{2} - L\frac{di_{na,\text{CL}}}{dt} + v_{\text{mid}}\frac{(1+\text{sgn})}{2} + v_a\frac{(1-\text{sgn})}{2} \end{cases} \tag{4}$$

$$\text{sgn} = \text{sign}(v_a). \tag{5}$$

One of the critical operation considerations in HM-HMMC is the design of the CL arm current. A trapezoidal current allocation scheme is proposed for use to regulate CL currents in HM-HMMC [23]. The scheme successfully eliminated the dc-split capacitors in HM-HMMC [22] and would be utilized here. HM-HMMC operating waveforms including ac voltage (v_a–v_c), ac current (i_a–i_c), arm voltages of phase A ($v_{pa,\text{CL}}$, $v_{na,\text{CL}}$), arm currents of phase A ($i_{pa,\text{CL}}$, $i_{na,\text{CL}}$), the trapezoidal current expressions for phase-A ($i_{\text{Trap},Pa}$, $i_{\text{Trap},Na}$), and the MVSS blocking voltages ($v_{S1\text{-}4}$) for HM-HMMC operating in nonunity power factor, for $M > 1$ are shown in Fig. 4.

Based on trapezoidal current allocation, the arm current references for the upper and lower arm can be defined as unified arm current equations for the whole line period as shown in (6). Here, $i_{\text{Trap},Pa}$ and $i_{\text{Trap},Na}$ are new mathematical functions developed to assist in obtaining a single definition for each of phase-A CL

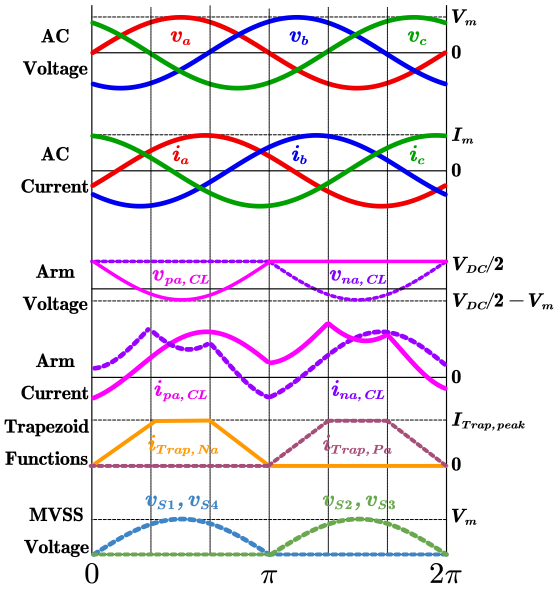

Fig. 4. HM-HMMC operating waveforms.

current across the whole line period. The mathematical definitions for these trapezoidal functions are listed in (7) and (8). Here, trapezoidal current function for each arm represents the dc current contribution of that arm. If the trapezoidal component of current for one arm is zero for a given section, as is for $i_{\text{Trap},Pa}$ during $0 \le \omega t \le \pi$, this arm does not contribute toward maintaining dc current constant for that period. If the trapezoidal component of arm current is rising or falling linearly, as is $i_{\text{Trap},Pa}$ during $\pi \le \omega t < 4\pi/3$, it means that the responsibility to maintain dc current constant is being shared by two arms, with one rising and other falling linearly. Such is the case also with $i_{\text{Trap},Pa}$ during $5\pi/3 \le \omega t < 2\pi$. If the trapezoidal component of arm current equal to $I_{\text{Trap,peak}}$, during a section, that arm handles all the dc current during that section, as is the case with $i_{\text{Trap},Pa}$ during $4\pi/3 \le \omega t < 5\pi/3$. This dc current sharing concept is expanded further in the next section discussing three-phase operation. The peak value for trapezoidal current waveforms is directly related to the dc side current, I_{DC}. I_{DC} can be derived based on power factor, cos(ϕ), V_m, V_{DC}, and I_m as shown in (9)

$$\begin{cases} i_{pa,\text{CL}} = i_{\text{Trap},Pa} + i_a \\ i_{na,\text{CL}} = i_{\text{Trap},Na} - i_a \end{cases} \tag{6}$$

$$i_{\text{Trap},Pa} = \begin{cases} 0 & 0 \le \omega t < \pi \\ 3I_{\text{DC}}((\omega t - \pi)/\pi) & \pi \le \omega t < 4\pi/3 \\ I_{\text{DC}} & 4\pi/3 \le \omega t < 5\pi/3 \\ 3I_{\text{DC}}((2\pi - \omega t)/\pi) & 5\pi/3 \le \omega t < 2\pi \end{cases} \tag{7}$$

$$i_{\text{Trap,Na}} = \begin{cases} 3I_{\text{DC}}((\omega t)/\pi) & 0 \le \omega t < \pi/3 \\ I_{\text{DC}} & \pi/3 \le \omega t < 2\pi/3 \\ 3I_{\text{DC}}((\pi - \omega t)/\pi) & 2\pi/3 \le \omega t < \pi \\ 0 & \pi \le \omega t < 2\pi \end{cases} \tag{8}$$

$$I_{\text{DC}} = I_{\text{Trap,peak}} = \frac{3V_m \cdot I_m \cdot \cos(\varphi)}{2V_{\text{DC}}}. \tag{9}$$

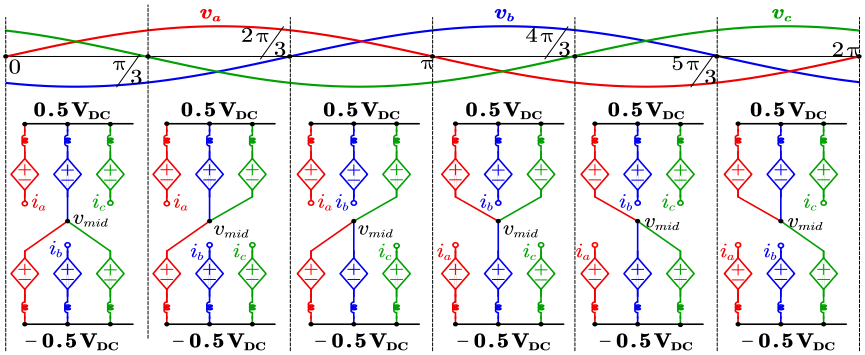

Fig. 5. Three-phase converter configuration.

As observed from the arm voltage waveforms in Fig. 4, if $M > 1$ or $V_m > 0.5V_{\rm DC}$, FBSM are required to generate a negative arm voltage. As observed, assuming v_N relatively close to zero, the blocking voltages are near sinusoidal.

1) HM-HMMC Three-Phase Converter Operation: The HM-HMMC three phases are all connected to the midpoint. However, as observed from Fig. 3, at any given instance, only one of the two CLs per phase is connected to the mid-point, while the other is connected to the ac node. Based on this understanding, the CL connections over a line cycle for HM-HMMC can be developed [23] and are shown in Fig. 5. The arm current allocation for other phases is like phase A, with the $2\pi/3$ phase shift in either direction. Here, as observed, either one or two arms are connected between either dc rail and midpoint, thus enabling the use of trapezoidal current allocation discussed earlier in this section.

2) Development of Model Definitions: With the basic operation established, the HM-HMMC converter model can now be developed. The objective of the model is as follows.

1) To develop an equivalent representation of converter with two ports/sides: side-1 and side-2. Either side can transfer energy to the other side depending on the inverter or rectifier mode of operation.
2) The model also must explain power flow changes with M and power factor (PF).
3) Model should lay the foundation for the development of HM-HMMC closed-loop SM capacitor balancing controls.
4) Since the control of sum and difference of arm capacitor voltages and arm currents are mature and well-understood concepts for MMCs already utilized in industry, a similar sum and difference approach toward the control of HM-HMMCs should be supported by the model for easy industrial adoption.

As the first step, the arm voltages shown in (4) are added and subtracted to develop equations pertinent to the sum and difference of arm voltages, as shown in the following:

$$\begin{cases} v_{pa,\rm CL}+v_{na,\rm CL}=V_{\rm DC}-(v_a-v_{\rm mid})\,\text{sgn}-2L\frac{d(i_{pa,\rm CL}+i_{na,\rm CL})}{2dt} \\ -v_{pa,\rm CL}+\ v_{na,\rm CL}=v_a\ +2L\frac{d(i_{pa,\rm CL}-i_{na,\rm CL})}{2dt}+v_{\rm mid}. \end{cases} \tag{10}$$

The sum and difference of arm current, relating to circulating and load currents are also important control variables in conventional MMCs. To get the equivalent circulating and load current expressions for HM-HMMC, the currents in (6) can also be added and subtracted to generate equations relating the sum and difference of arm currents for phase-A as shown in (11), referred to as $i_{\Sigma a}$ and $i_{\Delta a}$, respectively

$$\begin{cases} i_{\Sigma a}=\frac{i_{pa,\rm CL}+i_{na,\rm CL}}{2}\ =\frac{i_{\rm Trap,Pa}+i_{\rm Trap,Na}}{2} \\ i_{\Delta a}=\frac{i_{pa,\rm CL}-i_{na,\rm CL}}{2}\ =i_a\ +\frac{i_{\rm Trap,Pa}-i_{\rm Trap,Na}}{2} \end{cases}. \tag{11}$$

It can be inferred from (11) that, like MMCs [37], [38], the sum of both arm currents of HM-HMMC, $i_{\Sigma a}$ is proportional to the DC side current. The difference current, $i_{\Delta a}$ for HM-HMMC is also heavily influenced by the ac current, similar to MMCs [37], [38]. However, $i_{\Delta a}$ differs from MMCs in its consideration of additional trapezoidal functions. $i_{\Sigma a}$ and $i_{\Delta a}$ are hence circulating and load current equivalents for HM-HMMC. Based on (10) and (11), now sum and difference equivalent circuit diagrams concerning the arm voltage and arm current can be developed as shown in Fig. 6.

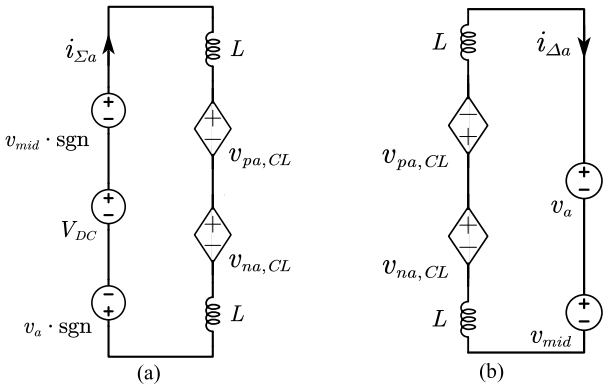

Fig. 6. Equivalent circuit for HM-HMMC with (a) sum of arm voltages and (b) difference of arm voltages.

It can be observed from Fig. 6(a) that the equivalent circuit concerning the sum of arm voltage comprises of all three voltage sources/sinks: dc voltage, ac voltage, and midpoint voltage. This is a sharp contrast from MMC, where such a sum circuit only has a dc voltage [37], [38]. The difference voltage loop is also shown in Fig. 6(b), and it can be established here that the difference of upper and lower arm voltage is related to ac and midpoint

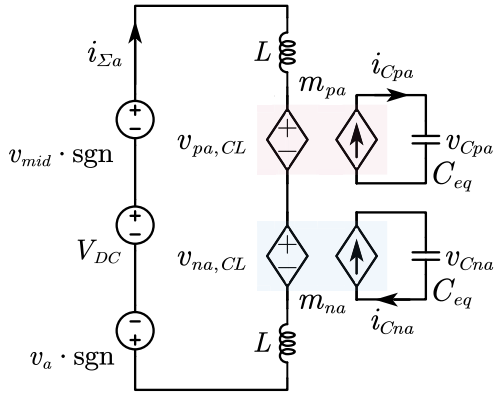

Fig. 7. Extended equivalent circuit for HM-HMMC for the sum of arm voltages.

voltages. This is also unlike MMCs, where mid-point voltage is not decoupled from ac voltage.

While the arm voltages and current sum and difference expressions shown in Fig. 6 are helpful in understanding converter behavior, they do not have explicit capacitor voltage information. Hence, Fig. 6 models cannot be directly used to model the capacitor voltage balancing or develop the related controls. Since one key objective of this model is the capacitor voltage balancing control, a converter model in terms of the sum and difference of capacitor voltages is a necessity. Thus, the model in Fig. 6 needs to be modified accordingly.

Like MMCs, the submodule capacitor voltages and arm voltages for HM-HMMC can be related using the SM capacitor insertion ratio, also called the arm modulation ratio. The insertion ratio governs how many SM capacitor(s) are inserted or bypassed within the arm at any given instant. Fig. 7 highlights this equivalent circuit extension concept for the circuit shown in Fig. 6(a), and a similar extension can be easily established for Fig. 6(b). Table II discusses various definitions necessary to transform the model shown in Fig. 6 into the sum and difference of the capacitor voltage equivalent model. The relevant mathematical expressions are also included.

For HM-HMMC, as observed from Fig. 3 and discussed before, there is no direct circulating current path between the upper and lower CLs. Since circulating current going through the upper and lower arm simultaneously does not exist, a physical variable that is common among both upper and lower CL is required to exchange energy between them. The v_{mid} is one such physical variable common between both upper and lower CL. The midpoint voltage is thus used for SM capacitor voltage balancing between the upper and lower arms.

While v_{mid} is a viable option, as observed from Fig. 3, v_{mid} cannot be directly controlled. Rather v_{mid} is indirectly regulated by changing CL voltages. The CL voltage change in turn is implemented through a change in the arm's insertion ratio. In order to regulate v_{mid}, upper and lower CL insertion ratios are changed by Δm_{pa} and Δm_{na}, from their original insertion ratios, m_{pa}, and m_{na}, respectively.

For deriving Δm_{pa} in terms of v_{mid}, (4) can be used as the base equation, focusing on $v_{pa,\text{CL}}$ term with its definition defined in Table II. Solving (4), the v_{mid} term is taken on the same side as the insertion ratio, m_{pa}. Since the final effective insertion ratio,

TABLE II
VARIABLE DEFINITIONS AND EXPRESSIONS FOR HM-HMMC PHASE-A

Variable	Definition	Relevant Expression
$v_{pa,CL}$	Upper CL voltage assuming v_{mid} is maintained at zero (v_{mid}=0)	$v_{pa,CL} = m_{pa} \cdot v_{Cpa}$
v_{Cpa}	Mean of SM capacitor voltages in upper CL	
m_{pa}	Insertion ratio in upper CL assuming v_{mid}=0	
$v_{na,CL}$	Lower CL voltage assuming v_{mid}=0	$v_{na,CL} = m_{na} \cdot v_{Cna}$
v_{Cna}	Mean of SM capacitor voltages in lower CL	
m_{na}	Insertion ratio in lower CL assuming v_{mid}=0	
Δm_{pa}	Change required in upper CL insertion ratio to account for v_{mid} deviation	$\Delta m_{pa} = \frac{v_{mid}(1-\text{sgn})}{v_{Cpa}}$ derived in (12)
Δm_{na}	Change required in lower CL insertion ratio to account for v_{mid} deviation	$\Delta m_{na} = -\frac{v_{mid}(1+\text{sgn})}{v_{Cna}}$ derived in (13)
M_{pa}	Effective (implemented) insertion ratio for upper CL	$M_{pa} = m_{pa} + \Delta m_{pa}$
M_{na}	Effective (implemented) insertion ratio for lower CL	$M_{na} = m_{na} + \Delta m_{na}$
C	The capacitance of each SM	$C_{eq} = C/N$
N	Number of SMs in each CL	
C_{eq}	Equivalent arm capacitance for each CL	
i_{Cpa}	Current in upper CL equivalent capacitor	$C_{eq}\frac{dv_{Cpa}}{dt} = i_{Cpa}$
i_{Cna}	Current in lower CL equivalent capacitor	$C_{eq}\frac{dv_{Cna}}{dt} = i_{Cna}$
$M_{\Sigma a}$	Effective duty ratio of side-1	$M_{\Sigma a} = M_{pa} + M_{na}$
$M_{\Delta a}$	Effective duty ratio of side-2	$M_{\Delta a} = M_{pa} - M_{na}$
$v_{C\Sigma a}$	The sum of mean capacitor voltages in both CL	$v_{C\Sigma a} = v_{Cpa} + v_{Cna}$
$v_{C\Delta a}$	Difference of mean capacitor voltages in CLs	$v_{C\Delta a} = v_{Cpa} - v_{Cna}$

M_{pa} with equivalent upper arm capacitor voltage, v_{Cpa}, would be utilized in actual converter control, both intermediary insertion ratios, m_{pa}, and Δm_{pa} can be lumped into M_{pa}, as also discussed in Table II. This gives the value of Δm_{pa} in terms of v_{mid}, v_{Cpa} and sgn as shown in (12). A similar analysis can be completed for Δm_{na}, considering (4) again as based with focus on $v_{na,\text{CL}}$ term as shown in (13)

$$\begin{cases} m_{pa} \cdot v_{Cpa} + v_{\text{mid}} \frac{(1-\text{sgn})}{2} = \frac{V_{\text{DC}}}{2} - L\frac{di_{pa,\text{CL}}}{dt} - v_a \frac{(1+\text{sgn})}{2} \\ M_{pa} \cdot v_{Cpa} = \frac{V_{\text{DC}}}{2} - L\frac{di_{pa,\text{CL}}}{dt} - v_a \frac{(1+\text{sgn})}{2} \\ M_{pa} = m_{pa} + \Delta m_{pa} \Rightarrow \Delta m_{pa} \cdot v_{Cpa} = v_{\text{mid}} \frac{(1-\text{sgn})}{2} \end{cases} \tag{12}$$

$$\begin{cases} m_{na} \cdot v_{Cna} - v_{\text{mid}} \frac{(1+\text{sgn})}{2} = \frac{V_{\text{DC}}}{2} - L\frac{di_{na,\text{CL}}}{dt} + v_a \frac{(1-\text{sgn})}{2} \\ M_{na} \cdot v_{Cna} = \frac{V_{\text{DC}}}{2} - L\frac{di_{na,\text{CL}}}{dt} + v_a \frac{(1-\text{sgn})}{2} \\ M_{na} = m_{na} + \Delta m_{na} \Rightarrow \Delta m_{na} \cdot v_{Cna} = -v_{\text{mid}} \frac{(1+\text{sgn})}{2}. \end{cases} \tag{13}$$

B. Equivalent HM-HMMC Model

With the system definitions and equations all established, the final converter model can now be developed. The model as discussed earlier should demonstrate the relationships between sum and difference variables. Here the relevant sum and difference variables are $i_{\Sigma a}$, $i_{\Delta a}$, $v_{c\Sigma a}$, $v_{c\Delta a}$, $M_{\Sigma a}$, and $M_{\Delta a}$. To develop such a model, the terms pertinent to sum of CL voltages, $v_{pa,\mathrm{CL}}$ and $v_{na,\mathrm{CL}}$ in (10) are transformed to desired sum and difference variables with definitions from Table II. Substituting definitions in (10) and (11), the following can be derived:

$$m_{pa}\cdot v_{Cpa}+m_{na}\cdot v_{Cna}-v_{\mathrm{mid}}\cdot \mathrm{sgn} = V_{\mathrm{DC}}\ -v_a\cdot \mathrm{sgn}-2L\frac{di_{\Sigma a}}{dt}. \tag{14}$$

The $v_{\mathrm{mid}}\cdot$sgn still contains the polarity dependency that is undesired. $v_{\mathrm{mid}}\cdot$sgn can thus be replaced by using (12) and (13) in (14) to finally obtain the following:

$$M_{pa}\cdot v_{Cpa}+M_{na}\cdot\ v_{Cna}=V_{\mathrm{DC}}\ -v_a\cdot \mathrm{sgn}-2L\frac{di_{\Sigma a}}{dt}. \tag{15}$$

The Table II variables, $M_{\Sigma a}$, $M_{\Delta a}$, $v_{c\Sigma a}$, and $v_{c\Delta a}$ can be further mathematically manipulated to develop an equivalence to M_{pa}, v_{Cpa}, M_{na}, and v_{Cna} in desired terms of $M_{\Sigma a}$, $M_{\Delta a}$, $i_{\Sigma a}$, $i_{\Delta a}$, $v_{c\Sigma a}$ and $v_{c\Delta a}$ as shown in the following:

$$\frac{M_{\Sigma a}\cdot v_{C\Sigma a}}{2}+\frac{M_{\Delta a}\cdot v_{C\Delta a}}{2}=V_{\mathrm{DC}}\ -v_a\cdot \mathrm{sgn}-2L\frac{di_{\Sigma a}}{dt}. \tag{16}$$

A similar process can be repeated to transform difference of CL voltages in (10) into desired format. Transformation and the final expressions are demonstrated in the following:

$$\begin{cases} -m_{pa}\cdot v_{Cpa}+m_{na}\cdot v_{Cna}-\ v_{\mathrm{mid}}=v_a\ +2L\frac{di_{\Delta a}}{dt} \\ -\frac{M_{\Sigma a}\cdot v_{C\Delta a}}{2}-\ \frac{M_{\Delta a}\cdot v_{\Sigma a}}{2}=v_a\ +2L\frac{di_{\Delta a}}{dt}. \end{cases} \tag{17}$$

The equivalent capacitor currents in upper and lower CL are shown in Fig. 7 and Table II as i_{Cpa} and i_{Cna}, respectively. The two CL currents can further be added and subtracted based on their definition in Table II as shown in (18) to get an expression in desired terms of $v_{c\Sigma a}$ and $v_{c\Delta a}$.

$$\begin{cases} C_S\ \frac{d(v_{Cpa}+v_{Cna})}{dt}=C_S\ \frac{dv_{C\Sigma a}}{dt}=i_{Cpa}\ +i_{Cna} \\ C_S\ \frac{d(v_{Cpa}-v_{Cna})}{dt}=C_S\ \frac{dv_{C\Delta a}}{dt}=i_{Cpa}\ -i_{Cna}. \end{cases} \tag{18}$$

However, (18) still should be modified to get an equation in desired $M_{\Sigma a}$, $M_{\Delta a}$, $i_{\Sigma a}$, and $i_{\Delta a}$, format. Like the arm voltage, arm current and capacitor current can also be related using insertion ratios. Considering the power balance, and effective insertion ratios of M_{pa} and M_{na}, the expression relating i_{Cpa}, $i_{pa,\mathrm{CL}}$, i_{Cna}, and $i_{na,\mathrm{CL}}$ can be derived as shown in the following:

$$i_{Cpa}=M_{pa}\ \cdot i_{pa,\mathrm{CL}},\ \ i_{Cna}=M_{na}\ \cdot i_{na,\mathrm{CL}}. \tag{19}$$

Substituting (19) in (18) to derive the sum of capacitor voltage expression, and plugging values from Table II, the expression can be solved for desired variables as in (20). A similar analysis can be completed for $v_{C\Delta a}$ to convert (18) into (20). The final current expressions can thus be derived

$$\begin{cases} C_S\ \frac{dv_{C\Sigma a}}{dt}=M_{\Sigma a}\ \cdot i_{\Sigma a}+M_{\Delta a}\cdot i_{\Delta a} \\ C_S\ \frac{dv_{C\Delta a}}{dt}=M_{\Sigma a}\ \cdot i_{\Delta a}+M_{\Delta a}\cdot i_{\Sigma a}. \end{cases} \tag{20}$$

With both voltage and current expressions derived: (16), (17), and (20) can be written as system matrix (21). Equation (21) governs the converter behavior

$$\frac{d}{dt}\begin{bmatrix} i_{\Sigma a} \\ i_{\Delta a} \\ v_{c\Sigma a} \\ v_{c\Delta a} \end{bmatrix}=\begin{bmatrix} 0 & 0 & -\frac{M_{\Sigma a}}{4L} & -\frac{M_{\Delta a}}{4L} \\ 0 & 0 & -\frac{M_{\Delta a}}{4L} & -\frac{M_{\Sigma a}}{4L} \\ \frac{M_{\Sigma a}}{C_S} & \frac{M_{\Delta a}}{C_S} & 0 & 0 \\ \frac{M_{\Delta a}}{C_S} & \frac{M_{\Sigma a}}{C_S} & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{\Sigma a} \\ i_{\Delta a} \\ v_{c\Sigma a} \\ v_{c\Delta a} \end{bmatrix} + \begin{bmatrix} \frac{1}{2L} & -\frac{\mathrm{sgn}}{2L} \\ 0 & -\frac{1}{2L} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} V_{\mathrm{DC}} \\ v_a \end{bmatrix}. \tag{21}$$

The singe-phase equivalent circuit based on (21) can now be developed as shown in Fig. 8. On the left is one port, here dc source, V_{DC}, which here can be assumed to send power through the converter. On the right, another port, the ac side, can be considered to receive power. The power flows through the HM-HMMC in the middle. It can be observed that for HM-HMMC, the power not only flows through the CL equivalent capacitors, but also has an additional power path through MVSS, shown in the bottom with green. The power through MVSS can also be observed to be always positive. The additional power flow path through MVSS is useful since the CL capacitors do not have to buffer all the energy between input and output ports, thus reducing their energy storage requirements. This is a key advantage for HM-HMMC compared to MMCs, allowing for lower SM capacitance requirements, as will be extensively discussed in the last section. This allows HM-HMMC to have smaller arm capacitor requirements, as was numerically observed in [22]. The exact magnitude and mathematical expressions of power transferred through the CL are calculated in the next section.

C. Modulation Ratio Optimization

SM capacitors occupy 50% of volume [40], and for some power-dense applications, there can be a huge impetus to optimize for the lowest SM capacitance for a given power rating, especially for industry. M is one of the tools for such optimization and this section explores this idea. The single-phase model discussed in the last section can be easily scaled to a three-phase system by considering two other phases. The power flow through the MVSS, shown in green in Fig. 8, can now be calculated. Based on Fig. 8, the average power flowing through MVSS, $P_{\mathrm{MVSS,avg}}$ as shown in (22) can be derived as a product of its voltage and current. Equation (22) can be further simplified to get an expression as shown in (23)

$$P_{\mathrm{MVSS,avg}}=\frac{2}{\pi}\left(\int_{\theta\ =\ 0}^{\theta=\pi/3} i_{\Sigma a}\cdot V_m\cdot d\theta+\int_{\theta=\pi/3}^{\theta=2\pi/3} i_{\Sigma a}\cdot V_m\cdot d\theta+\int_{\theta=2\pi/3}^{\theta\ =\ \pi} i_{\Sigma a}\cdot V_m\cdot d\theta\right) \tag{22}$$

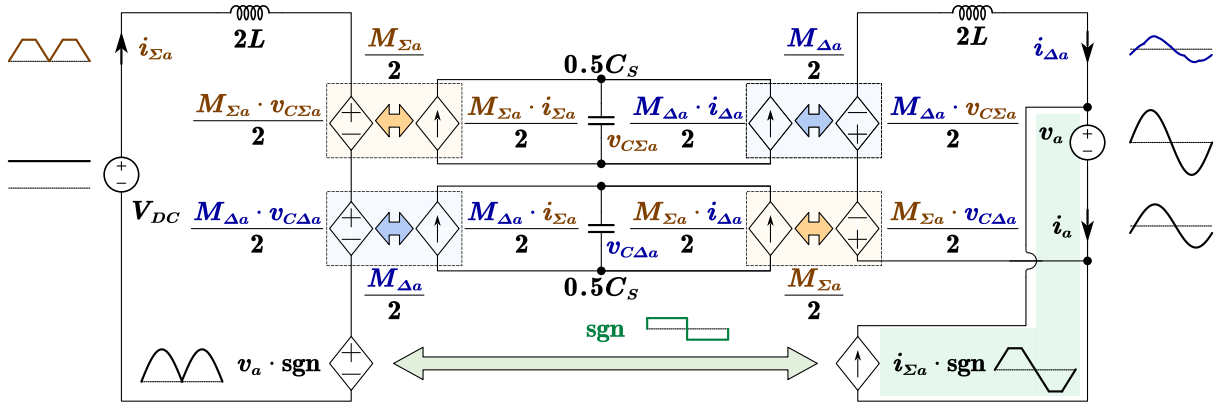

Fig. 8. Final single-phase equivalent circuit for HM-HMMC.

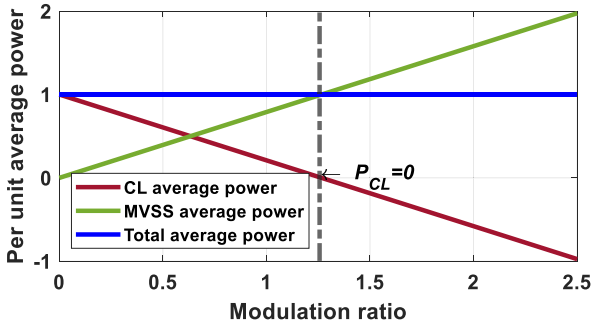

Fig. 9. Ratio of average power for HM-HMMC with modulation ratio change.

$$P_{\text{MVSS,avg}} = \frac{3}{2}\, M \cdot I_m \cdot \cos(\varphi) \cdot V_m \frac{9\sqrt{3}}{2\pi^2} \tag{23}$$

Since the power either flows through MVSS or CL, the power flowing through the CL, P_{CL} can be calculated in the following:

$$\begin{cases} P_{\text{CL}} = \frac{3}{2}\, V_m \cdot I_m \cdot \cos(\varphi) - \frac{3}{2} M \cdot I_m \cdot \cos(\varphi) \cdot V_m \frac{9\sqrt{3}}{2\pi^2} \\ P_{\text{CL}} = \; 3V_m \cdot I_m \cdot \cos(\varphi) \left(\frac{1}{2} - M \cdot \frac{9\sqrt{3}}{4\pi^2}\right). \end{cases} \tag{24}$$

The power flow variation for unity PF among the CL and MVSS is shown in Fig. 9. As observed, for higher modulation ratios, the MVSS carries higher per unit power. However, the power transfer through MVSS exceeds the total delivered power at $M = 1.266$. This $M = 1.266$ is the operating sweet spot for HM-HMMC from arm energy perspective as was also numerically demonstrated in [22]. Beyond this M, the MVSS and CL act against each other, and hence the SM capacitance requirements are seen to be increasing beyond this point [22].

D. Comparison of Power Flow With Conventional MMC

The MMC power flow has been widely studied and reported in literature. This section highlights the similarities and differences between the two models. Fig. 10 demonstrates the MMC power flow model as discussed in [37], [38]. Like the HM-HMC model in Fig. 8, the MMC model in Fig. 10 also has a source on the left, and the load on the right. Similar to HM-HMMC model, the power/energy is delivered through the converter. In Fig. 8, the top equivalent sum capacitor, $v_{c\Sigma a}$ relates to the energy deviation in CL capacitors as the result of total energy delivered from the load to source. The bottom capacitor, $v_{c\Delta a}$ relates to the energy swapping between the upper and lower arm capacitors. Both these changes on equivalent capacitor voltages are reflected as the SM capacitor ripples. However, while HM-HMMC and MMC both use the CL to buffer energy between the input and output; an additional path exists that transfers energy directly from one port to another in HM-HMMC. This additional path, shown as "green" in the bottom of Fig. 8, demonstrates the energy flowing directly through MVSS, without reflecting on CL capacitors. This energy flow reduces the energy flow through CL capacitors, allowing for lower CL capacitance requirements.

III. HM-HMMC Control Development

The model developed in Section II paves the way for the development of the HM-HMMC controls. The complete control architecture is shown in Fig. 11 and comprises of several different control targets and corresponding control implementations. While all controls are critical and elaborated later in this section, two controls are especially unique to HM-HMMC and must be considered thoroughly. These are as follows:

1) Control of energy between upper and lower CLs.
2) Control of energy among different phases.

These two unique controls are important for HM-HMMC because it cannot use conventional circulating current based methods. It must also be highlighted that CL energy is proportional to the charge stored in SM capacitors within CL, which in turn is proportional to the voltage of capacitors. The closed-loop SM balancing controls are developed in the next few sections to regulate the dc value of SM capacitor voltages at their desired reference. The closed-loop balancing controls do not significantly change the arm energy, and hence, the SM capacitor ripples. The controls are discussed in detail in the next few subsections.

A. Control of Energy Between Upper and Lower CLs

The energy exchange between upper and lower CL is governed by $v_{c\Delta a}$ in (20). As observed from (20), the energy difference between upper and lower CL is proportional to $M_{\Sigma a}$, $M_{\Delta a}$, $i_{\Sigma a}$, and $i_{\Delta a}$. Equation (20) can then be further expanded in terms of $M_{\Sigma a}$ and $M_{\Delta a}$ introduced in Table II. $i_{\Sigma a}$ and $i_{\Delta a}$ definitions are adapted from (11), respectively. These definitions,

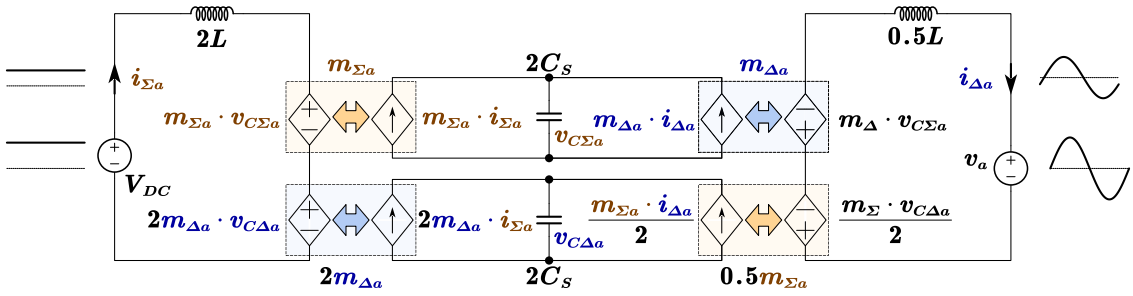

Fig. 10. Modular multilevel converter power flow model.

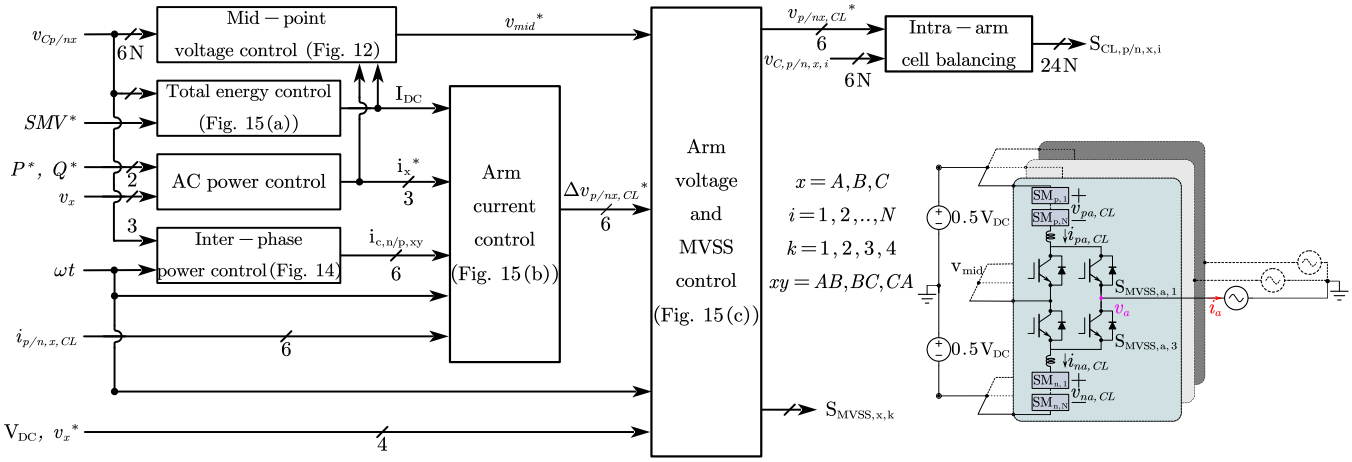

Fig. 11. HM-HMMC overall control.

substituted in (20) result in the following:

$$\frac{C_S}{2}\frac{dv_{C\Delta a}}{dt} = \begin{pmatrix} m_{pa} \\ +m_{na} \\ +\Delta m_{pa} \\ +\Delta m_{na} \end{pmatrix} \cdot \begin{pmatrix} i_a \\ +\frac{i_{\mathrm{Trap},Pa}}{2} \\ -\frac{i_{\mathrm{Trap},Na}}{2} \end{pmatrix} + \begin{pmatrix} m_{pa} \\ -m_{na} \\ +\Delta m_{pa} \\ -\Delta m_{na} \end{pmatrix} \cdot \begin{pmatrix} \frac{i_{\mathrm{Trap},Pa}}{2} \\ +\frac{i_{\mathrm{Trap},Na}}{2} \end{pmatrix}. \tag{25}$$

The absence of circulating current between upper and lower CL inhibits energy exchange through traditional means. Moreover, since the converter interaction with ac and dc side is governed by load or source, it must not be altered. Thus, only mid-point voltage, v_{mid} can be used as an adjustable physical variable that connects both upper and lower CLs. v_{mid} is hence used to enable energy exchange between upper and lower CLs. Considering this, (25) can be simplified in terms of v_{mid} such as only Δm_{pa} and Δm_{na} are considered as shown in (26). Here, m_{pa} and m_{na} are by definition not impacted by/impact v_{mid} as discussed in Table II, hence can be ignored

$$\frac{C_S}{2}\frac{dv_{C\Delta a}}{dt} \propto \begin{pmatrix} \Delta m_{pa} \\ +\Delta m_{na} \end{pmatrix} \cdot \begin{pmatrix} i_a \\ +\frac{i_{\mathrm{Trap},Pa}}{2} \\ -\frac{i_{\mathrm{Trap},Na}}{2} \end{pmatrix} + \begin{pmatrix} \Delta m_{pa} \\ -\Delta m_{na} \end{pmatrix} \cdot \begin{pmatrix} \frac{i_{\mathrm{Trap},Pa}}{2} \\ +\frac{i_{\mathrm{Trap},Na}}{2} \end{pmatrix}. \tag{26}$$

Expanding the Δm_{pa} and Δm_{na} in terms of v_{mid} definitions introduced in Table II yields the following:

$$\frac{C_S}{2}\frac{dv_{C\Delta a}}{dt} \propto \left(\begin{pmatrix} \frac{v_{\mathrm{mid}}(1-\mathrm{sgn})}{2v_{Cpa}} \\ -\frac{v_{\mathrm{mid}}(1+\mathrm{sgn})}{2v_{Cna}} \end{pmatrix} \cdot \begin{pmatrix} i_a \\ +\frac{i_{\mathrm{Trap},Pa}}{2} \\ -\frac{i_{\mathrm{Trap},Na}}{2} \end{pmatrix} + \begin{pmatrix} \frac{v_{\mathrm{mid}}(1-\mathrm{sgn})}{2v_{Cpa}} \\ +\frac{v_{\mathrm{mid}}(1+\mathrm{sgn})}{2v_{Cna}} \end{pmatrix} \cdot \begin{pmatrix} \frac{i_{\mathrm{Trap},Pa}}{2} \\ +\frac{i_{\mathrm{Trap},Na}}{2} \end{pmatrix} \right). \tag{27}$$

Now, the average CL capacitor voltage for the whole phase leg, v_{Ca} can be defined as in (28). Simplifying the expression in (27) using (28), (29) can be developed

$$v_{Ca} = \left(\frac{v_{Cpa} + v_{Cpa}}{2} \right) \tag{28}$$

$$\frac{C_S}{2}\frac{dv_{C\Delta a}}{dt} \propto \left(\begin{pmatrix} \frac{v_{\mathrm{mid}}(1-\mathrm{sgn})}{2v_{Ca}+v_{C\Delta a}} \\ -\frac{v_{\mathrm{mid}}(1+\mathrm{sgn})}{2v_{Ca}-v_{C\Delta a}} \end{pmatrix} \cdot \begin{pmatrix} i_a \\ +\frac{i_{\mathrm{Trap},Pa}}{2} \\ -\frac{i_{\mathrm{Trap},Na}}{2} \end{pmatrix} + \begin{pmatrix} \frac{v_{\mathrm{mid}}(1-\mathrm{sgn})}{2v_{Ca}+v_{C\Delta a}} \\ +\frac{v_{\mathrm{mid}}(1+\mathrm{sgn})}{2v_{Ca}-v_{C\Delta a}} \end{pmatrix} \cdot \begin{pmatrix} \frac{i_{\mathrm{Trap},Pa}}{2} \\ +\frac{i_{\mathrm{Trap},Na}}{2} \end{pmatrix} \right). \tag{29}$$

Assuming the difference of the two capacitor voltages, $v_{c\Delta a}$ is much smaller than the steady state average value, v_{ca}, (30)

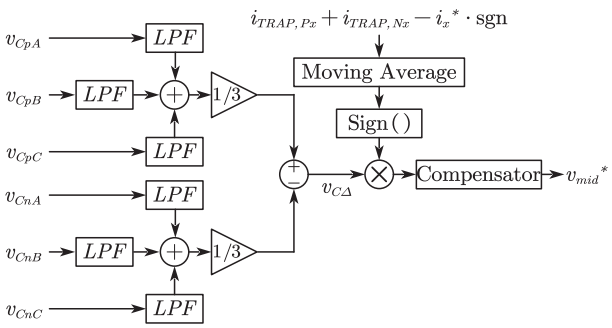

Fig. 12. Arm energy difference control: between upper and lower CL.

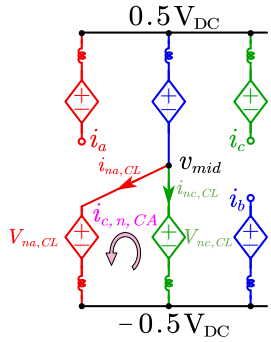

Fig. 13. Arm energy difference control: between different phases.

can be developed, which can be further simplified as (31)

$$\frac{C_S}{2}\frac{dv_{C\Delta a}}{dt} \propto \left(\frac{-v_{\text{mid}}\cdot \text{sgn}}{v_{Ca}}\cdot\begin{pmatrix} i_a \\ +\frac{i_{\text{Trap},Pa}}{2} \\ -\frac{i_{\text{Trap},Na}}{2}\end{pmatrix} + \frac{v_{\text{mid}}}{v_{Ca}}\cdot\begin{pmatrix} \frac{i_{\text{Trap},Pa}}{2} \\ +\frac{i_{\text{Trap},Na}}{2}\end{pmatrix}\right) \tag{30}$$

$$\frac{C_S}{2}\frac{dv_{C\Delta a}}{dt} \propto \frac{v_{\text{mid}}}{v_{Ca}}\left(i_{\text{Trap},Pa} + i_{\text{Trap},Na} - i_a.\text{sgn}\right). \tag{31}$$

It can be observed from (31) that arm energy difference is proportional to, and thus controllable using v_{mid}. The polarity of the "$i_{\text{TRAP},Px} + i_{\text{TRAP},Nx} - i_x\cdot$sgn" term on the right, in (31) is critical. Here, x is a phase. It varies as a function of trapezoidal current and load current, introduced in the last section. These currents in turn are functions of modulation index and power factor. Since energy is a relatively slower control, a moving average value of this term may be considered. Also, since all three phases share the same midpoint, and are assumed symmetrical, the value would be the same for all three phases.

The equivalent control diagram is presented in Fig. 12. Here, as observed, the average capacitor voltage of each arm is passed through a low-pass filter to eliminate the ripples and obtain the dc value. The dc value of SM capacitor voltages in either arm is compared to generate the average SM capacitor voltage difference, $v_{C\Delta}$. This is the energy difference between the upper and lower arm for the whole converter. The resultant $v_{C\Delta}$ is multiplied with the sign of ($i_{\text{TRAP},Px} + i_{\text{TRAP},Px} - i_x\cdot$sgn) followed by a simple compensator. The resultant midpoint voltage reference, $v_{\text{mid}}{}^*$ thus adjusts to balance the capacitor voltage difference between the upper and lower CL voltages of the whole converter. $v_{\text{mid}}{}^*$ is fed to arm voltage control as discussed in Fig. 11.

B. Control of Energy Among Different Phases

The CL energy balancing among the three phases of HM-HMMC is accomplished by using segmented circulating current concept introduced in this section. Unlike conventional MMCs, where the interphase circulating current, exchanging energy among phases can go through both CLs of the two parallel connected phases at all times, HM-HMMC circulating current can only flow among one CL each of the two parallel CLs connected between one dc rail and mid-point for a sixth of the line cycle. The three-phase converter operation was discussed in Section II-B and would be used here. As observed from Fig. 5, two CLs are connected between the mid-point and either dc rail in HM-HMMC at any given instance. A discontinuous segmented circulating current, different for each of the six segments, is used to transfer energy from one CL in one phase to another in another phase.

Considering the three-phase operation shown in Fig. 5 during the first region from 0 to $\pi/3$ as example, two lower CLs in phases A and C are connected between the midpoint and negative 0.5V_{DC} rail. For this region, an equivalent circuit shown in Fig. 13 can be developed. Also, a circulating current, $i_{c,n,CA}$ flowing from phase C to phase A can be considered. This circulating current transfers energy from one CL to other. The arm energy across the two CLs for this region can be calculated as (32). The difference between the two energies assuming a dc circulating current shown in Fig. 13, can be developed as in (33)

$$\begin{cases} E_{na} \propto v_{Cna} \propto \int_0^{\pi/3} v_{na,\text{CL}}\cdot(i_{na,\text{CL}} + i_{\text{cir}}) \\ E_{nc} \propto v_{Cnc} \propto \int_0^{\pi/3} v_{nc,\text{CL}}\cdot(i_{nc,\text{CL}} - i_{\text{cir}}) \end{cases} \tag{32}$$

$$\begin{cases} v_{Cna} - v_{Cnc} \propto \int_0^{\pi/3}\begin{pmatrix} v_{na,\text{CL}}\cdot(i_{na,\text{CL}} + i_{\text{cir}}) \\ -v_{nc,\text{CL}}\cdot(i_{nc,\text{CL}} - i_{\text{cir}})\end{pmatrix} \\ v_{Cna} - v_{Cnc} \propto \int_0^{\pi/3}\begin{pmatrix} v_{na,\text{CL}}\cdot i_{na,\text{CL}} + v_{na,\text{CL}}\cdot i_{\text{cir}} \\ -v_{nc,\text{CL}}\cdot i_{nc,\text{CL}} + v_{nc,\text{CL}}\cdot i_{\text{cir}}\end{pmatrix} \end{cases} \tag{33}$$

Assuming a small voltage drop across the inductor, $v_{na,\text{CL}}$ and $v_{nc,\text{CL}}$ can be considered the same equal to $0.5V_{\text{DC}}$. Also under the trapezoidal current consideration, the integral of $i_{na,\text{CL}}$ is the same as that of $i_{nc,\text{CL}}$ for the region of 0 to $\pi/3$ under analysis. Thus, the two terms $v_{na,\text{CL}}\cdot i_{na}$ and $v_{nc,\text{CL}}\cdot i_{nc,\text{CL}}$ cancel each other. The remainder of the terms are as shown in (34). Here, $v_{na,\text{CL}}$ and $v_{nc,\text{CL}}$ are both positive, leading to further simplification

$$\begin{cases} v_{Cna} - v_{Cnc} \propto \int_0^{\pi/3} v_{na,\text{CL}}\cdot i_{\text{cir}} + v_{nc,\text{CL}}\cdot i_{\text{cir}} \\ v_{Cna} - v_{Cnc} \propto \int_0^{\frac{\pi}{3}} i_{\text{cir}}. \end{cases} \tag{34}$$

As observed, the energy difference, proportional to SM capacitor voltage between the two lower CLs in phases A and C is proportional to dc circulating current. The control implementation is shown in Fig. 14. Similar concepts can be extended to the

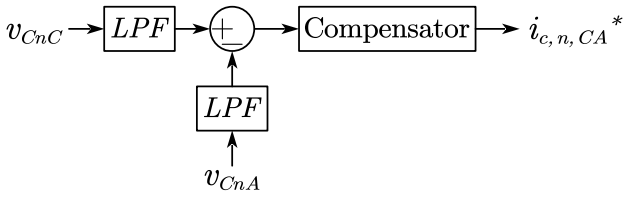

Fig. 14. Interphase circulating current control.

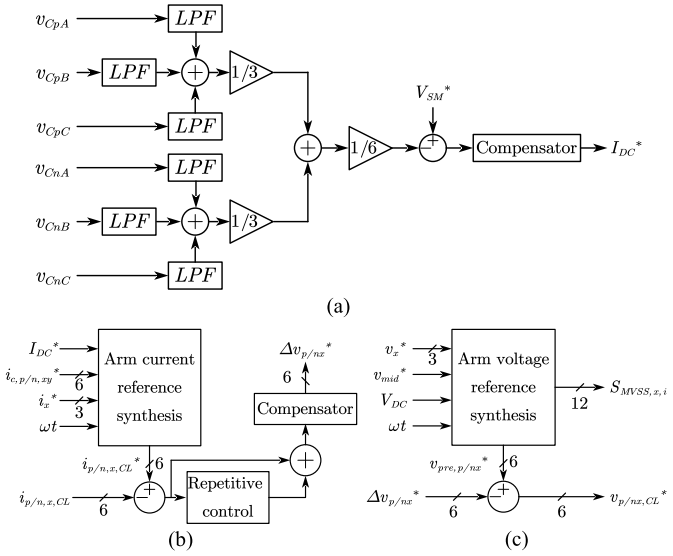

Fig. 15. Critical control loops. (a) Total energy control. (b) Arm current control. (c) Arm voltage control.

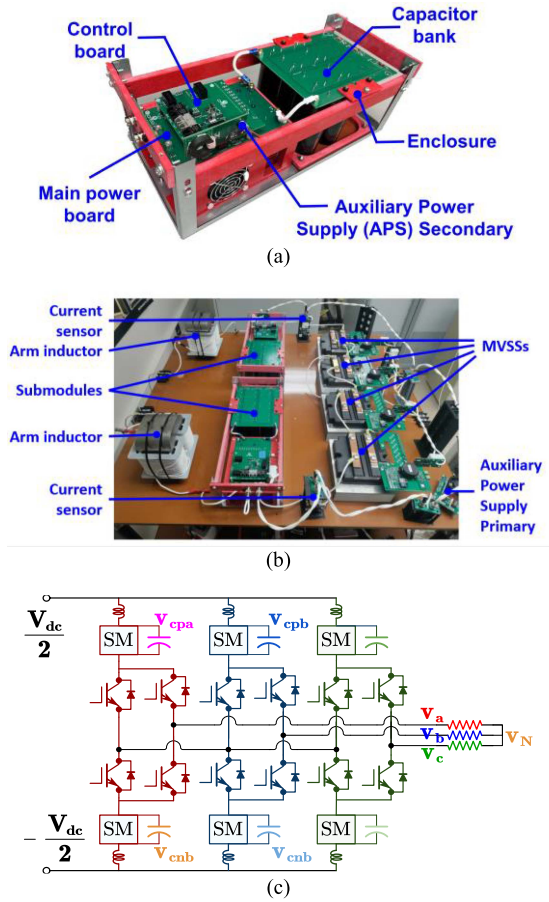

Fig. 16. Experimental test-bench (a) developed submodule (b) one phase-leg of three-phase converter (c) equivalent three-phase circuit diagram.

other sectors and phases, with a simple additional enable signal to only activate the respective control during the respective sixth of line period segments.

C. Other Control Loops

The three other controls different for HM-HMMC compared to conventional converters are shown in Fig. 15. Fig. 15(a) discusses the total energy control. This control is responsible for regulating the total energy stored in all HM-HMMC SM-Cs. As observed, for this control, the SM capacitor voltage reference, $V_{\rm SM}{}^*$ is compared to the average dc-value of SM capacitor voltage across the whole converter, v_c to generate the reference dc current, $I_{\rm DC}{}^*$. Fig. 15(b) discusses the arm current control. For this implementation, the trapezoid-based arm current reference, $i_{p/n,x,{\rm CL}}{}^*$ for each of the six arms for each of the six sections/regions is generated as a function of ac current, $i_x{}^*$, dc current, and interphase circulating current, $i_{c,p/n,xy}{}^*$ in the "arm current reference synthesis" block. The arm current reference is then compared to the measured arm current, $i_{p/n,x,{\rm CL}}$, generating the voltage change required in the arm voltage, $\Delta v_{p/nx}$ to regulate the current as needed. Fig. 15(c) discusses arm voltage control. Like arm current control, a reference synthesis block generates the arm voltage based on ac, $v_x{}^*$, dc, $V_{\rm DC,}$ and mid-point voltages, $v_{\rm mid}$ for each section. The arm voltage generated, $v_{{\rm pre},p/n,x}{}^*$ is then added to the small arm voltage change generated by arm current control, $\Delta v_{p/nx}$ to generate the total arm voltage, $v_{p/nx}$. The two other control loops, ac power control, and intra-arm cell balancing are similar to conventional MMC controls and hence are not elaborated on in this article.

IV. Experimental Verification

A three-phase medium-voltage converter testbench is developed to verify the HM-HMMC controls. The developed SM and one phase of three phase converter rack are shown in Fig. 16(a) and (b), respectively. One submodule is used per arm, with the used converter arrangement and relevant measured parameters as shown in Fig. 16(c). The converter testing parameters are listed in Table III, with the relevant devices and controller information discussed in Table IV.

First, the basic converter operation for the values given in Table III is verified in Fig. 17. As observed from Fig. 17(a), the overall converter operates well with the three phase ac voltage well-regulated and balanced. The SM capacitor voltages are also balanced around a reference value of 500 V. Some additional HM-HMMC operational results are also listed in Fig. 18. The ac currents can be observed to be symmetric in Fig. 18(a), with balanced ac voltages and SM-C voltages shown in Fig. 18(b)

TABLE III
PARAMETERS FOR EXPERIMENTS

Parameter	Notation	Three-Phase
Submodules per arm	N	1
Submodule voltage	V_{SM}	500 V
DC voltage	V_{DC}	800 V
AC voltage L-G pk-pk	$V_{AC,pk\text{-}pk}$	1.2 kV /1.6 kV
AC frequency	f_{AC}	60 Hz
Impedance	Z	50Ω per phase
Deadtime for SM switches	T_{dead}	780 ns
Module capacitance	C	1 mF
Module switching frequency	f_{sw}	20 kHz
Arm inductance	L_{arm}	2 mH

TABLE IV
PARAMETERS FOR EXPERIMENTAL SETUP

Location	Module/Controller	Manufacturer	Type	Rated blocking voltage
MVSS	CM600HG-90H	MITSBUSHI	IGBT	4.5 kV
SM	G3R20MT17K	Genesic	SiC MOSFET	1.7 kV
Controller	TMS320F28379D	TI	DSP	N/A
Controller	Cyclone V	Altera	FPGA	N/A

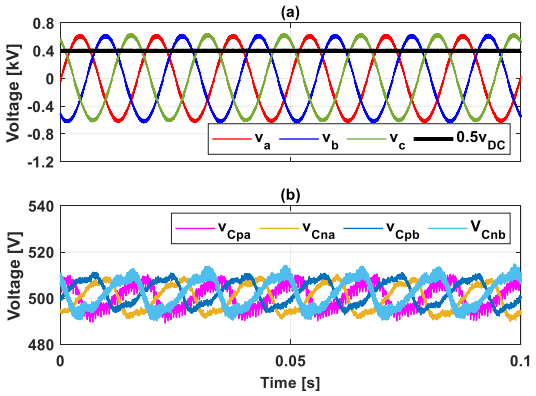

Fig. 17. Experimental HM-HMMC operating as inverter waveforms. (a) AC and DC voltages. (b) SM capacitor voltages for phase-A and phase-B.

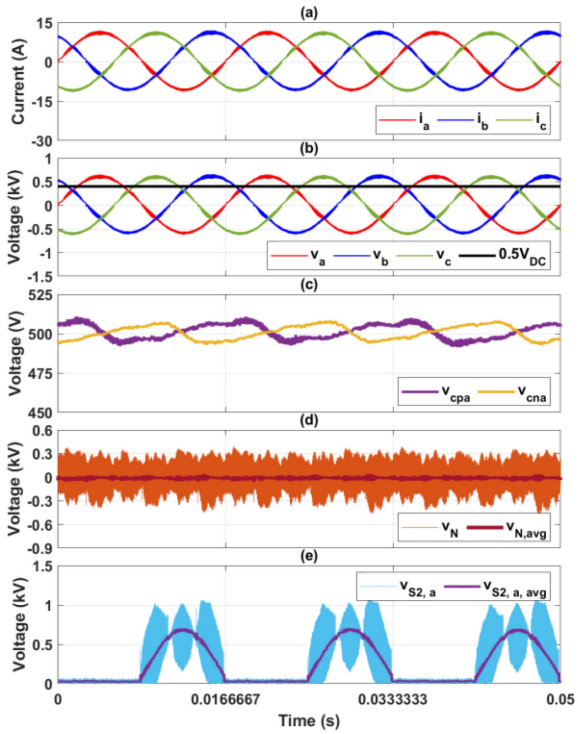

Fig. 18. Experimental operation waveforms for HM-HMMC as inverter. (a) AC currents. (b) AC and DC voltages. (c) SM capacitor voltages. (d) Neutral point voltage. (e) MVSS blocking voltage for S_2 in phase-A.

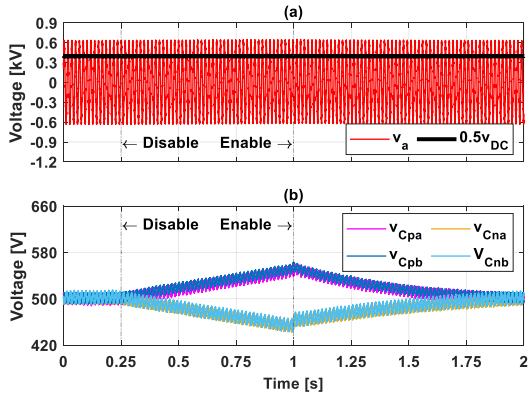

Fig. 19. HM-HMMC operation with and without mid-point balancing control. (a) AC and DC voltages. (b) SM capacitor voltages.

and (c), respectively. The neutral point voltage, v_N can be seen to have high-frequency harmonics in Fig. 18(d), with moving average close to zero. This is very similar to conventional MMC operation [41]. Similar high-frequency harmonics are reflected on MVSS voltage across S_2 in phase-A as shown in Fig. 18(e). The v_N oscillations have a peak less than one SM voltage and hence for more than one SM per arm operation, as is the case with practical MMCs, MVSS blocking voltage would resemble the half-sinusoid, as shown in Fig. 4.

To verify the performance of control in dynamically changing operations, a wide series of tests are performed. First, the upper and lower arm balancing which is governed by midpoint control discussed in Section III-A is disabled and enabled subsequently. The results are presented in Figs. 19 and 20. As observed, from Fig. 19(a), as the balancing is disabled, while the impact on the load side is negligible, it can be observed from Fig. 19(b) that the capacitor voltages do diverge very fast from $t = 0.25$ s to $t = 1$ s. The control is re-enabled at $t = 1$ s and as observed, the capacitor voltages do converge back, verifying the efficacy of control. The zoomed-in waveforms at transition points are also included in Fig. 20(a) and (b), verifying the transition from disable to enable is smooth.

Furthermore, to verify the dynamic performance of the converter, the capacitor voltage reference is changed at $t = 0.25$ seconds from 450 to 550 V. The results are presented in Fig. 21, with zoomed-in results shown in Fig. 22. As observed from Figs. 21(a) and 22(a), the dc side voltage drops slightly to instantaneously provide the power needed to charge the capacitors from 450 to 550 V. The capacitor voltages are also seen to change fast from 450 to 550 V as observed from Fig. 21(b). Fig. 22(b) also demonstrates that the transition is almost instantaneous.

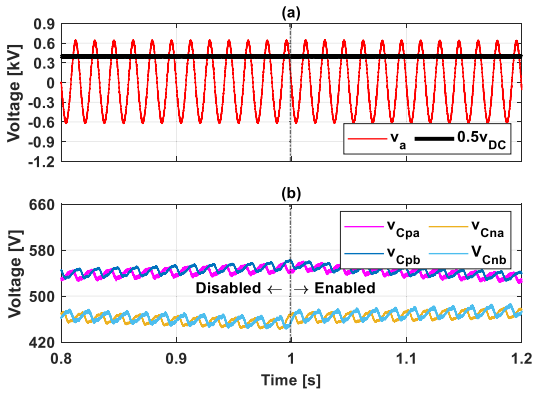

Fig. 20. HM-HMMC operation with and without mid-point balancing control (zoomed in). (a) AC and DC voltages. (b) SM capacitor voltages.

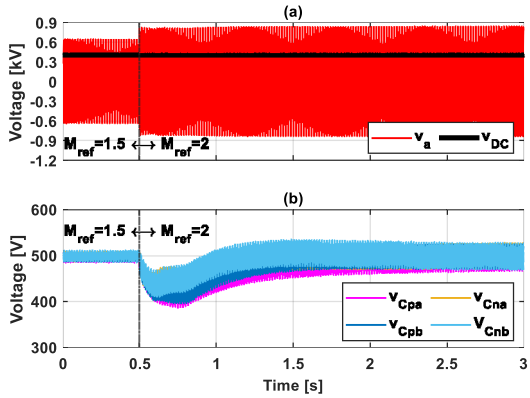

Fig. 23. Dynamic change in modulation ratio reference for HM-HMMC. (a) AC and DC voltages. (b) SM capacitor voltages.

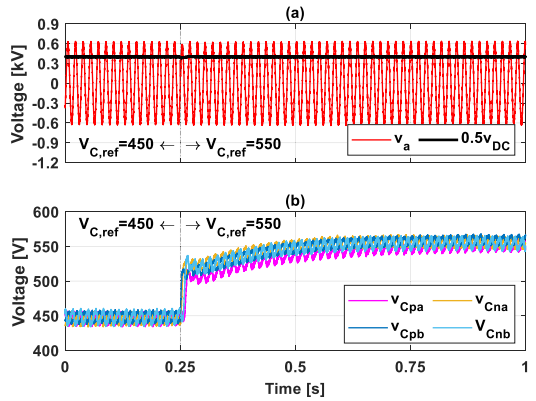

Fig. 21. Dynamic change in capacitor voltage reference for HM-HMMC. (a) AC and DC voltages. (b) SM capacitor voltages.

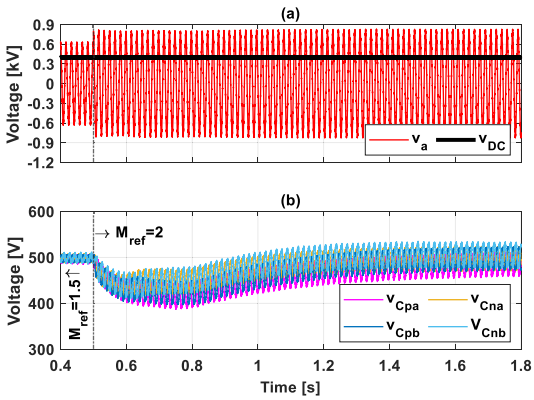

Fig. 24. Dynamic change in modulation ratio reference for HM-HMMC (zoomed in). (a) AC and DC voltages. (b) SM capacitor voltages.

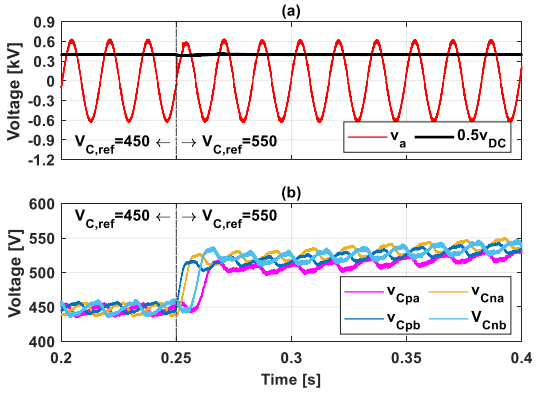

Fig. 22. Dynamic change in capacitor voltage reference for HM-HMMC (zoomed in). (a) AC and DC voltages. (b) SM capacitor voltages.

To further verify the transient performance of the converter, the modulation ratio is changed in the middle of the operation at $t = 0.5$ s from 1.5 to 2. The results are presented in Fig. 23, with zoomed-in results shown in Fig. 24. As observed from Figs. 23(a) and 24(a), the ac voltage easily changes from 600 to 800 V amplitude. The capacitor voltages, while dropping slightly at the transient to provide ac side power at the expense of capacitor energy, easily recovers to the set value in a few line cycles. The capacitor voltage ripple expectedly increases as modulation increases because more energy is now buffered by the capacitors. This can also be corelated to Fig. 9 where CL has to buffer more energy at $M = 2$ than $M = 1.5$.

B. *Rectifier Operation and* V_{mid}

The developed control can also be used for rectifier mode operation, with a minor polarity change. Since all rectifier currents (arm, ac, dc) are opposite to inverter, the v_{mid} control discussed in Fig. 12 needs to be reversed for rectifier implementation. All other controls remain the same. To demonstrate rectifier mode operation, HM-HMMC is tested for the parameters listed in Table V. The results are listed in Fig. 25.

As observed from Fig. 25, the converter can follow the grid voltage, shown in Fig. 25(c), generating current in phase with voltage as seen in Fig. 25(a). The arm currents, shown in Fig. 25(b), can be seen to follow the theoretical waveforms shown in Fig. 4. The balancing controls can also be seen working well, maintaining the capacitor voltages around its set reference of 325 V in Fig. 25(d). The v_{mid}, shown in Fig. 25(e), can be observed to have high frequency harmonics. However, the v_{mid} moving average is close to zero, as is expected for balanced system operation.

TABLE V
PARAMETERS FOR RECTIFIER EXPERIMENTS

Parameter	Notation	Value
Submodules per arm	N	1
Submodule voltage	V_{SM}	325 V
DC voltage	V_{DC}	300 V
AC voltage L-G pk-pk	$V_{AC,pk\text{-}pk}$	850 V
AC frequency	f_{AC}	60 Hz
DC Impedance	Z	18.3 Ω
Module capacitance	C	1 mF
Module switching frequency	f_{sw}	18 kHz
Power factor	PF	1
Arm inductance	L_{arm}	2 mH

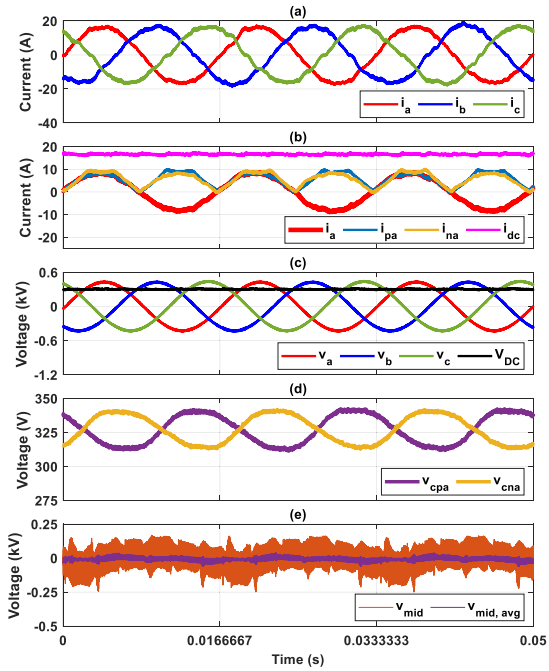

Fig. 25. Experimental operation waveforms for HM-HMMC operating as rectifier. (a) AC currents. (b) CL, AC and DC currents. (c) AC and DC voltages (d). SM capacitor voltages. (e) Mid-point voltage and its moving average.

V. CONCLUSION

This article develops a detailed average model of a hybrid modular converter, HM-HMMC. The model demonstrated the underlying converter power flow characteristics, demonstrating that an additional path of power from input to output through MVSS exists, that allows to transfer power directly between dc and ac sides. The use of additional path leaves CL SM with less power to buffer, resulting in much smaller CL SM capacitors. The proposed model also allows the development of new controls for HM-HMMC operation. The new controls are necessary for HM-HMMC because of the absence of circulating currents, commonly utilized in conventional control methods. The model allows intelligent use of mid-point voltage variation to alleviate the circulating current absence limitation. The proposed model and controls are also developed similar to conventional MMC controls in their common use of sum and difference control. This allows for simple control and permits easy future adoption of HM-HMMC in the industry. The HM-HMMC operation is verified on a medium voltage testbench for a range of operations including enable–disable balancing control and dynamic changes in modulation and capacitor voltage references. The converter and controls perform well for both inverter and rectifier operation in HM-HMMC, balancing capacitors in all operating conditions. Future research efforts would explore the impact of various faults on HM-HMMC and their mitigation methods.

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