Model Predictive-Based Fault-Tolerant and Power Balancing Control for Cascaded H-Bridge Inverter

Xiaogang Wang, *Member, IEEE*, Yongtian Zhao, Ru Yang, *Member, IEEE*, Wei Hu, *Member, IEEE*, and Tao Zou

***Abstract*—This article presents a fault-tolerant control method combined with a novel power balancing approach based on model predictive control for a three-phase cascaded H-bridge inverter. The fault-tolerant control uses redundant voltage vectors and combination voltages to redistribute the output voltage under switch open-fault and short-fault conditions. To overcome the output power imbalance problem of the conventional fault-tolerant control strategy, inter- and inner-phase power balancing approaches are proposed based on novel reward functions. The effects of H-bridge cell faults on the inverter are analyzed in detail, followed by the operational principles of the proposed power balancing and fault-tolerant control methods. Hardware-based experimental results validate the effectiveness of the proposed strategy.**

***Index Terms*—Cascaded H-bridge (CHB) inverter, fault-tolerant control, model predictive control (MPC), power balancing, reward function.**

I. Introduction

DUE to the accelerated exploitation and development of renewable energy sources, power electronic converters are applied to a wider range of scenarios. Multilevel cascade topologies, such as neutral point clamped converter, flying capacitor converter, and cascaded H-bridge (CHB) converter, are used in distributed energy systems because they have increased voltage and power levels [1], [2], [3], [4], [5].

The CHB topology is a mature structure with the advantages of high efficiency, improved power quality, and reduced output voltage variation (dv/dt) [6]. The CHB inverter consists of single-phase H-bridge cells connected in series, and each cell is supplied by an independent dc source with equal voltage to provide the total output voltage to the load without the need for additional transformers, as shown in Fig. 1. In addition, the CHB topology has the advantage of a modular structure and increased fault-tolerant reliability in the event of a failure in the switching devices of the H-bridge cells [6], [7].

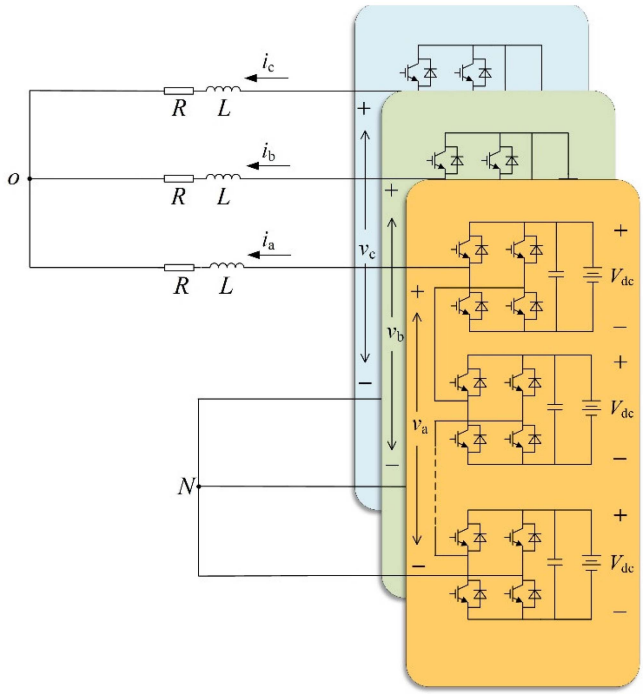


Fig. 1. Topology of a CHB inverter.

In recent years, model predictive control (MPC) has achieved many advantages over the traditional control methods for controlling power electronic converters [8], [9], [10], such as faster dynamic performance, multiobjective control, and simplified design of control loops [11]. MPC method can be divided into continuous control set MPC (CCS-MPC) and finite control set MPC (FCS-MPC) [12]. CCS-MPC produces continuous output and requires a pulsewidth modulation (PWM) generator to generate switching pulses before applied to the power switching devices of the converter [13], [14]. Compared with the CCS-MPC, the FCS-MPC approach considers a discrete model by solving the optimization problem over a finite horizon at each sampling time to predict the future behavior of the system and directly applies the switching signals to the power converter without requiring a PWM generator [15], [16].

The CHB inverter is usually utilized in high-power applications; its reliability is very important. However, as the numbers of

Manuscript received 25 April 2023; revised 7 September 2023 and 29 November 2023; accepted 28 December 2023. Date of publication 1 February 2024; date of current version 20 March 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 52171331, in part by Guangdong Basic and Applied Basic Research Foundation under Grant 2021A1515010616, and in part by the Guangzhou Science and Technology Project under Grant 202102010404. Recommended for publication by Associate Editor A. Kuperman. *(Corresponding author: Tao Zou.)*

Xiaogang Wang, Yongtian Zhao, Ru Yang, and Tao Zou are with the School of Mechanical and Electrical Engineering, Guangzhou University, Guangzhou 510006, China (e-mail: wxg@gzhu.edu.cn; 2112107037@e.gzhu.edu.cn; yangru@gzhu.edu.cn; tzou@gzhu.edu.cn).

Wei Hu is with Lab Center, Guangzhou University, Guangzhou 510006, China (e-mail: pehuwei@gzhu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3349311.

Digital Object Identifier 10.1109/TPEL.2023.3349311

cascaded modules and power switches increase, the possibility of faults in the CHB inverter also increases, leading to a reduction in reliability [17]. When a switch fault occurs, continuous operation of the CHB inverter may lead to unbalanced output voltages, which adversely affect the operation of load [18], [19], [20]. However, sudden interruptions in industrial production are not permitted. Therefore, continuous operation of the CHB converter in fault states is particularly important in industrial production.

The fault-tolerant control methods include three broad categories.

The first method is the direct method based on the faulty H-bridge cell removal [21], [22], [23], [24], [25], [26], [27], [28], [29]. In [21], output voltage symmetry is ensured by cutting off the same number of cells for each phase of the CHB converter during a switch fault. However, this method reduces the converter's output voltage level. In [22], the faulty cell is disconnected and the direct neutral shift method is used to calculate the phase neutral voltage of the CHB converter to achieve normal operation. In [23], a selective harmonic elimination-based fault-tolerant control method is proposed to eliminate the harmonics after a fault, thus ensuring the current quality. In [24], the injection of fundamental frequency zero-sequence voltages enables the CHB converter to maintain continuous operation after fault and achieve state-of-battery balancing of the remaining healthy battery cells. The method proposed in [25] achieves normal operation of the CHB inverter and solves the problem of unequal power generation during fault in large-scale photovoltaic power plants. In [26], the proposed method cannot only maximize the available output voltage but also suppress the backflow of real power effectively under fault conditions. The method in [27] reduces both the amplitude and fundamental harmonic of the injected common-mode voltage to minimize its impact on the load and inverter functionality. In [28], the zero-sequence voltage ensures maximum line voltage availability from the CHB converter, and the power handled by each cell remains equal. A method for power balancing under fault-tolerant control is proposed in [29], but it is not flexible enough.

The second type of method is based on the use of redundant cell. A new replacement cell is added to make up for the missing voltage levels after the faulty cell is directly removed [30], [31], [32]. In [30], by adding an auxiliary cell in series to a three-phase CHB inverter and with the aid of redundant switching states generated in the space vector pulsewidth modulator, a balanced output is achieved with low harmonic distortion. In [32], a new hybrid CHB inverter with a fault-tolerant method is proposed, and a new *X*-H-bridge cell with five-level voltage is mixed in each phase of the CHB inverter to compensate the voltage-level loss. However, the approach increases the size and cost of the converter.

The third type of method performs the fault-tolerant control on the faulty cell under switch fault conditions [33], [34]. A new control method for the CHB inverter operating under switch fault conditions is proposed in [33] to improve the reliability. Fault-tolerant control under the level-shifted PWM approach is proposed in [34]; the neutral point offset method is applied to ensure normal operation of the inverter and improves the power sharing among the H-bridge cells at the same time.

When fault-tolerant control is conducted after H-bridge cell failure, the modulation ratio of healthy H-bridge cells increases. If the power of a cell exceeds the limit, over temperature may cause in the cell [28]. Therefore, it is expected to ensure that the power of each cell is balanced even under the fault condition. At the same time, it is also desirable to ensure power balance among the phases. However, inter- and inner-phase power balancing with the fault-tolerant control is a problem that has not been sufficiently studied in the current literature. Meanwhile, the combination of the fault-tolerant control and MPC is rarely used to control the CHB inverter. The lack of output voltage levels during switch faults leads to unequal inter- and inner-phase power sharing among the H-bridge cells. To address these issues, this article proposes a model predictive-based combined control strategy of power balancing control and fault-tolerant control that can balance the interphase power and inner-phase power with good output current quality when one of the switching devices in each H-bridge cell is open or short circuited. By analyzing the effect of open fault and short fault on the H-bridge cell, the principle of the fault-tolerant control with power balancing function is described in detail. The effectiveness of the proposed method is demonstrated through experimental results.

The rest of this article is organized as follows. Section II presents the circuit configuration of the CHB inverter, and a detailed modeling procedure is provided. Section III analyzes the effect of open fault and short fault on the H-bridge cell. In Section IV, methods for balancing the power inter and inner phases are presented. A fault-tolerant control combining power balancing method is proposed in Section V. Section VI introduces the experimental environment and shows the experimental results. Finally, Section VII concludes this article.

II. Standard FCS-MPC of a CHB Inverter

This section describes a generalized CHB inverter system model and presents an FCS-MPC-based optimal voltage vector selection method.

A. Model of CHB Inverter

Fig. 1 shows that the topology of a three-phase $(2N+1)$-level CHB inverter with N cells per phase feeds a three-phase R–L load. L and R are the inductance and resistance of the load, respectively. V_{dc} is the individual H-bridge dc-link voltage. i_a, i_b, and i_c are the output currents, and v_a, v_b, and v_c are the inverter output voltages. The continuous-time dynamical equations for each phase can be obtained as follows:

$$\frac{di_y}{dt} = \frac{1}{L}\left(v_y + v_{No} - Ri_y\right)(y = a, b, c) \tag{1}$$

and

$$v_y = \sum_{n=1}^{N} v_{yn} = \sum_{n=1}^{N} S_{yn} V_{\mathrm{dc}} \tag{2}$$

where v_y denotes the total inverter output voltage per phase, v_{yn} is the individual H-bridge output voltage, v_{No} is the common-mode voltage, and S_{yn} is the switching function of each H-bridge, which has three states: -1, 0, and 1.

By using the Clark transformation, the model of the CHB inverter in (1) can be transferred into the α--β reference frame

$$\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{L}\left(\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} - R\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}\right) \tag{3}$$

where i_α and i_β are the inverter's output currents, and v_α and v_β are the inverter's output voltages. All the above voltages and currents are in the α–β reference frame.

B. Discrete Model and Prediction

Forward Euler discretization can be applied to (3), and the discrete-time dynamic model can be obtained as

$$\begin{bmatrix} i_\alpha(k+1) \\ i_\beta(k+1) \end{bmatrix} = \frac{T_s}{L}\left(\begin{bmatrix} v_\alpha(k) \\ v_\beta(k) \end{bmatrix} - R\begin{bmatrix} i_\alpha(k) \\ i_\beta(k) \end{bmatrix}\right) + \begin{bmatrix} i_\alpha(k) \\ i_\beta(k) \end{bmatrix} \tag{4}$$

where T_s is the sampling period (also the control cycle), and $T_s = t(k+1)$–$t(k)$. When T_s is small enough, the error introduced by the forward Euler method can be neglected, and (4) is the approximate expression of (3). Equation (4) will be used in the controller to predict the future values of the currents for a given voltage vector. Using an absolute value of the current errors to construct the cost function, which will be as follows:

$$g(k+1) = |i^*_\alpha(k+1) - i_\alpha(k+1)| + \left|i^*_\beta(k+1) - i_\beta(k+1)\right| \tag{5}$$

where $i^*_{\alpha,\beta}(k+1)$ is the predicted reference current vector, and $i^*_{\alpha,\beta}(k+1) \approx i^*_{\alpha,\beta}(k)$ can be assumed for sufficiently small sampling periods.

For a CHB inverter with N cells per phase, the cost function (5) is evaluated for each possible voltage vector, and the ones that minimize it are selected using the following equation:

$$\{v_\alpha, v_\beta\} = \arg(\min(g(k+1))). \tag{6}$$

These selected vectors are redundant to each other; although they achieve the same current-tracking errors, they generate different common-mode voltages for the CHB inverter; therefore, the vector among them that generates the smallest common-mode voltage is determined as the optimal vector and applied to system (4) in normal operation [35]. While in fault conditions, to achieve power balance control and fault-tolerant control, the vector applied to the system is reselected from the optimal vector and its redundant vectors, at the cost of increasing the common-mode voltage, as described in Sections IV and V.

III. Failure Analysis of H-Bridge Cell

This section summarizes the effect of faults on the output voltage by analyzing various switch open faults that occur in the H-bridge cell.

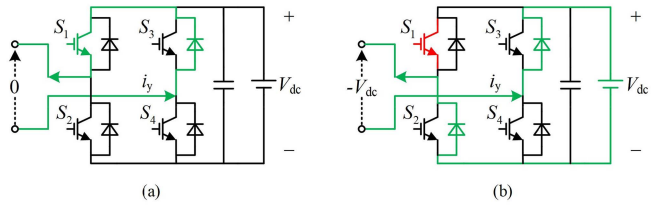


Fig. 2. Example of an open fault occurs in switch S_1 when $v_{yn} = 0$ and i_y>0. (a) Nonopen fault in S_1. (b) Open fault in S_1.

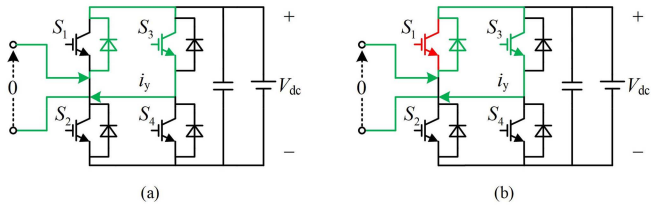


Fig. 3. Example of an open fault occurs in switch S_1 when $v_{yn} = 0$ and i_y<0. (a) Nonopen fault in S_1. (b) Open fault in S_1.

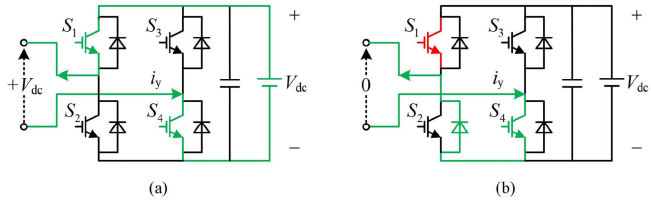


Fig. 4. Example of an open fault occurs in switch S_1 when $v_{yn} = +V_{\rm dc}$ and i_y>0. (a) Nonopen fault in S_1. (b) Open fault in S_1.

A. Open-Fault Analysis

The switching state of each H-bridge cell determines the output voltage level of the CHB inverter. However, if an open fault occurs in a switch in one of the H-bridge cells, the output voltage of the inverter will lose voltage levels, affecting the power quality. Therefore, fault-tolerant control of the CHB inverters is based on the analysis of fault conditions.

Consider an open fault that occurs in switch S_1 of an H-bridge cell. When S_1 and S_3 are ON together, the ideal output voltage $v_{yn} = 0$. If current i_y>0, it will pass through the bypass diode of S_3 to achieve $v_{yn} = 0$, as shown in Fig. 2(a). However, when an open fault occurs in S_1, it is not possible for i_y to conduct through the bypass diode of S_1 when i_y>0. Instead, the bypass diode of S_2 is conducted, resulting in an output voltage of $-V_{\rm dc}$, as shown in Fig. 2(b). If i_y<0 and open fault occurs in S_1, i_y passes through the bypass diode of S_1 to produce a zero output voltage, which does not cause an output voltage error, as shown in Fig. 3.

Consider the case that S_1 and S_4 are ON together and the ideal output voltage $v_{yn} = +V_{\rm dc}$. When i_y>0 and S_1 is open fault, i_y will pass through the bypass diode of S_2 instead of S_1, which causes the actual output voltage $v_{yn} = 0$, as shown in Fig. 4. If i_y<0, i_y passes through the bypass diode of S_1, and the H-bridge cell outputs the ideal voltage $v_{yn} = +V_{\rm dc}$, as shown in Fig. 5.

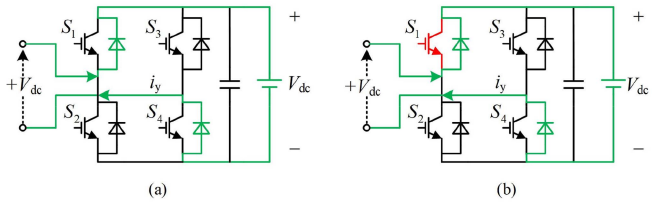


Fig. 5. Example of an open fault occurs in switch S_1 when $v_{yn} = +V_{dc}$ and $i_y<0$. (a) Nonopen fault in S_1. (b) Open fault in S_1.

TABLE I
OPEN-FAULT ANALYSIS OF H-BRIDGE CELL FOR DIFFERENT SWITCHES

Ideal output voltage	Open-fault switch	Current direction	Actual output voltage
$+V_{dc}$	S_1	$i_y>0$	0
	S_4		
0	S_1	$i_y>0$	$-V_{dc}$
	S_4		$-V_{dc}$
	S_2	$i_y<0$	$+V_{dc}$
	S_3		$+V_{dc}$
$-V_{dc}$	S_2	$i_y<0$	0
	S_3		0

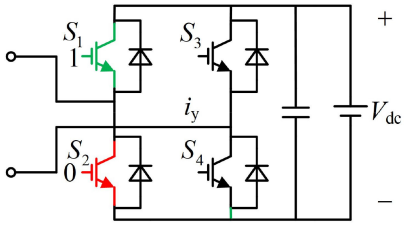


Fig. 6. Example of a short fault occurs in switch S_1 (Green is a short circuit, and red is an open circuit).

The effects of one switch open on the output voltage are summarized in Table I. For an open fault in S_1 or S_4, the error between the ideal output voltage and the actual output voltage is caused only when $i_y>0$. For an open fault in S_2 or S_3, the error between the ideal output voltage and the actual output voltage is caused only when $i_y<0$. A CHB inverter with N cells can generate output voltages in the range of $[-NV_{dc}, NV_{dc}]$ during the fault-free condition. However, if an open fault occurs in S_1 or S_4 of an H-bridge cell and $i_y>0$, the CHB inverter will generate output voltages in the range of $[-NV_{dc}, (N–1)V_{dc}]$; some voltage vectors will be lost.

B. Short-Fault Analysis

When a switch short fault occurs in a CHB cell, the counterpart of the failed switch in the same leg must be permanently turned OFF to avoid the system collapse caused by a sharp short-circuit current generated by the dc power supply. This method is usually implemented by a hardware circuit.

For example, when a short fault occurs in S_1 of an H-bridge cell, S_1 becomes a permanent short-circuit switch and S_2 is forced to be always OFF, which can effectively avoid short circuit of the power supply, as shown in Fig. 6. In this condition, when S_3 is ON and S_4 is OFF, the output voltage of the H-bridge cell is 0. When S_3 is OFF and S_4 is ON, the output voltage is $+V_{dc}$. In the case of a short fault in S_1, the output voltage of the H-bridge cell loses the voltage level $-V_{dc}$. The values of the output voltage for the four fault cases are summarized in Table II.

TABLE II
OUTPUT VALUES OF AN H-BRIDGE CELL FOR DIFFERENT FAULT CASES

Faulty switch	Switch state S_1	S_2	S_3	S_4	Output voltage	Voltage missed
S_1	Short (1)	Open (0)	1	0	0	$-V_{dc}$
			0	1	$+V_{dc}$	
S_2	Open (0)	Short (1)	1	0	$-V_{dc}$	$+V_{dc}$
			0	1	0	
S_3	1	0	Short (1)	Open (0)	0	$+V_{dc}$
	0	1			$-V_{dc}$	
S_4	1	0	Open (0)	Short (1)	$+V_{dc}$	$-V_{dc}$
	0	1			0	

IV. POWER BALANCING CONTROL

In fault conditions, the output power loss occurs in faulty phase due to the improper operation of the faulty H-bridge cell, which is discussed in Section III, causing an inter- and inner-phase imbalance in the CHB inverter. Therefore, this section focuses on the study and control of inter- and inner-phase power balancing of the CHB inverter. First, the average output power over a fundamental period is defined and calculated. Then, the voltage vector and corresponding switching combination are determined based on the proposed reward functions to achieve inter- and inner-phase power balance.

A. Calculation of the Average Output Power of H-Bridge Cell

The instantaneous power p_y at the output of each phase of the CHB inverter can be calculated as

$$\begin{aligned} p_y = v_y i_y &= (S_{y1} + S_{y2} + \cdots + S_{yN}) i_y V_{dc} \\ &= p_{y1} + p_{y2} + \cdots + p_{yN} (y = a, b, c) \end{aligned} \tag{7}$$

where $p_{yn}(y = a,b,c; n = 1–N)$ is the individual instantaneous output power of the H-bridge cell.

The average output power $p_{ave,yn}$ over half a fundamental period can be expressed as

$$\begin{aligned} p_{ave,yn} &= \frac{2}{T} \int_t^{t+\frac{T}{2}} p_{yn} dt \\ &= \frac{V_{dc}}{m} \begin{pmatrix} \frac{1}{T_s} \int_t^{t+T_s} S_{yn} i_y dt \\ + \cdots + \frac{1}{T_s} \int_{t+(k-1)T_s}^{t+kT_s} S_{yn} i_y dt + \cdots \\ + \frac{1}{T_s} \int_{t+(m-1)T_s}^{t+mT_s} S_{yn} i_y dt \end{pmatrix} \\ &= \sum_{k=1}^{m} p_{ave,yn}(k) \end{aligned} \tag{8}$$

where T is the fundamental period, T_s is the control cycle, m is the carrier ratio, and $m = T/(2T_s)$, and $p_{ave,yn}(k)$ is the average power in the kth control cycle. In (8), half of the fundamental period is divided into m control intervals and it is assumed that the average power $p_{ave,yn}(k)$ over each control period is

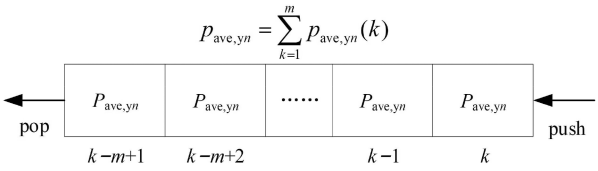


Fig. 7. Real-time average output power calculation.

accumulated and the sum is equal to the average output power $p_{\text{ave},yn}$.

In one control interval, i_y can be approximated as a constant and $p_{\text{ave},yn}(k)$ can be obtained as

$$p_{\text{ave},yn}(k) = \frac{V_{\text{dc}}}{m} i_y(k) \frac{1}{T_s} \int_{t+(k-1)T_s}^{t+kT_s} S_{yn} dt = \frac{V_{\text{dc}}}{m} i_y(k) S_{\text{ave},yn}(k) \tag{9}$$

where $S_{\text{ave},yn}(k)$ is the average switching state during the kth control cycle.

To conveniently calculate the average output power of each H-bridge cell in real time, a queuing operation is performed, as shown in Fig. 7. Using the "first-in-first-out" method, the average power for m control cycles is always stored in the queue. According to (8), $p_{\text{ave},yn}$ for half a fundamental period is obtained by accumulating $S_{\text{ave},yn}(k)$ over m control cycles in the queue.

The total average output power of each phase is

$$p_{\text{ave},y} = p_{\text{ave},y1} + p_{\text{ave},y2} + \cdots + p_{\text{ave},yN}. \tag{10}$$

The average output power of the CHB inverter is

$$p_{\text{ave}} = p_{\text{ave},a} + p_{\text{ave},b} + p_{\text{ave},c}. \tag{11}$$

Calculate the power error of each H-bridge as

$$\Delta p_{\text{ave},yn} = \frac{p_{\text{ave},y}}{N} - p_{\text{ave},yn} (y = a, b, c; n = 1 \sim N) \tag{12}$$

and calculate the power error of each phase as

$$\Delta p_{\text{ave},y} = \frac{p_{\text{ave}}}{3} - p_{\text{ave},y} (y = a, b, c). \tag{13}$$

To achieve power balancing, a reward function based on MPC is proposed and proved in the next. For $\Delta p_{\text{ave},y}$, the following relationship exists:

$$p_{\text{ave},y}(k+1) = p_{\text{ave},y}(k) + \int_{kT_s}^{(k+1)T_s} i_y v_y dt (y = a, b, c) \tag{14}$$

where $p_{\text{ave},y}(k)$ and $p_{\text{ave},y}(k+1)$ are the values of $p_{\text{ave},y}$ at the kth and $(k+1)$th instant, respectively.

The tracking target of $p_{\text{ave},y}$ is

$$\lim_{t \to \infty} p_{\text{ave},y} = \frac{p_{\text{ave}}}{3}. \tag{15}$$

Define the tracking error as

$$\Delta p_{\text{ave},y}(k) = \frac{p_{\text{ave}}}{3} - p_{\text{ave},y}(k). \tag{16}$$

The stability of the proposed reward function for the CHB inverter is investigated with a Lyapunov function with the form as

$$V(k) = \frac{1}{2} [\Delta p_{\text{ave},y}(k)]^2 \geq 0. \tag{17}$$

Then, the derivative of the Lyapunov function with respect to time can be written as

$$\dot{V}(k) = \Delta p_{\text{ave},y}(k) \cdot \Delta \dot{p}_{\text{ave},y}(k). \tag{18}$$

In one control cycle, $p_{\text{ave},y}(k) \approx p_{\text{ave},y}(k+1)$, and (18) can be written as

$$\dot{V}(k) = -\Delta p_{\text{ave},y}(k) i_y v_y. \tag{19}$$

A reward function is proposed as

$$g_{\text{reward}} = \Delta p_{\text{ave},yn}(k) i_y v_y. \tag{20}$$

The Lyapunov function V is positive definite and its derivative is negative definite, so the system is asymptotically stable. Therefore, it requires that $\Delta p_{\text{ave},y}(k) i_y v_y > 0$ to ensure $\dot{V}(k) < 0$ in (19). Assuming that $\Delta p_{\text{ave},y}(k) > 0$, to ensure $\dot{V}(k) < 0$, it is necessary that $i_y v_y > 0$. $i_y v_y$ is expressed as the power in a control cycle. The higher the value of $i_y v_y$, the higher the power output by the H-bridge cell and the faster the error converges. i_y is determined by the output current, so only the output voltage of the inverter can be changed. To obtain better power balance performance, the output voltage v_y should be carefully chosen to achieve maximum g_{reward}.

The reward function can be applied not only to interphase power balancing but also to inner-phase power balancing. As the proof procedure is similar, it will not be repeated.

B. Interphase Power Balancing Control

In Section II, an optimal vector is determined by the cost function to minimize the current-tracking errors in normal operation. The optimal vector has several redundant voltage vectors distributed at different voltage levels and generates different common-mode voltages, which have the same effect on the current-tracking error, as illustrated in Fig. 8. In fault conditions, by redistributing the output voltages using redundant voltage vectors, the output power can be reallocated. In $\alpha\beta$ reference framework, the redundant voltage vector $[\hat{v}_\alpha, \hat{v}_\beta]^{\text{T}}$ can be expressed as

$$\begin{bmatrix} \hat{v}_\alpha \\ \hat{v}_\beta \end{bmatrix} = T_{3s-2s} \left(\begin{bmatrix} \hat{v}_a \\ \hat{v}_b \\ \hat{v}_c \end{bmatrix} + \lambda \begin{bmatrix} V_{\text{dc}} \\ V_{\text{dc}} \\ V_{\text{dc}} \end{bmatrix} \right) \tag{21}$$

where

$$T_{3s-2s} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & \frac{1}{3} \\ 0 & \frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} \end{bmatrix}$$

is the Clark transformation matrix, $[\hat{v}_a, \hat{v}_b, \hat{v}_c]^{\text{T}}$ is the optimal vector with minimum common-mode voltage, λ is an integer coefficient, and the maximum range of λ is $[-N, N]$.

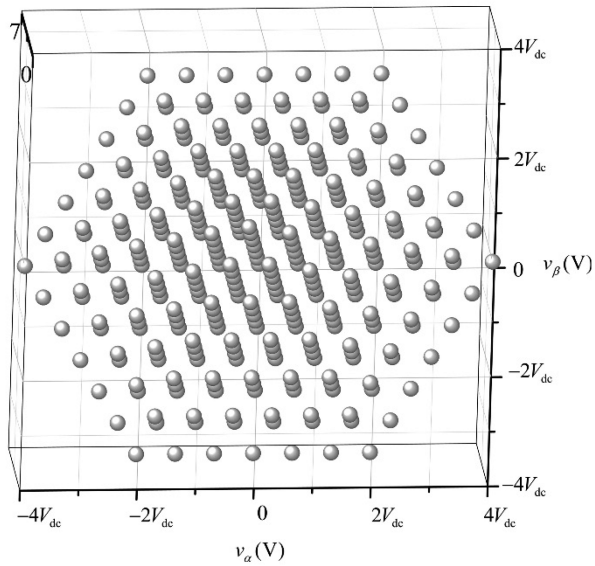


Fig. 8. Voltage vectors with different numbers of redundant voltages in α–β coordinate (N=3).

To maintain interphase power balance, a reward function is proposed and written as

$$g_p(k) = \sum_{y=a,b,c} i_y(k)(\hat{v}_y + \lambda V_{\rm dc})\Delta p_{{\rm ave},y}(k). \quad (22)$$

For different λ, different redundant voltage vectors with the same voltage vectors in the α--β coordinate are calculated in (22), and different results for $g_p(k)$ can be obtained. For instance, when $\Delta p_{{\rm ave},a}(k)>0$ and $i_a(k)>0$, to allocate more power to phase-a, $(\hat{v}_\alpha+\lambda V_{\rm dc})>\hat{v}_\alpha$ should be satisfied as far as possible. When $\Delta p_{{\rm ave},a}(k)<0$ and $i_a(k)>0$, to allocate more power to phase-a, $(\hat{v}_\alpha+\lambda V_{\rm dc})<\hat{v}_\alpha$ should be satisfied as much as possible. The optimal three-phase power balancing output voltage combination is the one that maximizes $g_p(k)$

$$\{\hat{v}'_a, \hat{v}'_b, \hat{v}'_c\} = \arg(\max(g_p(k))). \quad (23)$$

Compared with normal operation, a redundant vector instead of the optimal vector may be selected and applied to the system, resulting in increased common-mode voltage, but it is acceptable for fault conditions.

C. Inner-Phase Power Balancing Control

The voltage vector $\{\hat{v}'_a,\hat{v}'_b,\hat{v}'_c\}$ obtained in (23) determines the voltage level of each phase. For a CHB inverter, each phase has some switching combinations that achieve the same voltage levels; the voltage levels and their corresponding switching combinations of a seven-level CHB inverter are listed in Table III.

The switching combination can be selected by another reward function to achieve inner-phase power balancing, which is written as

$$g_{py}(k) = \sum_{n=1}^{N} i_y(k) S_{yn} V_{\rm dc} \Delta p_{{\rm ave},yn}(k) (y = a, b, c). \quad (24)$$

TABLE III
SWITCHING COMBINATIONS OF SEVEN-LEVEL CHB INVERTER ($N = 3$)

Voltage level	switching combinations
$+3V_{dc}$	(1, 1, 1)
$+2V_{dc}$	(1, 1, 0) (1, 0, 1) (0, 1, 1)
$+V_{dc}$	(1, 0, 0) (0, 1, 0) (0, 0, 1)
0	(0, 0, 0)
$-V_{dc}$	(−1, 0, 0) (0, −1, 0) (0, 0, −1)
$-2V_{dc}$	(−1, −1, 0) (−1, 0, −1) (0, −1, −1)
$-3V_{dc}$	(−1, −1, −1)

By calculating different switching combinations that satisfy the output voltage level, different results for $g_{py}(k)$ can be obtained. For example, when $\Delta p_{{\rm ave},a1}>0$ and $i_a(k)>0$, to allocate more power to the first H-bridge cell in phase-a, $S_{a1}V_{\rm dc}\geq 0$ should be satisfied as far as possible. When $\Delta p_{{\rm ave},a1}<0$ and $i_a(k)>0$, to allocate less power to the first H-bridge cell in phase-a, $S_{a1}V_{\rm dc}\leq 0$ should be satisfied as far as possible. The optimal power balancing switching combination is the one that maximizes $g_{py}(k)$. Therefore, the switching combination corresponding to the maximum $g_{py}(k)$ is selected and applied to the CHB inverter

$$\{S_{y1}, S_{y2}, \ldots, S_{yN}\} = \arg(\max(g_{py}(k))). \quad (25)$$

V. FAULT-TOLERANT CONTROL

This section presents the fault-tolerant control method based on power balancing control by using redundant voltage vectors and inner-phase voltage combinations.

A. Preparations for Fault-Tolerant Control

To achieve redundant control, it is necessary to calculate the number of levels lost for each phase. A matrix is defined to store the switching states of all H-bridges in each phase in the fault state

$$\text{state}_y = \begin{bmatrix} \text{state}_{y11} & \text{state}_{y12} & \text{state}_{y13} & \text{state}_{y14} \\ \text{state}_{y21} & \text{state}_{y22} & \text{state}_{y23} & \text{state}_{y24} \\ \vdots & \vdots & \vdots & \vdots \\ \text{state}_{yN1} & \text{state}_{yN2} & \text{state}_{yN3} & \text{state}_{yN4} \end{bmatrix}. \quad (26)$$

If an open fault occurs in a certain switch of a certain H-bridge cell, the corresponding switching state is recorded as 1. Similarly, if a short fault occurs, the switching state is recorded as 2, and if the switch operates normally, the switching state is recorded as 0.

If an open fault occurs in S_1 or S_4 of the H-bridge cell, it will cause a loss of the positive voltage levels in the CHB inverter, which can be written as

$$V_{\text{open\_lost}+y} = \sum_{n=1}^{N} (\text{state}_{yn1}+\text{state}_{yn4}) V_{\rm dc} (y = a, b, c). \quad (27)$$

If an open fault occurs in S_2 or S_3 of the H-bridge cell, it will cause a loss of the negative voltage levels in the CHB inverter,

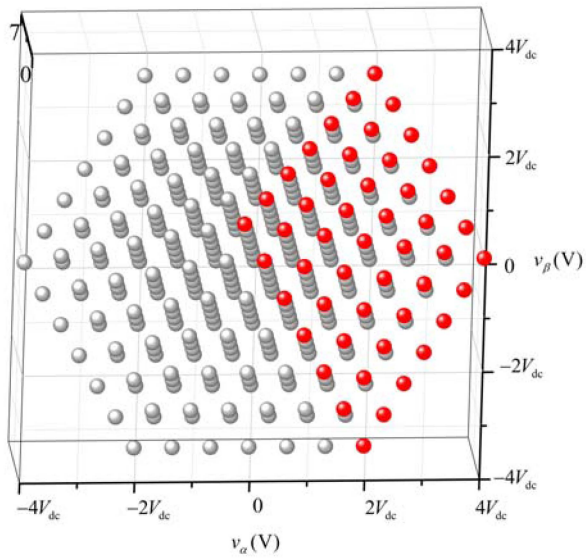


Fig. 9. Voltage vectors with different numbers of redundant voltages in α–β coordinate when the CHB inverter only generates voltages in the range of $[-3V_{\rm dc}, 2V_{\rm dc}]$ (red points are the lost voltage vectors, N=3).

which can be obtained as follows:

$$V_{\text{open\_lost}-y} = \sum_{n=1}^{N} (\text{state}_{yn2}+\text{state}_{yn3})V_{\rm dc}(y = a, b, c). \quad (28)$$

If a short fault occurs in S_2 or S_3 of the H-bridge cell, it will cause a loss of the positive voltage levels in the CHB inverter, which is expressed as

$$V_{\text{short\_lost}+y} = \frac{1}{2}\sum_{n=1}^{N} (\text{state}_{yn2}+\text{state}_{yn3})V_{\rm dc}(y = a, b, c). \quad (29)$$

If a short fault occurs in S_1 or S_4 of the H-bridge cell, it will cause a loss of the negative voltage levels in the CHB inverter, which can be expressed as

$$V_{\text{short\_lost}-y} = \frac{1}{2}\sum_{n=1}^{N} (\text{state}_{yn1}+\text{state}_{yn4})V_{\rm dc}(y = a, b, c). \quad (30)$$

B. Interphase Voltage Redistribution in Switch Failure

For a seven-level CHB inverter, when $i_a>0$ and a switch open fault occurs in S_1 or S_4 of only one of the H-bridge cells, or when $i_a>0$ and a switch short fault occurs in S_2 or S_3 of only one of the H-bridge cells, the inverter only generates output voltages in the range of $[-3V_{\rm dc}, 2V_{\rm dc}]$ in phase-a. In this case, the output voltages can be replaced by the redundant voltage vectors, and some of the edge voltage vectors will be lost, as shown in Fig. 9. For example, if the CHB inverter needs to generate the output voltage combination $[3V_{\rm dc}, -2V_{\rm dc}, -V_{\rm dc}]$ and phase-a of the inverter only generates an output voltage in the range of $[-3V_{\rm dc}, 2V_{\rm dc}]$, the vector $[3V_{\rm dc}, -2V_{\rm dc}, -V_{\rm dc}]$ can be replaced by the redundant voltage vector $[2V_{\rm dc}, -3V_{\rm dc}, -2V_{\rm dc}]$ to overcome the limitation of the output voltage caused by the fault.

To ensure that the output performance of the CHB inverter can be maintained during the fault, the priority of fault-tolerant control is set higher than that of interphase power balancing control. The redundant voltage vectors $\hat{v}_y(k)+\lambda V_{\rm dc}$ selected by (22) to balance the interphase power should be constrained in the case of fault-tolerant control.

The positive voltage-level loss due to a switch open fault occurs only if $i_y>0$ and the negative voltage-level loss caused by a switch open fault occurs only if $i_y<0$. Therefore, when S_1 or S_4 has an open fault and $i_y>0$ or S_2 or S_3 has a short fault, $\hat{v}_y(k)+\lambda V_{\rm dc}<NV_{\rm dc}-V_{\text{open\_lost}+y}-V_{\text{short\_lost}+y}$ needs to be satisfied. While for $i_y\le 0$, $\hat{v}_y(k)+\lambda V_{\rm dc}<NV_{\rm dc}-V_{\text{short\_lost}+y}$ needs to be satisfied. Similarly, when S_2 or S_3 has an open fault and $i_y<0$ or S_1 or S_4 has a short fault, $\hat{v}_y(k)+\lambda V_{\rm dc}>-NV_{\rm dc}+V_{\text{open\_lost}-y}+V_{\text{short\_lost}-y}$ needs to be satisfied. While for $i_y\ge 0$, $\hat{v}_y(k)+\lambda V_{\rm dc}>-NV_{\rm dc}+V_{\text{short\_lost}-y}$ needs to be satisfied. If $\hat{v}_y(k)+\lambda V_{\rm dc}$ does not satisfy the above conditions, rewrite (22) as

$$g_p(k) = \sum_{y=a,b,c} i_y(k)(\hat{v}_y + \lambda V_{\rm dc})\Delta p_{\text{ave},y}(k) - g_{\max} \quad (31)$$

where $g_{\max}$ is a constant and satisfies $|\sum_{y=a,b,c} i_y(k)(\hat{v}_y + \lambda V_{\rm dc})\Delta p_{\text{ave},y}(k)| << g_{\max}$. Since the optimal output voltage combination $\{\hat{v}'_a,\hat{v}'_b,\hat{v}'_c\}$ must maximize $g_p(k)$, the redundant vectors are not considered if they do not satisfy the fault-tolerant control condition. Subtracting $g_{\max}$ from (22) can exclude these redundant vectors in the power balancing control. This allows a normal output range to be maintained and a small interphase power-sharing error to be guaranteed in the event of a switch fault.

C. Inner-Phase Voltage Redistribution in Switch Failure

Compared with the conventional modulation methods, MPC has a high flexibility in controlling the switching states. If a faulty H-bridge cell can only generate $-V_{\rm dc}$ and 0, the whole phase of the CHB inverter can only generate output voltages in the range of $[-NV_{\rm dc}, (N-1)V_{\rm dc}]$. Interphase voltage redistribution using redundant voltages allows the faulty phase to generate a voltage that is within the permissible range. When $(N-1)V_{\rm dc}$ is to be generated, a switching state producing an output voltage of 0 is applied to the faulty switch of the H-bridge cell, while the switching states producing an output voltage of $+V_{\rm dc}$ are applied to other H-bridge cells.

Similarly, the fault-tolerant control must have a higher priority than that of inner-phase power balancing control. Therefore, the selection of switching combinations is also constrained.

If there is a faulty H-bridge cell in the CHB inverter, the output voltage of the faulty cell must be limited in the inner-phase power balancing control. There are four cases.

Case (1): If an open fault occurs in S_1 or S_4, State_{yn1} or State_{yn4} is 1, the output voltage level $V_{\rm dc}$ is lost at $i_y>0$.

Case (2): If a short fault occurs in S_2 or S_3, State_{yn2} or State_{yn3} is 2, the output voltage level $V_{\rm dc}$ is lost.

Case (3): If an open fault occurs in S_2 or S_3, State_{yn2} or State_{yn3} is 1, the output voltage level $-V_{\rm dc}$ is lost at $i_y<0$.

TABLE IV
MAIN PARAMETERS

Symbol	Description	Value
N	Number of cells in each phase	3
V_{dc}	Dc voltage of each H-bridge cell	12 V
I_m	Nominal output line current (amplitude)	4 A
f	Fundamental frequency	50 Hz
R	Filter resistance	10 Ω
L	Filter inductance	1 mH
f_s	Sampling frequency (control frequency)	10 kHz

Case (4): If a short fault occurs in S_1 or S_4, State$_{yn1}$ or State$_{yn4}$ is 2, the output voltage level $-V_{dc}$ is lost.

Therefore, when selecting the switching combination with the optimal inner-phase power balancing, for case (1) or (2) and $S_{yn}V_{dc} = V_{dc}$ in the voltage combination, or for case (3) or (4) and $S_{yn}V_{dc} = -V_{dc}$ in the voltage combination, (24) must be rewritten as

$$g_{py}(k) = \sum_{n=1}^{N} i_y(k) S_{yn} V_{dc} \Delta p_{ave,yn}(k) - g_{pmax}(y = a, b, c) \tag{32}$$

where g_{pmax} is a positive constant and satisfies $|\sum_{n=1}^{N} i_y(k) S_{yn} V_{dc} \Delta p_{ave,yn}(k)| << g_{pmax}$. Subtracting g_{pmax} from (24) can limit the switching state of the faulty H-bridge cell, allowing the fault-tolerant control to take priority over the inner-phase power balancing control.

When the ideal output voltage is 0, and when an open fault occurs in S_1 or S_3, or a short fault occurs in S_2 or S_4, S_2 or S_4 is conducted to generate the output voltage of 0. When an open fault occurs in S_2 or S_4, or a short fault occurs in S_1 or S_3, S_1 or S_3 is conducted to generate the output voltage of 0.

VI. EXPERIMENTAL RESULTS

To validate the performance of the proposed fault-tolerant control and power balancing control strategies, hardware experiments are conducted based on a three-phase seven-level CHB inverter. The proposed fault-tolerant and power balancing control algorithms are implemented in the rapid control prototype. The main parameters are listed in Table IV. And the photo of the experimental platform is shown in Fig. 10.

A. Case I: Single-Cell Fault

In this case, the switch S_1 of the first H-bridge cell in phase-a is open during the fault condition. Figs. 11–13 show the output waveforms of the CHB inverter in the case of power balancing control, and Figs. 14–16 give the output waveforms in the case of without power balancing control. The amplitude of the reference current is set to 4 A. It can be seen from the left image of Fig. 11(a) that the output voltage of each phase has seven levels in the normal operation, and the currents in the left image of Fig. 11(b) track the reference and have a total harmonic distortion (THD) of 2.59%. Comparing the left image of Fig. 12(a) with the left image of Fig. 15(a), and the left image of Fig. 13(a) with the left image of Fig. 16(a), the output powers of the H-bridge cells in phase-a, as well as the three-phase output

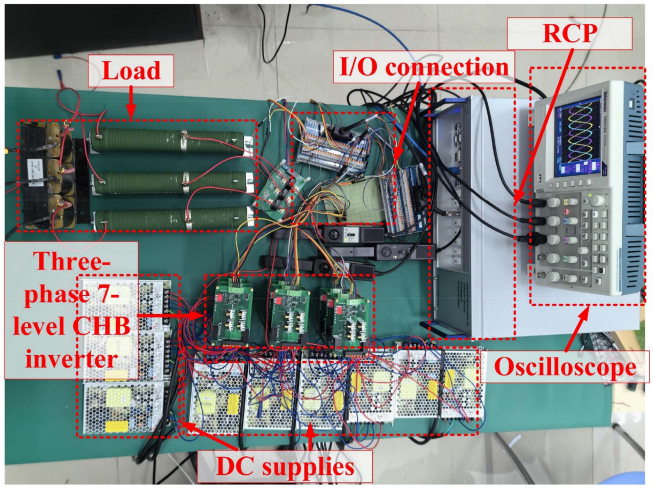


Fig. 10. Photograph of the experimental platform.

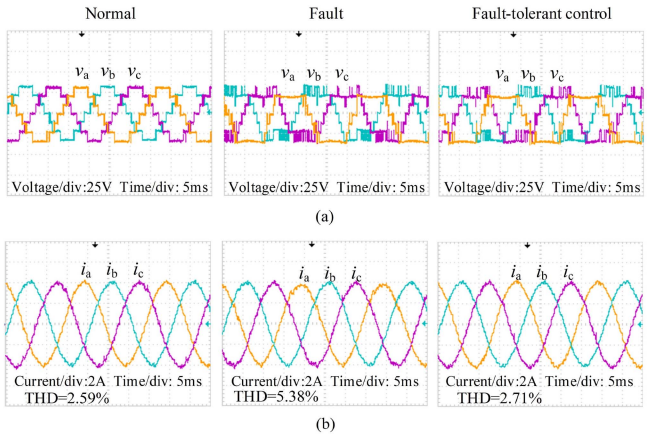


Fig. 11. Waveforms of the three-phase CHB inverter under power balancing control in case I. (a) Three-phase output voltages. (b) Three-phase currents.

powers, are maintained balance in normal condition under power balancing control.

During the fault condition, phase-a cannot generate the output voltage level of $+V_{dc}$ due to the open fault in S_1 of the first H-bridge cell, as shown in the middle and right images of Fig. 17. The inability to generate the required voltage level will affect the amplitude and quality of the currents. The amplitude of the currents decreases to about 3.6 A and the THDs of the currents are 5.74% under the fault condition, as shown in the middle image of Fig. 14(b). Without power balancing control, the output powers of the H-bridge cells in phase-a are unbalanced due to the loss of voltage level, as shown in the middle image of Fig. 15(a) and the middle image of Fig. 16(a). Moreover, there are losses of voltage levels in the output voltage of phase-a, resulting in a lack of output power in phase-a, as shown in the middle image of Fig. 15(b) and the middle image of Fig. 16(b). When using power balancing control under the fault condition, as shown in the middle image of Fig. 11(b), the THDs of the currents are 5.38%. As shown in the middle image of Fig. 12(a) and the middle image of Fig. 13(a), the output power of each cell in phase-a converges as much as possible when the power of the

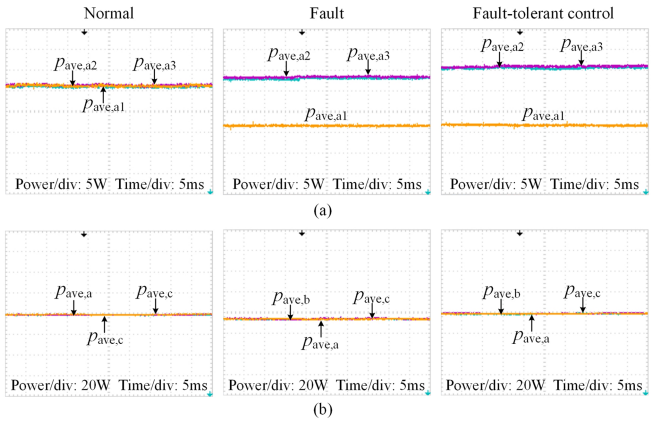


Fig. 12. Output powers under power balancing control in case I. (a) Output powers of H-bridge cells in phase-a. (b) Three-phase output powers.

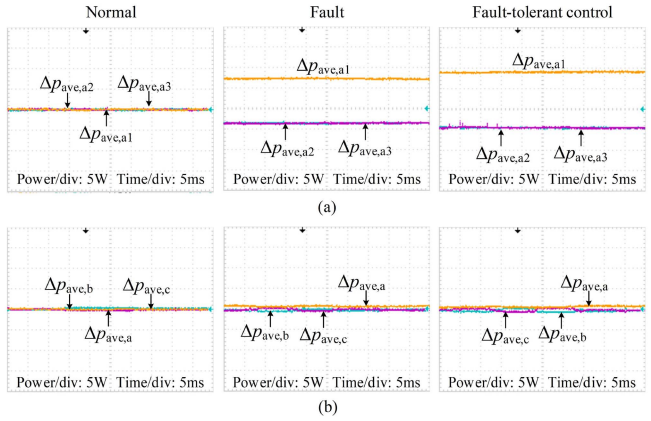


Fig. 13. Output power errors under power balancing control in case I. (a) Output power errors of H-bridge cells in phase-a. (b) Three-phase output power errors.

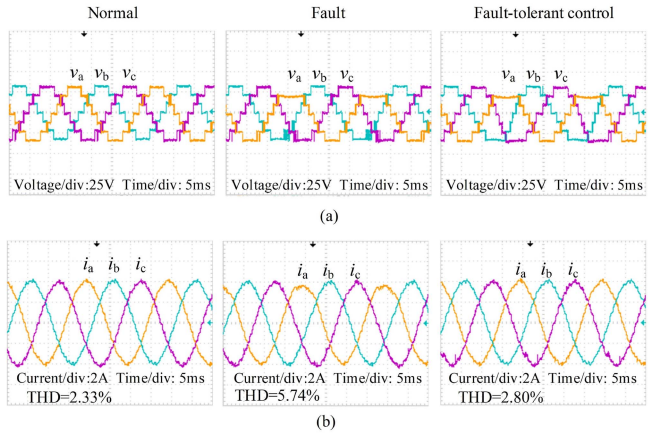


Fig. 14. Waveforms of three-phase CHB inverter without power balancing control in case I. (a) Three-phase output voltages. (b) Three-phase currents.

first cell in phase-a reaches its maximum value. To maintain the normal output power of phase-a, the second and third cells in phase-a handle more power at this time. It is noted that the interphase power balancing control has a higher priority than the inner-phase power balancing control, and there are limited

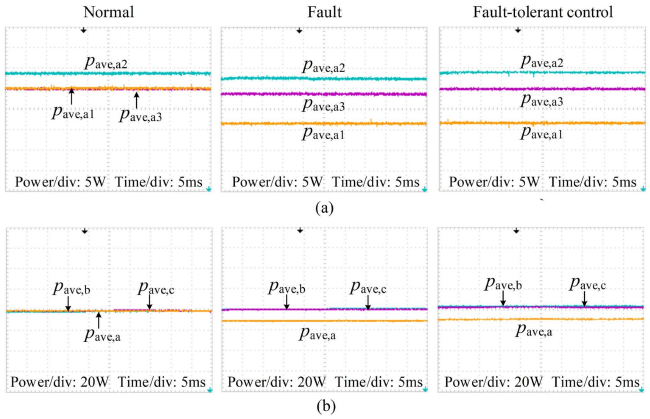


Fig. 15. Output powers without power balancing control in case I. (a) Output powers of H-bridge cells in phase-a. (b) Three-phase output powers.

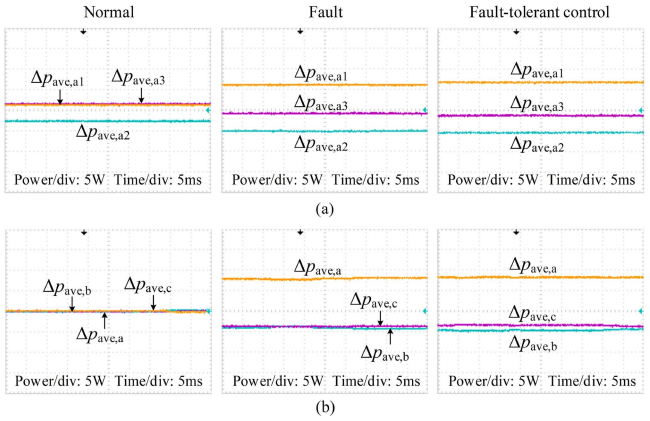


Fig. 16. Output power errors without power balancing control in case I. (a) Output power errors of H-bridge cells in phase-a. (b) Three-phase output power errors.

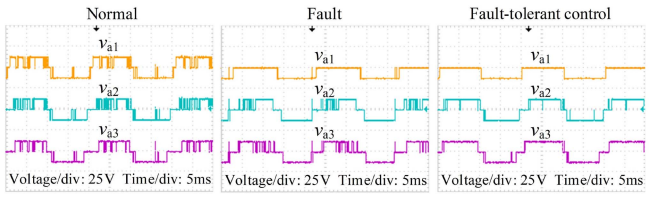


Fig. 17. Output voltage of each cell in phase-a under fault-tolerant control and power balancing control in case I.

switching combinations available to achieve inner-phase power balance in phase-a; therefore, the power error of the first H-bridge cell in phase-a ($p_{\mathrm{ave},a1}$) is large, but $p_{\mathrm{ave},a2}$ and $p_{\mathrm{ave},a3}$ are converged. Moreover, the phase power errors of the inverter are minimized as much as possible, as shown in the middle image of Fig. 12(b) and the middle image of Fig. 13(b). Comparing the middle images of Fig. 12 with the middle images of Fig. 15, and the middle images of Fig. 13 with the middle images of Fig. 16, under the fault condition, the proposed power balancing algorithms converge inner-phase and interphase powers as much as possible and the proposed interphase and inner-phase power balancing methods are proved to be effective.

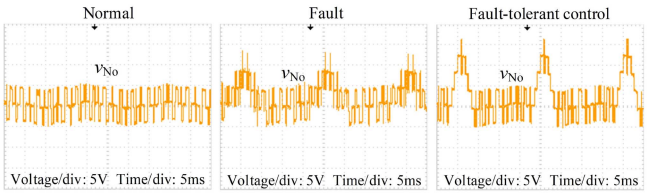


Fig. 18. Common-mode voltage of the CHB inverter under fault-tolerant control and power balancing control in case I.

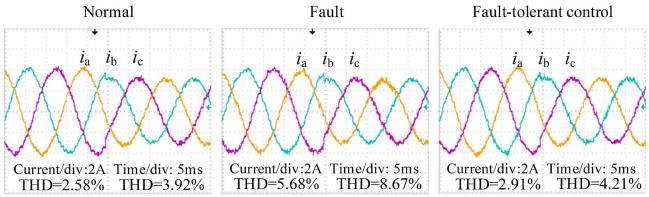


Fig. 19. Dynamic responses of the inverter's output currents under power balancing control in case I.

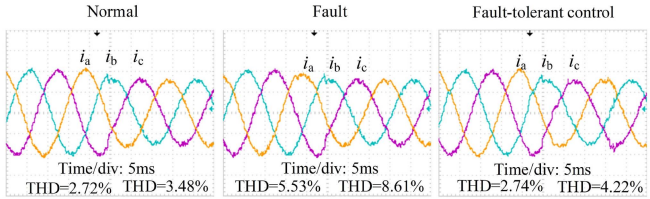


Fig. 20. Dynamic responses of the inverter's output currents without power balancing control in case I.

Under the fault-tolerant control condition, the power balancing control continues to operate to ensure that the faulty phase can recover the voltage level within a certain range. In this way, the output current amplitude can also be recovered. As shown in the right image of Fig. 11(b) and the right image of Fig. 14(b), the amplitudes of the currents in phase-*a* are recovered to the reference value, and the THDs of the currents are 2.71%. Meanwhile, the interphase and inner-phase power balancing methods are still valid, which can be seen from the waveforms in the right images of Fig. 12 and the right images of Fig. 13.

When the fault lasts, phase-*a* is unable to output the desired voltage, and the redundant vectors are used to achieve interphase power balance control during the fault condition and achieve interphase power balance control as well as fault-tolerant control in fault-tolerant control condition, resulting in a larger common-mode voltage, as shown in Fig. 18.

To investigate the transient performance of the proposed scheme, the amplitude of the reference current is abruptly changed from 4 to 3 A. During the fault condition, the switch S_1 of the first H-bridge cell in phase-*a* is open, and phase-*a* cannot generate the output voltage level of $+V_{\rm dc}$. During the fault-tolerant control condition, the proposed fault-tolerant control method executes. The dynamic responses of the current with and without power balancing control are shown in Fig. 19 and Fig. 20, respectively. The currents are able to quickly follow the reference current.

TABLE V
SUMMARY OF EXPERIMENTAL RESULTS OF SINGLE-CELL OPEN FAULT

	With power balancing control			Without power balancing control		
Operation	Normal	Fault	Fault tolerant	Normal	Fault	Fault tolerant
Current THD	2.59%	5.38%	2.71%	2.33%	5.74%	2.80%
Maximum inner-phase power error of phase-a (W)	0.2	7.2	9.2	2.8	5.2	6.7
Maximum inter phase power error (W)	0.3	0.8	1.0	0.5	7.9	8.2

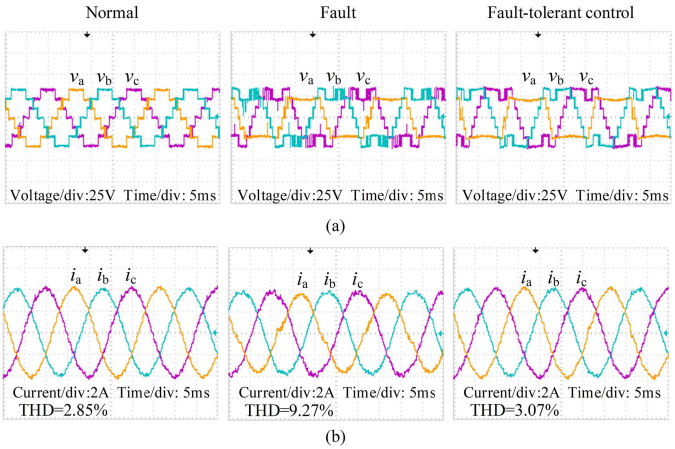


Fig. 21. Waveforms of three-phase CHB inverter under power balancing control in case II. (a) Three-phase output voltages. (b) Three-phase currents.

According to Figs. 11–16, a summary of the experimental results of single-cell fault is given in Table V; it can be seen that the combination of power balancing control and fault-tolerant control can achieve good power balancing performance.

B. Case II: Double-Cell Fault

This is a more extreme case. Under the fault condition, the switch S_3 in the first H-bridge cell of phase-*a* is open, and phase-*a* cannot generate the output voltage level of $-V_{\rm dc}$. At the same time, the switch S_2 in the second H-bridge cell of phase-*a* is shorted, and phase-*a* cannot generate the output voltage level of $+V_{\rm dc}$. The inability to generate the required voltage levels will affect the amplitude and quality of the currents. Figs. 21–23 show the output waveforms of the CHB inverter in the case of power balancing control, and Figs. 24–26 give the output waveforms in the case of no power balancing control. The current amplitudes decrease to about 3.6 A and the THDs of the currents are 9.27% under the fault condition, as shown in the middle image of Fig. 21(b). The powers of the H-bridge cells of phase-*a* are unbalanced due to the faults, as shown in the middle image

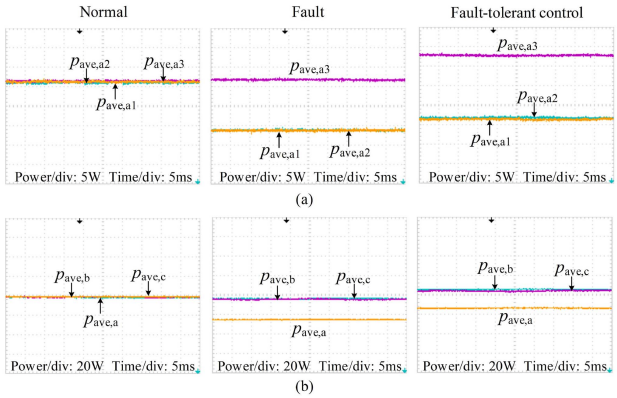


Fig. 22. Output powers under power balancing control in case II. (a) Output powers of H-bridge cells in phase-*a*. (b) Three-phase output powers.

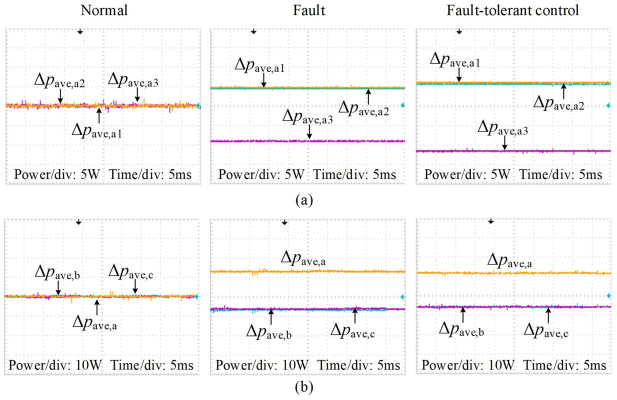


Fig. 23. Output power errors under power balancing control in case II. (a) Output power errors of H-bridge cells in phase-*a*. (b) Three-phase output power errors.

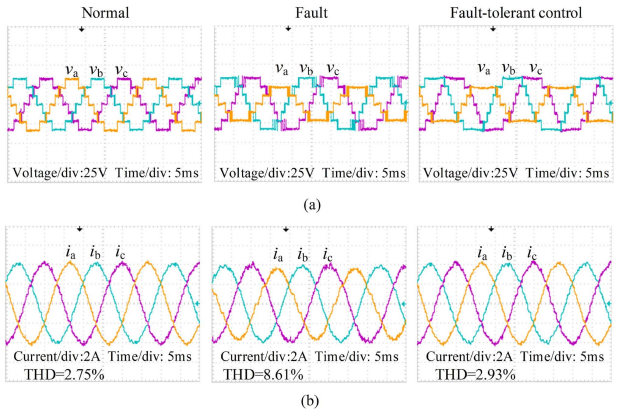


Fig. 24. Waveforms of three-phase CHB inverter without power balancing control in case II. (a) Three-phase output voltages. (b) Three-phase currents.

of Fig. 22(a) and the middle image of Fig. 23(a). Moreover, there are losses of voltage levels in the output voltage of phase-*a*, resulting in a lack of output power handled by phase-*a*, as shown in the middle image of Fig. 22(b) and the middle image of Fig. 23(b).

Under the fault condition, because the output voltage of phase-*a* is limited due to the failures of the first and second cells,

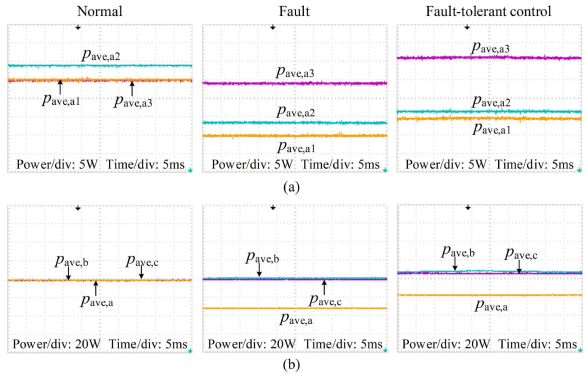


Fig. 25. Output powers under fault-tolerant control without power balancing control in case II. (a) Output powers of H-bridge cells in phase-*a*. (b) Three-phase output powers.

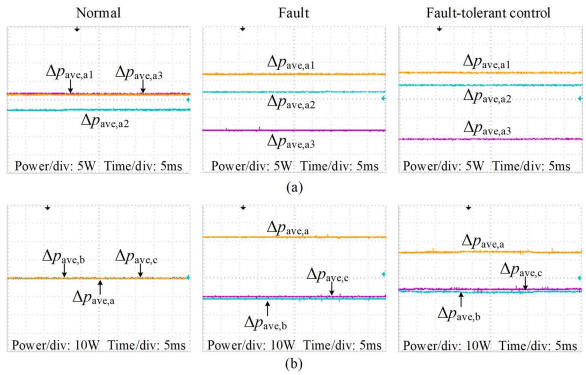


Fig. 26. Output power errors without power balancing control in case II. (a) Output power errors of H-bridge cells in phase-*a*. (b) Three-phase output power errors.

the output power of each cell in phase-*a* converges as much as possible when the powers of the first and second cells in phase-*a* reach their maximum values. And to maintain the normal output power of phase-*a*, the third cell in phase-*a* handles more power at this time, as shown in the middle image of Fig. 22(a). The phase power errors of the inverter are also minimized as much as possible, as shown in the middle image of Fig. 22(b) and the middle image of Fig. 23(b).

During the fault-tolerant control condition, the proposed fault-tolerant control method ensures that the faulty phase can output voltage levels within a certain range. The THDs of the currents are 3.07% and the amplitudes of the currents in phase-*a* are recovered to the reference value, as shown in the right image of Fig. 21(b).

According to Figs. 21–26, a summary of the experimental results of double-cell fault is given in Table VI; it can be seen that the combination of power balancing and fault-tolerant control can still achieve good power balancing performance.

C. Comparisons With Other Fault-Tolerant Control Methods

To further illustrate the superiority of the proposed method, the fault-tolerant control methods in [24] (Method 1), [31] (Method 2), and [34] (Method 3) are tested for comparison.

TABLE VI
SUMMARY OF EXPERIMENTAL RESULTS OF DOUBLE-CELL OPEN FAULT

	With power balancing control			Without power balancing control		
Operation	Normal	Fault	Fault tolerant	Normal	Fault	Fault tolerant
Current THD	2.88%	9.27%	3.07%	2.75%	8.61%	2.93%
Maximum inner-phase power error of phase-a (W)	0.2	8.4	10.1	3.3	8.1	9.9
Maximum inter phase power error (W)	0.3	14.5	11.5	0.5	21.4	16.4

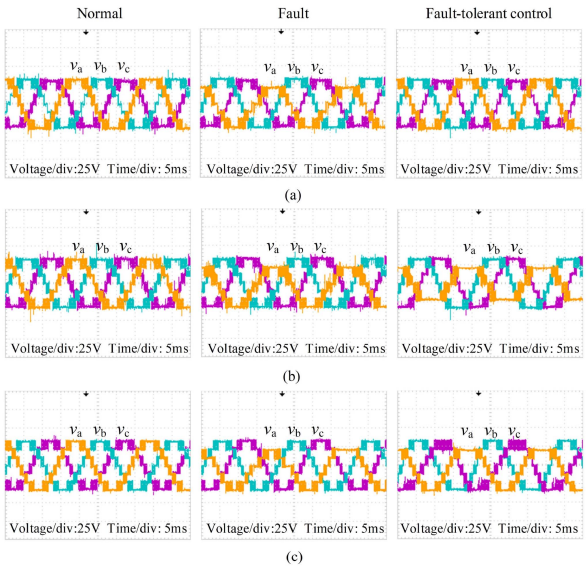


Fig. 27. Output voltages of three-phase CHB inverter under other fault-tolerant control methods. (a) Method 1. (b) Method 2. (c) Method 3.

Methods 1 and 3 are based on the injection of a fundamental frequency zero-sequence voltage, while Method 2 requires redundant cells. The three methods do not consider interphase power balancing, and inner-phase power balancing is considered only in Method 3. A PWM generator is used in each method, and the switching frequency is 10 kHz. An open fault still occurs in the first cell of phase-*a*. Figs. 27 and 28 show the output voltages and currents of the CHB inverter with the three methods, respectively. One of the advantages of FSC-MPC method is its low average switching frequency, which can be seen by the comparison between Figs. 11(a) and 27, or between Figs. 21(a) and 27. Thus, the total switching loss can be lowered. Moreover, it can be seen from Fig. 28 that the three-phase currents are unbalanced during the fault condition. The output powers and output power errors of the CHB inverter with Method 3 are shown in Fig. 29 and Fig. 30, respectively. As shown in the figures, large fluctuations occur in the output powers of the

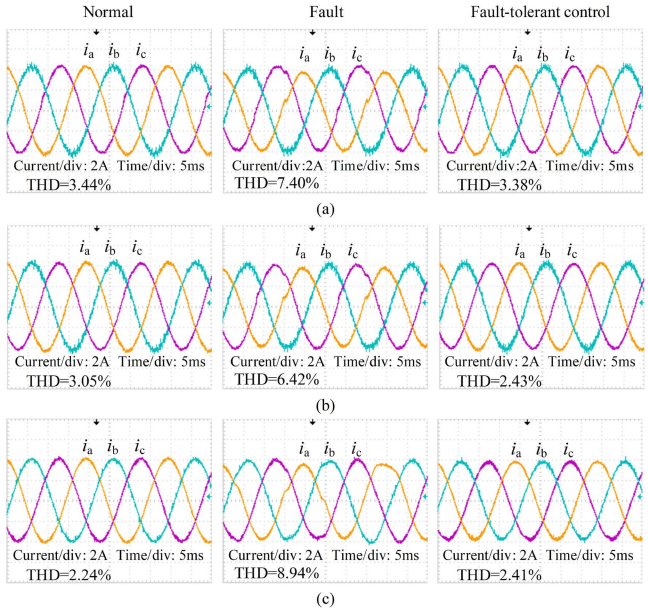


Fig. 28. Output currents of three-phase CHB inverter under other fault-tolerant control methods. (a) Method 1. (b) Method 2. (c) Method 3.

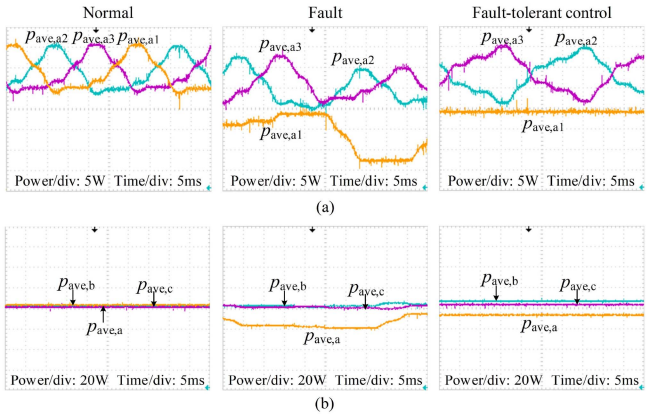


Fig. 29. Output powers of CHB inverter under Method 3. (a) Output powers of H-bridge cells in phase-*a*. (b) Three-phase output powers.

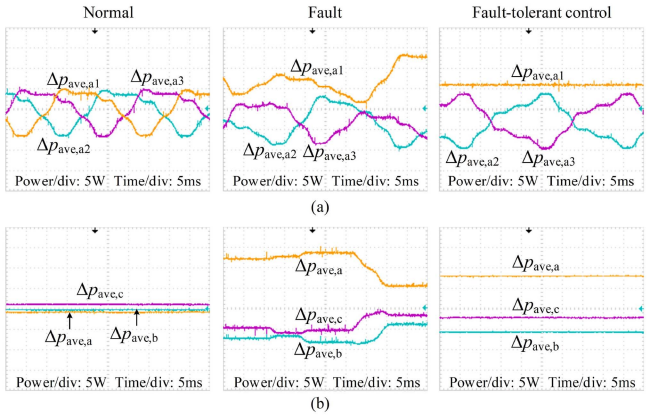


Fig. 30. Output power errors of CHB inverter under Method 3. (a) Output power errors of H-bridge cells in phase-*a*. (b) Three-phase output power errors.

TABLE VII
SUMMARY OF EXPERIMENTAL RESULTS OF SINGLE-CELL OPEN FAULT IN METHOD 3

Operation	Normal	Fault	Fault tolerant
Current THD	2.24%	8.94%	2.41%
Maximum inner-phase power error of phase-a (W)	6.5	13.2	9.6
Maximum inter phase power error (W)	0.8	13.4	7.9

H-bridge cells in phase-*a* due to the slow rotation speed of the switching carriers, and the three-phase output powers cannot be balanced.

According to Figs. 28–30, a summary of the experimental results of single-cell fault in Method 3 is listed in Table VII. Compared with the results in Tables V and VI, the proposed control strategy has superior performance.

VII. CONCLUSION

In this article, a model predictive-based interphase and inner-phase power balancing control strategies are proposed at first. A novel reward function is used to balance the interphase power by carefully selecting appropriate redundant voltage vectors. Another reward function is presented to balance the inner-phase power by selecting suitable switching combinations. The interphase power and inner-phase power can be balanced based on these strategies in normal and fault conditions. Then, when fault-tolerant control is introduced to maintain the normal operation of the CHB inverter, the reward functions are corrected due to the voltage-level loss. In this case, both the interphase power and inner-phase power converge as much as possible. Compared with the fault-tolerant control without power balancing and other reported methods, the proposed combination of power balancing control and fault-tolerant control scheme achieves better performance. The effectiveness of the scheme is validated by hardware experimental studies.

REFERENCES

[1] F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," in *Proc. Int. Power Electron. Conf.*, Sapporo, Japan, Jun. 2010, pp. 492–501.

[2] J. Rodriguez, J. S. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[4] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[5] A. El-Hosainy, H. A. Hamed, H. Z. Azazi, and E. E. El-Kholy, "A review of multilevel inverter topologies, control techniques, and applications," in *Proc. 19th Int. Middle East Power Syst. Conf.*, Cairo, Egypt, 2017, pp. 1265–1275.

[6] L. Zhang, Y. Tang, S. Yang, and F. Gao, "Decoupled power control for a modular-multilevel-converter-based hybrid ac–dc grid integrated with hybrid energy storage," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2926–2934, Apr. 2019.

[7] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kV neutral-point-clamped, flying-capacitor, and series-connected H-bridge multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1032–1040, Jul./Aug. 2007.

[8] P. Cortes, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodriguez, "Predictive control in power electronics and drives," *IEEE Trans. Ind. Electron.*, vol. 55, no. 12, pp. 4312–4324, Dec. 2008.

[9] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model predictive control—A simple and powerful method to control power converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1826–1838, Jun. 2009.

[10] P. Tatjewski, "Model-based predictive control," in *Advanced Control of Industrial Processes*. London, U.K.: Springer, 2007, pp. 107–271.

[11] A. Taheri and M. H. Zhalebaghi, "A new model predictive control algorithm by reducing the computing time of cost function minimization for NPC inverter in three-phase power grids," *ISA Trans.*, vol. 71, pp. 391–402, Nov. 2017.

[12] E. Espinosa, J. Espinoza, P. Melín, J. Rohten, M. Rivera, and J. Muñoz, "FCS–MPC with nonlinear control applied to a multicell AFE rectifier," *Sensors*, vol. 22, no. 11, May 2022, Art. no. 4100.

[13] A. A. Ahmed, B. K. Koh, and Y. I. Lee, "A comparison of finite control set and continuous control set model predictive control schemes for speed control of induction motors," *IEEE Trans. Ind. Inform.*, vol. 14, no. 4, pp. 1334–1346, Apr. 2018.

[14] H. T. Nguyen, E.-K. Kim, I.-P. Kim, H. H. Choi, and J.-W. Jung, "Model predictive control with modulated optimal vector for a three-phase inverter with an LC filter," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2690–2703, Mar. 2018.

[15] N. Panten, N. Hoffmann, and F. W. Fuchs, "Finite control set model predictive current control for grid-connected voltage-source converters with LCL filters: A study based on different state feedbacks," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5189–5200, Jul. 2016.

[16] J. Rodriguez et al., "State of the art of finite control set model predictive control in power electronics," *IEEE Trans. Ind. Inform.*, vol. 9, no. 2, pp. 1003–1016, May 2013.

[17] H. Mhiesan et al., "A method for open-circuit faults detecting, identifying, and isolating in cascaded H-bridge multilevel inverters," in *Proc. 9th IEEE Int. Symp. Power Electron. Distrib. Gener. Syst.*, Charlotte, NC, USA, 2018, pp. 1–5.

[18] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, San Jose, CA, USA, 2009, pp. 3151–3157.

[19] A. Hanif, Y. Yu, D. DeVoto, and F. Khan, "A comprehensive review toward the state-of-the-art in failure and lifetime predictions of power electronic devices," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4729–4746, May 2019.

[20] T. Peng et al., "A uniform modeling method based on open-circuit faults analysis for NPC-three-level converter," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 66, no. 3, pp. 457–461, Mar. 2019.

[21] W. Song and A. Q. Huang, "Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2700–2708, Aug. 2010.

[22] I. Sanz, E. J. Bueno, M. Moranchel, and F. J. Rodriguez, "Fault-tolerant cascaded H-bridge converter for an induction motor drive," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc.*, Yokohama, Japan, 2015, pp. 3980–3985.

[23] M. Aleenejad, P. Moamaei, H. Mahmoudi, and R. Ahmadi, "Unbalanced selective harmonic elimination for fault-tolerant operation of three phase multilevel cascaded H-bridge inverters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Charlotte, NC, USA, 2015, pp. 1589–1594.

[24] L. Maharjan, T. Yamagishi, H. Akagi, and J. Asakura, "Fault-tolerant operation of a battery-energy-storage system based on a multilevel cascade PWM converter with star configuration," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2386–2396, Sep. 2010.

[25] Y. Yu, G. Konstantinou, B. Hredzak, and V. G. Agelidis, "Operation of cascaded H-bridge multilevel converters for large-scale photovoltaic power plants under bridge failures," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7228–7236, Nov. 2015.

[26] L. Sun, Z. Wu, F. Xiao, and X. Cai, "Suppression of real power back flow of non-regenerative cascaded H-bridge inverters operating under faulty conditions," in *Proc. IEEE Energy Convers. Congr. Expo.*, Pittsburgh, PA, USA, Sep. 2014, pp. 3075–3082.

[27] M. Fathi and S. A. Khajehoddin, "A fault compensation scheme for cascaded H-bridge inverter with reduced common mode voltage," *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 3257–3267, Apr. 2023.
[28] R. Sharma and A. Das, "Postfault operation of cascaded H-bridge converter for equal power handling by the healthy cells," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9174–9183, Nov. 2020.
[29] H. Lee, J.-W. Kang, B.-Y. Choi, K.-M. Kang, and C.-Y. Won, "Fault-tolerance control for power equalization of cascaded NPC/H-bridge inverter system," in *Proc. 10th Int. Conf. Power Electron. ECCE Asia*, Busan, South Korea, 2019, pp. 2479–2485.
[30] B. H. Kumar, M. M. Lokhande, R. R. Karasani, and V. B. Borghate, "Fault tolerant operation of CHB multilevel inverters based on the SVM technique using an auxiliary unit," *J. Power Electron.*, vol. 18, no. 1, pp. 56–69, 2018.
[31] M. Aleenejad, S. Jafarishiadeh, H. Mahmoudi, and R. Ahmadi, "Reduced number of auxiliary H-bridge power cells for post-fault operation of three phase cascaded H-bridge inverter," *IET Power Electron.*, vol. 12, no. 11, pp. 2923–2931, Sep. 2019.
[32] H. Mhiesan, Y. Wei, Y. P. Siwakoti, and H. A. Mantooth, "A fault-tolerant hybrid cascaded H-bridge multilevel inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12702–12715, Dec. 2020.
[33] Y. Zang, X. Wang, B. Xu, and J. Liu, "Control method for cascaded H-bridge multilevel inverter failures," in *Proc. 6th World Congr. Intell. Control Autom.*, Dalian, China, 2006, pp. 8462–8466.
[34] S.-M. Kim, J.-S. Lee, and K.-B. Lee, "A modified level-shifted PWM strategy for fault-tolerant cascaded multilevel inverters with improved power distribution," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7264–7274, Nov. 2016.
[35] P. Cortés, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, "Model predictive control of multilevel cascaded H-bridge inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2691–2699, Aug. 2010.

Xiaogang Wang (Member, IEEE) was born in Jilin, China, in 1976. He received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 2000, the M.S. degree in power electronics from the Institute of Electrical Engineering, Academy of Sciences, Beijing, China, in 2003, and the Ph.D. degree in power electronics from the South China University of Technology, Guangzhou, China, in 2009.

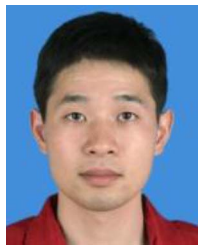
Since 2003, he has been with Guangzhou University, Guangzhou, China, where he is currently the Vice Professor of power electronics with the School of Mechanical and Electrical Engineering. He has authored more than 60 published technical papers. His current research interests include high-power converters, microgrid, and renewable energy power generation systems.

Yongtian Zhao was born in Guangdong, China, in 1998. He received the B.S. degree in electrical engineering from Guangzhou Maritime University, Guangzhou, China, in 2021. He is currently working toward the M.S. degree in electronic information engineering with Guangzhou University, Guangzhou, China.

His current research interests include advanced control of grid-connected inverters and model predictive control.

Ru Yang (Member IEEE) was born in Hunan, China, in 1971. She received the M.S. degree in electronic engineering from the Guangdong University of Technology, Guangzhou, China, in 1999, and the Ph.D. degree in power electronics from the South China University of Technology, Guangzhou, China, in 2007.

Since 1999, she has been with Guangzhou University, Guangzhou, China, where she is currently a Professor of power electronics with the School of Mechanical and Electrical Engineering. She has authored more than 50 published technical papers. Her current research interests include time- and frequency-domain analysis of power electronics, chaotic switching techniques, electromagnetic interference, and chaos detection.



Wei Hu (Member, IEEE) was born in Hunan, China, in 1980. He received the B.S. and M.S. degrees in measurement and control technology and instruments from the College of Electrical and Information Engineering, Hunan University, Changsha, China, in 2003 and 2006, respectively, and the Ph.D. degree in power electronics from the South China University of Technology, Guangzhou, China, in 2017.

Since 2006, he has been with Guangzhou University, Guangzhou, China. He has authored more than 30 published technical papers. His current research interests include modeling and nonlinear control of power converters, stability analysis, and EMI prediction of dc–dc converters.

Tao Zou was born in Liaoning, China, in 1975. He received the Ph.D. degree in control theory and control engineering from Shanghai Jiao Tong University, Shanghai, China, in 2005.

Since 2019, he has been a Professor with the School of Mechanical and Electrical Engineering, Guangzhou University, Guangzhou, China. His research interests include model predictive control, industrial process modeling and simulation, advanced process control, decision making, and real-time optimization theory and application.