LLC Converter With Hold-Up Time Compensation Using Partial Power Process With Semiactive Bridge Rectifier

Jong-Woo Kim, *Member, IEEE*

***Abstract*—This article proposes an *LLC* converter using a semiactive bridge partial power processing (P^3) circuit capable of hold-up time compensation. In a nominal state, the P^3 circuit provides a small amount of the output power, reducing the power rating of the main *LLC* converter. During the hold-up time, the P^3 circuit provides a boosting gain with pulsewidth modulation (PWM). By utilizing a semiactive bridge rectifier, the proposed P^3 circuit does not require an additional converter, which is commonly utilized in most P^3 concepts, while providing both partial power and boosting gain. Furthermore, the proposed concept suppresses the peak of the resonant current in PWM-controlled resonant converters. The prototype converter with 400–300 V input and 50 V/500 W output is built to verify its effectiveness.**

***Index Terms*—Center-tapped rectifier, hold-up time, *LLC* converter, pulsewidth modulation (PWM) control, wide range.**

I. Introduction

THE *LLC* converter is a mainstream converter nowadays due to its superb performance with fewer components [1], [2], [3], [4], [5]. In data center applications, where a relatively low output voltage is required, the *LLC* converter with a center-tapped rectifier is prevalently utilized as the dc–dc stage of the ac–dc offline power supply, as shown in Fig. 1(a). The power supply in a data center needs to maintain its output voltage for tens of milliseconds although it loses its ac input voltage. This requirement is called a hold-up time requirement, to allow sufficient time for an uninterrupted power supply or battery backup unit to engage. As shown in Fig. 1(b), during the hold-up time, the energy stored in the link capacitor provides the output power. The input voltage of *LLC* converter V_{LINK} decreases, requiring the boosting gain of the *LLC* converter. In conventional *LLC* converters utilizing switching frequency control, the need for boosting gain results in a large circulating current, causing an efficiency drop and a large size of the magnetic components.

To solve this problem, there have been hold-up time compensation techniques reported by researchers. Existing technologies

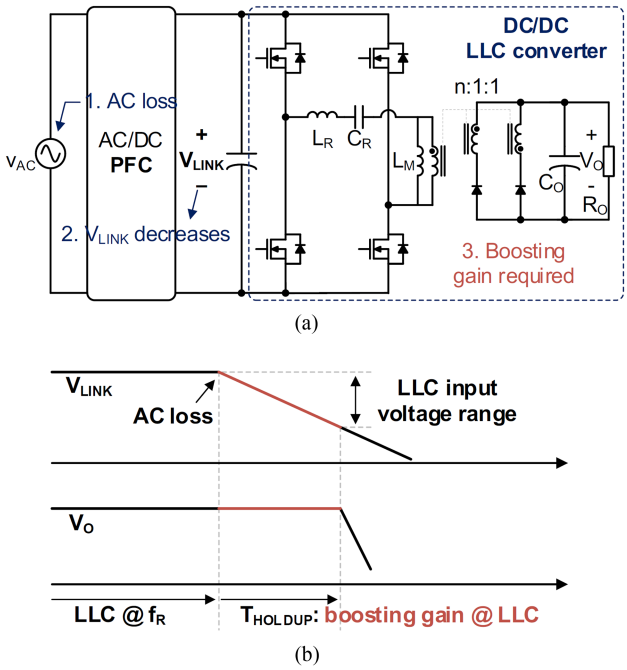


Fig. 1. (a) *LLC* converter in AC–DC power supply and hold-up requirement. (b) Operation of AC–DC power supply during the hold-up time after AC loss.

can be categorized into two concepts: resonant tank modification [6], [7], [8], [9] and pulsewidth modulation (PWM) control. Resonant tank modification methods adjust the values of the resonant tank (L_{M}, L_{R}, and C_{R} in Fig. 1) of the *LLC* converter during the hold-up time. As an example, the magnetizing inductance of the transformer L_{M} has its maximum value in the nominal state to minimize the circulating current, but the additional circuit adds magnetic flux to reduce L_{M} only during the hold-up time [7]. Also, additional C_{R} can be added during the hold-up time for a lower quality factor to obtain a higher peak gain of an *LLC* converter [8]. The resonant tank modification concept reduces the circulating current in the nominal state. However, it still depends on the circulating current utilizing additional components. Furthermore, the additional circuits are used only during the hold-up time, so the use of additional circuits is not efficient.

PWM control methods [3], [5], [10], [11], [12], [13], [14], [15], [16], [17], [18] can allow an *LLC* converter to operate as an isolated boost converter during the hold-up time. This method

Manuscript received 15 November 2023; revised 9 January 2024; accepted 16 January 2024. Date of publication 30 January 2024; date of current version 20 March 2024. This work was supported by Konkuk University in 2024. Recommended for publication by Associate Editor M. Wang.

The author is with the Department of Electrical and Electronics Engineering, Konkuk University, Seoul 05029, South Korea (e-mail: jongwookim@konkuk.ac.kr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3360085.

Digital Object Identifier 10.1109/TPEL.2024.3360085

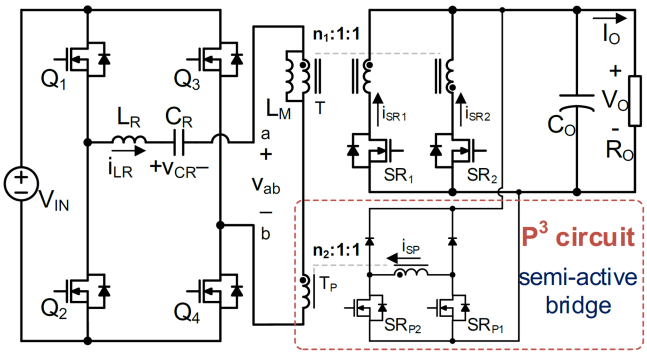


Fig. 2. Proposed converter.

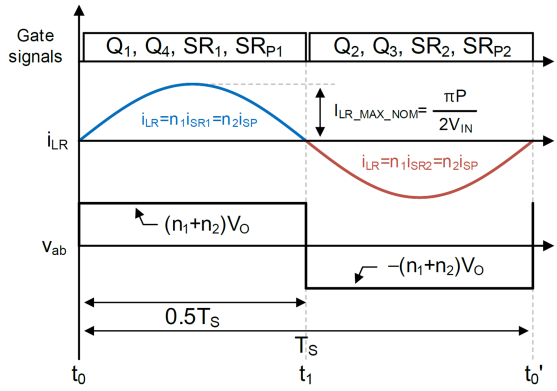


Fig. 3. Operation in the nominal state.

utilizes an additional switch or synchronous rectifier (SR) to provide a boosting duty ratio. The advantage of this method is that the boosting capability is independent of the resonant tank. However, when a PWM control method employs an additional switch [10], [11], [12], it is burdened by extra components and complex control. Moreover, when its topology is asymmetric [11], it even shows an offset current in the transformer. Utilizing SR for PWM control is an attractive way because it does not need additional components. However, its application is limited to full-bridge and voltage doubler rectifiers [2], [3], [5], [14], [15], [16], [17], excluding center-tapped rectifiers. This is because SR PWM control on center-tapped rectifier causes a large discharging current from the output capacitor resulting in a huge current peak. Furthermore, PWM control shows a distortion on the resonant current with a higher peak resonant current. Since the distortion becomes severe while the boosting gain increases, the peak current becomes the maximum during the hold-up time. This imposes a larger maximum flux density on the resonant inductor, increasing the size of the magnetic component.

This article proposes a partial power processing (P^3) circuit for hold-up time compensation in an *LLC* converter. The proposed converter has only a semiactive bridge for P^3 without any additional converter, which is commonly used in conventional P^3 methods for output voltage regulation [18], [19], [20], [21], [22]. Also, by obtaining the sinusoidal current waveform at the minimum input voltage during the hold-up time, the proposed converter reduces the peak current caused by PWM control. Furthermore, it can be implemented in *LLC* converters with any type of rectifier. In the following section, the proposed converter, its operation, steady-state analysis, and experimental verification will be discussed.

II. Proposed Converter and its Operation

Fig. 2 illustrates the proposed converter. The proposed converter utilizes a transformer T_P and a semiactive bridge for partial power processing (P^3). It can be noted that the proposed converter does not use an additional dc–dc converter, which is commonly used in conventional P^3 methods. On the primary side, T_P is connected in series with the main transformer T. On the secondary side, the semiactive bridge is connected to the output in parallel. For simplicity, T_P is considered an ideal transformer.

A. Operation in the Nominal State

The proposed converter operates at the resonant frequency $1/(2\pi\sqrt{L_R C_R})$ in the nominal state. The resonant current is purely sinusoidal, and the voltage across the transformer windings, i.e., v_{ab}, is synchronized with the resonant current, as shown in Fig. 3. So, the voltage conversion ratio can be obtained by the turns ratio of the transformers T and T_P as follows:

$$\frac{V_O}{V_{IN}} = \frac{1}{n_1 + n_2} \tag{1}$$

where V_{IN}, V_O, n_1, and n_2 represent the input voltage, output voltage, and the turns ratio of T and T_P, respectively. Since T and T_P share the current due to the series connection at the primary side, the power delivered by T and T_P can be found as follows:

$$P_T = \frac{n_1}{n_1 + n_2} P_O \tag{2}$$

$$P_{TP} = \frac{n_2}{n_1 + n_2} P_O. \tag{3}$$

where P_T and P_{TP} and P_O represent the amount of power delivered by T and T_P and the total output power of the proposed converter, respectively.

B. Operation During the Hold-Up Time

Figs. 4 –6 illustrate the key waveforms, equivalent resonant circuits, and current paths of the proposed converter during the hold-up time. To obtain a boosting gain, the gate signals for the semiactive bridge are extended by $D_B T_S$, where D_B is the boosting duty cycle and T_S is the switching period. The switching period is still fixed at the resonant frequency. Since the proposed converter does not rely on the circulating current to obtain a boosting gain, the magnetizing inductor of the main transformer is large enough to consider its current zero. From now, the resonant inductor current $i_{LR}(t)$ and the resonant capacitor voltage $v_{CR}(t)$ at the time t_N will be expressed by i_{LRN} and v_{CRN} for simplicity.

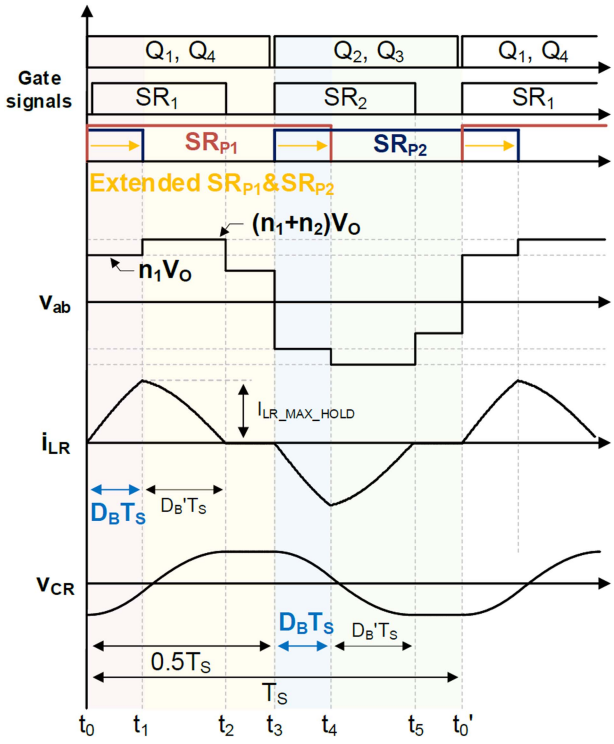


Fig. 4. Key waveforms of the proposed converter during the hold-up time.

From t_0 to t_1, the main switches Q_1 and Q_4 are turned ON, and the resonant current $i_{LR}(t)$ becomes positive. However, SR_{P2} is still turned ON, forming a short circuit across T_P. Therefore, the voltage reflected to the primary side by transformers, i.e., v_{ab}, becomes n_1V_O, not $(n_1+n_2)V_O$. $i_{LR}(t)$ is rapidly boosted during this period because a larger voltage is applied to the resonant tank components. The state equations during this period can be obtained as follows:

$$Zi_{LR}\ (t-t_0) = [V_{IN}-n_1V_O-v_{CR0}]\ \sin[\omega(t-t_0)] \quad (4)$$

$$v_{CR}(t-t_0)-[V_{IN}-n_1V_O] = -[V_{IN}-n_1V_O-v_{CR0}]\cos[\omega(t-t_0)] \quad (5)$$

$$[v_{CR}(t-t_0)-(V_{IN}-n_1V_O)]^2+[Zi_{LR}(t-t_0)]^2 = (V_{IN}-n_1V_O-v_{CR0})^2 = R_1^2 \quad (6)$$

where Z, ω, and v_{CR0} represent $\sqrt{\frac{L_R}{C_R}}$, $\frac{1}{\sqrt{L_RC_R}}$, and $v_{CR}(t_0)$, respectively. It can be noted that the state (6) forms a circle with the center at O_1 [V_{IN}–n_1V_O, 0] and the radius R_1.

At t_1, SR_{P2} is turned OFF and the boosted resonant current is delivered to the output capacitor through the semiactive bridge. Now, v_{ab} becomes $(n_1+n_2)V_O$ and $i_{LR}(t)$ decreases. The state equations are as follows:

$$Zi_{LR}\ (t-t_1) = [V_{IN}-(n_1+n_2)V_O-v_{CR1}]\ \sin[\omega(t-t_1)] + Zi_{LR1}\cos[\omega(t-t_1)] \quad (7)$$

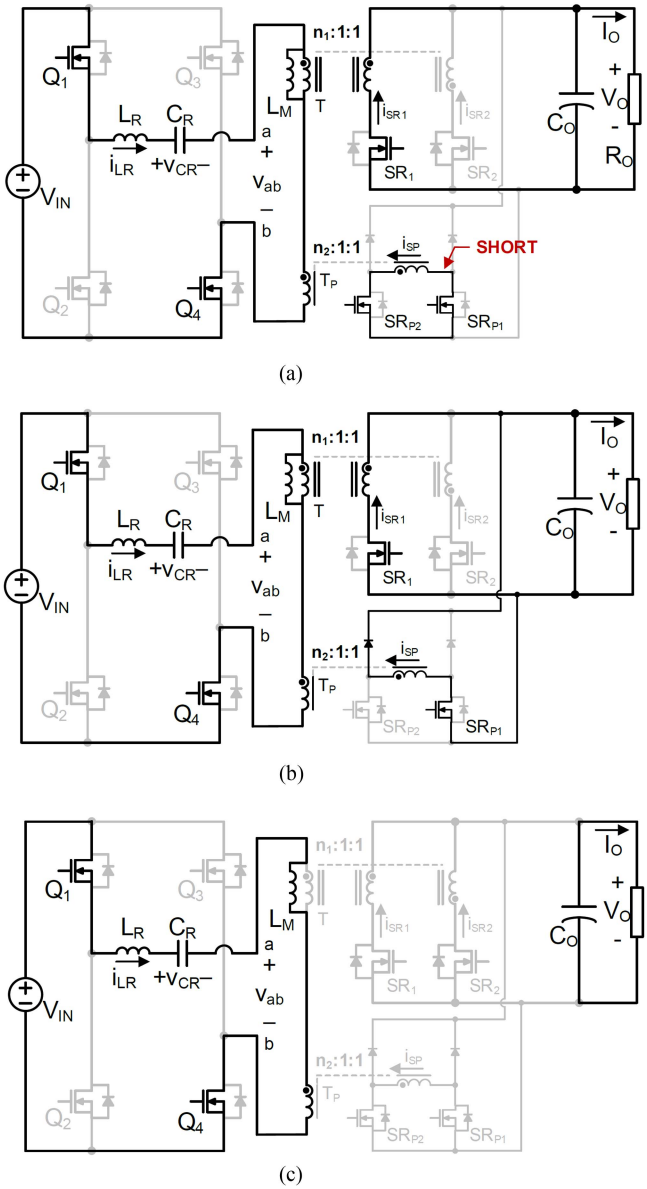


Fig. 5. Current paths of the proposed converter during the hold-up time during (a) t_0–t_1, (b) t_1–t_2, and (c) t_2–t_3.

$$v_{CR}(t-t_1)-[V_{IN}-n_1V_O] = -[V_{IN}-n_1V_O-v_{CR0}]\cos[\omega(t-t_1)] + Zi_{LR1}\sin[\omega(t-t_1)] \quad (8)$$

$$[v_{CR}(t-t_1)-\{V_{IN}-(n_1+n_2)V_O\}]^2+[Zi_{LR}(t-t_1)]^2 = [V_{IN}-(n_1+n_2)V_O-v_{CR1}]^2 = R_2^2 \quad (9)$$

where $v_{CR1}=v_{CR}(t_1)$. It can be noted that the state (9) forms a circle with the center at O_2 [V_{IN}–$(n_1+n_2)V_O$, 0] and the radius R_2. After $i_{LR}(t)$ becomes zero at t_3, $i_{LR}(t)$ maintains zero till Q_1 and Q_4 are turned OFF and Q_2 and Q_3 are turned ON. The operation during the remaining half of the switching period is symmetric.

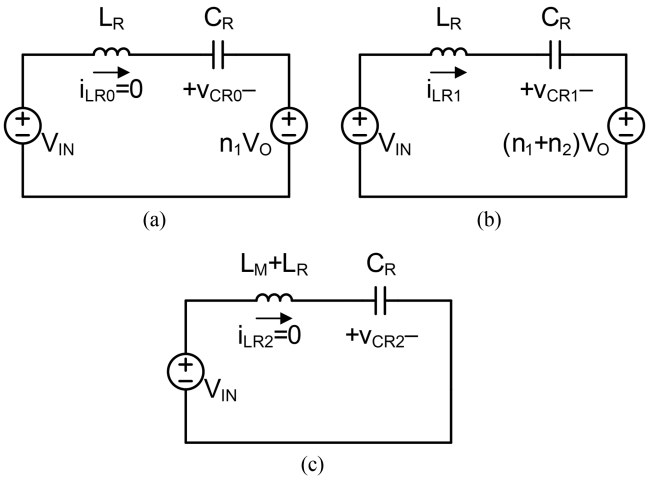


Fig. 6. Equivalent resonant circuits of the proposed converter during the hold-up time during (a) t_0–t_1, (b) t_1–t_2, and (c) t_2–t_3.

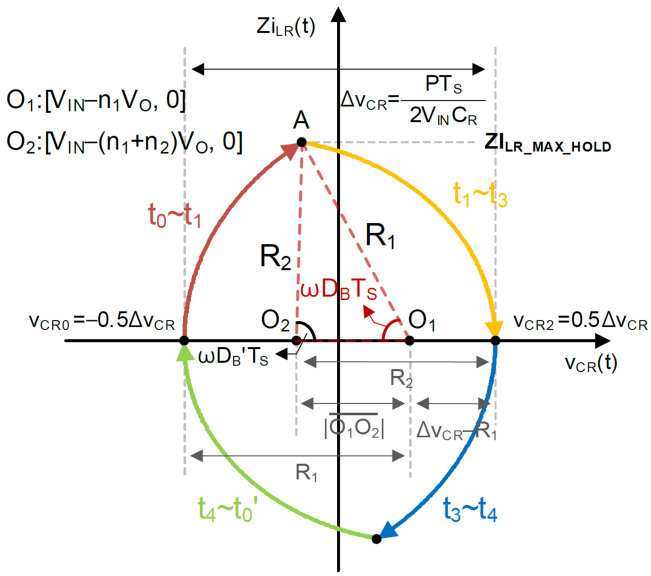


Fig. 7. State trajectory of the proposed converter during the hold-up time.

Based on the circles (6) and (9), Fig. 7 illustrates the state trajectory of the proposed converter during the hold-up time. Since all the input current flows through the resonant capacitor C_R, the ripple voltage can be obtained as follows:

$$\Delta v_{CR} = \frac{PT_S}{2V_{IN}C_R} \tag{10}$$

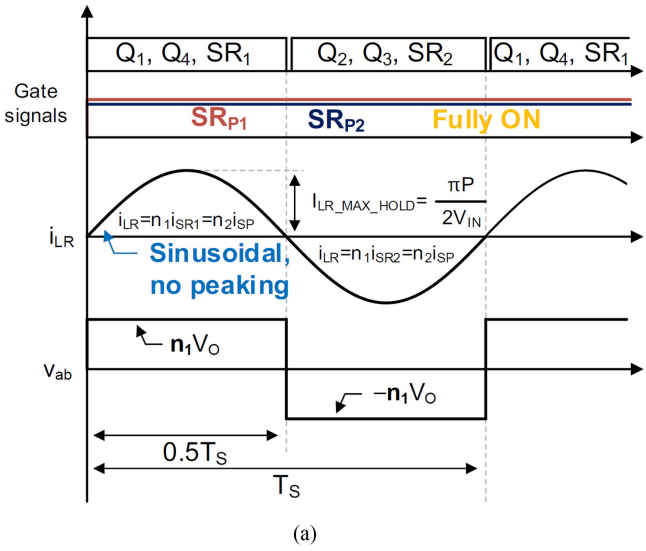
where P is the operating power of the proposed converter.

Since the operation of the proposed converter is symmetric, v_{CR0} and v_{CR2} can be expressed as follows:

$$v_{CR2} = -v_{CR0} = \frac{\Delta v_{CR}}{2} = \frac{PT_S}{2V_{IN}C_R}. \tag{11}$$

Then, R_1 in (6) and R_2 in (9) can be expressed by the operating condition as follows:

$$R_1 = V_{IN} - n_1V_O + \frac{PT_S}{4V_{IN}C_R} \tag{12}$$



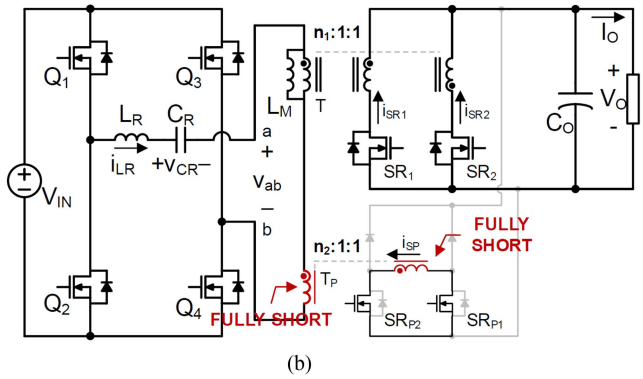


Fig. 8. Operation of the proposed converter when the input voltage is the minimum. (a) Key waveforms and (b) short-circuited P^3 circuit for the maximum gain.

$$R_2 = \Delta v_{CR} - R_1 + |\overline{O_1O_2}| = \frac{PT_S}{4V_{IN}C_R} - V_{IN} + (n_1 + n_2)V_O. \tag{13}$$

Applying the cosine law to the angle AO_1O_2 leads to the required boosting duty D_B in an operating condition:

$$D_B = \frac{1}{\omega T_S}\cos^{-1}\left[\frac{R_1^2 + n_2V_O{}^2 - R_2^2}{2n_2R_1V_O}\right]. \tag{14}$$

In a similar manner, applying the cosine law to the angle AO_2O_1 leads to the duration of t_1–t_2 ($=\omega D_B{}'T_S$) and $D_B{}'$ can be expressed as follows:

$$D'_B = \frac{1}{\omega T_S}\cos^{-1}\left[\frac{R_2^2 + n_2V_O{}^2 - R_1^2}{2n_2R_2V_O}\right]. \tag{15}$$

Fig. 8 illustrates the key waveforms and operation of the proposed converter when the input voltage is the minimum during the hold-up time. D_B increases to 0.5 and SR_{P1} and SR_{P2} are fully turned on. In this case, the P^3 transformer becomes a short circuit and only the main transformer delivers the output power. Accordingly, the voltage conversion ratio becomes $V_O/V_{IN} = 1/n_1$. Because the proposed converter operates at

the resonant frequency even during the hold-up time, it should be noted that the proposed converter has a purely sinusoidal current waveform again without any distortion. Accordingly, it can be concluded that the proposed converter suppresses the distortion of the resonant current in PWM-controlled resonant converters.

III. Design Example

The effectiveness of the proposed converter is verified with 400–300 V input voltage, 50 V output voltage, and 500 W output power prototype. In the nominal state, the input voltage is 400 V. During the hold-up time, the input voltage decreases down to 300 V. In this example, the switching frequency of the prototype converter is selected as 75 kHz for the concept verification, but a higher switching frequency leads to a smaller size of the prototype converter.

A. Turns Ratio of the Transformers, n_1 and n_2

According to previous analysis, the maximum voltage conversion ratio of the proposed converter is $V_O/V_{\mathrm{IN}} = 1/n_1$. In this example, the minimum input voltage $V_{\mathrm{IN\_MIN}}$ is 300 V. Accordingly, the turns ratio of the main transformer can be obtained as follows:

$$n_1 = \frac{V_{\mathrm{IN\_MIN}}}{V_O} = 6. \tag{16}$$

The turns ratio of T_P can be obtained by the voltage conversion ratio in the nominal state (1) as follows:

$$n_2 = \frac{V_{\mathrm{IN\_NOM}}}{V_O} - n_1 = \frac{400}{50} - 1 = 2 \tag{17}$$

where $V_{\mathrm{IN\_NOM}}$ represents the input voltage in the nominal state. According to (2) and (3), it can be noted that the P^3 circuit in the proposed converter delivers one-fourth of the total output power, i.e., 125 W.

B. Resonant Inductor, L_R

In PWM resonant converters, a smaller L_R (smaller Q) results in increased distortion of the resonant current, which is accompanied by a higher peak value. This larger peak value imposes larger flux density stress on L_R. Therefore, the peak resonant current value $I_{\mathrm{LR\_MAX}}$ needs to be investigated according to L_R value.

The maximum resonant current in the nominal state $I_{\mathrm{LR\_MAX\_NOM}}$ can be obtained as follows:

$$I_{\mathrm{LR\_MAX\_NOM}} = \frac{\pi}{2}\frac{P}{V_{\mathrm{IN}}} = \frac{\pi}{2}\frac{500}{400} = 1.96\ (\mathrm{A}). \tag{18}$$

According to Fig. 7, the maximum resonant current in the hold-up time $I_{\mathrm{LR\_MAX\_HOLD}}$ can be obtained as follows:

$$I_{\mathrm{LR\_MAX\_HOLD}} = \begin{cases} R_1/Z, & \text{if } \omega D_B T_S > \frac{\pi}{2} \\ R_2/Z, & \text{if } \omega D'_B T_S > \frac{\pi}{2} \\ R_1 \sin\left(\omega D_B T_S\right)/Z, & \text{else} \end{cases}. \tag{19}$$

Fig. 9 represents the ratio of $I_{\mathrm{LR\_MAX\_HOLD}}$ to $I_{\mathrm{LR\_MAX\_NOM}}$ according to V_{IN} in the maximum output power (500 W) condition, for different L_R (Q) values, where Q is defined as $\frac{\pi^2}{8(n_1+n_2)^2 R_O}\sqrt{\frac{L_R}{C_R}}$. At the beginning of the hold-up time, $I_{\mathrm{LR\_MAX\_HOLD}}$ increases due to PWM control. However, $I_{\mathrm{LR\_MAX\_HOLD}}$ decreases again at the minimum input voltage condition as it recovers the sinusoidal resonant current waveform. Therefore, it can be noted that the proposed converter and control successfully suppress the peak of resonant current caused by PWM control. Also, it can be noted that $I_{\mathrm{LR\_MAX\_HOLD}}$ decreases as L_R and Q increase. In this example, a ferrite core for L_R is assumed. To achieve the maximum efficiency in the nominal condition, the maximum flux density B_{MAX} during the nominal state is selected to be 0.15 T. Since B_{MAX} is directly proportional to $I_{\mathrm{LR\_MAX}}$, it can be noted that 75 μH L_R will limit B_{MAX} at 0.26 T during the hold-up time. The size of L_R can be selected using area product (AP) as follows:

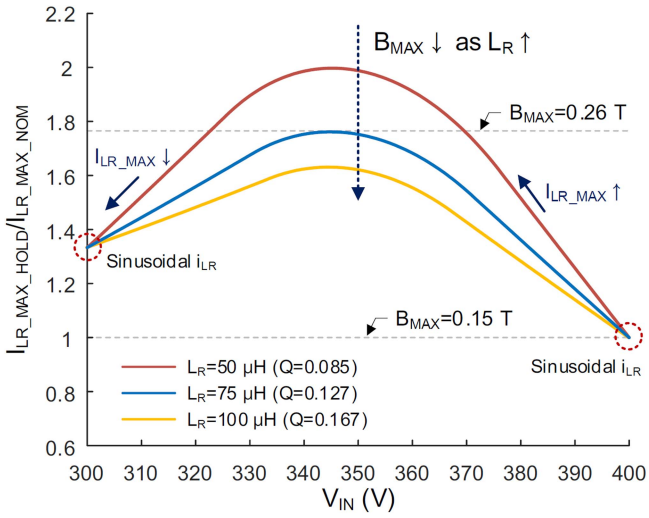


Fig. 9. Ratio $I_{\mathrm{LR\_MAX\_HOLD}}/I_{\mathrm{LR\_MAX\_NOM}}$ according to V_{IN} during the hold-up time, with different L_R (Q) values at the maximum output power condition.

$$\mathrm{AP} = \max\left[\frac{L_R I_{\mathrm{LR\_MAX\_HOLD}} I_{\mathrm{LR\_RMS\_NOM}}}{K_u J B_{\mathrm{MAX\_HOLD}}}\right] \tag{20}$$

where $I_{\mathrm{LR\_RMS\_NOM}}$, K_u, J, and $B_{\mathrm{MAX\_HOLD}}$ represent the RMS value of $i_{\mathrm{LR}}(t)$ in the nominal state, the utilization factor of the window area, the current density of the winding, and the maximum flux density during the hold-up time. $I_{\mathrm{LR\_RMS\_NOM}} = 1.39$ A, $K_u = 0.35$, $J = 5\mathrm{A/mm}^2$, and $B_{\mathrm{MAX\_HOLD}} = 0.26$ T is used in this example. Fig. 10 represents the AP values for L_R according to V_{IN} at the maximum output power condition. The AP value increases as L_R increases. Therefore, it can be noted that there is a tradeoff between the maximum flux density value and the size of L_R. RM6 core is selected with sufficient margin.

It should be noted that a designer can select powder cores or even leakage inductors of transformers for L_R, relieving the limitation on B_{MAX}. In these cases, the maximum current stress itself will be a parameter for L_R design. It would depend on the designer's choice.

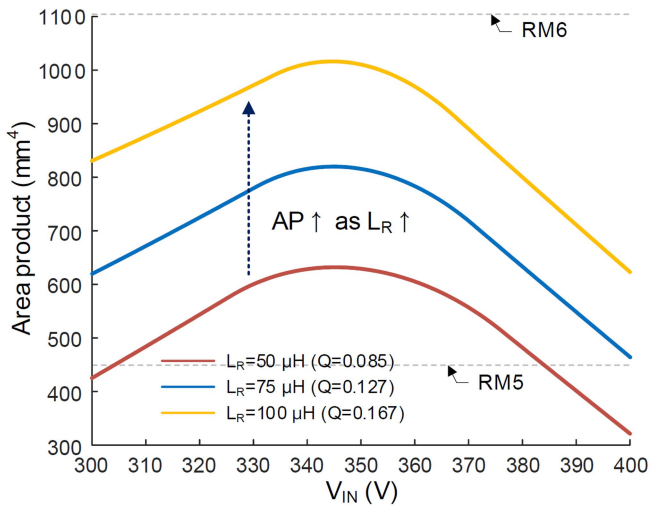


Fig. 10. Area product (AP) of L_R according to V_{IN} at the maximum output power condition.

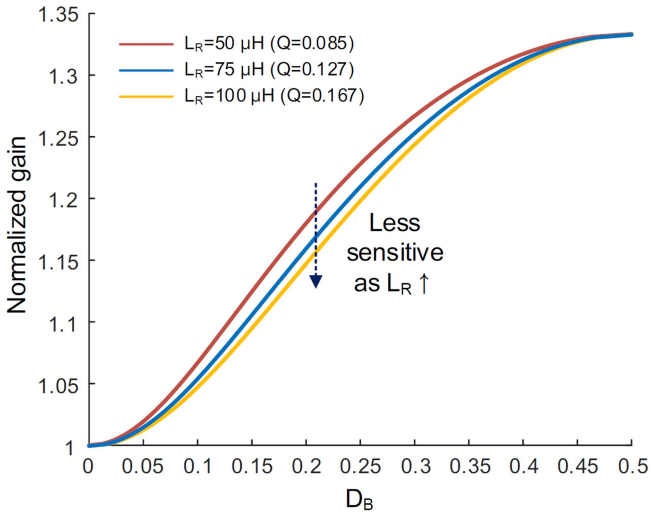


Fig. 11. Normalized gain of the proposed converter according to D_B, with different L_R (Q) values at the maximum output power condition.

Fig. 11 represents the normalized gain of the proposed converter during the hold-up time according to D_B. The gain is normalized by the gain during the nominal state. Since V_{IN} decreases from 400 to 300 V, the normalized gain increases to 1.33. It can be noted that the gain steadily increases as D_B increases. Also, the sensitivity of the gain to D_B decreases as D_B increases, but it does not show a huge difference.

C. Magnetizing Inductor of the Main Transformer, L_M

The proposed control does not rely on the circulating current of the magnetizing inductor of the transformer, so L_M can be as large as possible, only considering zero voltage switching (ZVS) conditions in the nominal state. Fig. 12 shows the ZVS current path of the proposed converter in the nominal state, during the deadtime at t_1 in Fig. 3. C_{OSS} and C_j represent the output capacitance of the primary side switches and the

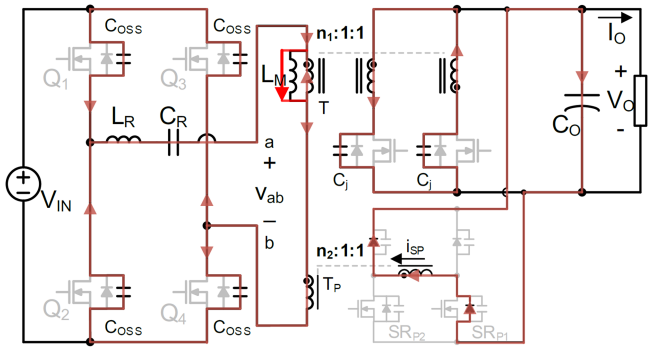


Fig. 12. ZVS current path of the proposed converter in the nominal state (at t_1 in Fig. 3).

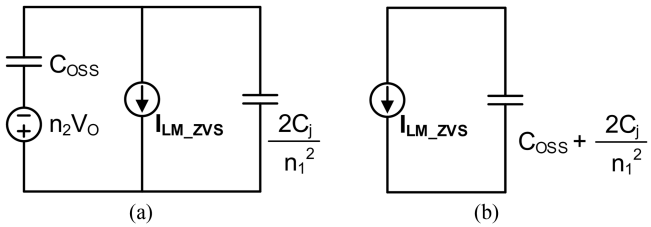


Fig. 13. (a) Equivalent ZVS circuit with current source I_{LM_ZVS} and (b) simplified one to obtain ZVS condition.

secondary side SRs, respectively. Fig. 13(a) and (b) shows the equivalent circuits during the ZVS transition. The ZVS current I_{LM_ZVS} is $n_1 V_O T_S/4L_M$. The voltage source $n_2 V_O$ in Fig. 13(a) can be neglected assuming that the deadtime is too short so that I_{LM_ZVS} is constant during the transition, allowing us to obtain the simplified ZVS equivalent circuit in Fig. 13(b). During the deadtime, all the parasitic capacitors are charged and discharged and v_{ab} varies from V_{IN} to $-V_{IN}$. With a given deadtime T_D, L_M can be calculated as follows:

$$I_{LM\_ZVS}\, T_D = 2V_{IN}C_{tot} \tag{21}$$

$$L_M = \frac{n_1 V_O T_S T_D}{8V_{IN}C_{tot}} \tag{22}$$

where C_{tot} is $C_{OSS} + 2C_j/n_1^2$, the total capacitance to be charged and discharged during the deadtime.

D. Transformer Cores for T and T_P

AP is still effective in determining the size of the transformer cores. AP is the product of the cross-section area and the window area. The cross-section area is closely related to the maximum flux density of the transformer core, and the window area is related to the maximum current density of the transformer.

Since the proposed converter operates at a constant frequency even during the hold-up time, the voltage–second of the transformer windings is directly proportional to the maximum flux density in the transformer core. Comparing v_{ab} waveforms in Figs. 3 and 4, it can be noted that the voltage across the transformer windings becomes even smaller during the hold-up time.

Therefore, the flux density of the transformer is the maximum in the nominal state.

On the other hand, the maximum current density occurs during the hold-up time due to the distortion of the resonant current. However, it should be noted that the hold-up time is a short time period to increase the winding temperature.

Furthermore, the proposed method suppresses the maximum resonant current as we analyzed. Therefore, the wire can be selected considering the RMS current in the nominal state. Accordingly, we can conclude that the transformers in the proposed converter can be designed considering the waveforms in the nominal state, where the current waveforms are purely sinusoidal. The AP of the transformer core for *LLC* converters with purely sinusoidal waveforms can be calculated as follows:

$$\mathrm{AP} = \frac{\pi P}{4\sqrt{2}K_u J B_{\max} f_s} \tag{23}$$

where $P, K_{\mathrm{u}}, J, B_{\max}$, and f_{S} represent the rated power, utilization factor of the window area, current density, the maximum flux density, and the switching frequency, respectively. The rated power for T and $\mathrm{T_P}$ is already obtained as 375 and 125 W, respectively, according to (2), (3), (16), and (17). Although the proposed converter utilizes two transformers, it should be noted that the total A_{P} remains the same, as long as the total output power remains constant.

E. Control of the Proposed Converter

Fig. 14 presents the control concept, implementation, and control-to-output transfer function of the proposed converter. As shown in Fig. 14(a), one of f_{S} and D_{B} controls the voltage conversion ratio (gain) of the proposed converter. It should be noted that there is no region where both f_{S} and D_{B} engage to gain control, to avoid the interaction between them. When the gain is less than $1/(n_1 + n_2)$, only f_{S} is controlled. In the nominal state, $f_{\mathrm{S}} = f_{\mathrm{R}}$ and $D_{\mathrm{B}} = 0$ because the gain needs to be $1/(n_1+n_2)$. The gain increases as f_{S} decreases. When the gain becomes larger than $1/(n_1+n_2)$ during the hold-up time, f_{S} maintains at f_{R}, but D_{B} increases to obtain the boosting gain. D_{B} increases from 0 to 0.5 to increase the gain from $1/(n_1+n_2)$ to $1/n_1$. By doing so, the proposed converter achieves a smooth gain increase. Fig. 14(b) presents the implementation of the control. The proposed converter can be controlled traditional PI controller. PI controller produces the control voltage v_{C} to provide f_{S} and D_{B}. As v_{C} increases, the gain of the proposed converter increases.

From Fig. 14(c), it can be noted that the control-to-output transfer function in a high-frequency region still maintains a similar level. If we want to set the crossover frequency of the loop gain around 2–3 kHz, the same control parameters can be used regardless of the loading conditions, which makes the design of the control parameters simple.

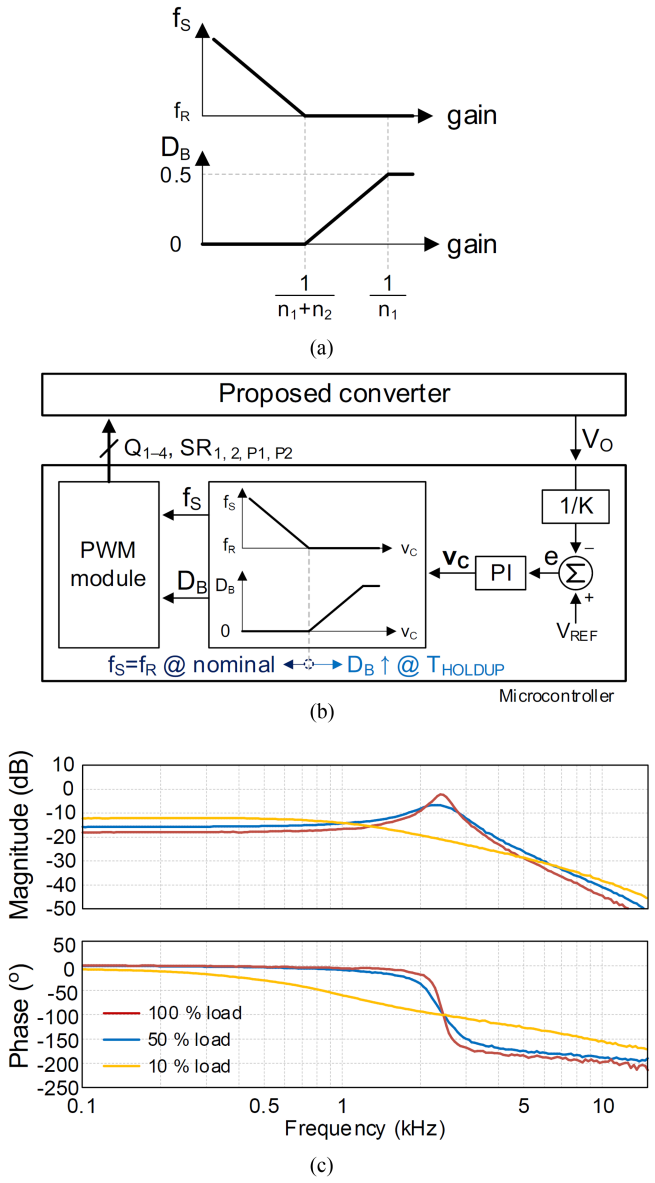


Fig. 14. (a) Control concept, (b) implementation, and (c) control-to-output transfer function ($\hat{v}_O/\hat{v}_C$) of the proposed converter.

IV. Experimental Results

A prototype converter to verify the effectiveness of the proposed converter has been built with 400–300 V input, 50 V output, and 500 W rated power. Table I represents the components list of the prototype converter, and Table II presents the comparison of the main transformer in the proposed and conventional *LLC* converter. It can be noted that the maximum magnetizing current ($I_{\mathrm{LM\_PEAK}}$) of the proposed converter is much smaller because it operates at a constant frequency. On the other hand, the conventional *LLC* converter has more than two times $I_{\mathrm{LM\_PEAK}}$ causing a larger maximum flux density, due to the switching frequency control to obtain boosting gain during the hold-up time. Accordingly, the conventional converter requires a much higher AP value for the transformer, although it is compared with the sum of the AP values of T and $\mathrm{T_P}$ in the proposed converter. Fig. 15 illustrates the prototype converter. It can be noted that the $\mathrm{P^3}$ subboard in the prototype converter is

TABLE I
COMPONENTS LIST OF THE PROTOTYPE CONVERTER

Item	Details	
Specification	V_{IN}: 400–300 V, V_O: 50 V, I_O: 10 A	
Main transformer T	PQ3230 N95 core n_1:1:1=48:8:8	pri: 0.1Φx50 litz wire sec: 0.1Φx100 litz wire L_M=550 μH, L_{LKG}=18.8 μH
Q_1–Q_4	IPW60R070C6 (600 V, 70 mΩ)	
SR_1, SR_2	FDH055N15A (150 V, 5.9 mΩ)	
P^3 transformer T_P	PQ2620 N95 core n_2:1=16:8	pri: 0.1Φx50 litz wire sec: 0.1Φx100 litz wire L_{MP}=281 μH, L_{LKGP}=2.5 μH
SR_{P1}, SR_{P2}	IRFS3607TRLPBF (75 V, 7.3 mΩ)	
D_{P1}, D_{P2}	SDT30B100D1 (100 V, V_F=0.85 V)	
C_R	66 nF (630 V 22 nF MLCC 3 EA)	
L_R	47 μH, RM8 N95 core 0.1 Φx50 litz wire 12 turns	
C_O	1.32 mF (100 V 330μF electrolytic cap. 4 EA)	

TABLE II
COMPARISON WITH CONVENTIONAL *LLC* CONVERTER

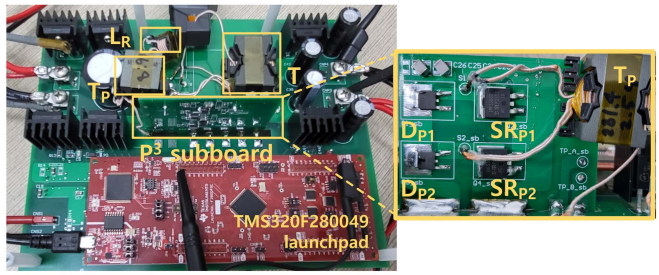
	Proposed	Conventional LLC
L_M	550 μH	
I_{LM_PEAK}	**1.2 A**	**2.54 A**
B_{MAX}	**0.15 T**	**0.2 T**
J	4 A/cm^2	
K_U	0.25	
I_{RMS_PRI}	1.57 A	1.78 A
I_{RMS_SEC}	11.74 A	15.88 A
n_1	6	8
Area product of T	**15517 mm^4**	**26298 mm^4**
Area product of T_P	**6611 mm^4**	**0 mm^4**
Total area product	**22218 mm^4**	**26298 mm^4**
Transformer cores	PQ3230 + PQ2620	PQ3535

compact because it does not use an additional converter for the regulation.

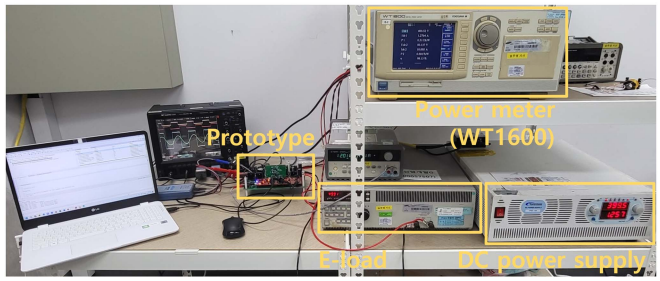
Fig. 16 illustrates the key waveforms of the proposed converter at 400-V input and 50 V/10 A output condition. As discussed, the proposed converter operates at the resonant frequency, and all the gate signals are synchronized with the sinusoidal resonant current. ZVS is achieved by the energy stored in the magnetizing inductor of the main transformer, but the current is small to minimize the circulating current.

Fig. 17 illustrates the key waveforms of the proposed converter during the hold-up time at 340-V input and 50 V/10 A output condition. The gate signals for SRs in the P^3 circuit have been extended by $D_B T_S$, to induce a short circuit across T_P. During the period, the resonant current is boosted and the distorted waveform can be seen due to PWM control.

Fig. 18 illustrates the key waveforms of the proposed converter during the hold-up time at 300-V input and 50 V/10 A output condition. SRs in P^3 circuit are fully turned ON, to maximize the voltage conversion ratio of the proposed converter. The



(a)



(b)

Fig. 15. (a) Prototype converter and (b) experimental setup.

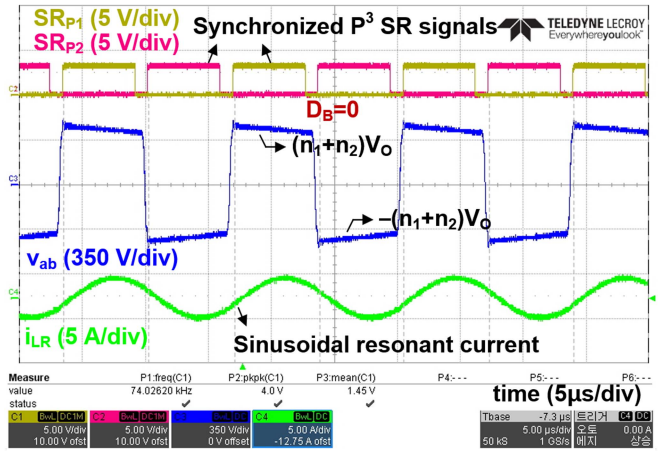


Fig. 16. Key waveforms at 400-V input/full load condition.

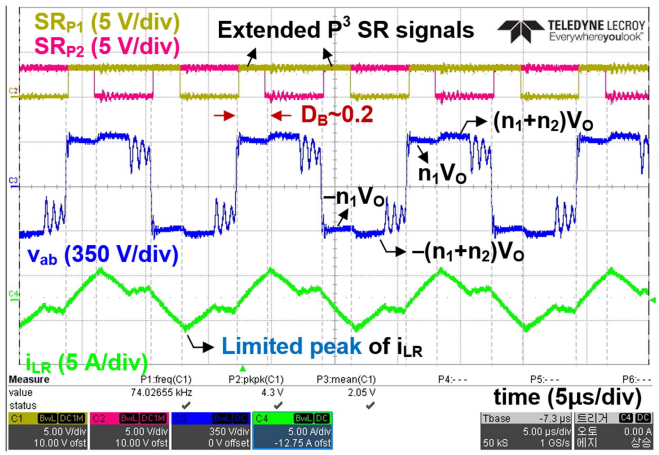


Fig. 17. Key waveforms at 340-V input/full load condition.

TABLE III
COMPARISON WITH PRIOR WORKS FOR HOLD-UP TIME COMPENSATION IN *LLC* CONVERTER

Technologies / Requirements	Resonant tank modification [8], [9]	PWM control [10], [13]	SR PWM control [2], [3]	Partial power processing [18], [19]	**Proposed**
Additional components	Switching network or resonant components	Switching network	Synchronous rectifier instead of diodes	Rectifier circuit + additional converter	Semi-active bridge
Effective use of additional components	No	No	Yes	Yes	Yes
Circulating current minimization	No	Yes	Yes	Yes	Yes
Compatibility with any rectifier	Yes	Yes	No	Yes	Yes
Distortion in the resonant current	Less	Yes	Yes	No	Less

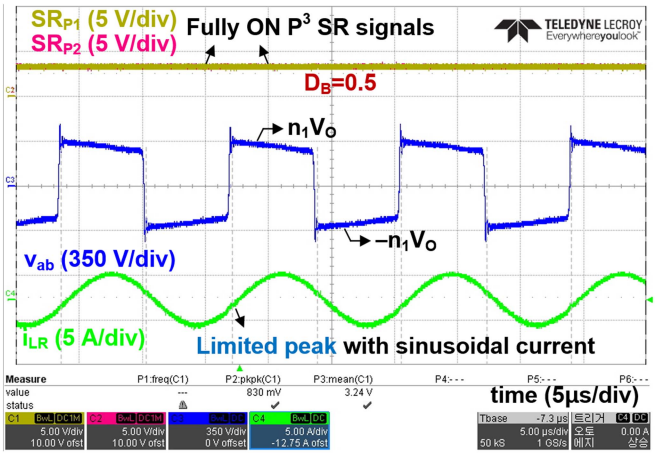


Fig. 18. Key waveforms at 300-V input/full load condition.

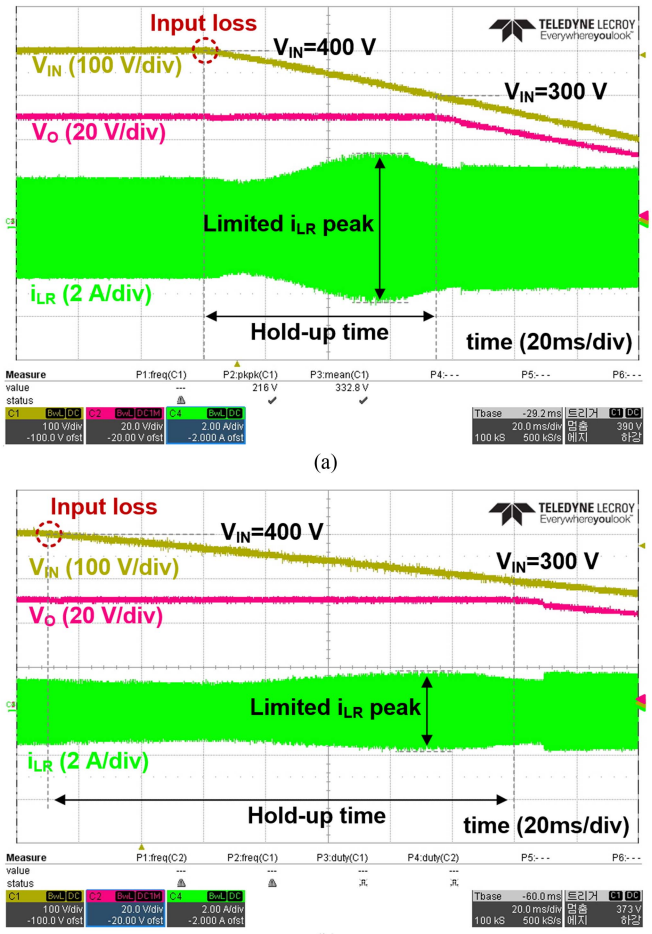


Fig. 19. Waveforms during the hold-up time at (a) full load and (b) 50% load conditions.

resonant current waveform becomes purely sinusoidal again, suppressing the resonant current distortion caused by PWM control. Accordingly, it can be noted that the proposed converter modifies its effective turns ratio utilizing extended PWM signals.

Fig. 19 illustrates the key waveforms of the proposed converter during the whole hold-up time with feedback control. Since the proposed converter smoothly increases the boosting duty ratio D_B from zero to 0.5, it can be noted that the peak of the resonant current increases and then decreases during the hold-up time, as we analyzed in Fig. 9.

Fig. 20 illustrates the efficiency of the prototype converter. The proposed converter achieves higher efficiency in the entire load condition compared to the conventional *LLC* converter, due to the smaller size of the transformer core. In data center applications, efficiency in light and medium load conditions is especially important because the data center power is designed with sufficient power and traffic margins. Therefore, the efficiency profile of the proposed converter is well in accordance with the data center's requirements.

Fig. 21 illustrates the loss breakdown of prototype converters. The proposed converter significantly reduces the losses from the main transformer. Although the P3 circuit adds losses, earnings from the proposed converter outweigh the losses.

V. COMPARISON WITH PRIOR ARTS

Table III represents the characteristics of the proposed converter compared to prior works. Based on the review of the previous works in Section I, several criteria to compare the candidates for the hold-up time compensation as follows.

1) *Less additional components:* Additional components need to be minimized for less price. The proposed converter adds only semiconductor devices for active P^3 bridges.

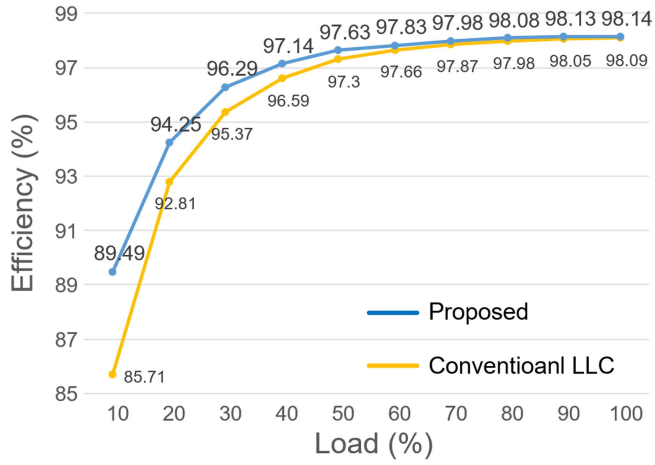


Fig. 20. Efficiency of the prototype converters.

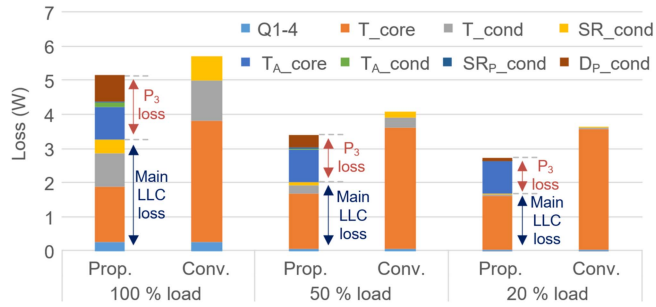


Fig. 21. Loss breakdown of prototype converters.

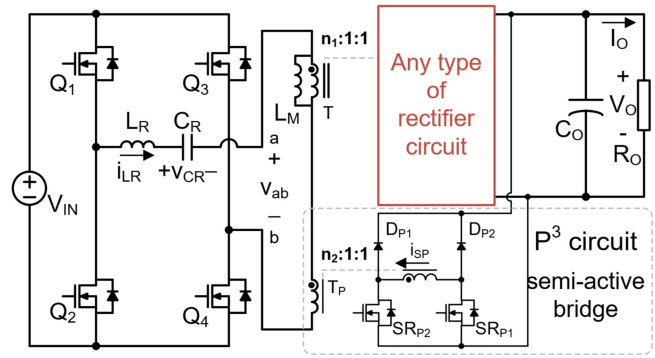


Fig. 22. Extension of the proposed concept.

As discussed in the previous section, the transformer for the P^3 circuit is not considered an additional component since it reduces the size of the main transformer. Compared to other P^3 approaches, the proposed converter achieves output voltage regulation using only an active bridge, without an additional buck/boost converter.

2) *Effective use of additional components:* If it is inevitable to use additional components, they need to be used effectively. In other words, it is better to use them to deliver the output power in the nominal state, not only during the hold-up time. The active bridge in the proposed converter delivers the output current in both the nominal state and the hold-up time, whereas some of the prior works do not.
3) *Circulating current minimization:* The proposed converter achieves regulation through an alternative control method that minimizes circulating current in the transformer. This contrasts with some methods that still rely on circulating current, particularly those that modify the resonant tank.
4) *Compatibility with any rectifier of the main converter:* The hold-up time extension method should be compatible with any type of secondary side rectifier in the main *LLC* converter. As shown in Fig. 22, the proposed method meets this requirement by employing a semiactive full bridge rectifier in the P^3 circuit that can work with any rectifier configuration in the main *LLC* converter.
5) *Less distortion in the resonant current:* The proposed converter minimizes distortion by restoring the sinusoidal waveform during the hold-up period, mitigating the excessive flux density stress typically imposed on the resonant inductor by PWM control.

VI. Conclusion

The proposed converter presented in this article utilizes a semiactive bridge to realize P^3 for hold-up time compensation. By adapting the extended PWM to the semiactive bridge, the proposed converter modifies its effective turns ratio smoothly. The proposed converter has beneficial characteristics for hold-up time compensation such as fewer additional components, effective use of additional components, minimized circulating current, and compatibility with any rectifier type of the main converter.

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Jong-Woo Kim (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from KAIST, Daejeon, South Korea, in 2010, 2012, and 2016, respectively.

From 2016 to 2019, he was a Research Assistant Professor and a Postdoctoral Researcher with Virginia Tech, Blacksburg, VA, USA. From 2019 to 2021, he was a Member of the R&D Staff at Milan M. Jovanović Power Electronics Laboratory, Delta Electronics (Americas), Research Triangle Park, NC, USA. From 2021 to 2022, he was a Power Hardware Engineer with Meta Platforms (formerly Facebook, Inc.), Menlo Park, CA, USA. Since 2022, he has been an Assistant Professor with Konkuk University, Seoul, South Korea. He has authored/coauthored 24 journal articles and more than 20 technical papers in conference proceedings. His research interests include high-efficiency power converters, high power density design with magnetic component integration/PCB winding/widebandgap devices, electromagnetic interference noise reduction techniques, and advanced converter control for data center power and electric vehicle charging infrastructure.