Impact of the Threshold Dispersity Evolution on the Current Sharing of Parallel SiC MOSFETs

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***Abstract*—Parallel connection of silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs) is an efficient solution for high-capacity power converters. However, a more or less dispersity of the parallel chip parameters is inevitable, which may lead to the current imbalance. Due to the existence of dynamic threshold voltage drift, the dispersity of the threshold voltage of the parallel devices during the whole life is vital for the long-term reliability. This article aims to investigate how dispersity evolves and how it affects the current sharing. It is found that the threshold voltage dispersity indeed does not keep constant during the operation, but on the opposite, it increases with gate stress time, especially at elevated temperatures. This leads to the deterioration of the current sharing of parallel devices. A boost converter with two devices paralleled was built and tested, which validated that the threshold voltage dispersity and current imbalance ratio increase with stress time. Finally, a classification method is proposed to suppress the increase in threshold voltage dispersity and current imbalance ratio. These findings are believed to be useful to improve the performance of SiC MOSFETs in parallel applications.**

***Index Terms*—Current imbalance, dynamic threshold voltage drift, parallel silicon carbide (SiC) metal oxide semiconductor field effect transistors (MOSFETs), SiC.**

I. Introduction

DUE to the superior material properties of silicon carbide (SiC), the SiC-based power metal oxide semiconductor field effect transistor (MOSFET) is more suitable for high frequency and high temperature applications compared to silicon-based insulated gate bipolar transistor [1], [2], [3], [4], [5]. These properties make SiC MOSFETs commonly used in high-frequency and high-capacity power converters to improve power density [6], [7], [8], [9].

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However, the current rating of commercial SiC chips is limited due to the low yield rate and complex manufacturing processes in the wafer [10]. The lower current rating of a single chip is insufficient to meet the demands of high-capacity power converters. Thus, it is necessary to parallel multiple discrete devices or modules to achieve a higher current rating [11].

For parallel applications, the current imbalance has always been an important concern [12], [13]. A difference in the threshold voltage (V_{TH}) of parallel devices caused by manufacturing variation can induce static and transient current imbalance [14]. The unequal distribution of transient current can lead to increased current overshoot within the device, posing a risk of exceeding the safe operation area. Besides, the current imbalance can lead to temperature differences among parallel devices, which may induce a thermal runaway situation.

To minimize the influence of threshold voltage difference on parallel current sharing, devices with similar V_{TH} are selected by classification and used in parallel [15], [16]. However, while classification can be effective, it relies on the assumption that device parameters remain constant, which is not true in practice. The presence of electrical and thermal stresses induces device aging, which may lead to modifications in the device parameters.

As a typical case, SiC MOSFETs are used in parallel for the motor drive of electric vehicles (EVs) [17], [18]. However, SiC MOSFETs are not reliable enough, which is believed as a potential cause for EVs being recalled. The rear motor inverter power semiconductor components of EVs included in the recall may have minor manufacturing differences [19]. The point is that the vehicle malfunction occurred after a period of operation. The root cause may be attributed to the parameters of the paralleled SiC MOSFETs are not stable during operation, which results in the deterioration of the current sharing. It takes time for the parameters to change or drift, and this explains why the issue is not detected during the routine test in the production of EVs.

Among the parameters of SiC MOSFETs which can be unstable, the dynamic threshold voltage drift which stems from the high-density traps in the SiC/SiO_2 system is pronounced [20], [21]. According to the mode of gate stress, threshold voltage drift can be classified into static and dynamic [22]. Positive gate bias leads to positive threshold drift, while negative gate bias results in negative threshold drift [23]. The influence of static gate stress on threshold voltage dispersity is reported in [24], which finds that static gate stress has limited influence on threshold voltage dispersity. Compared with static gate stress, the influence of dynamic gate stress on threshold voltage dispersity is more

attractive. This is because the gate stress is dynamic in practical applications, and the threshold voltage drift caused by dynamic gate stress is significantly larger than that caused by static gate stress [25], [26]. For single device, threshold voltage drift under high-bias switching, buck-boost, PFC converter, and three-phase full-bridge inverter has been reported in [27], [28], [29], [30]. The focus of these research works is on the threshold drift and power losses in a single device, rather than different threshold drift among paralleled devices. The influence of dynamic gate stress on threshold voltage dispersity of parallel devices remains to be revealed. The influence of initial threshold mismatch on current sharing has been investigated, but the influence of the evolution of threshold voltage dispersity on current sharing is unknown [11], [31]. Besides, it is unclear how to suppress the increase of threshold voltage dispersity.

The main contributions of this article are as follows.

1) Demonstrated the devices with similar initial threshold voltage display different drifts under the same aging condition, which may provide insights into the potential triggers for the Tesla EVs recall incident.
2) Provided an explanation on why devices with similar initial threshold exhibit different threshold shifts under the same gate stress.
3) Investigated the evolution of threshold voltage dispersity and current sharing characteristics in paralleled devices under practical operating conditions.
4) Proposed a classification method to effectively mitigate the increase in threshold voltage dispersity and improve current sharing characteristics.

In this article, studies are made to investigate the influence of dynamic gate stress on the evolution of threshold voltage dispersity and its impact on current sharing. The threshold voltage drift dispersity under different temperatures is discussed in Section II. After that, the influence of the evolution of threshold voltage dispersity on paralleling SiC MOSFETs is presented in Section III. Section IV presents the boost converter setup and tests. A chips classification method is proposed in Section V. Finally, Section VI concludes this article.

II. Evolution of Threshold Voltage Dispersity

Threshold voltage drift remains an issue that needs to be addressed in SiC MOSFETs. For SiC MOSFETs parallel applications, threshold voltage drift can be divided into two cases. When the dynamic threshold voltage drift (ΔV_{TH}) of each device in parallel is the same, the conduction loss of the devices increases but the current sharing characteristics do not show degradation. Second, threshold voltage drift causes an increase in V_{TH} differences among parallel devices, and devices may lose synchronism during switching and induce electrothermal failures.

A. Dynamic Gate Stress Induced Threshold Drift

To investigate the influence of dynamic gate stress on the threshold voltage dispersity (δ_{VTH}), a test rig is developed, as shown in Fig. 1(a). Sand bath heating is used in the heating system, achieving a maximum heating temperature of 380 °C, while ensuring temperature fluctuations remain within 0.5 °C. Besides, all devices are fixed onto a homogenization plate, ensuring optimal temperature uniformity. The device under test (DUT.P) is a planar SiC MOSFET (SCT10N120AG), and type DUT.T is a trench SiC MOSFET (SCT3120AL).

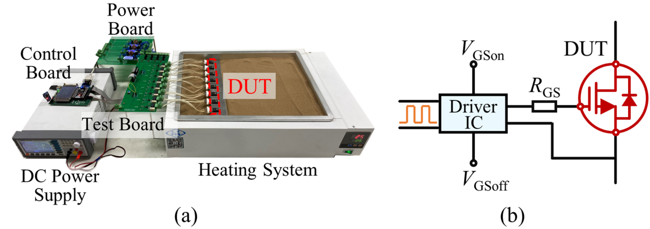


Fig. 1. (a) Test rig for measuring threshold voltage drift under dynamic gate stress. (b) Gate drive circuit for generating dynamic gate stress. The gate stress of the eight channels is identical.

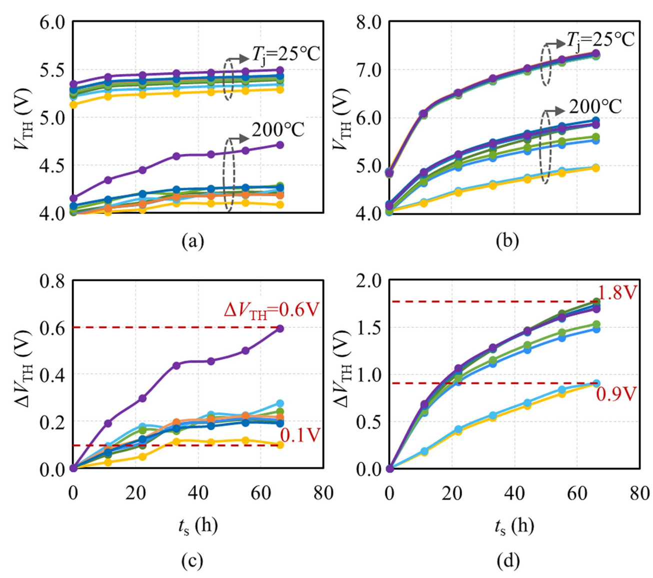


Fig. 2. Threshold voltage of (a) DUT.P and (b) DUT.T under dynamic gate stress with V_{GS} of 20 / –15 V, T_{j} of 25 °C and 200 °C, switching frequency of 150 kHz, duty cycle of 50%. Threshold voltage drift ΔV_{TH} of (c) DUT.P and (d) DUT.T under T_{j} of 200 °C. The number of device samples is 8.

The threshold voltage was measured at $I_{\mathrm{D}} = 10$ mA with gate and drain electrodes shorted. To shorten the gate stress time (t_{s}), the ON-state (V_{GSon}) and OFF-state gate voltage (V_{GSoff}) of dynamic gate stress were set to +20 and –15 V, and the duty cycle is 50%. To avoid overshoot in the gate stress waveform, the gate resistor R_{GS} in Fig. 1(b) is 27 Ω.

As shown in Fig. 2, the threshold voltage of DUT.P and DUT.T drift positively under dynamic gate stress with $T_{\mathrm{j}} = 25 / 200$ °C, which is attributed to the charging and discharging of traps [22], [26]. When a voltage is applied to the gate electrode, an electric field is introduced, driving carriers in SiC tunneling into or out from the traps. The captured charges establish an extra electric field, resulting in a change in the threshold voltage. Besides, the dynamic drift of the threshold voltage persists over extended periods of hours without significant self-recovery [25].

TABLE I
STATISTICAL PARAMETERS UNDER DIFFERENT TEMPERATURE

t_s	R_{VTH}(25 °C) DUT.P/T	R_{VTH}(200 °C) DUT.P/T	C.V$_{VTH}$(25 °C) DUT.P/T	C.V$_{VTH}$(200 °C) DUT.P/T
0 h	4.0%/0.9%	4.5%/4.1%	1.1%/0.3%	1.6%/1.5%
33 h	3.9%/0.9%	11.0%/17.4%	1.1%/0.3%	3.3%/6.5%
66 h	3.8%/1.0%	12.4%/17.8%	1.1%/0.4%	4.0%/6.8%

To present the aging extent of the threshold voltage of DUT.P and DUT.T, Fig. 2 demonstrates the threshold voltage drift of devices. When T_j = 25 °C, ΔV_{TH} of eight samples is almost the same, i.e., the threshold voltage drift dispersity is small at room temperature. However, ΔV_{TH} of eight samples is not exactly the same at T_j = 200 °C, which means the threshold voltage drift dispersity becomes larger at high temperature, as shown in Fig. 2(c) and (d). This may be caused by variances introduced during the manufacturing process. After 66 h high temperature dynamic gate stress, the largest drift magnitude of DUT.P / DUT.T is 0.6 / 1.8 V, followed by 0.3 / 1.7 V, while the smallest is 0.1 / 0.9 V.

B. Evolution of Threshold Dispersity

As mentioned previously, the threshold voltage of DUT.P and DUT.T drift dispersedly under high temperature. To investigate the evolution of threshold voltage dispersity under dynamic gate stress, the statistical parameters are analyzed in Table I. It can be seen from Table I that the statistical parameters such as the relative range ($R_{VTH} = (V_{THmax} - V_{THmin}) / V_{THavg}$) and coefficient of variation (C.V$_{VTH} = \sigma_{VTH} / V_{THavg}$) of threshold voltage are used to describe δ_{VTH}, where V_{THmax}, V_{THmin}, V_{THavg} are the maximum, minimum, and average threshold voltage of the samples, and σ_{VTH} is the standard deviation of V_{TH}. R_{VTH} and C.V$_{VTH}$ increase with the increase of t_s when T_j = 200 °C.

As the relative range is commonly used to characterize the imbalance of parameters, it is used in this article as a representation of threshold voltage dispersity [10], [13]. Therefore, δ_{VTH} is determined by

$$\delta_{VTH} = \frac{V_{THmax} - V_{THmin}}{V_{THavg}}. \quad (1)$$

When T_j = 200 °C, δ_{VTH} of DUT.P and DUT.T increase rapidly at first and gradually saturate afterward, as shown in Fig. 3. For DUT.P, δ_{VTH} increases from 4.5% to 12.4%, and δ_{VTH} of DUT.T increases from 4.1% to 17.8%. However, δ_{VTH} is almost unchanged at 25 °C. Thus, there arises a question of why δ_{VTH} increases at high temperature.

C. Analysis of the Increase in Threshold Dispersity

As mentioned previously, the previous experiments in Fig. 3 have shown that parallel devices demonstrate an acceptable threshold voltage dispersity in the initial stage. However, the threshold voltage dispersity worsens with extended gate stress time, especially at high temperature. This result may provide insights into the potential triggers for the Tesla EVs recall incident, i.e., there are no problems with EVs during their early usage, but the vehicle malfunction occurred after a period of operation.

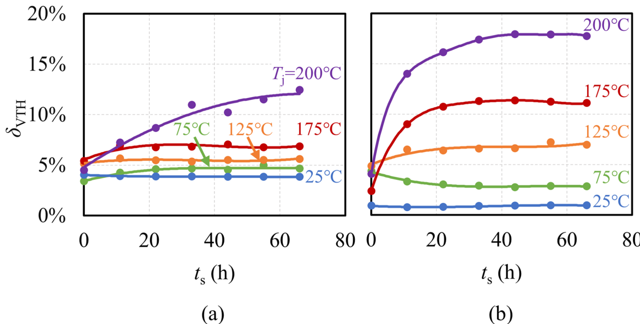


Fig. 3. Threshold voltage dispersity of (a) DUT.P and (b) DUT.T under dynamic stress with frequency of 150 kHz. The number of device samples is 8 at each temperature. The ordinate of (b) is the same to that of (a).

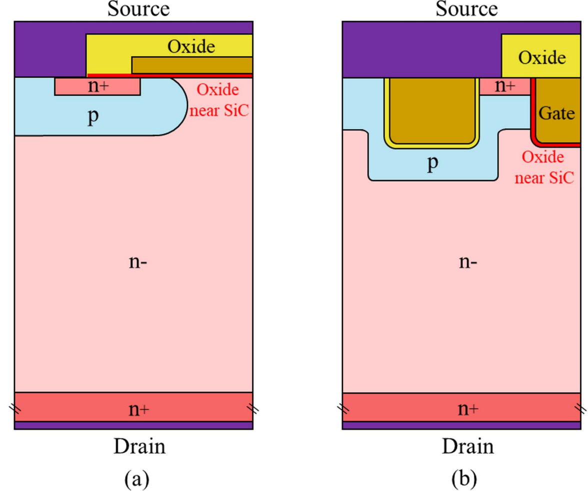


Fig. 4. Cell structure of (a) DUT.P and (b) DUT.T. There is a higher concentration of traps in the oxide near silicon carbide.

Compared to Si MOSFET, a lot of traps exist in the gate oxide near the channel of SiC MOSFET due to the immature process, as shown in Fig. 4. Charges are trapped or released by traps, resulting in threshold voltage instability. The threshold voltage is given by

$$V_{TH} = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_S \cdot q \cdot N_A}}{C_{OX}}\sqrt{2\psi_B} \quad (2)$$

where Ψ_B is the Fermi level from intrinsic Fermi level, N_A is the effective channel doping concentration, ε_s is the SiC dielectric constant, and q is the elementary charge. The flat band voltage V_{FB} is given by

$$V_{FB} = \phi_{MS} - \frac{Q_{OX}}{C_{OX}} \quad (3)$$

where ϕ_{MS} is the work function difference between metal and semiconductor, and Q_{OX} is the oxide charge density. As traps capture positive charges, Q_{OX} increases, resulting in a decrease in threshold voltage. Conversely, when traps release positive

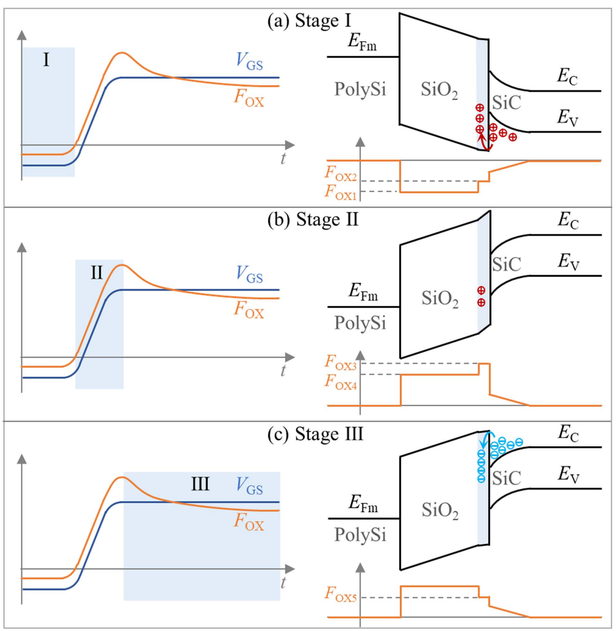


Fig. 5. Evolution of the total electric field in gate oxide near the interface of SiO_2/SiC with the gate voltage transfers from OFF-state gate voltage to ON-state gate voltage.

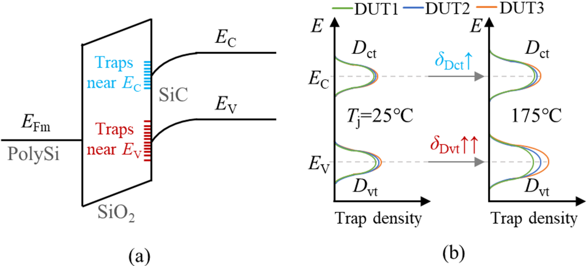


Fig. 6. (a) Traps near the conduction band E_C are primarily composed of electron traps, while traps near the valence band E_V are predominantly hole traps. (b) Normal distribution of trap density in different devices at room and elevated temperatures, and the trap density dispersity increases with temperature, especially in the case of hole trap density.

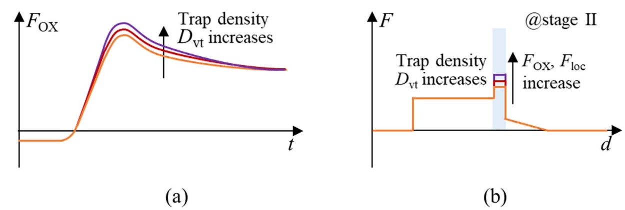


Fig. 7. Influence of trap density on the total electric field in gate oxide near the interface of SiO_2/SiC.

charges or capture negative charges, Q_{OX} decreases, leading to an increase in threshold voltage.

Compared to positive bias temperature instability, the amplitude of dynamic threshold voltage drift is larger. This is attributed to the local electric field enhancement in the gate oxide region, i.e., threshold drift is accelerated due to the local electric field enhancement. The total electric field in gate oxide near the interface of SiO_2/SiC, i.e., F_{OX} is given by $F_{OX} = F_{GS} + F_{loc}$, where F_{GS} is the electric field induced by the gate voltage and F_{loc} is the local electric field induced by trapped charges. Under dynamic gate stress, when the gate is switched from negative to positive bias, the change in electric field can be divided into the following three stages, as shown in Fig. 5.

1) Gate voltage and F_{OX} are less than 0. The direction of electric field is directed from SiC to SiO_2 (the positive direction of the electric field is defined as from SiO_2 to SiC), and most electrons within the gate oxide are released. Holes are captured under a negative electric field, which induces a positive local electric field, and the number of captured holes is primarily determined by the trap density near the valence band (D_{vt}). The local electric field is opposite to the direction of F_{GS}, leading to a reduction in F_{OX} by F_{OX2}–F_{OX1}.
2) F_{OX} transfers from negative to positive. Oxide traps capture electrons and release holes, and the capture or release of carriers takes time, especially for holes. Due to the short period in Stage II, the holes captured in Stage I are not entirely released in Stage II, meaning that some holes still exist within the traps in Stage II. Unreleased holes form $F_{loc} = F_{OX3} - F_{OX4}$, which is in the same direction as F_{GS}, resulting in an increase of F_{OX} by $F_{OX3} - F_{OX4}$. A larger F_{OX} results in a greater tunneling probability, consequently driving more electrons into the oxide, i.e., Q_{OX} decreases and threshold voltage drift is accelerated. The acceleration of threshold voltage drift is attributed to the enhanced local electric field, and the acceleration phase occurs only during switch transitions.
3) As the gate voltage rises to the ON-state gate voltage, most of the holes are released, and the traps continue to capture electrons. The captured electrons induce a local electric field, leading to a decrease in F_{OX}–F_{OX5}.

The threshold voltage drift is influenced by the trap density [32]. Traps distribution is shown in Fig. 6(a), and the traps near the valence band E_V are primarily hole traps. The higher the trap density near the valence band, the more holes are trapped in Stage I, which means that a higher concentration of holes is retained in the traps during Stage II. Higher hole density in Stage II corresponds to an increased local electric field, i.e., F_{OX} and F_{loc} increase, which drives more electrons into the oxide, as shown in Fig. 7. In other words, according to (2) and (3), an increase in D_{vt} results in a more significant decrease in Q_{OX}, consequently leading to a greater rise in threshold voltage.

As the channel mobility can be improved by decreasing electron trap density near the conduction band E_C, present gate oxide optimization processes primarily focus on reducing the trap density near E_C. However, the optimization of traps near E_V remains insufficient. Thus, trap density near E_V might be higher than that near E_C, as shown in Fig. 6(b). Besides, the oxide trap density in devices may differ from one another, especially at high temperature. Some traps are activated as the temperature rises, and the number of activated traps may be different in devices [23]. Differences in trap density among parallel devices

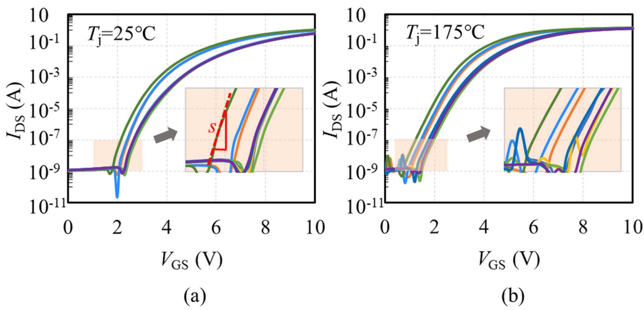


Fig. 8. Subthreshold I_{DS}–V_{GS} characteristics of DUT.T with T_j of 25 °C and 175 °C, V_{DS} of 1 V. The number of device samples is 8 at $T_j = 25$ °C or 175 °C.

TABLE II
SUBTHRESHOLD SWING IMBALANCE

T_j	δ_S DUT.P	δ_S DUT.T
25 °C	7.6%	16.3%
175 °C	18.7%	28.0%
200 °C	34.1%	34.7%

cause differences in the local electric field of parallel devices during switching transitions, consequently inducing potential differences in threshold voltage drift among parallel devices.

Trap density in MOSFET can be characterized by the subthreshold swing of device [33], [34]. The number of electrons in the channel is very small at the subthreshold region, and the transfer characteristics can be affected by the trapping and emission electrons of traps. The subthreshold swing of the SiC MOSFET is a function of the trap density in the device. The higher the trap density, the larger the subthreshold swing, and vice versa. The subthreshold swing is given by

$$s = \frac{dV_{GS}}{d(\log_{10} I_{DS})}. \quad (4)$$

The subthreshold characteristic of DUT.T is shown in Fig. 8, which is measured by Keithley 2612A, and the gate potential was swept from –3 to 10 V. The subthreshold swing of the eight devices at 25 °C showed better consistency compared to that at 175 °C. The ratio of subthreshold swing imbalance (δ_S) which is defined as ($s_{max} - s_{min}$) / s_{avg} is shown in Table II, and the device samples of DUT.P and DUT.T are 8. δ_S increases with the increase of T_j, i.e., an increase in T_j leads to a greater dispersity of trap density, which means δ_{VTH} may become larger as T_j increases.

The trap density of devices at 25 °C is almost the same, which can be observed from similar drift magnitudes of different devices. As shown in Fig. 2, devices exhibit similar ΔV_{TH} at room temperature, but ΔV_{TH} of devices become dispersive at high temperature. This is because high temperature causes an increase in the differences in the trap density among devices, and the dispersity of trap density near valence band δ_{Dvt} increases significantly, as shown in Fig. 6(b), which means the dispersity of F_{OX} and F_{loc} increase. The increased dispersity of F_{OX} leads to an increased difference in the number of captured electrons. According to (2) and (3), the dispersity of ΔV_{TH} becomes larger under high temperature dynamic gate stress, and δ_{VTH} increases, as shown in Fig. 3. Besides, threshold voltage decreases with increasing temperature, and δ_{VTH} increases with the decrease in V_{THavg} according to (1).

When measuring the initial threshold voltage of the devices, the gate voltage gradually increases from 0 V to V_{TH}. At this point, according to (2) and (3), the initial V_{TH} depends on the charge captured by traps near E_C at the time of V_{TH} measurement and the pre-existing charge in the oxide layer. The tested devices in Fig. 3 are all from the same batch, and the present gate oxide process effectively controls the range of trap density near the conduction band D_{ct}, i.e., the dispersity of trap density near conduction band δ_{Dct} is small at both high and room temperature. This means the pre-existing charge in the oxide layer and the charge captured by traps near E_C during V_{TH} measurement of the fresh parallel devices are almost the same. Thus, at $t_s = 0$ h, parallel devices demonstrate an acceptable threshold voltage dispersity at both high and room temperature. However, high temperature leads to a significant increase in δ_{Dvt} of parallel devices. Devices with different D_{vt} capture a varying number of holes, which means the local electric fields vary among different devices. Thus, the dispersity of ΔQ_{OX} and ΔV_{TH} increase with stress time, which means the threshold dispersity worsens with extended t_s. Besides, ΔV_{TH} caused by dynamic gate stress does not self-recover within several hours.

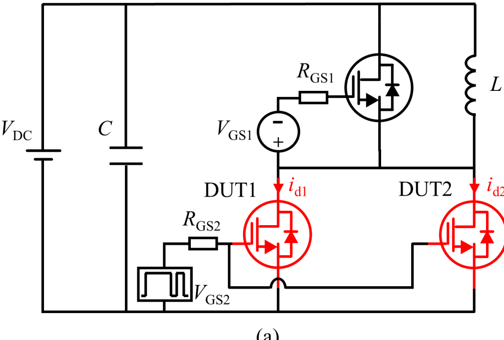
III. IMPACT OF THRESHOLD VOLTAGE DISPERSITY ON CURRENT IMBALANCE

Dynamic threshold drift results in an increase in threshold voltage, and the magnitude of threshold drift may vary among parallel devices, i.e., the threshold voltage dispersity may increase with stress time. The impact of threshold mismatch on the complementary switch is limited, and the focus of this article is to investigate the influence of threshold mismatch on current sharing characteristics. With higher threshold voltage dispersity, there is a greater likelihood of unequal current distribution among the parallel devices. This imbalance can result in performance degradation and potential reliability issues in the system.

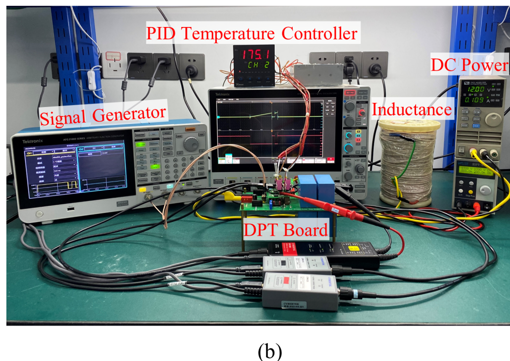
To analyze the influence of the evolution of threshold voltage dispersity on current imbalance, a double pulse test (DPT) circuit is developed, as shown in Fig. 9. Two devices are parallel connected in the lower arm, and the waveforms of their gate-to-source voltages are the same. Besides, to ensure uniform parasitic inductance in the circuits of DUT1 and DUT2, the current path length of DUT1 is almost equivalent to that of DUT2, as shown in Fig. 10. Overall test conditions are selected as $V_{dc} = 300$ V, $I_L = 20$ A, $V_{GS1} = -5$ V, $V_{GS2} = 20$ / –5 V, $R_{GS1} = R_{GS2} = 5.1\ \Omega$, and $L = 860\ \mu$H.

The static and transient current sharing of parallel SiC MOSFETs are analyzed by using a parallel DPT platform. The ratio of current imbalance (δ_i) at parallel devices is given by

$$\delta_i = \frac{i_{max} - i_{min}}{i_{avg}} \quad (5)$$



(a)



(b)

Fig. 9. (a) Circuit diagram of DPT. The input voltage is 300 V, and the total current is 20 A. (b) Experimental setup of DPT. The heating platform is mainly composed of a temperature controller, two ceramic heating plates.

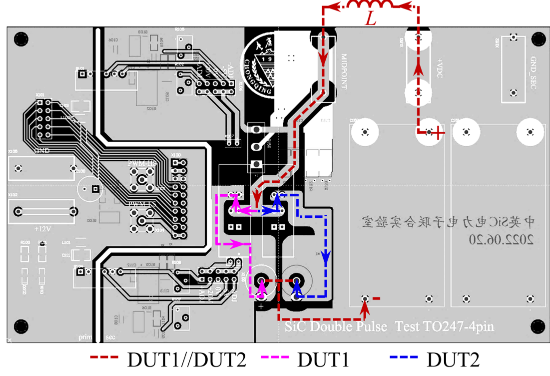


Fig. 10. Current flow in devices of DPT. The red line represents the shared current path for DUT1 and DUT2, the purple line is the current path for DUT1, and the blue line represents the current path for DUT2.

where i_{max}, i_{min}, and i_{avg} are the maximum, minimum, and average current of samples, respectively.

To study the influence of the evolution of threshold voltage dispersity on δ_i, identical dynamic gate stress is applied to both DUT.T1 and DUT.T2 under the test rig in Fig. 1. The threshold voltage difference between DUT.T1 and DUT.T2 ($\Delta V_{TH} = V_{TH2}–V_{TH1}$) increases from –0.1 to 0.3 V at $t_s = 36$ h, followed

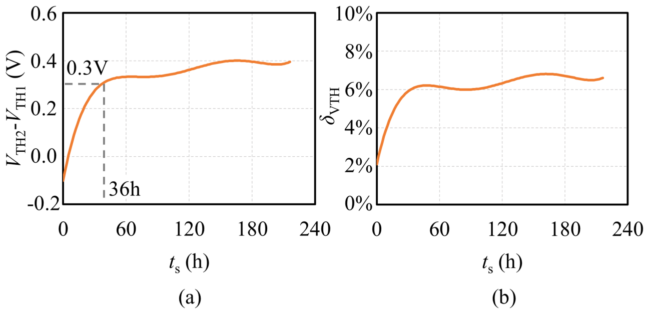


Fig. 11. (a) Impact of the gate stress time on the threshold difference between DUT.T1 and DUT.T2 with T_j of 175 °C, switching frequency of 300 kHz. (b) Impact of the gate stress time on δV_{TH} with T_j of 175 °C.

TABLE III
STATIC CURRENT IMBALANCE

t_s	δ_{is}(25 °C)	δ_{is}(175 °C)
0 h	0.8%	0.7%
36 h	6.3%	4.8%
216 h	5.7%	4.3%

by a gradual increase to 0.4 V at 216 h, as shown in Fig. 11(a). δ_{VTH} shows a similar growth trend as $V_{TH2}–V_{TH1}$.

A. Static Current Sharing

For parallel devices, the static imbalance current Δi_s which is defined as $i_{smax} - i_{smin}$. Static current sharing can be simplified as the current sharing among parallel resistors. The ON-resistance (R_{dson}) of SiC MOSFET is mainly composed of the channel resistance (R_{ch}) and drift region resistance (R_{drift}), which is not affected by t_s. Δi_s is given by, (6) shown at the bottom of this page, where $R_{ch\text{-}imax}$ and $R_{drift\text{-}imax}$ are the channel and drift region resistance of the device with maximum static current, $R_{ch\text{-}imin}$ and $R_{drift\text{-}imin}$ are the channel and drift region resistance of the device with minimum static current, R_{chn} and R_{driftn} are the channel and drift region resistance of DUTn. For DUT.T1 and DUT.T2, can be rewritten as

$$\Delta i_s = \left| \frac{R_{ch2} - R_{ch1} + R_{drift2} - R_{drift1}}{R_{ch1} + R_{ch2} + R_{drift1} + R_{drift2}} \right| \times I_{total}. \quad (7)$$

At $T_j = 25$ °C, Δi_s first rises from 0.07 to 0.6 A ($t_s = 36$ h) and then gradually drops to 0.5 A ($t_s = 216$ h) with prolonged t_s, as shown in Fig. 12. According to (5), the static current imbalance (δ_{is}) is given by Δi_s / 10 A, as shown in Table III. δ_{is} rapidly increases at first and then slightly decreases.

R_{ch1}, R_{ch2}, and $R_{ch2}–R_{ch1}$ increase with the increment of V_{TH} and $V_{TH2}–V_{TH1}$, as shown in Fig. 13 [35]. R_{drift} remains stable during dynamic gate stress. When R_{dson} of DUT.T2 is larger

$$\Delta i_s = \frac{1/\left(R_{ch-imax} + R_{drift-imax}\right) - 1/\left(R_{ch-imin} + R_{drift-imin}\right)}{1/\left(R_{ch-imin} + R_{drift-imin}\right) + 1/\left(R_{ch-imax} + R_{drift-imax}\right) + \cdots + 1/\left(R_{chn} + R_{driftn}\right)} \times I_{total} \quad (6)$$

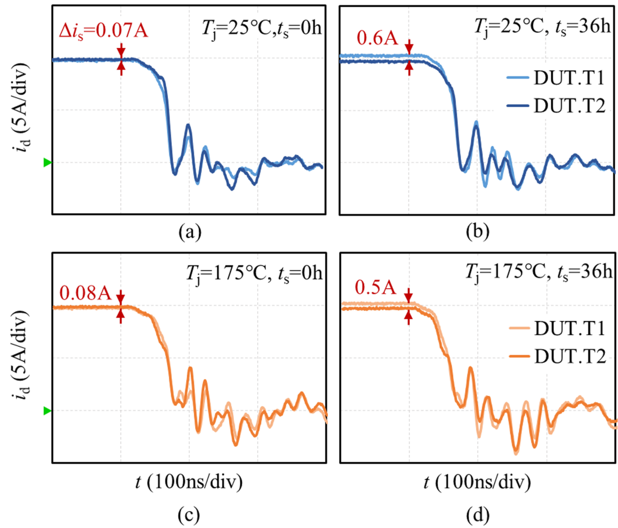


Fig. 12. Turn OFF characteristics of DUT.T with T_j of 25 °C and 175 °C. Threshold drift with T_j of 175 °C and switching frequency of 300 kHz.

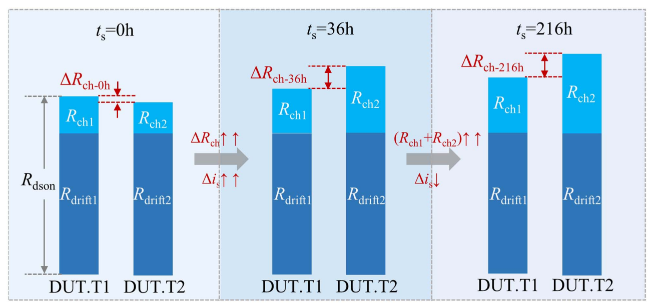


Fig. 13. Evolution of channel resistance and drift region resistance with T_j of 25 °C. ΔR_{ch} is defined as R_{chmax}–R_{chmin}. $\Delta R_{\text{ch-0h}}$ is the difference between R_{ch1} and R_{ch2} at $t_s = 0$ h.

than that of DUT.T1, (7) is rewritten as

$$\Delta i_s = \frac{R_{\mathrm{ch2}} - R_{\mathrm{ch1}} + R_{\mathrm{drift2}} - R_{\mathrm{drift1}}}{R_{\mathrm{ch1}} + R_{\mathrm{ch2}} + R_{\mathrm{drift1}} + R_{\mathrm{drift2}}} \times I_{\mathrm{total}} \quad (8)$$

according to (8), Δi_s increases with the increase of R_{ch2}–R_{ch1}, and Δi_s decreases with the increase of $R_{\mathrm{ch1}} + R_{\mathrm{ch2}}$. When t_s is between 0 and 36 h, R_{ch2}–R_{ch1} increases rapidly. Δi_s is dominated by R_{ch2}–R_{ch1}, and Δi_s increases as t_s increases, i.e., δ_{is} increases as t_s increases. δ_{is} in $t_s = 216$ h is smaller than that in $t_s = 36$ h. This is because R_{ch2}–R_{ch1} at $t_s = 216$ h is almost the same as R_{ch2}–R_{ch1} at $t_s = 36$ h, and $R_{\mathrm{ch1}} + R_{\mathrm{ch2}}$ at $t_s = 216$ h is larger than that at 36 h.

In addition, δ_{is} of 175 °C is smaller than that of 25 °C at the same aging time, as shown in Table III. As T_j goes up, R_{ch} decreases, which is caused by the decrement of threshold voltage, but R_{drift} and R_{dson} increase due to the positive temperature coefficient, as shown in Fig. 14. The proportion of R_{ch} in R_{dson} decreases as T_j increases, and the influence of R_{ch2}–R_{ch1} on Δi_s is weakened. Devices exhibit a linear relationship between V_{TH} and temperature, with their slopes being almost the same [36]. As the temperature increases, V_{TH2}–V_{TH1} remains essentially unchanged, and the same holds true for R_{ch2}–R_{ch1}. The

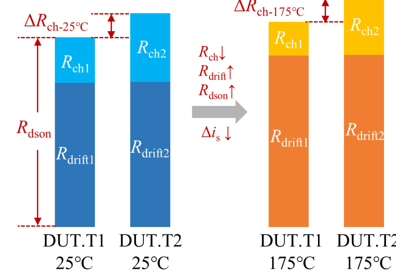


Fig. 14. Impact of temperature on channel resistance and drift region resistance. $\Delta R_{\mathrm{ch}-25^\circ\mathrm{C}}$ is the difference between R_{ch1} and R_{ch2} at $T_j = 25$ °C.

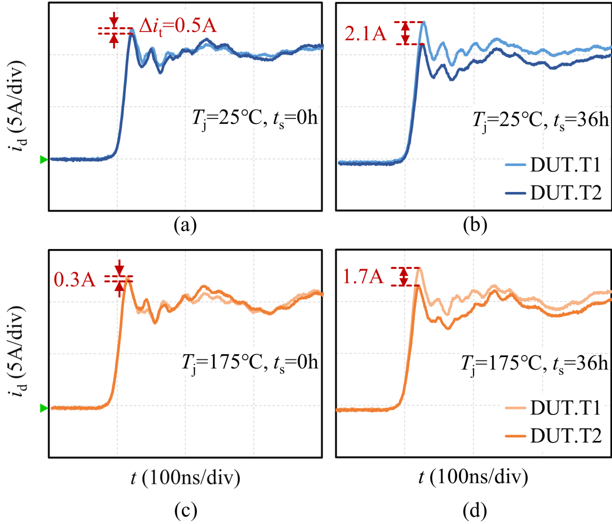


Fig. 15. Turn ON characteristics of DUT.T with T_j of 25 °C and 175 °C. Threshold drift with T_j of 175 °C and switching frequency of 300 kHz.

numerator of Δi_s in (8) remains almost unchanged, while its denominator increases. Thus, Δi_s decreases with the increase of temperature, i.e., δ_{is} is smaller at high temperature.

B. Dynamic Current Sharing

The peak value of transient imbalance current Δi_t which is defined as i_{tmax}–i_{tmin} increased from 0.5 to 2.1 A at $T_j = 25$ °C, as shown in Fig. 15. The drain-source current of SiC MOSFET is given by [35]

$$i_d = \frac{\mu_{\mathrm{ch}} C_{\mathrm{OX}} Z}{2L_{\mathrm{ch}}} (V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 \quad (9)$$

where μ_{ch} is the channel mobility, C_{OX} is the gate oxide capacitance per unit area, Z is the channel width, and L_{ch} is the channel length. When $V_{\mathrm{TH2}} \geq V_{\mathrm{TH1}}$, Δi_t caused by the threshold difference between DUT.T1 and DUT.T2 can be obtained by [14]

$$\begin{aligned} \Delta i_t &= -\Delta i_{ds} = -\frac{\partial i_d}{\partial V_{\mathrm{TH}}} \Delta V_{\mathrm{TH}} \\ &= \frac{\mu_{\mathrm{ch}} C_{\mathrm{OX}} Z}{L_{\mathrm{ch}}} (V_{\mathrm{GS}} - V_{\mathrm{TH1}})(V_{\mathrm{TH2}} - V_{\mathrm{TH1}}). \end{aligned} \quad (10)$$

TABLE IV
DYNAMIC CURRENT IMBALANCE

t_s	δ_{it}(25 °C)	δ_{it}(175 °C)
0 h	3.8%	2.4%
36 h	16.6%	13.5%
216 h	15.9%	12.6%

According to (10), Δi_t increases with the increase of V_{TH2}–V_{TH1}. However, it should be noted that Δi_t does not always exhibit an increasing trend with increasing t_s. Δi_t at 25 °C first increases from 0.5 to 2.1 A ($t_s = 36$ h) and then slowly decreases to 1.9 A (216 h), which is caused by the variation in V_{TH2}–V_{TH1}. According to (5), the ratio of transient current imbalance (δ_{it}) is given by (i_{tmax}–i_{tmin}) / i_{tavg}. For DUT.T1 and DUT.T2, δ_{it} can be rewritten as Δi_t / 10A, as shown in Table IV. V_{TH1}, V_{TH2}, and V_{TH2}–V_{TH1} increase with t_s. According to (10), Δi_t is influenced not only by V_{TH2}–V_{TH1} but also by V_{TH1}. Δi_t increases with the increase of V_{TH2}–V_{TH1}, and decreases as V_{TH1} increases. Δi_t is dominated by V_{TH2}–V_{TH1} when t_s is $0 \sim 36$ h, and Δi_t increases as V_{TH2}–V_{TH1} increases, i.e., δ_{it} increases as t_s increases. When t_s is extended from 36 to 216 h, V_{TH1} and V_{TH2} increased by more than 1 V, while V_{TH2}–V_{TH1} only increased by 0.1 V. Consequently, δ_{it} shows a decrease, which is attributed to the dominance of V_{TH}.

It can be seen from Table IV that δ_{it} of $T_j = 175$ °C is smaller than that of 25 °C, i.e., the transient current sharing characteristic is better at $T_j = 175$ °C. This is because high temperatures can cause a decrease in channel mobility (μ_{ch}) [37]. According to (10), Δi_t decreases with the decrease of μ_{ch}. High temperature increases Δi_t by reducing the threshold voltage, but the effect of the decrease in μ_{ch} on Δi_t is more dominant. Thus, δ_{it} is smaller at high temperature.

IV. IMPACT OF THRESHOLD VOLTAGE DISPERSITY ON PARALLEL APPLICATION

The increase in threshold dispersity of parallel devices under dynamic gate stress has been analyzed in previous sections. All devices were fixed onto a homogenization plate in Fig. 1, ensuring optimal temperature uniformity. Besides, only gate stress was applied to the devices, while excluding drain voltage and current stress. In parallel applications, devices not only experience stress from the gate voltage but also from the drain voltage and current. Besides, the threshold voltage stability may be influenced by the drain voltage and current. Threshold voltage imbalance can cause current imbalance, leading to temperature differences among devices. At the same time, threshold voltage dispersity is affected by current and temperature imbalances.

To investigate the influence of combined stress (gate voltage, drain voltage, drain current and temperature) on threshold voltage dispersity in the parallel application, a boost circuit is developed. Two devices are parallel connected as a switch unit, and the waveforms of their gate-to-source voltages are the same, as shown in Fig. 16(b). The converter waveforms are shown in Fig. 16(c), V_{OUT} is about 200 V. The temperature change of devices is monitored using a temperature monitor, as shown in Fig. 17. Facilities utilized in the boost circuit are listed in Table V. Probes are far away from the heat source, and they are within the typical working temperature range. The device under test (DUT. T) is a trench SiC MOSFET (SCT3120AL). Overall test conditions are selected as $V_{dc} = 100$ V, $V_{OUT} = 200$ V, $V_{GS} = 15$ / –8 V, $R_{GS} = 39$ Ω, $L = 2$ mH, $i_{OUT} = 5$ A, and the total current of DUTs is 10 A. When the inductance is

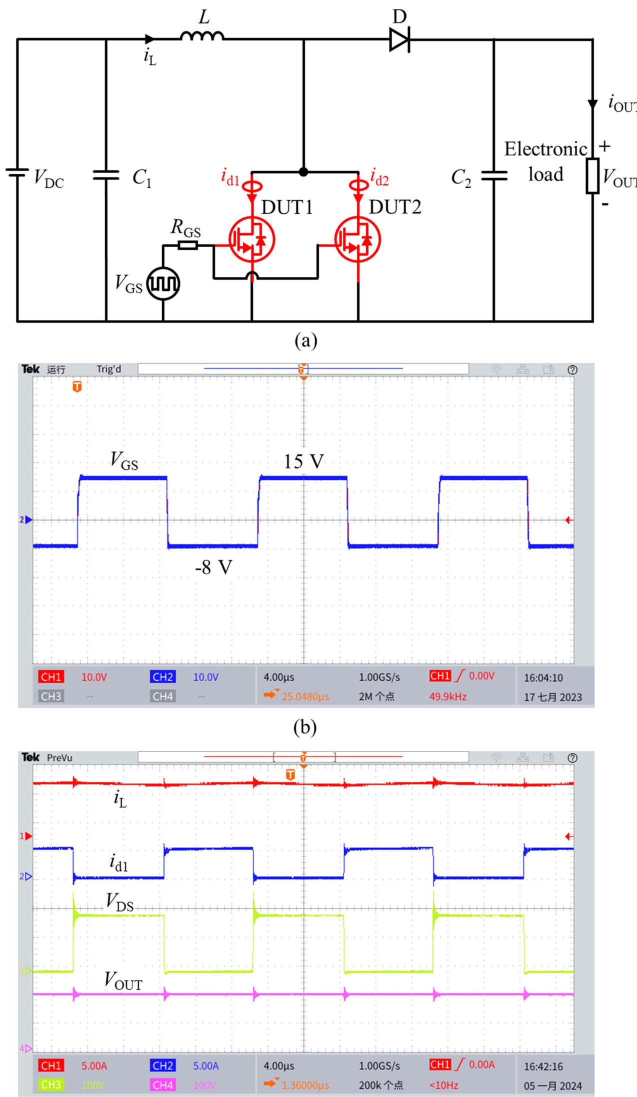


Fig. 16. (a) Circuit diagram of Boost, and the total current of DUT1 and DUT2 is 10 A. (b) Dynamic gate stress of DUT1 and DUT2 with V_{GS} of 15 / –8 V, switching frequency of 50 kHz, and duty cycle of 50%. The gate stress of DUT1 and DUT2 are the same. (c) Converter waveforms.

TABLE V
FACILITIES USED IN BOOST

Facilities	Type	Parameter	Function
Digital oscilloscope	Tektronix TBS2204B	200MHz	Capture curves
Current probe	Cybertek HCP8030D	100MHz	Measure i_d
Voltage probe	Cybertek DP6150A	100MHz	Measure V_{OUT}
Temperature monitor	Yudian AIP5	1point/s	Measure T_j

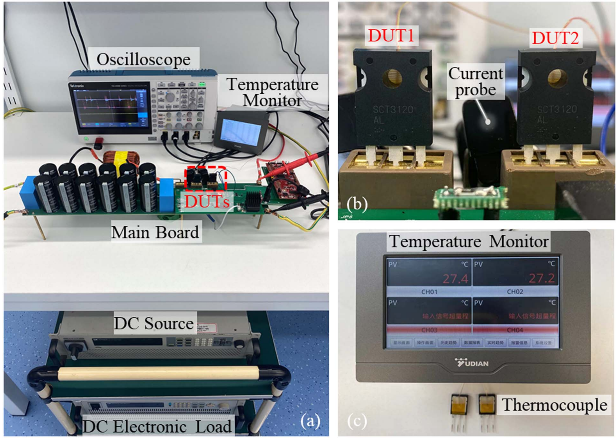


Fig. 17. (a) Experimental setup of boost. (b) Two devices are connected in parallel in the boost circuit. (c) Temperature monitor is used for monitoring the temperature difference between the parallel devices, collecting temperature data every 1 s through the thermocouple.

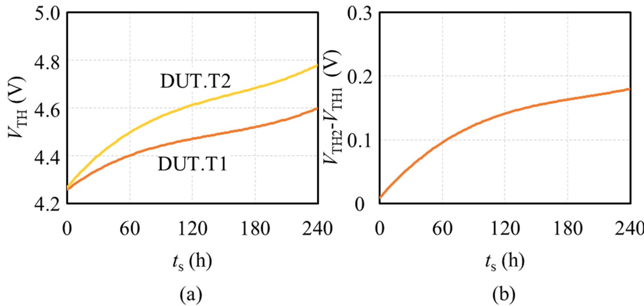


Fig. 18. Threshold voltage drift of DUT.T under boost circuit application. DUT.T under dynamic gate stress with V_{GS} of 15 / –8 V, switching frequency of 50 kHz, and duty cycle of 50%. V_{TH1} is the threshold voltage of DUT.T1, and V_{TH2} is the threshold voltage of DUT.T2.

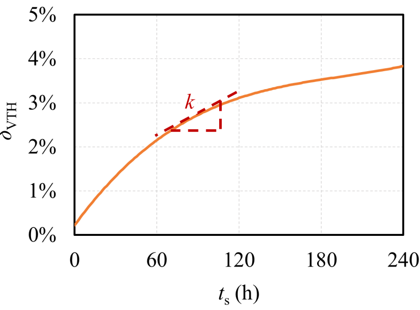


Fig. 19. Threshold voltage dispersity of DUT.T under boost circuit application. DUT.T under dynamic gate stress with V_{GS} of 15/–8 V, switching frequency of 50 kHz, and duty cycle of 50%.

small, analyzing the static current sharing becomes challenging, as the device current fails to reach stability after overshooting. Thus, there is a preference for selecting inductances with larger values. Besides, small differences in current sharing behavior were observed among 500 μH, 1 mH, and 2 mH when V_{TH} of parallel devices is mismatched.

The choice of a larger R_{GS} is intended to suppress significant gate voltage overshoot, ensuring the comparability of ΔV_{TH} under different stress conditions [38]. Although R_{GS} is set to 39 Ω, the switching speed of device remains adequate, meeting the application conditions for SiC MOSFETs. The dV_{GS}/dt of DUT.T (dV_{GS}/dt_ON = 0.11 V/ns, dV_{GS}/dt_OFF = 0.17 V/ns) is within the recommended range given in JEP195. The threshold voltage dispersity is a function of gate resistance. Reducing gate resistance accelerates the rise in threshold voltage dispersity of parallel devices when devices have different oxide trap densities.

A. Evolution of Threshold Dispersity

Under boost application, the threshold voltage of DUT.T1 and DUT.T2 drift positively. After 240 h gate stress, the drift magnitude of DUT.T1 is 0.34 V, and that of DUT.T2 is 0.51 V, as shown in Fig. 18(a). Besides, the threshold difference between DUT.T1 and DUT.T2 increases with aging time, and V_{TH2}–V_{TH1} increase from 0.01 to 0.18 V, which means the threshold dispersity may increase with the aging time.

The evolution of threshold voltage dispersity is shown in Fig. 19, the threshold voltage dispersity increases with aging time, which is similar to V_{TH2}–V_{TH1}. Besides, it can be observed that the slope (k) of curve in Fig. 19 decreases with the aging time, i.e., δ_{VTH} exhibits a rapid growth rate at the beginning, followed by a slower growth rate.

B. Evolution of Current Sharing

As mentioned previously, δ_{VTH} increases with the aging time, which means a possible deterioration in current sharing. To investigate the evolution of current sharing in boost application, the current sharing between DUT.T1 and DUT.T2 in the steady state (the device temperature and current remain relatively stable in the short term) under different t_s is analyzed. Besides, the current sharing process of parallel devices with unequal threshold voltage from room temperature startup to steady state is studied.

When t_s is 0.5 h, DUT.T1 and DUT.T2 have already achieved thermal stability, as shown in Fig. 20. Due to the similar initial threshold of DUT.T1 and DUT.T2, devices exhibit acceptable current sharing performance. Δi_t at t_s = 0.5 h is 0.32 A, and Δi_s is 0.08 A. With about 240 h of stress aging, the threshold difference between DUT.T1 and DUT.T2 increases, resulting in a deterioration in the current sharing of the devices. Δi_t at t_s = 240 h is 1.44 A, and Δi_s is 0.64 A.

For the boost application in Fig. 17, the static current imbalance and dynamic current imbalance can be written as Δi_s / 5 A and Δi_t / 5 A, as shown in Fig. 21. δ_{it} and δ_{is} rapidly increase at first and then the rate of increase becomes slower, which is similar to δ_{VTH}. According to (10), during the stage of rapid growth, Δi_t is dominated by V_{TH2}–V_{TH1}, and Δi_t increases as V_{TH2}–V_{TH1} increases, i.e., δ_{it} increases as t_s increases. Δi_s is dominated by R_{ch2}–R_{ch1} or V_{TH2}–V_{TH1}. According to (8), Δi_s increases as R_{ch2}–R_{ch1} increases, i.e., δ_{is} increases as t_s increases. After the stage of rapid growth, the growth rate of V_{TH2}–V_{TH1} declines, and the same trend is observed for δ_{it} and δ_{is}. Besides, δ_{is} increases with total current of parallel devices,

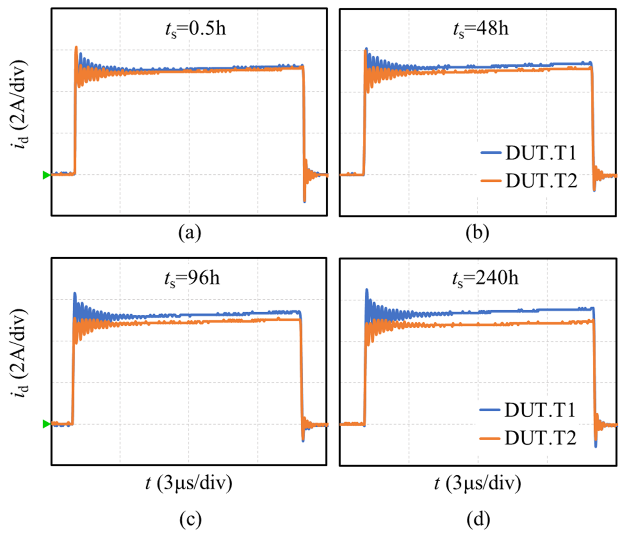


Fig. 20. Evolution of steady state current sharing under boost circuit application. The total current of DUT.T1 and DUT.T2 is 10 A, and V_{GS} is 15/–8 V with switching frequency of 50 kHz and duty cycle of 50%.

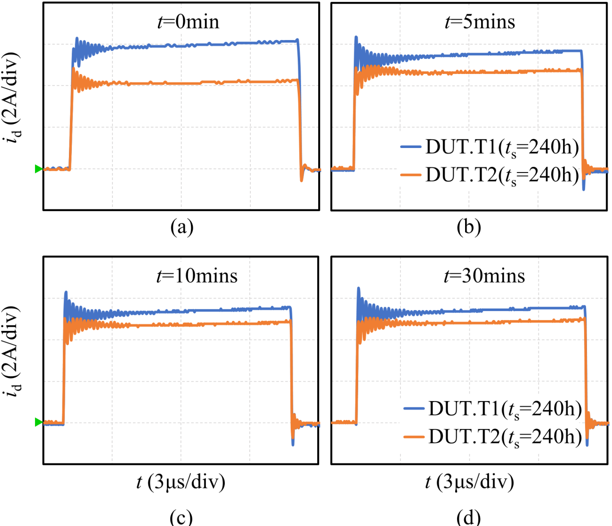


Fig. 22. Current sharing during room temperature startup to steady state. DUT.T1 and DUT.T2 have been aged for 240 h. t = 0 min indicates the commencement of the boost circuit operation.

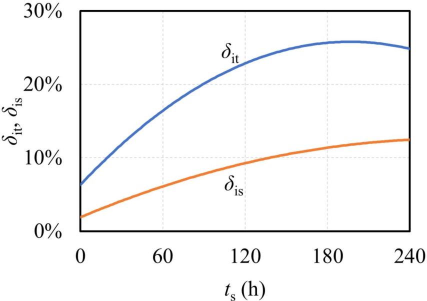


Fig. 21. Evolution of steady state dynamic and static current imbalance. The total current of DUT.T1 and DUT.T2 is 10 A.

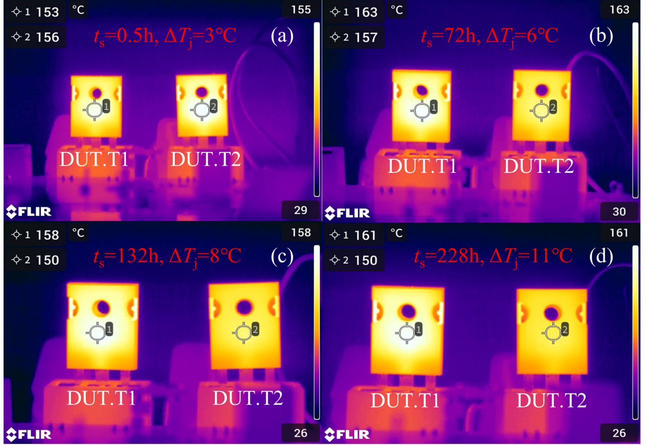


Fig. 23. Evolution of steady state temperature difference between DUT.T1 and DUT.T2 under boost circuit application. The steady state temperature difference ΔT_j is defined as $\Delta T_j = T_{jmax} - T_{jmin}$.

and δ_{it} is similar between total currents of 10 and 20 A. Δi_s and Δi_t increase with the increase in total current, and the current in individual devices may exceed safe operating value at high total current levels. This means that the parallel SiC MOSFETs may suffer thermal runaway if the total current and threshold voltage dispersity are large enough.

The current sharing process from room temperature startup to steady state is shown in Fig. 22, and the devices have already experienced 240 h of aging stress. At the moment of startup, the temperatures of both DUT.T1 and DUT.T2 are 28 °C. The current imbalance between DUT.T1 and DUT.T2 reaches its maximum, which implies that parallel devices with higher threshold voltage dispersity may encounter current overrange issues during low-temperature startup. Subsequently, the parallel devices demonstrate better current sharing characteristics. This is because SiC MOSFET has a negative current temperature coefficient, which is favorable for device paralleling. Device with higher current at room temperature exhibit a gradual reduction in current as the temperature increases.

C. Evolution of Temperature Dispersity

As mentioned previously, the difference in threshold voltage of parallel devices leads to an imbalance in current. Device with higher current exhibits greater heat generation, and current imbalance results in temperature imbalance among the parallel devices. The temperature difference between DUT.T1 and DUT.T2 in the steady state with different t_s is analyzed. Besides, the temperature variation process from room temperature startup to thermal steady state is studied.

When DUT.T1 and DUT.T2 are initially powered on in the boost application, they reach a thermal steady state after 0.5 h, with a small temperature difference ($\Delta T_j = T_{jmax} - T_{jmin}$) of only 3 °C, as shown in Fig. 23. After undergoing an aging time of over 200 h, the temperature difference between devices increases to 11 °C, which is caused by the increase of current imbalance.

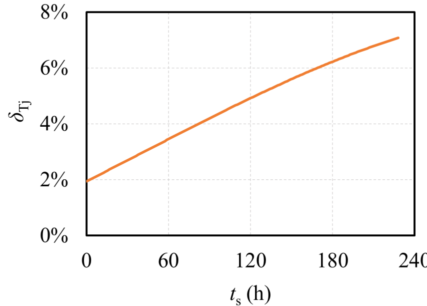


Fig. 24. Evolution of steady state temperature dispersity between DUT.T1 and DUT.T2 under boost circuit application.

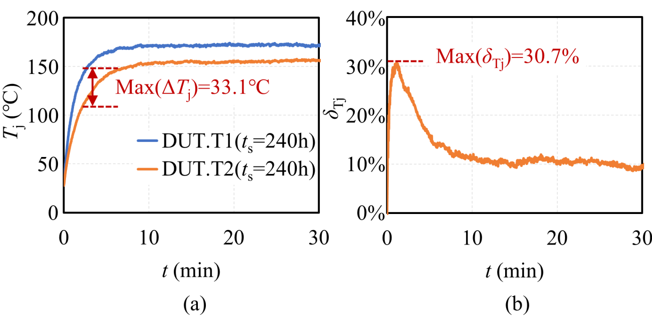


Fig. 25. (a) Temperature of DUT.T1 and DUT.T2 during startup to steady state. (b) Temperature dispersity during startup to steady state. DUT.T1 and DUT.T2 have been aged for 240 h. $t = 0$ min indicates the commencement of the boost circuit operation.

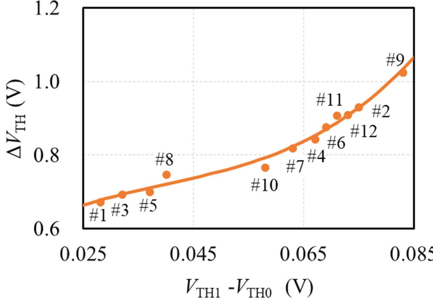


Fig. 26. Relationship between V_{TH1}–V_{TH0} and ΔV_{TH}. V_{TH0} and V_{TH1} correspond to the threshold voltage at $t_s = 0$ and 1 h, respectively. ΔV_{TH} is the threshold voltage drift magnitude at $t_s = 33$ h. Threshold voltage drift under dynamic gate stress with V_{GS} of 20 / –15 V, T_j of 175 °C, switching frequency of 150 kHz, duty cycle of 50%.

The temperature dispersity δ_{Tj} is given by ΔT_j / T_{javg}, and δ_{Tj} increases with the increment of t_s, as shown in Fig. 24.

After about 240 h of stress aging, the temperature evolution of DUT.T1 and DUT.T2 from room temperature startup to thermal steady state is shown in Fig. 25. At the moment of startup, the temperature of DUT.T1 and DUT.T2 are 28 °C. Subsequently, DUT.T1 demonstrates a faster temperature increase rate compared to that of DUT.T2, and the temperature difference between DUT.T1 and DUT.T2 increases, which is caused by the difference in current sharing or threshold voltage. The temperature difference reaches the peak value of 33.1 °C within 3 min after the startup. δ_{Tj} during room temperature startup to thermal steady state is shown in Fig. 25(b). δ_{Tj} rapidly increases at first and then decreases, and the peak value is 30.7%.

As mentioned previously, with the increase of stress time, the threshold dispersity of parallel devices increases, leading to the deterioration of both dynamic and static current sharing characteristics. Consequently, a greater temperature difference between parallel devices is observed in Fig. 23. The chain reaction provided an analytical perspective on a potential trigger for the Tesla car recall incident.

V. Chips Classification and Experimental Validation

A. Chips Classification Based on Short-Term Threshold Drift

As demonstrated by the experiments and analyses in the previous sections, the threshold voltage dispersity increases with gate stress time. Moreover, the increased threshold voltage dispersity results in poorer current sharing and a larger temperature difference.

Basically, three methods are used to improve the current sharing as follows.

1) Device classification.
2) Circuit parameter matching.
3) Active gate driving.

Device classification is widely used in industry for its simplicity and high reliability. However, Fig. 18 indicates that simply selecting devices with similar initial threshold voltages cannot prevent the increase in threshold voltage dispersity. Besides, parallel devices are also classified based on the transfer characteristic curves, where devices exhibiting similar transfer characteristic curves are grouped together and this method may be more effective than classification method based on threshold voltage [15]. However, for the two methods to be effective, it is assumed that the threshold voltage and transfer characteristic curve remain unchanged during operation, which is not true in practice. Thus, there raises a question of how to suppress threshold voltage imbalance caused by aging.

As mentioned previously, because the threshold voltage increases with aging time, classifying parallel devices based on the initial thresholds is insufficient to effectively avoid the increase in threshold dispersity. Classifying parallel devices based on short-term threshold voltage drift may be a better choice. Threshold voltage grows fastest at the beginning, and device with a higher initial growth rate showed a larger threshold voltage drift amplitude after tens of hours of gate stress. A short-term gate stress is applied to devices at first, then the threshold voltage drift amplitudes are classified, and finally, the devices with similar drift amplitudes are selected for parallel connection. However, excessive gate stress time used in classification can cause a significant threshold voltage rise in devices, while insufficient gate stress time results in minimal threshold voltage change, making precise classification challenging.

One hour of dynamic gate stress (V_{GS} = 20 / –15 V, f = 150 kHz, T_j = 175 °C) was used for classification in this article, and the device sample size is 12, as shown in Fig. 26. The threshold voltage drift amplitude at t_s = 1 h, i.e., the threshold voltage drift

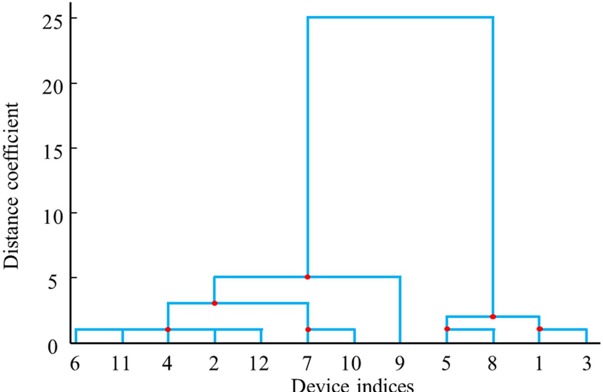


Fig. 27. Hierarchical cluster diagram of DUT.T. The sample size of DUT.T is 12. The diagram was generated by SPSS software.

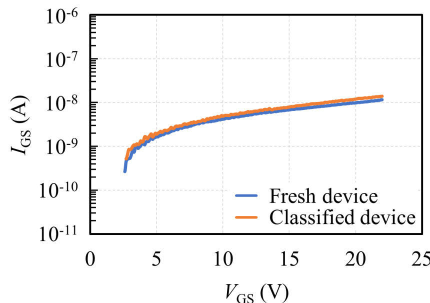


Fig. 28. Gate leakage current of fresh device and classified device. The maximum gate voltage is 22 V, with the drain and source shorted.

caused by classification is defined as V_{TH1} (t_{s} = 1 h)–V_{TH0} (t_{s} = 0 h). It can be seen from Fig. 26 that ΔV_{TH} at t_{s} = 33 h increases with V_{TH1}–V_{TH0}, and devices with similar V_{TH1}–V_{TH0} have similar ΔV_{TH}. The devices with similar V_{TH1}–V_{TH0} are more suitable for parallel connection. Besides, the increase in threshold voltage which induced by classification is very small, with a maximum of around 2%.

In addition, to standardize the classification process, intelligent methods of classification can be used. The focus of this section is not on the choice of intelligent classification method, and the key point is utilizing V_{TH1}–V_{TH0} as the classification variable. The hierarchical clustering method was used to classify the 12 devices in Fig. 26, and V_{TH1}–V_{TH0} is the variable, as shown in Fig. 27. When the samples were divided into four clusters, devices no. 6, 11, 4, 2, and 12 formed cluster 1, devices no. 7 and 10 formed cluster 2, device no. 9 was classified into cluster 3, and devices no. 5, 8, 1, and 3 formed cluster 4. Selecting devices with similar V_{TH1}–V_{TH0} from the same cluster for parallel connection is an effective method to suppress the increase of threshold voltage dispersity.

Gate leakage current is commonly used to assess the health condition of SiC MOSFET gate oxide [39]. To assess the potential damage to the device oxide layer caused by the 1 h gate stress, the gate leakage current of the device was measured. The gate leakage current of the classified device is almost the same as that

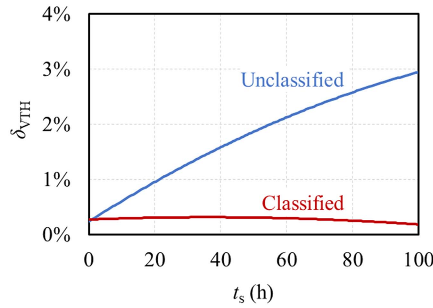


Fig. 29. Threshold voltage dispersity of classified and unclassified DUT.T under boost circuit application. DUT.T under dynamic gate stress with V_{GS} of 15/–8 V, switching frequency of 50 kHz, and duty cycle of 50%.

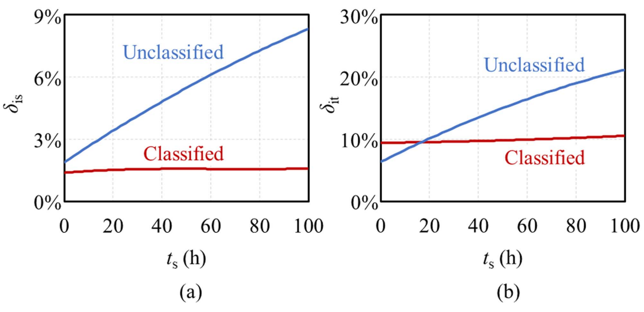


Fig. 30. Evolution of steady state dynamic and static current imbalance. The total current of parallel devices is 10 A.

of the fresh device, as shown in Fig. 28, which means that the classification does not lead to gate oxide degradation.

To verify whether the classification can improve current mismatch, two devices with similar V_{TH1}–V_{TH0} (0.061 and 0.062 V) were selected by classification for validation in the boost circuit. The output voltage V_{OUT} is 200 V, and the total current of parallel devices is 10 A. Devices under dynamic gate stress with V_{GS} of 15 / –8 V, switching frequency of 50 kHz, and duty cycle of 50%. The evolution of threshold voltage dispersity is shown in Fig. 29, the threshold voltage dispersity of unclassified devices increases with stress time. In contrast, the threshold voltage dispersity of classified devices exhibits minimal changes, which means the classification is effective.

For the boost application, the static current imbalance and dynamic current imbalance of classified and unclassified devices can be written as Δi_{s} / 5 A and Δi_{t} / 5 A, as shown in Fig. 30. After 100 h of aging stress, δ_{is} and δ_{it} of unclassified devices increased by 6.4% and 14.7%, respectively, i.e., the current sharing became worse. However, the current sharing characteristics of the classified devices remain almost unchanged. δ_{is} and δ_{it} of classified devices increased by 0.2% and 1.1%, respectively. This is because the threshold voltage dispersity variation of classified devices is small.

After undergoing an aging time of 100 h, the temperature difference between unclassified devices increases from 3 °C to 7 °C, which is caused by the increase of current imbalance. The temperature dispersity δ_{Tj} of unclassified devices increases with the increment of t_{s}, as shown in Fig. 31. However, δ_{Tj} of

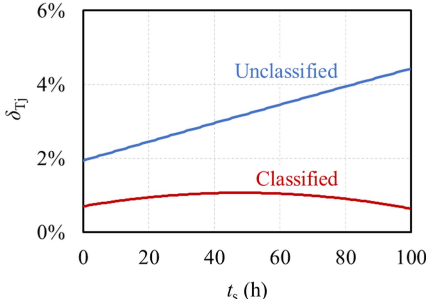


Fig. 31. Evolution of steady state temperature dispersity of classified and unclassified DUT.T under boost circuit application.

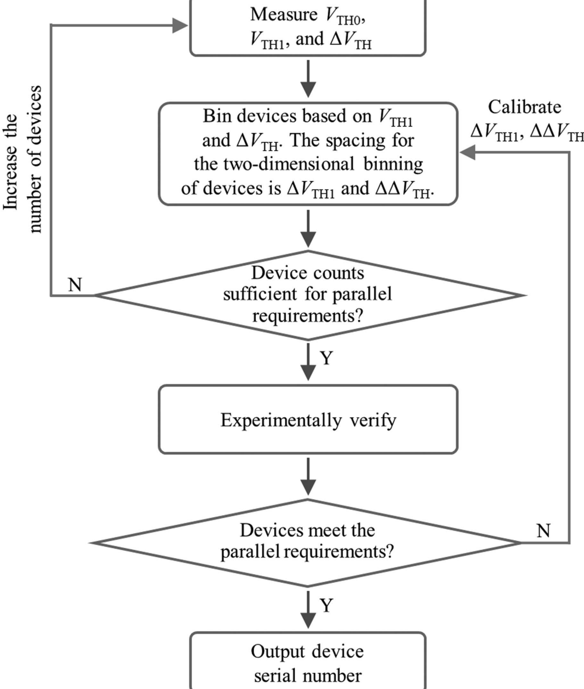


Fig. 32. Design guidelines for device selection in power converters with paralleled devices.

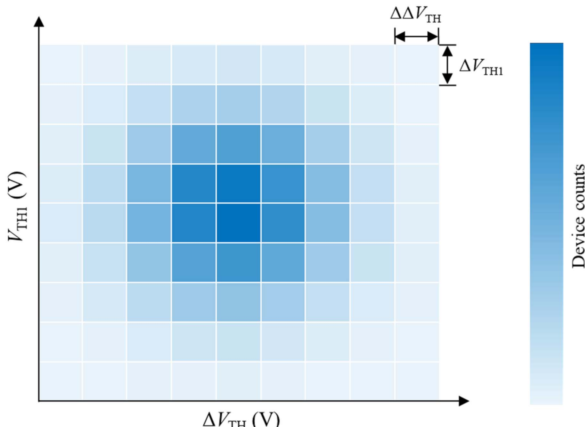


Fig. 33. 2-D binning based on V_{TH1} and ΔV_{TH}, where darker colors indicate a higher device counts in the corresponding region. The spacing for the 2-D binning of devices is ΔV_{TH1} and $\Delta\Delta V_{TH}$.

classified devices exhibits minimal changes, and this is attributed to the small change in the current sharing characteristics.

B. Guidelines for Device Selection in Parallel Applications

The effectiveness of device classification for parallel applications based on short-term gate stress has been discussed in the previous experiments. A flowchart is given in Fig. 32 to provide a systematic approach. The generalized procedure for selecting devices involves six main steps as follows.

1) Measure V_{TH0}, V_{TH1}, and ΔV_{TH}. V_{TH0} is the initial threshold voltage of device, V_{TH1} is the threshold voltage after applying gate classification stress, and the threshold voltage drift caused by classification is defined as $\Delta V_{TH} = V_{TH1}–V_{TH0}$. The typical gate classification stress is provided in Section V-A.
2) Bin devices based on V_{TH1} and ΔV_{TH}. The hierarchical clustering method is applicable to research, and binning is widely used in industry for its simplicity and high reliability. The focus of this section is not on the choice of intelligent classification method, and the key point is utilizing ΔV_{TH} as the classification variable. Therefore, binning is selected as the method for parallel device classification in practical applications. A 2-D binning diagram based on V_{TH1} and ΔV_{TH} is shown in Fig. 33, where darker colors indicate a higher device counts in the corresponding region. The spacing for the 2-D binning of devices is ΔV_{TH1} and $\Delta\Delta V_{TH}$, and both ΔV_{TH1} and $\Delta\Delta V_{TH}$ require calibration based on practical application requirements.
3) Confirm whether the device counts meet the requirements for parallel. If the device counts of a single bin after classification meets the parallel requirements, proceed to the next step. However, when the initial total sample size is limited, it may result in insufficient device counts within individual bins postclassification, failing to meet the requirements for parallel devices. Therefore, increasing the sample size is necessary.
4) Experimentally verify. Take a long-term assessment in practical application, with monitoring of threshold dispersity and current sharing characteristics.
5) Confirm whether the current sharing characteristics of binned devices meet the requirements. If requirements are not met, calibration of ΔV_{TH1} and $\Delta\Delta V_{TH}$ is necessary.
6) Output device serial number.

VI. Conclusion

The evolution of threshold voltage dispersity of parallel SiC MOSFETs under dynamic gate stress is investigated, and its impact on current sharing of parallel applications is analyzed in this article. The threshold voltage of SiC MOSFET increases under dynamic gate stress, and threshold voltage dispersity (δ_{VTH}) of parallel SiC MOSFETs cannot remain constant during operation; instead, it increases with gate stress time at high temperature. In consequence, the current sharing deteriorates due to the increase

of $\delta_{\rm VTH}$, and the parallel devices may suffer thermal runaway if the total current and threshold voltage dispersity is large enough. In parallel application, the peak of current imbalance ratio in threshold mismatched devices is observed during room temperature startup, and subsequently, the current imbalance is improved as the device temperature increases. At last, a classification method that uses short-term threshold voltage drift as the classification variable was proposed to improve the current imbalance in parallel applications. In the parallel boost circuit, the increment of static current imbalance improved from 6.4% to 0.2%, and the increment of dynamic current imbalance improved from 14.7% to 1.1%. It is hoped that the findings reported in this article will be useful for the parallel application of SiC MOSFETs in power converters.

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