Gate Robustness and Reliability of P-Gate GaN HEMT Evaluated by a Circuit Method

Bixuan Wang, *Student Member, IEEE*, Ruizhe Zhang, *Student Member, IEEE*, Qihao Song, *Student Member, IEEE*, Hengyu Wang, *Member, IEEE*, Quanbo He, Qiang Li, *Senior Member, IEEE*, Florin Udrea, *Member, IEEE*, and Yuhao Zhang, *Senior Member, IEEE*

***Abstract*—The small gate overvoltage margin is a key reliability concern of the GaN Schottky-type p-gate high electron mobility transistor (GaN SP-HEMT). Current evaluation of gate reliability in GaN SP-HEMTs relies on either the dc bias stress or pulse *I–V* method, neither of which resembles the gate voltage (V_{GS}) overshoot waveform in practical converters. This article develops a new circuit method to characterize the gate robustness and reliability in GaN SP-HEMTs, which features a resonance-like V_{GS} ringing with pulse width down to 20 ns and an inductive switching concurrently in the drain-source loop. Using this method, the gate's single-pulse failure boundary, i.e., dynamic gate breakdown voltage (BV_{DYN}), is first obtained under the hard switching (HSW) and drain-source grounded (DSG) conditions. The gate's switching lifetime is then tested under the repetitive V_{GS} ringing, and the number of switching cycles to failure (SCTF#) is fitted by Weibull or Lognormal distributions. The SCTF# shows a power law relation with the V_{GS} peak value and little dependence on the switching frequency. More interestingly, the gate's BV_{DYN} and lifetime are both higher in HSW than those in DSG, as well as at higher temperatures. Such findings, as well as the gate degradation behaviors in a prolonged overvoltage stress test, can be explained by the time-dependent Schottky breakdown mechanism. The gate leakage current is found to be the major precursor of gate degradation. At 125 °C and 100 kHz, the V_{GS} limits for a 10-year lifetime are projected to be ∼6 V and ∼10 V under the DSG and HSW conditions, respectively. These results provide a new qualification method and reveal new physical insights for gate reliability and robustness in p-gate GaN HEMTs.**

***Index Terms*—Breakdown, Gallium nitride (GaN) high-electron mobility transistor (HEMT), gate, inductive power switching, lifetime, reliability, ringing, robustness, spike.**

I. Introduction

GALLIUM nitride (GaN) high-electron mobility transistors (HEMTs) are gaining increasing adoptions in power electronics applications [1], [2]. Among various types of GaN HEMTs, the Schottky-type p-gate GaN HEMT (SP-HEMT) has become a popular platform adopted by many GaN device vendors and foundries [3], [4]. However, the gate reliability of SP-HEMTs under overvoltage is regarded as a primary concern in applications [3]. Many datasheets suggest a maximum gate-to-source voltage (V_{GS}) of 7 V from reliability considerations, while the device is usually operated under a V_{GS} of 5.5 to 6 V to lower the device on-resistance. The V_{GS} margin is as low as 1 V [5], [6] and much smaller than that (>5 V) in Si insulated gate bipolar transistors (IGBTs) and SiC MOSFETs. Moreover, the degradation of the Schottky-type p-GaN gate have been found to differ from the classic time-dependent dielectric breakdown (TDDB) theory that governs the MOS gate degradation [7]. The effectiveness of the conventional high-temperature gate-bias (HTGB) test for the gate qualification of GaN SP-HEMTs is questionable [3]. This is because, according to the JEDEC standard [8], the HTGB best applies to the gate dielectrics with the percolation-induced TDDB degradation.

To quantify the gate lifetime and V_{GS} operation limit of this emerging GaN gate structure, it is essential to deploy a test method that best mimics the gate stress in practical applications. Here we first provide a brief survey of the gate reliability test methods for GaN HEMTs in the literature [7], [9], [10], [11], [12], [13], [14], [15] (see Table I), as well as the major findings from these studies.

Inherited from the HTGB test, the constant-voltage stress (CVS) test at V_{GS} of 9–11 V was used in many studies [9], [10], [11], [12], [13]. Several variations of dc tests, e.g., the staircase-voltage stress [7], [9], [10] and the multiple gate current (I_G) sweep [16], have also been reported. All dc tests see a destructive increase in I_G at gate failure. Other common findings include: a power law relation between the time to failure (TTF) and the V_{GS}-stress magnitude; the TTF follows the Weibull distribution with the shape parameter (β) higher than unity (i.e., wear-out failure) [7], [9]; and a longer gate lifetime at higher temperature, which is opposite to the classic TDDB theory.

Recently, the pulse-IV test with the continuous square-wave V_{GS} stress is used to mimic the ON/OFF gate biases in switching applications. Despite the lack of a full consensus among various reports, the effective gate lifetime is found to generally show a weak dependence on frequency (f_{SW}) up to 100 kHz [7] and a decrease with f_{SW} at >100 kHz [17]. These results suggest the sensitivity of gate lifetime on switching parameters. This pulse

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Bixuan Wang, Ruizhe Zhang, Qihao Song, Qiang Li, and Yuhao Zhang are with the Center of Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24060 USA (e-mail: bixuanwang@vt.edu; rzzhang@vt.edu; qihao95@vt.edu; lqvt@vt.edu; yhzhang@vt.edu).

Hengyu Wang, Quanbo He, and Florin Udrea are with the Department of Engineering, University of Cambridge, CB2 1TN Cambridge, U.K. (e-mail: hw595@cam.ac.uk; qh243@cam.ac.uk; fu10000@cam.ac.uk).

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TABLE I
COMPARISON OF PROPOSED METHOD WITH PRIOR METHODS FOR GAN HEMT GATE RELIABILITY STUDIES

Ref.	Test Method	V_{GS} Waveform	Min. Pulse Width	Max. V_{GS} (V)	Drain-source Condition	Temp (ºC)
[9]	Constant-volt. stress (CVS)	DC	N/A	9	Drain-source grounded (DSG)	25~125
[10]	CVS, Staircase-volt. stress (SVS)	DC	N/A	9		25
[11]	CVS	DC	N/A	10		25~150
[12]	CVS, Static-IV	DC	N/A	9.25		25~150
[13]	CVS	DC	N/A	11		-125~50
[7]	Pulse-IV, SVS	Square	5 µs	17.8		25~150
[14]	Pulse-IV	Square	50 ns	9.4		150
[15]	Pulse-IV	Square	5 µs	11	Resistive load (50 kΩ)	25
This Work	Overvoltage Circuit	Resonance-like	20 ns	~30	DSG and inductive load	25~150

IV method is also used to determine a single-pulse V_{GS} limit. Some device datasheet include such limit measured in a single square-wave V_{GS} pulse with a pulse width (PW) of 1 μs [18].

Despite the popularity of the dc and pulse IV tests, the gate overvoltage stress in practical power converters has different profiles. The V_{GS} profile usually consists of the gate overvoltage ringing added to a dc bias, i.e., the rated driving voltage. The ringing component is usually induced by the gate-loop parasitic inductances, featuring a resonance-like waveform with a dV_{GS}/dt of 1∼2 V/ns [5]. Multiple GaN device vendors have reported very low device failure rates tested under the dc rated driving voltage. However, the gate robustness and reliability under the resonant V_{GS} ringing beyond the gate rated voltage has not been fully understood.

Moreover, such gate ringing usually occurs during the device turn-ON transient, in which high drain-to-source voltage (V_{DS}) and drain current (I_D) can be present in the power loop. In hard switching (HSW), a concurrence of high V_{DS}, high I_D, and V_{GS} overshoot is expected. Some prior studies suggest that the high V_{DS} may induce the additional device degradation due to the inverse piezoelectric effect [19], [20], [21]. However, most prior dc and pulse *I–V* tests were performed under a drain-source-grounded (DSG) condition. A recent pulse *I–V* test used a large resistive load to achieve switching with high OFF-state drain bias, however the low I_D and the switching locus are still distinct from the inductive switching [15]. Thus, a new test method associated with practical applications is needed to evaluate the gate reliability and robustness of GaN HEMTs.

In this article, we present a circuit method that produces a resonance-like V_{GS} overshoot with a PW down to 20 ns (dV_{GS}/dt up to 3 V/ns) under both DSG and HSW conditions. We then employ this method to test the single-pulse gate failure boundary, i.e., the dynamic gate breakdown voltage ($\mathrm{BV_{DYN}}$), and the device lifetime under the repetitive gate ringing stress with various peak gate overvoltage ($V_{\mathrm{GS(PK)}}$). The test results not only provide the direct references for device applications, but also reveal the strong impact of the drain-loop switching locus on the gate $\mathrm{BV_{DYN}}$ and lifetime for the first time. We reported the preliminary setup and $\mathrm{BV_{DYN}}$ results in [22]. This article is significantly distinct by including the comprehensive circuit design and analysis as well as the new switching lifetime and failure analysis results.

In addition to evaluating the gate reliability under the parasitic-induced V_{GS} ringing, this article can provide crucial references for additional applications. First, in a resonant gate driver which is widely used in high-frequency power converters (e.g., class-E) [23], the gate overdrive could occur when control failure happens in switches. Under this condition, the device gate needs to withstand the surge energy stored in the resonant inductor, which usually has a much higher inductance than the parasitic inductance in the usual gate driver. Hence, studying the gate robustness and reliability under the high transient V_{GS} is critical to the fault protection for the resonant gate driver. Second, the current gate voltage rating of GaN HMETs is largely determined by the dc-based HTGB, which differs from the gate stress in practical converters. The accurate V_{GS} rating is important not only to device reliability but also to the device performance, die size, and cost (e.g., a higher operational V_{GS} allows for lower specific on-resistance and smaller die size for a specific current rating).

The rest of this article is organized as follows. Section II discusses the circuit design and prototype. Sections III and IV present the gate BV_{DYN} and switching lifetime results, respectively. Section V illustrates the physical explanations of the test results through failure analysis and device simulations. Finally, Section VI concludes the article.

II. Circuit Design and Prototype

A. DUTs and Test Platform

The GaN SP-HEMT tested in this article is the commercially available 650-V, 50-mΩ GS66508T [18]. Fig. 1(a) shows the schematic of the DUT and the microscopic image of the DUT's gate region. Fig. 1(b) shows the DUT's I_G-V_G characteristics at $V_{\mathrm{DS}} = 0$ V under temperature from 25 °C to 150 °C, measured using the Keysight B1505 Power Device Analyzer with a 0.1-A I_G compliance.

The proposed test platform enables both single-pulse and repetitive gate overvoltage tests and is configured for the following functionalities.

1) Drain-source schemes: DSG or 400-V HSW.
2) PW of the V_{GS} overshoot: ranging from 20 ns to 30 μs under the DSG condition, and from 20 ns to 1 μs under the HSW condition.

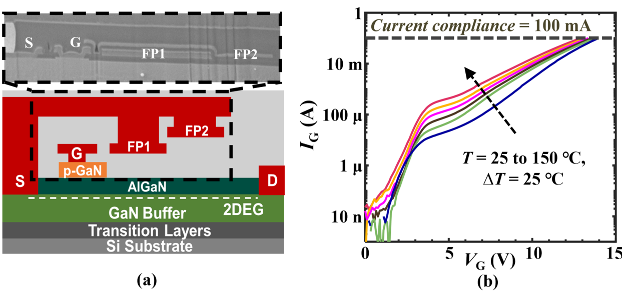


Fig. 1. (a) (Bottom) DUT schematics and (top) the microscopic photo of the DUT's gate region. (b) Static I_G-V_G characteristics at 25 to 150 °C.

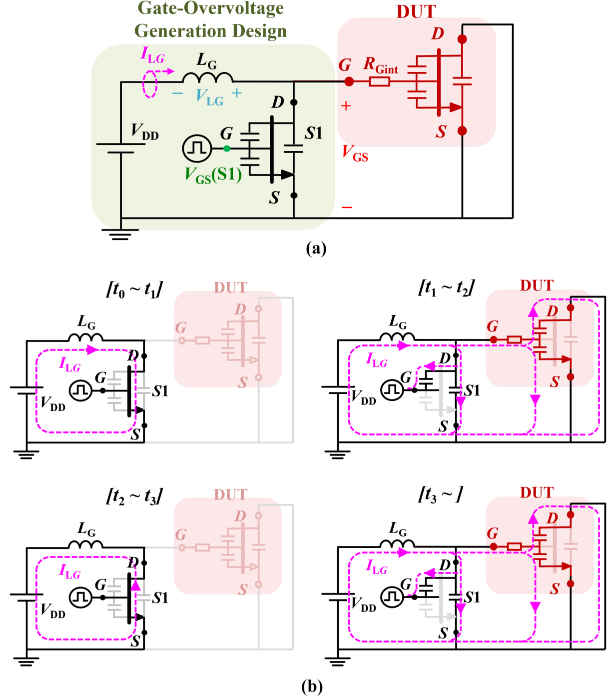


Fig. 2. (a) Schematics of gate overvoltage test circuit in DSG condition. (b) Working stages of the circuit.

3) DUT can be heated by a power resistor attached to its case, and the case temperature (T_C) is calibrated by a K-type thermocouple as well as a thermal camera.

B. Circuit in Drain-Source-Grounded Condition

Fig. 2(a) shows the circuit schematics in the DSG condition. The V_{GS} overshoot is generated in the DUT's gate-source loop. The generation section consists of an inductor L_G to mimic the gate-loop parasitic inductance, a dc voltage source V_{DD} with capacitor bank, and a fast switch (S_1) [24]. Table II gives the major components in the prototyped circuit. V_{DD} is 0.5 V in this article, which is designed to be lower than the DUT's threshold voltage (V_{TH}) to keep the DUT OFF in the steady state.

The general principle of this circuit is to use the energy stored in an inductor to produce a V_{GS} overshoot similar to how a V_{DS} overshoot is generated in the unclamped inductive switching test [25], [26], [27], [28], [29]. The circuit operation can be divided

TABLE II
COMPONENTS OF THE PROTOTYPED CIRCUIT

Specification	Symbol	Value or Part #
Gate-loop inductor	L_G	60 nH ~ 300 μH
Input DC voltage	V_{DD}	0.5 V
Fast switch	S_1	EPC2214
On time of S_1	$t_{\mathrm{ON,S1}}$	300 ns ~ 1 ms
Pulse width of gate overvoltage	PW	20 ns ~ 30 μs
Peak value of gate overvoltage	$V_{\mathrm{GS(PK)}}$	0.5 ~ 30 V
Bus voltage	V_{BUS}	400 V
Load inductor	L_{LOAD}	24 mH
Inductor to mimic D-S loop parasitics	L_P	1 μH
Free-wheeling diode	FWD	3 ES1JFL in parallel
Switching frequency in lifetime test	f_{SW}	10 ~ 100 kHz

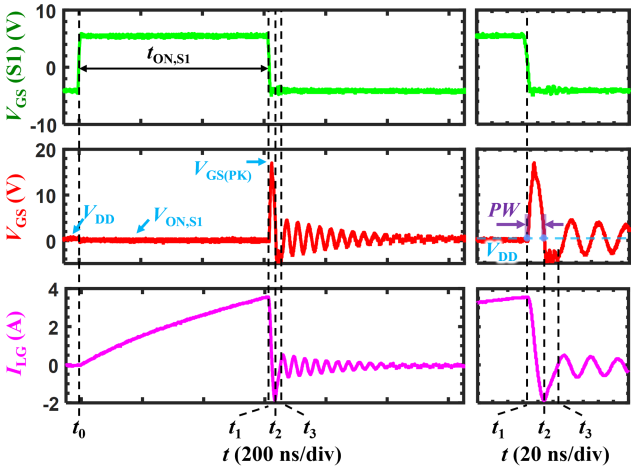


Fig. 3. Test waveforms in DSG condition with PW = 20 ns and $V_{\mathrm{GS(PK)}}$ = 17 V. (Left) A whole switching cycle. (Right) zoom-in view of V_{GS} overshoot period.

into four stages [see Fig. 2(b)]. Fig. 3 shows the exemplar test waveforms with a V_{GS} overshoot of 20-ns PW and 17-V peak value.

1) *Stage I [$t_0 \sim t_1$]:* S_1 turns ON, and L_G is charged by V_{DD}. The current flowing through L_G (I_{LG}) can be tuned by the ON time of S_1 ($t_{\mathrm{ON,S1}}$)

$$I_{\mathrm{LG}} = V_{\mathrm{DD}} \times \frac{t_{\mathrm{ON,S1}}}{L_G}. \quad (1)$$

In this stage, the DUT's V_{GS} equals to the forward voltage drop of S_1 ($V_{\mathrm{ON,S1}}$), which is much lower than the DUT's V_{TH}.

2) *Stage II [$t_1 \sim t_2$]:* S_1 turns OFF; the energy stored in L_G creates a voltage overshoot (V_{LG}) across the L_G. As the DUT's $V_{\mathrm{GS}} = V_{\mathrm{LG}} + V_{\mathrm{DD}}$, a resonant overvoltage added on a dc component (V_{DD}) is applied directly across the DUT's gate and source. In this operation, the reactance of the DUT's input capacitance is much larger than DUT's inner gate resistance ($R_{G\mathrm{int}}$ = 1.1 Ω), so the latter can be ignored. Thus, the V_{LG} overshoot can be characterized by a resonance between L_G and an equivalent capacitance

(C_{EQ})

$$C_{\mathrm{EQ}} = C_{\mathrm{ISS}}\ (\mathrm{DUT}) + C_{\mathrm{OSS}}\,(\mathrm{S1}) \tag{2}$$

where C_{ISS}(DUT) and C_{OSS}(S1) are the input capacitance of the DUT at $V_{\mathrm{DS}} = 0$ V and the S_1's output capacitance, respectively.

The PW of V_{GS} overshoot can be estimated as a half of the resonant period (T)

$$\mathrm{PW} = 0.5 \times T = \pi\sqrt{L_G \times C_{\mathrm{EQ}}}. \tag{3}$$

Multiple L_G ranging from 60 nH to 300 μH are used to tune the PW in this article. For a selected L_G, $V_{\mathrm{GS(PK)}}$ can be modulated by $t_{\mathrm{ON},S1}$

$$V_{\mathrm{GS(PK)}} = V_{\mathrm{DD}} + V_{\mathrm{DD}} \times \frac{t_{\mathrm{ON,S1}}}{\sqrt{L_G \times C_{\mathrm{EQ}}}}. \tag{4}$$

The average slew rate of V_{GS} overshoot is estimated by

$$\frac{dV_{\mathrm{GS}}}{dt} = \frac{V_{\mathrm{GS(PK)}}}{0.5 \times \mathrm{PW}}. \tag{5}$$

When the V_{GS} PW is down to 20 ns and $V_{\mathrm{GS(PK)}}$ up to 10–30 V, the average dV_{GS}/dt is 1–3 V/ns, which is comparable to that in high-frequency GaN converters.

3) *Stage III [$t_2 \sim t_3$]:* When DUT's V_{GS} resonates to negative and turns ON the S_1 in the third quadrant, the DUT's V_{GS} is clamped to the S_1's reverse conduction voltage ($\sim$ -5 V).
4) *Stage IV [$t_3 \sim$]:* The resonance between L_G and C_{EQ} is gradually damped by the parasitic resistance until the steady state (i.e., when V_{GS} settles down to V_{DD}). The amplitude of V_{GS} ringing in this stage is below 5 V, which is within the DUT's gate safe operating area. Hence, the primary overvoltage stress onto the DUT's gate is in the stage II.

C. Circuit in Hard Switching With Inductive Load

Fig. 4 shows the circuit schematic and operation principles in the HSW condition. The DUT's power loop comprises a 400-V bus voltage (V_{BUS}) with capacitor bank, a load inductor (L_{LOAD}), a free-wheeling diode (FWD), and an inductor (L_{P}) to mimic the power-loop parasitics and to suppress the high I_D-V_{DS} overlap (and thermal runaway). The photos of the test setup and circuit board are shown in Fig. 5 with the component specifications given in Table II. Fig. 6(a) shows the exemplar waveforms with the hard turn-ON by the V_{GS} overshoot of 20-ns PW and 21-V peak value. The circuit operation under the HSW condition can be divided into four stages.

1) *Stage I [$t_0 \sim t_1$]:* At t_0, S_1 turns ON, the gate-loop sees the similar process as the *stage I* in the DSG condition. DUT is in OFF state with $V_{\mathrm{DS}} = V_{\mathrm{BUS}}$.
2) *Stage II [$t_1 \sim t_2$]:* At t_1, S_1 turns OFF, a positive V_{GS} overshoot is produced at the DUT's gate, resulting in a hard turn-ON. This hard turn-ON is featured by an overlap among high V_{GS}, high V_{DS}, and high I_D. The V_{GS}-V_{DS} switching locus during the V_{GS} charging period is shown in Fig. 6(b). Note here the measured I_D is the channel current minus the output capacitance discharging current, suggesting an even higher channel current. After turn-ON, the DUT's I_D through the channel is composed of a linearly increasing DC component flowing through the L_{LOAD}, and a high-frequency *RLC*-resonant component with the total magnitude up to ∼4 A, as shown in Fig. 4(b). In this resonance, R is the power-loop parasitic resistance, L is L_P, and C is the FWD's equivalent junction capacitance ($C_{\mathrm{JD}} \sim 20$ pF),
3) *Stage III [$t_2 \sim t_3$]:* At t_2, the DUT turns OFF when $V_{\mathrm{GS}} < V_{\mathrm{TH}}$. In this stage, I_D no longer flow through the channel [see Fig. 4(b)] and is composed of a second-order dc component through the L_P and L_{LOAD} which keeps charging the DUT's C_{OSS}, and a high-frequency *RLC*-resonant

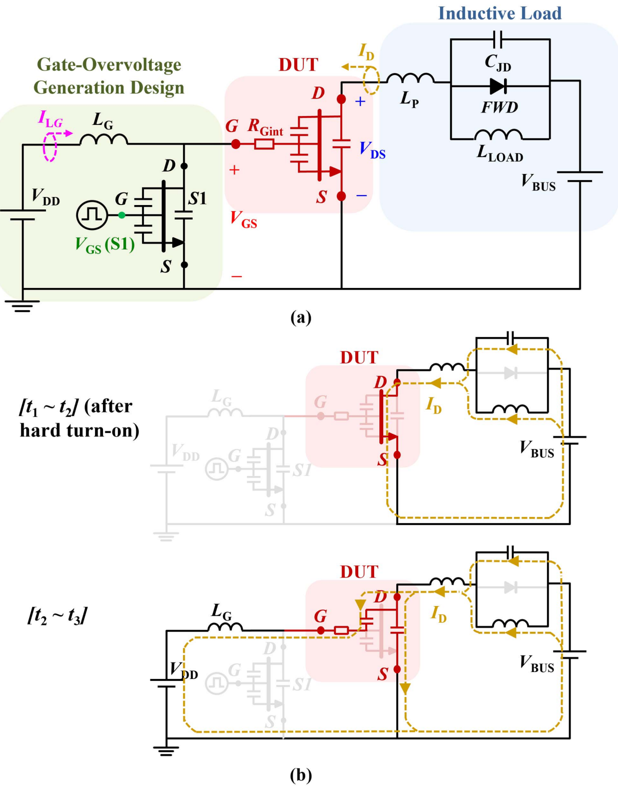


Fig. 4. (a) Schematics of the gate overvoltage test circuit in the HSW condition. (b) (Top) Stage II ($V_{\mathrm{GS}} > V_{\mathrm{TH}}$) and (bottom) stage III ($V_{\mathrm{GS}} < V_{\mathrm{TH}}$) of the circuit.

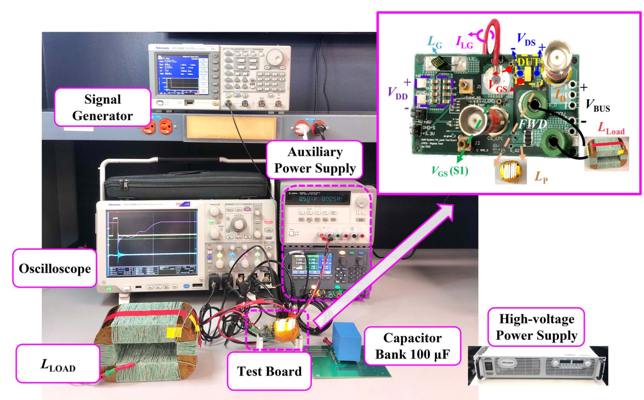


Fig. 5. Photos of the gate overvoltage test setup and the circuit board for HSW condition.

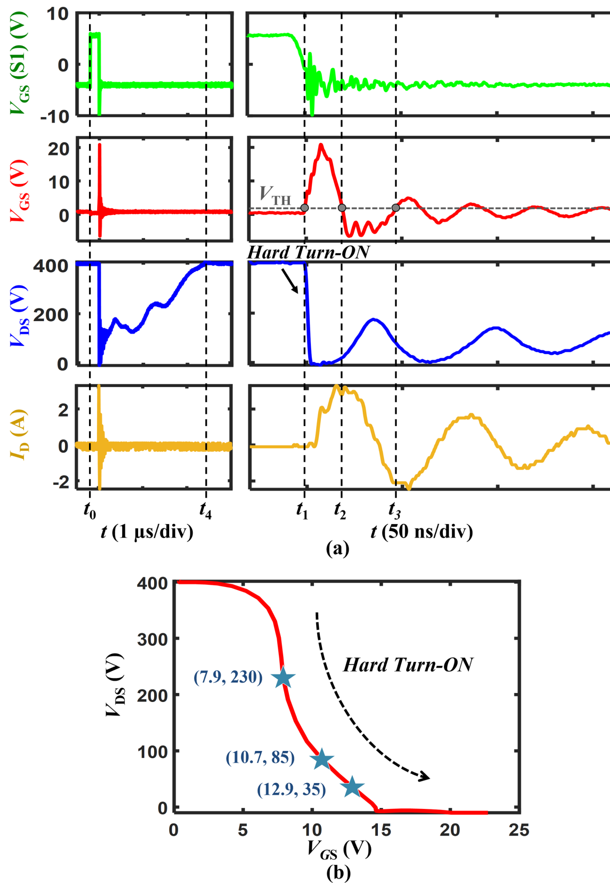


Fig. 6. (a) Test waveforms in the 400-V inductive HSW with PW = 20 ns and $V_{GS(PK)}$ = 21 V. (Left) A whole switching cycle. (Right) zoom-in view of the V_{GS} overshoot period. (b) V_{GS}-V_{DS} locus of the hard turn-ON process extracted from test waveforms. The symbols correspond to the simulation conditions in Fig. 18.

component. Here, R is the power-loop parasitic resistance, L is L_P, and C is the C_{JD} in series with the DUT's C_{OSS}.

4) *Stage IV [$t_3 \sim t_4$]:* As the DUT's V_{GS} continues ringing, the DUT repeats the ON and OFF states. In I_D, the resonant component gradually attenuates to zero, and the DC current becomes dominant. The I_D gradually charges the DUT's C_{OSS} until the DUT's V_{DS} reaches V_{BUS}.

5) *Stage V [$t_4 \sim$]:* After t_4, the DUT is OFF, and the load current circulates with the FWD. The V_{GS} of the DUT gradually damps to V_{DD} until the circuit reaches the steady state finally.

As shown in Fig. 6, as compared to the DSG condition, the primary V_{GS} stress in the HSW condition also occurs in *stage II* but is accompanied by high V_{DS} (during the V_{GS} charging) and high channel I_D (mainly during the V_{GS} discharging).

During the HSW, the DUT's T_C is monitored by the thermal cameral, and the DUT's junction temperature (T_J) is estimated to close to T_C. From experimental waveforms, the energy loss in each cycle is extracted to be <20 μJ produced within 2 μs. Hence, the average power dissipation (P_{diss}) is about 10 W. The DUT's transient junction-to-case thermal impedance ($R_{\theta JC}$) is expected to be lower than the dc value [$R_{\theta JC}$(DC)], which is 0.5 °C/W from the datasheet. Therefore, the maximum increase in T_J over T_C (ΔT_{JC}) is estimated to be within 5 °C

$$\Delta T_{JC} = R_{\Theta jc} \times P_{\text{diss}} < R_{\Theta JC}(\text{DC}) \times P_{\text{diss}} < 0.5\ ^{\circ}\text{C/W} \times 10\ \text{W} = 5^{\circ}\text{C}. \tag{6}$$

In this article, the device failure and degradation are identified from the anomaly in switching waveforms and verified by the comprehensive post-switching device characterizations on Keysight B1505 Power Device Analyzer.

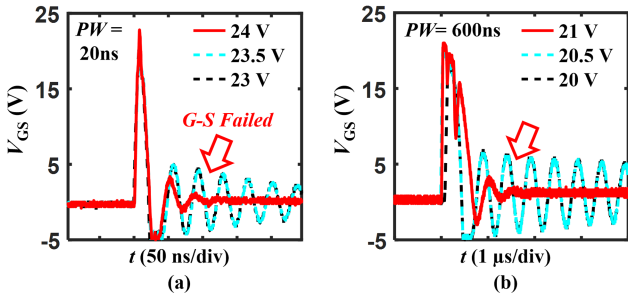


Fig. 7. Last two survival and failure V_{GS} waveforms in DSG, at PW of (a) 20 ns and (b) 600 ns.

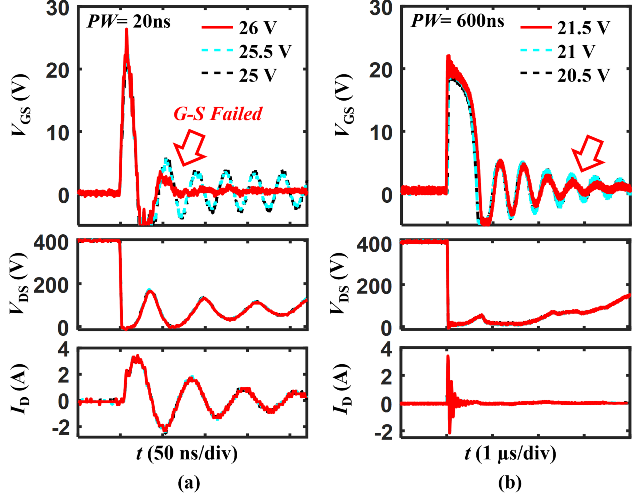


Fig. 8. DUT's V_{GS}, V_{DS}, and I_D waveforms in 400-V HSW, before and after gate failure at PW of (a) 20 ns and (b) 600 ns. The V_{DS} and I_D waveforms verify DUT's D-S voltage blocking capability after G-S short failure.

III. Dynamic Gate Breakdown Voltage

To investigate the DUT's single-pulse gate BV_{DYN}, $V_{GS(PK)}$ is increased with a 0.5-V step in each single pulse until the gate failure. After each pulse, possible device degradation is examined on the curve tracer from the *I–V* characteristics.

Fig. 7(a) and (b) shows the V_{GS} waveforms of two DUTs tested with the increased $V_{GS(PK)}$ under the PW of 20 ns and 600 ns, respectively, under the DSG at 25 °C. In the 20-ns case, at $V_{GS(PK)}$ of 24 V, the V_{GS} ringing damps fast after the overshoot, suggesting a gate-source (G-S) failure. In the 600-ns case, a similar G-S failure appears at $V_{GS(PK)}$ = 21 V. Fig. 8(a) and (b) shows the V_{GS}, V_{DS}, and I_D waveforms of two DUTs tested

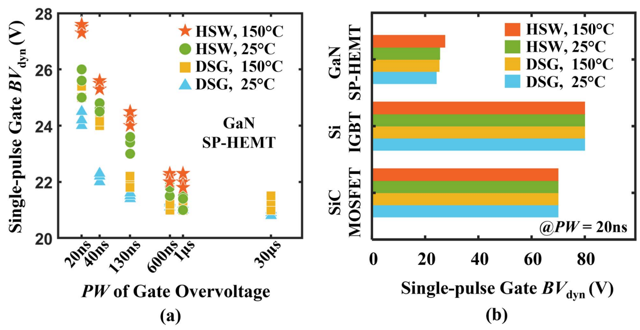


Fig. 9. (a) Gate $\mathrm{BV_{dyn}}$ of GaN SP-HEMT as a function of PW under the DSG and HSW and at 25 and 150 °C. Three devices are tested for each condition. (b) Gate $\mathrm{BV_{dyn}}$ of Si IGBT, SiC MOSFET, and GaN SP-HEMT under the DSG and HSW and at 25 °C and 150 °C, all at a PW of 20 ns. Multiple Si and SiC devices are tested, showing nearly no variation.

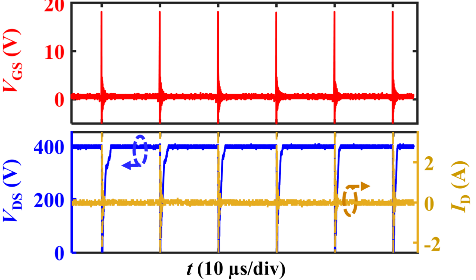


Fig. 10. Repetitive 400V/4A/100kHz HSW waveforms with $V_{\mathrm{GS(PK)}} = 18$ V in each cycle.

under the PW of 20 ns and 600 ns, respectively, both under the HSW at 25 °C. Similar G-S failure signatures are observed at $V_{\mathrm{GS(PK)}}$ of 26 and 21.5 V for two PW. The intact V_{DS} and I_D waveforms verify that DUT retains the V_{DS} blocking capability after the G-S short failure. The *I–V* characterizations further confirm the destructive G-S failure without degradation in the V_{DS} blocking capability.

Fig. 9(a) summarizes the measured gate $\mathrm{BV_{DYN}}$ of GaN SP-HEMTs under various PW, two T_C (25 and 150 °C), and two D-S conditions (DSG and HSW). Under each condition, three devices are tested to failure, presenting a good statistical consistency with $\mathrm{BV_{DYN}}$ variation within 1 V. The gate $\mathrm{BV_{DYN}}$ presents a decreasing-then-saturation trend with the increased PW, and under the same PW, the gate $\mathrm{BV_{DYN}}$ is higher at higher T_C and in the HSW condition. In the DSG at 25 °C, with PW increased from 20 ns to 30 μs, the gate $\mathrm{BV_{DYN}}$ decreases from 24 to 21 V and then saturates. At 150 °C, the gate $\mathrm{BV_{DYN}}$ is 1–2 V higher than at 25 °C in short pulses and also saturates to 21 V. In HSW, the gate $\mathrm{BV_{DYN}}$ is 1–2 V higher than that in DSG. The highest gate $\mathrm{BV_{DYN}}$ (27.5 V) is observed in HSW at 150 °C with 20-ns PW ($dV_{\mathrm{GS}}/dt \sim 3$ V/ns).

As an extended study, the gate $\mathrm{BV_{DYN}}$ of a Si IGBT [30] and a SiC MOSFET [31] are also measured using the same circuit, as shown in Fig. 9(b). The measurements are performed in both HSW and DSG, as well as at 25 °C and 150 °C, all with a PW of 20 ns. The Si IGBT and SiC MOSFET show a consistent gate $\mathrm{BV_{DYN}}$ of 80 V and 70 V, respectively, under all these conditions. This suggests the $\mathrm{BV_{DYN}}$ of the MOS gate is independent of temperature and the D-S switching scheme. As compared to Si IGBT and SiC MOSFET, the GaN SP-HEMT not only shows a much lower gate $\mathrm{BV_{DYN}}$, but also possesses a different gate breakdown mechanism, which will be explored in Section V.

IV. Gate Switching Lifetime

The switching lifetime is measured using repetitive V_{GS} overshoots. A customized program is developed to record test waveforms and count the number of switching cycles to failure (SCTF#). To best mimic the common transient overshoots in applications, the PW is selected as 20 ns with dV_{GS}/dt up to ~2 V/ns. Tests are performed in DSG and HSW conditions at DUT's $T_{\mathrm{C}} = 125$ °C to investigate the impact of D-S loop switching scheme on switching lifetime, as well as at a lower practical $T_C = 50$ °C in the DSG condition to study the temperature impact. The T_C is carefully monitored throughout the entire test. The f_{SW} is first selected as 100 kHz. The $V_{\mathrm{GS(PK)}}$ is selected to range from 15.5 to 17.5 V and from 17.5 to 19.5 V in DSG and HSW conditions, respectively, both at 125 °C, as well as from 14.5 to 16.5 V at 50 °C in the DSG condition. Ten devices are tested to failure in each condition for statistical significance. Fig. 10 shows exemplar waveforms in the 18-V $V_{\mathrm{GS(PK)}}$, 100-kHz f_{SW}, HSW (400V/4A) condition, revealing stable parameters in repetitive cycles.

Under each test condition, the failure probability (*P*), i.e., the cumulative distribution function of failure, can be obtained using the SCTF# data of ten devices. It is found that under a specific condition, the relation between *P* and SCTF# can be fitted by both Weibull and lognormal distributions. The fitting data under multiple $V_{\mathrm{GS(PK)}}$ in DSG and HSW at 125 °C are shown in Fig. 11(a) and (b). The relevant data in DSG at 50 °C are shown in Fig. 11(c).

The Weibull distribution is characterized by a function of ln(-ln(1-*P*)) on SCTF#, as shown in Fig. 12. The β is extracted to be >1 in all conditions, suggesting a wear-out failure. The SCTF# at $P = 63\%$ and 0.1% ($\mathrm{SCTF\#_{63\%}}$ and $\mathrm{SCTF\#_{0.1\%}}$) under a specific test condition can be extracted from either Weibull or lognormal fitting curve (see Fig. 11). As shown in Fig. 13, both the extracted $\mathrm{SCTF\#_{63\%}}$ or $\mathrm{SCTF\#_{0.1\%}}$ show power law relations with $V_{\mathrm{GS(PK)}}$.

Note that it is a common practice to extrapolate the gate lifetime of GaN HEMTs assuming that the time-dependent failure mechanism is consistent from the use conditions to the acceleration test conditions [7], [13], [32], [33]. For our DUT, as shown in Fig. 1(b), the I_G-V_{GS} characteristics at $V_{\mathrm{G}} > 5$ V shows a relatively consistent function, suggesting a consistent mechanism of gate leakage current and gate degradation. Hence, here we predict the gate switching lifetime (= SCTF# / f_{SW}) at various $V_{\mathrm{GS(PK)}}$, with the assumption that the SCTF# power law relation is also valid at lower $V_{\mathrm{GS(PK)}}$.

Fig. 13 presents the projected maximum allowable $V_{\mathrm{GS(PK)}}$ for a target 10-year gate switching lifetime operating at

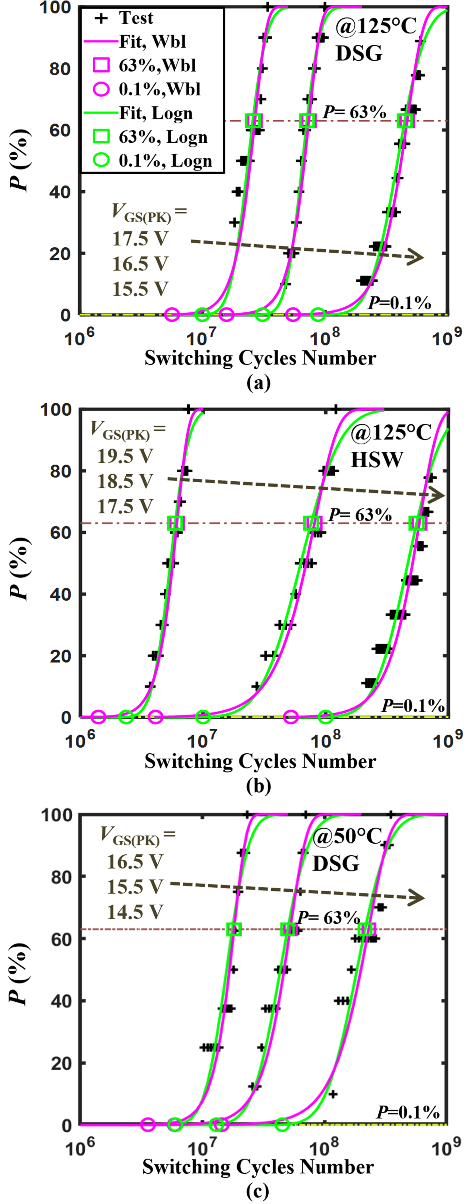


Fig. 11. Failure probability (P) as a function of *SCTF#* at $f_{\mathrm{SW}} = 100$ kHz under various $V_{\mathrm{GS(PK)}}$, in (a) 125°C, DSG, (b) 125°C, HSW, and (c) 50°C, DSG conditions. The SCTF# under each $V_{\mathrm{GS(PK)}}$ is fitted by both Weibull and lognormal distributions.

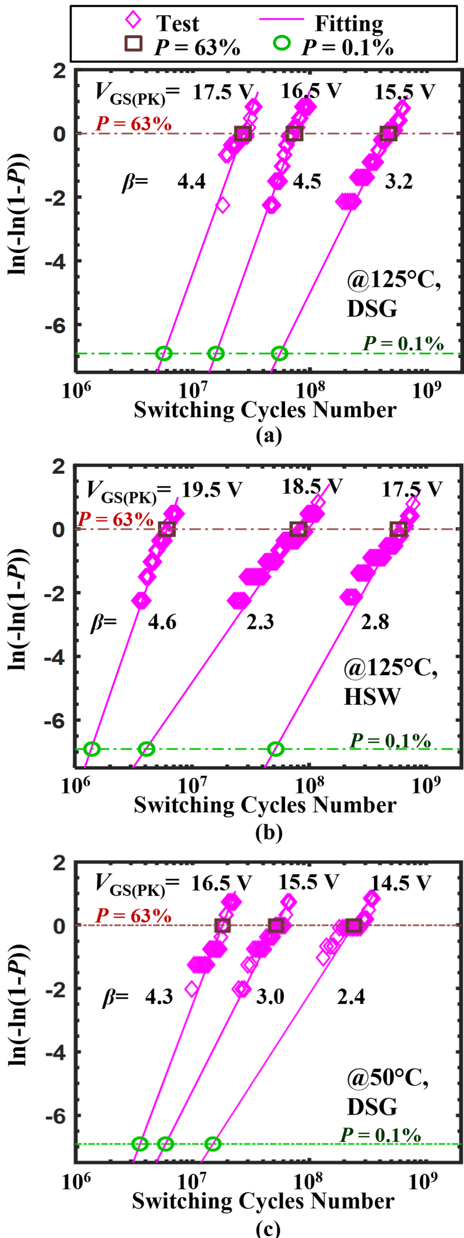


Fig. 12. Weibull distribution of SCTF# at $f_{\mathrm{SW}} = 100$ kHz under various $V_{\mathrm{GS(PK)}}$ in (a) 125°C, DSG, (b) 125°C, HSW, and (c) 50°C, DSG conditions.

$f_{\mathrm{SW}} = 100$ kHz, with both $P = 63\%$ and 0.1%. Based on Weibull-distribution fitting, the maximum allowable $V_{\mathrm{GS(PK)}}$ for 10-year lifetime in DSG at 125 °C is 5.7 and 7.6 V for $P = 0.1\%$ and 63%, respectively. In HSW, the predicted maximum $V_{\mathrm{GS(PK)}}$ for a ten-year lifetime is $\sim$5 V higher than that in DSG. This higher V_{GS} margin in HSW is also verified by the longer switching lifetime in HSW than in DSG under the same $V_{\mathrm{GS(PK)}} = 17.5$ V (see Fig. 12) and is consistent with the higher gate BV_{DYN} in the HSW condition (see Fig. 9). At 50 °C, the predicted maximum $V_{\mathrm{GS(PK)}}$ for a ten-year lifetime is 0.1–0.2 V lower than that at 125 °C. Such enhanced gate reliability at higher temperatures is consistent with the results of the single-pulse dynamic gate breakdown tests.

Note that, in general, Weibull distribution is more commonly used than the lognormal distribution for the classic gate oxide TDDB failure [34]. As the gate failure mechanism in GaN SP-HEMTs could be different, both Weibull and lognormal fittings have been reported [12]. As the first report on the statistics of the circuit test data, this article intends to show the viability of applying both statistical fitting methods. The in-depth study on the physics associated with each statistical distribution will be performed in the future work. The ten-year maximum $V_{\mathrm{GS(PK)}}$ predicted by using two distributions show a generally good consistency with a maximum difference of 0.8 V.

Finally, we explore if the gate lifetime is dominated by the switching cycle number or is also dependent on f_{SW}. Fig. 14

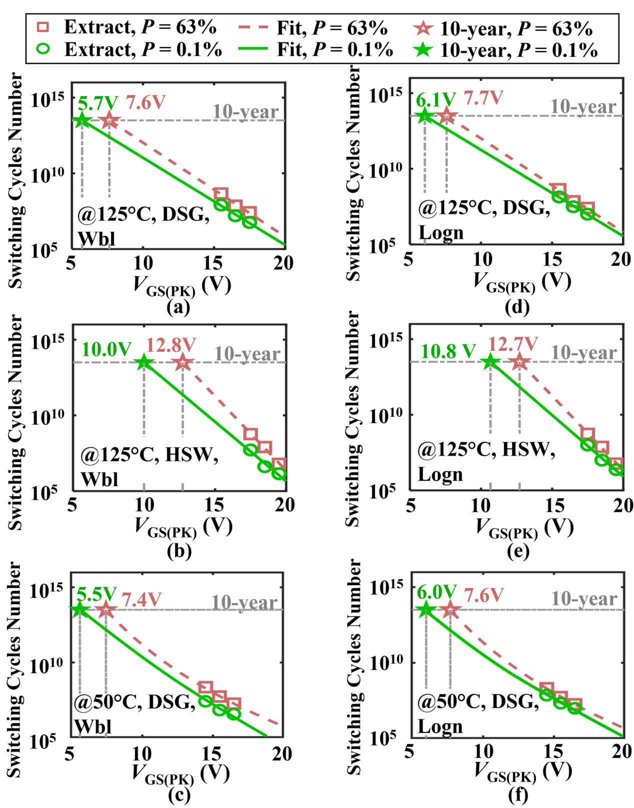
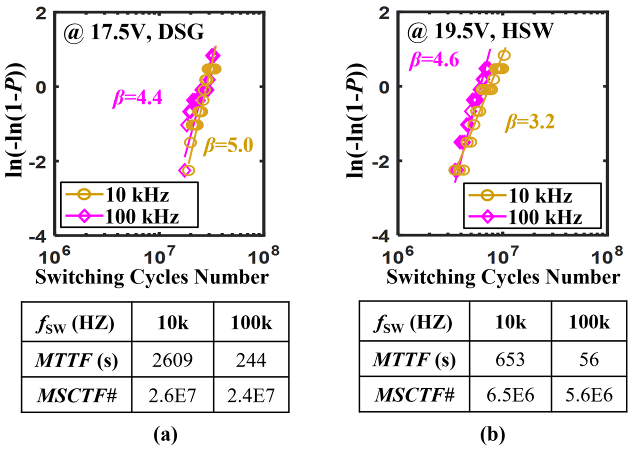


Fig. 13. Max $V_{GS(PK)}$ predicted for 10-year lifetime at $f_{SW} = 100$ kHz in 125°C DSG, 125°C HSW, and 50°C DSG conditions, with $P = 63\%$ and 0.1%, based on the power law extrapolation from SCTF# data at multiple $V_{GS(PK)}$ extracted from (a)–(c) Weibull distribution and (d)–(f) lognormal distribution.



f_{SW} (HZ)	10k	100k
***MTTF* (s)**	2609	244
MSCTF#	2.6E7	2.4E7

f_{SW} (HZ)	10k	100k
***MTTF* (s)**	653	56
MSCTF#	6.5E6	5.6E6

Fig. 14. (Top) comparison of Weibull distributions of SCTF# at f_{SW} of 10 and 100 kHz, under $V_{GS(PK)}$ of (a) 17.5 V in DSG and (b) 19.5 V in HSW. (Bottom) the corresponding MTTF and the mean-SCTF# of the tested ten DUTs in each switching condition.

shows the Weibull distributions of the 10-device *SCTF#* data at $f_{SW} = 10$ and 100 kHz. The mean SCTF# (MSCTF#) of the DUTs at $f_{SW} = 10$ kHz is found to be similar to that at 100 kHz, and the mean-time-to-failure (MTTF = MSCTF# / f_{SW}) differs by about 10 times. This result indicates the gate switching lifetime is primarily dominated by the switching cycle number and thereby will be longer at lower f_{SW}. This is generally

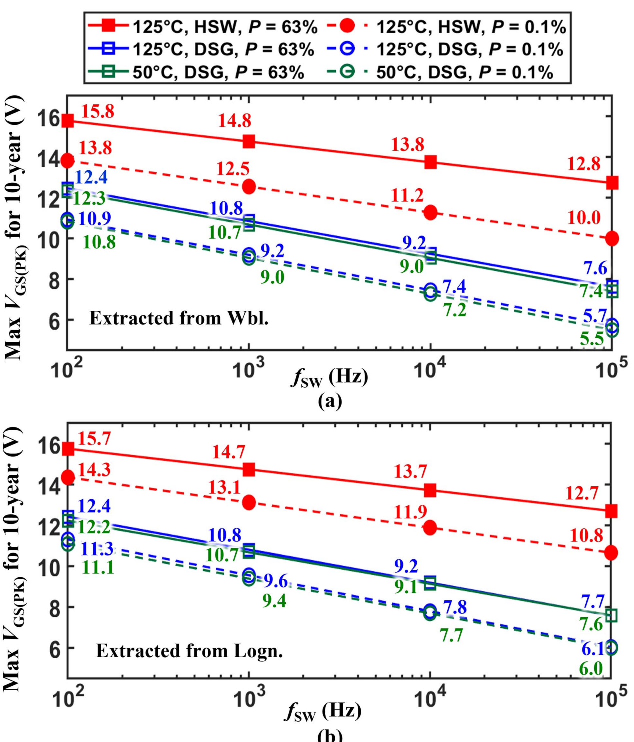


Fig. 15. Projected max $V_{GS(PK)}$ for 10-year lifetime as a function of f_{SW} (100 Hz ∼100 kHz) under the 125°C, DSG, 125°C, HSW, and 50°C, DSG conditions, at $P = 63\%$ and 0.1%. The max $V_{GS(PK)}$ is estimated by the $SCTF\#_{63\%}$ and $SCTF\#_{0.1\%}$ at $f_{SW} = 100$ kHz, assuming the same SCTF# ∼ $V_{GS(PK)}$ relation in this f_{SW} range. The $SCTF\#_{63\%}$ and $SCTF\#_{0.1\%}$ are extracted from (a) Weibull and (b) lognormal distributions, respectively.

consistent with the finding from the pulse *I–V* studies at f_{SW} up to 100 kHz [7]. It also reveals a higher maximum allowable $V_{GS(PK)}$ at lower f_{SW} for a certain lifetime target.

Fig. 15 shows the projected maximum allowable $V_{GS(PK)}$ for a ten-year lifetime with f_{SW} ranging from 100 Hz to 100 kHz at both 125 °C and 50 °C. The projection uses the $SCTF\#_{63\%}$ and $SCTF\#_{0.1\%}$ data at 100 kHz extracted from either Weibull or lognormal fitting curves. For $P = 0.1\%$, the ten-year $V_{GS(PK)}$ can increase by up to ∼5 V under the DSG and up to ∼4 V under the HSW when f_{SW} drops from 100 kHz to 100 Hz.

V. Failure Analysis and Physics-Based Simulation

A. Postfailure Analysis

Failure analyses are performed on multiple DUTs failed in the single-event-breakdown tests and switching-lifetime tests, under different temperatures and D-S conditions, revealing a consistent failure mechanism. Here we present the failure analysis results of a representative DUT.

After the failed DUT is decapsulated, optical microscopic images reveal no observable damage on the chip surface, as shown in Fig. 16(a). The optical beam induced resistance change (OBIRCH) technique is then employed to identify the leakage spot by applying a small G-S voltage. As shown in Fig. 16(b), an emission site is observed between gate and a source finger, indicating a leakage path between G-S. No emission site is

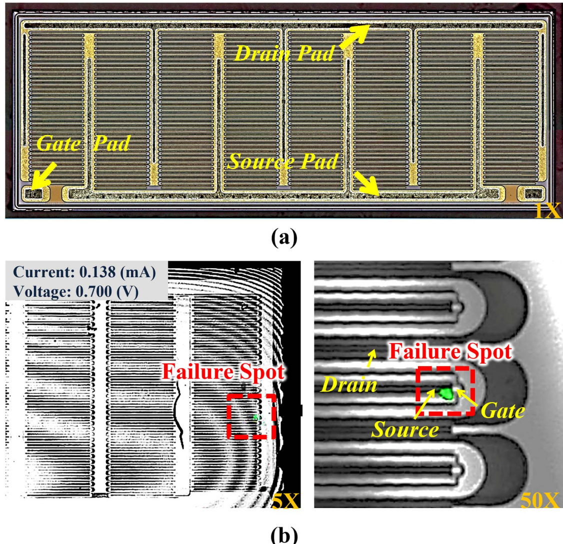


Fig. 16. (a) Optical microscope photo of the surface of the failed DUT after decapsulation. (b) OBIRCH analysis result of the decapsulated failed device with an emission spot shown in green. (Left) 5X zoom-in view. (Right) 50X zoom-in view.

observed in the gate-drain (G-D) access region, which is consistent with the retained functional voltage blocking capability of the failed DUT measured by curve tracer. Finally, the failed DUT is delayered all the way to the removal of the polymer and passivation layers. The microscopic imaging reveals no anomaly on any of these layers. This suggests a failure in the gate stack rather than the passivation layer.

B. Gate Failure Physics and Simulation

The gate BV_{DYN} and gate lifetime shows a positive temperature coefficient (η_T), while the percolation-induced failure in the MOS structure usually has a negative η_T [9], [10]. This difference in GaN SP-HEMTs can be explained by a gate degradation process recently reported in [7]. Under high V_{GS}, the SP-HEMT gate stack is composed of a reverse-biased gate/p-GaN Schottky junction in series with a forward-biased p-GaN/AlGaN/GaN PIN junction. At high V_{GS}, electrons inject from the two-dimensional electron gas into p-GaN and then diffuse to the depleted p-GaN region, get accelerated by high electric field, bombard the Schottky interface, and destructively degrade the Schottky contact to Ohmic-like. Such contact degradation can then produce a low-resistivity, high-leakage-current path through the gate stack. Under the further V_{GS} stress, this localized leakage path is likely to result in the destructive G-S shorting.

The gate BV_{DYN}'s decreasing and saturation trend at longer PW implies an accumulation effect of electron bombardment as well as a threshold in electric field (and bombardment energy) for the Schottky contact degradation. Above this threshold, the local Schottky contact degradation may progressively accumulate until the destructive failure occurs. This progressive process can be accelerated by a higher electron energy, which explains the higher gate BV_{DYN} in the shorter PW.

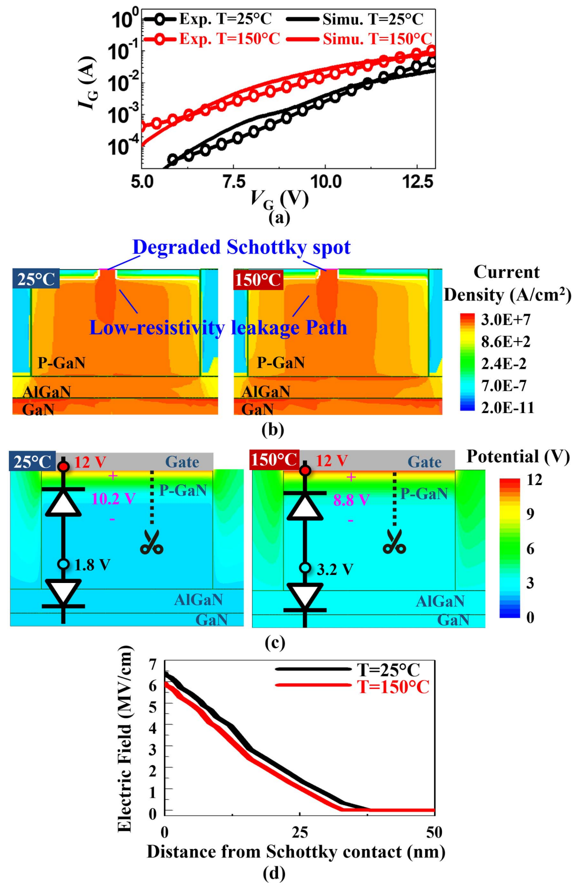


Fig. 17. (a) Simulated I_G-V_G characteristics calibrated with experimental results. (b) Simulated current density contour in the gate stack at (left) 25 °C and (right) 150 °C assuming the appearance of the localized Schottky contact degradation (implemented by setting a low tunneling mass and high tunneling probability locally). (c) Simulated potential contour in gate stack at $V_{GS} = 12$ V at (left) 25 °C and (right) 150 °C. (d) E-field profile in p-GaN along the cutline in (c) at 25 and 150 °C.

To consolidate this mechanism and explain the positive η_T of the gate BV_{DYN} and lifetime, technology computer aided design simulation is performed. The generic GaN HEMT models are based on [35], [36], [37], and the gate leakage current model in the Schottky p-gate is based on [22], [38]. Here we consider the leakage current through the gate stack under the forward V_{GS} to be mainly determined by the reversely-biased p-GaN/Schottky contact, and this Schottky leakage current is governed by the thermally assisted carrier tunneling [12].

By tuning the tunneling mass and its temperature dependence [22], the simulated I_G-V_G characteristics is calibrated with experimental data, as shown in Fig. 17(a). To mimic a localized Schottky junction degradation, the tunneling mass is set as very small in a localized area. As shown in Fig. 17(b), the simulation confirms that the degraded Schottky area will induce a localized, high-leakage-current path.

Fig. 17(c) shows the simulated potential contour in the gate stack under $V_{GS} = 12$ V at 25 and 150 °C. Fig. 17(d) shows the simulated electric field in the p-GaN as a function of distance from the gate/p-GaN Schottky contact. At a higher temperature, the Schottky tunneling current increases, which induces larger

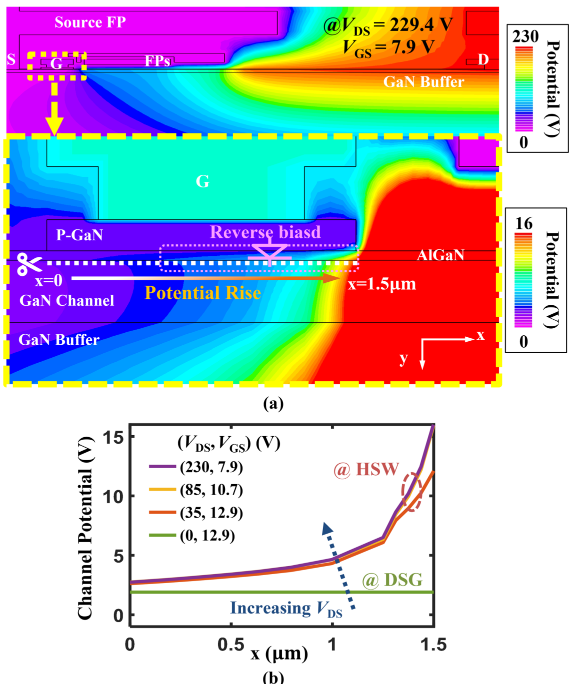


Fig. 18. (a) Simulated potential contour in (top) entire device unit cell and (bottom) gate region. (b) Simulated channel potential below gate at three biases along the turn-ON locus in HSW [see Fig. 6(b)] as compared with that at high V_{GS} in DSG condition.

voltage drops in the non-depleted p-GaN and PIN junction, decreasing the actual voltage drop across the Schottky junction and resulting in a lower electric field and electron bombardment energy. Thus, the gate BV_{DYN} and gate lifetime increase.

Finally, simulations are used to explain the higher gate BV_{DYN} and longer lifetime in HSW as compared to DSG. Fig. 18(a) shows the simulated potential contour in the whole device unit-cell and the channel region at a bias point (V_{DS} = 229.4 V and V_{GS} = 7.9 V) along the HSW locus shown in Fig. 6(b). The high V_{DS} expands the pinch-off region in the channel, raising the potential along the channel. Fig. 18(b) compares the simulated channel potential under V_{GS}- and V_{DS}-biases extracted from the switching locus in HSW and DSG conditions, further confirming the elevated channel potential by high V_{DS}. In the HSW, the concurrent high channel I_D also raises the channel potential due to resistive drop. This elevated channel potential can raise the gate BV_{DYN} by: (i) reducing the actual voltage drop across the gate/p-GaN Schottky junction (and the electric field as well as electron bombardment energy) and (ii) making the PIN junction reverse-biased at the drain-side of the gate, which suppresses the electron injection into p-GaN. Note that (ii) is also consistent with the results in Fig. 16 that suggests the failure spot is primarily at the source-side of the gate.

Note that such a channel potential rise in HSW is also expected in Si IGBT and SiC MOSFET. However, their gate breakdown voltage is governed by the oxide failure, which is minimally impacted by channel potential and temperature. The Schottky p-GaN gate is in nature a non-insulating gate, and the electric field in the critical region (i.e., the p-GaN Schottky region) is dependent on the Schottky leakage current, which is known to be strongly bias- and temperature-dependent.

In addition to the HSW process, the high V_{DS} blocking state, which is absent in DSG, may also contribute to the higher gate BV_{DYN}. According to [15], high OFF-state V_{DS} can induce the hole insufficiency in the gate stack during the turn-ON process; the remaining depletion region in p-GaN can reduce the actual potential drop across the Schottky junction, thus suppress the hot-electron bombardment during the positive V_{GS} overshoot.

VI. Device Degradation Under Stress

To further validate the gate failure mechanisms presented in Section V, device degradation behaviors are intermittently characterized during the circuit stress tests until device failure. These characterizations are performed by taking the device from the circuit board and measuring it on the B1505 curve tracer at 25 °C. Hence, the measured parametric shifts reflect those that cannot recover in a few minutes. Note that a relatively low current compliance (2 mA) is set in the measurement of gate leakage current to avoid the additional degradation produced by the I–V sweep.

Such measurements are performed for a variety of circuit test conditions, including the single-pulse and repetitive stress, the DSG or HSW, as well as the different temperatures, $V_{GS(PK)}$, and f_{SW}. It is found that the device degradation under these test conditions is consistent. Here we present the representative results under three test conditions: single-pulse stress under DSG, as well as the repetitive stress under DSG and HSW.

Fig. 19(a) shows the evolution of the gate leakage, transfer, and output characteristics after single-pulse V_{GS} overshoot with $V_{GS(PK)}$ of 23, 23.5, and 24 V. As $V_{GS(PK)}$ increases, the device shows a two-step degradation behavior. After the 23-V overshoot, significant increase in I_G is observed under the forward V_{GS}, while the I_G under reverse V_{GS} remains low. This suggests the degradation first occurring at the p-GaN Schottky junction instead of the p-GaN/AlGaN/GaN PIN junction. After the 23.5-V overshoot, I_G increases under both forward and reverse V_{GS}, suggesting the second degradation at the PIN junction. Additionally, from the decomposition of I_G, the significant increase in gate-source current (I_{GS}) with the gate-drain current (I_{GD}) keeping at its initial value implies a degradation spot located at the source-side of the gate. After the 24-V overshoot, the device shows a gate failure with both I_{GS} and I_{GD} ramping up. Besides the increase in gate leakage current, the gate's functionality to modulate the I_D is largely retained, as proved by the transfer and output characteristics. This suggests the gate leakage current could be the primary precursor for device gate degradation.

Under the same DSG condition, Fig. 19(b) shows the evolution of the gate leakage, transfer, and output characteristics intermittently measured during the repetitive V_{GS} overshoot with $V_{GS(PK)}$ = 10 V and f_{SW} = 100 kHz at 125 °C. A similar two-step degradation behavior first in the Schottky junction and second in the PIN junction is observed after the 30 min and 1 h of V_{GS} overshoot, respectively. The device test after a recovery of 2 months confirms the degradation is destructive and non-recoverable. Such destructive behavior is also confirmed by

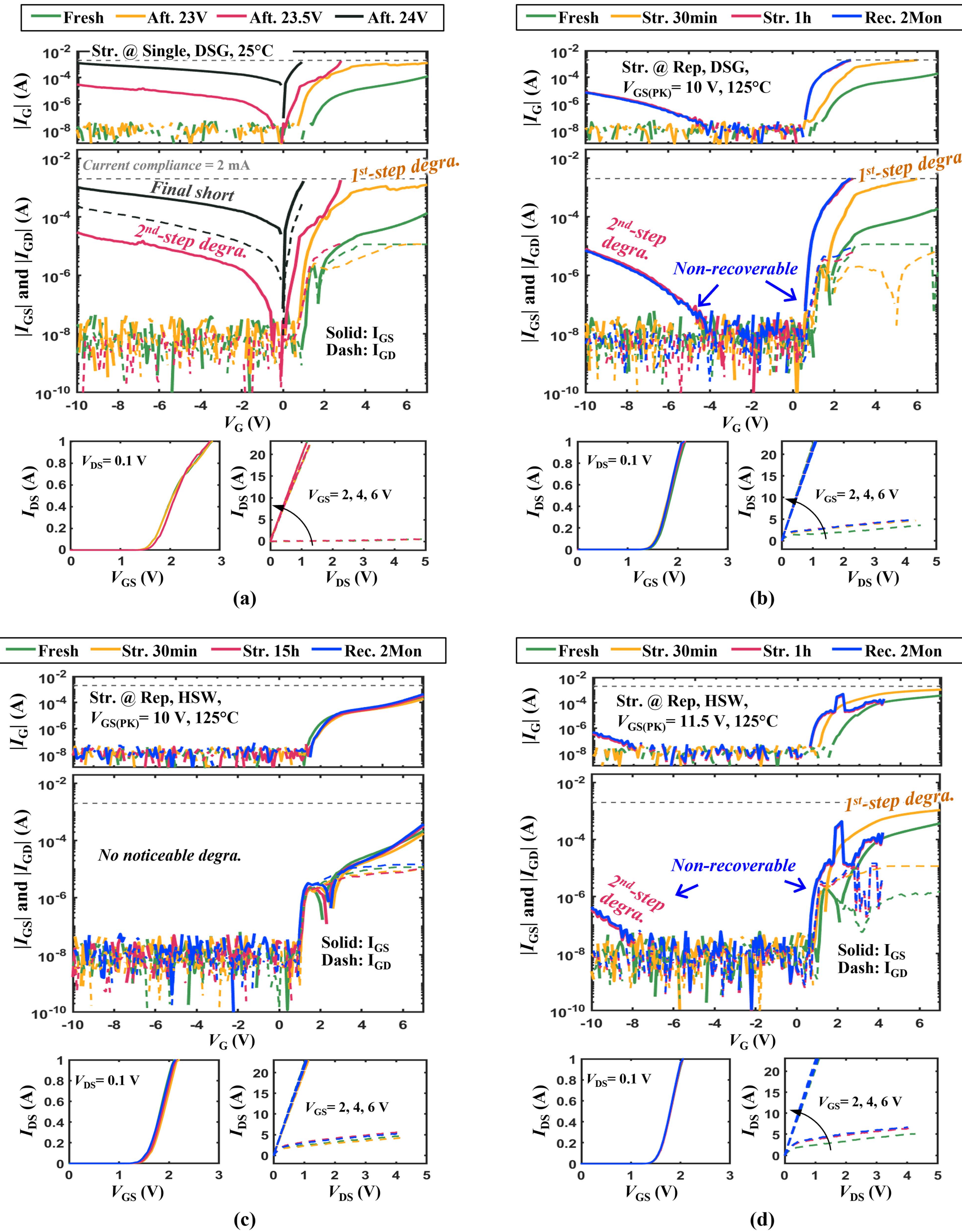


Fig. 19. Device *I–V* characteristics when being fresh and (a) after single-pulse overshoot at $V_{\mathrm{GS(PK)}} = 23$, 23.5, and 24 V in DSG condition at 25 °C, (b) after 30 min and 1 h of repetitive stress at $V_{\mathrm{GS(PK)}} = 10$ V in DSG condition at 125 °C, (c) after 30 min and 15 h of repetitive stress at $V_{\mathrm{GS(PK)}} = 10$ V in HSW condition and 125 °C, and (d) after 30 min and 1 h of repetitive stress at $V_{\mathrm{GS(PK)}} = 11.5$ V in HSW condition at 125 °C. For devices stressed under repetitive overshoots, the *I–V* characteristics after a 2-month natural recovery are also measured [not shown in (a) as the device G-S has destructively failed to low resistivity]. (Top) I_G-V_G characteristics with I_{G} compliance of 2 mA. (Middle) I_{GS}-V_G (solid) and I_{GD}-V_G (dash) characteristics. Total gate current $I_G = I_{\mathrm{GS}} + I_{\mathrm{GD}}$. (Bottom) Transfer and output characteristics. All characteristics are measured at 25°C by B1505.

the absence of recovery after the DUT is heated under 175 °C for 2 weeks (this post-stress bake is an effective recovery method if the degradation is trapping-related and recoverable [37].

The switching lifetime tests in Section IV reveal a relaxed gate overvoltage stress under the HSW condition as compared to the DSG condition. This finding is further supported by the gate degradation behavior in the repetitive stress test. Under the same $V_{GS(PK)}$ = 10 V and f_{SW} = 100 kHz at 125 °C, minimal shifts in gate leakage, transfer, and output characteristics are observed after 15 hours of stress [see Fig. 19(c)]. When $V_{GS(PK)}$ is increased to 11.5 V, the device shows the similar two-step degradation with the prolonged stress, as illustrated in Fig. 19(d). These results confirm the consistent gate degradation mechanism under the DSG and HSW in spite of a reduced gate stress in the latter condition.

Finally, under the HSW condition, the inverse piezoelectric effect induced by the high drain-to-gate bias in the OFF state has been reported to be another possible mechanism for gate degradation [19], [20], [21]. The results in this article, including the longer gate lifetime under HSW and the consistent gate degradation behavior with DSG, suggest that the inverse piezoelectric effect is not a major degradation mechanism for the DUT under the forward gate overvoltage stress. This is possibly because the optimized field plate designs in commercial GaN HEMTs significantly reduce the E-field crowding near the gate edge, and the peak E-field is migrated to the field plate edge or the drain region [36], [37], [39], [40].

VII. Conclusion

This article presents a new circuit method to evaluate the gate robustness and reliability in GaN SP-HEMTs in the application-use conditions that cannot be accessed by dc-bias or pulse IV methods. The method allows for generating the resonance-like V_{GS} overshoot in concurrence with an inductive switching in the D-S loop. Using this circuit, the gate BV_{DYN} and switching lifetime are studied, both of which show strong impact by the D-S switching scheme. The gate BV_{DYN} increases from 21 V to nearly 28 V under a shorter PW, at a higher temperature, and in HSW compared to DSG.

The gate switching lifetime at a specific $V_{GS(PK)}$ can be well fitted by both Weibull and lognormal distributions, and the extracted SCTF# can be fitted by a power law relation with $V_{GS(PK)}$. The gate lifetime is found to be primarily determined by the number of switching cycles and is longer in HSW as compared to DSG, as well as show a positive temperature coefficient. Finally, the maximum allowable $V_{GS(PK)}$ for a ten-year lifetime is predicted at various f_{SW} in both DSG and HSW conditions, at 50 °C and 125 °C.

The above experimental findings can be explained by the time-dependent Schottky breakdown mechanism, which is supported by the failure analysis and physics-based simulation. Finally, the device degradation behaviors are characterized under the prolonged stress of V_{GS} overshoot. The gate leakage current is revealed to be the major degradation precursor, and the degradation is confirmed to first occur at the p-GaN Schottky contact in the gate stack.

These results provide direct references for GaN SP-HEMT applications and suggest the importance of using the inductive circuit method for the gate qualification of GaN SP-HEMTs.

Acknowledgment

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Bixuan Wang (Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2018 and 2021, respectively. She is currently working toward the Ph.D. degree in electrical engineering with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA.

Her current research interests include characterization, robustness, and reliability of wide-bandgap power devices.

Ruizhe Zhang (Student Member, IEEE) received the B.S. degree in material physics from Fudan University, Shanghai, China, in 2018, and the Ph.D. degree in electrical engineering from the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, in 2023.

He is currently an Associate Principal System Engineer with Innoscience America, Santa Clara, CA, USA. His current research interests include design, characterization, reliability, and ruggedness of wide-bandgap power devices.

Qihao Song (Student Member, IEEE) received the B.S. degree in electrical engineering from Virginia Tech, Blacksburg, VA, USA, in 2019. He is currently working toward the Ph.D. degree in electrical engineering with the Center for Power Electronics Systems, Virginia Poly-technic Institute and State University, Blacksburg, VA, USA.

His current research interests include characterization, robustness, reliability, and physics of failure of wide-bandgap power semiconductor devices, as well as the impact and integration of these devices into power electronics converters. Mr. Song is the recipient of the Best Presentation Award of the 2021 Applied Power Electronics Conference.

Hengyu Wang (Member, IEEE) received the B.S. degree in information science and electronic engineering and Ph.D. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2014 and 2020, respectively.

He is currently a Tenure-track Assistant Professor with the College of Electrical Engineering, Zhejiang University. He was a Visiting Research Fellow with the University of Cambridge, from 2021 to 2022 and a Visiting Graduate with the Massachusetts Institute of Technology, from 2018 to 2019. He has authored or coauthored more than 30 journal papers and conference proceedings in electron device and power electronics communities and holds eight granted Chinese patents. His research interest includes power electronic device and its application, and wide and ultra-wide bandgap semiconductor material

Dr. Wang is the recipient of the 2022 China Power Supply Society Doctoral Dissertation Award.

Quanbo He received the B.S. degree in electronic science and technology from Beijing University of Technology, Beijing, China, in 2020. Since 2020, she has been currently working toward the Ph.D. degree in electrical engineering with the High Voltage Microelectronics Laboratory, University of Cambridge, Cambridge, U.K.

Her current research interests include design, simulation, and characterization of wide-bandgap power semiconductor devices.

Qiang Li (Senior Member, IEEE) received the B.S. and M.S. degrees in power electronics from Zhejiang University, Hangzhou, China, in 2003 and 2006, respectively, and the Ph.D. degree in electrical engineering from Virginia Tech, Blacksburg, VA, USA, in 2011.

He is currently a Professor with the Center for Power Electronics Systems, Virginia Tech. His research interests include power management for distributed power systems, applications of wide-bandgap power devices, high-frequency power conversion and controls, magnetics and EMI, high-density electronics packaging and integration, and renewable energy.

Dr. Li was the recipient of the First Place Prize Paper Award for 2016 in the IEEE TRANSACTIONS ON POWER ELECTRONICS. He is also a recipient of the 2017 National Science Foundation Career Award.

Florin Udrea (Member, IEEE) received the Ph.D. degree in power devices from the University of Cambridge, Cambridge, U.K., in 1995.

Since 1998, he has been an Academic position with the Department of Engineering, University of Cambridge. He is currently a Professor in semiconductor engineering and the Head of the High Voltage Microelectronics and Sensors Laboratory, University of Cambridge, Cambridge, U.K. He is currently leading a research group in power semiconductor devices and solid-state sensors that has received an international reputation during the last 30 years. He is also the founder of five companies in the area of power devices and sensors. He has authored or coauthored more than 500 articles in journals and international conferences. He is an inventor of more than 200 patents in semiconductors.

Yuhao Zhang (Senior Member, IEEE) received the B.S. degree in physics from Peking University, Beijing, China, in 2011, and the M.S. and Ph.D. degrees in electrical engineering from Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2013 and 2017, respectively.

From 2017 to 2018, he was a Postdoctoral Associate with MIT. Since 2018, he has been an Assistant Professor with the Center for Power Electronics Systems, Virginia Tech. He has authored or coauthored more than 150 journal articles and conference proceedings and is an inventor of five granted U.S. patents. His research interests include power semiconductor devices, (ultra-) wide-bandgap semiconductor materials, power electronics applications, and machine learning assisted co-design.

Dr. Zhang is the recipient of the 2017 MIT Microsystems Technologies Laboratory Doctoral Dissertation Seminar Award, 2019 IEEE George Smith Award, 2021 National Science Foundation CAREER Award, 2021 Outstanding Assistant Professor Award and 2022 Faculty Fellow Award of Virginia Tech Engineering, and 2023 Office of Naval Research Young Investigator Award. He is an Associate Editor for IEEE TRANSACTIONS OF POWER ELECTRONICS.