GaN-Based *LLC* Converters With Digital Synchronous Rectifier and Copper Foil Planar Transformer in High-Output Current Applications

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***Abstract*—With a gallium nitride (GaN) switching speed of 3.7 ns, high *dv/dt* of 105 kV/μs for 390 V poses serious challenges for synchronous rectification (SR) using extra circuit sensing high-frequency signal of drain-to-source voltage method. A digital SR algorithm based on charge conservation is proposed in this article, which deduces the SR on-time by calculating the time of current flowing through the SR MOSFET junction capacitor. The proposed SR requires no additional detection circuit, which effectively avoids the effect of high *dv/dt* and minimizes the SR conduction loss to improve the efficiency. Furthermore, in high-output current applications, printed circuit board planar transformers face problems of huge winding loss and limited winding current-carrying capacity. A design is proposed for a planar transformer using secondary-parallel multiple interleaved copper foil winding. To diminish dc resistance, the secondary side of the transformer is connected in parallel with three copper foil layers. Additionally, the primary and secondary windings are interleaved to achieve lower ac resistance. A 1.5-kW GaN *LLC* prototype is built with a 650 kHz resonant frequency. The *LLC* power density is 524 W/in^3 and the efficiency is up to 98% with 28 V/53.5 A output at full load.**

***Index Terms*—Gallium nitride (GaN), *LLC* converter, planar transformer, synchronous rectification (SR).**

I. Introduction

HIGH efficiency and high power density are attractive in modern industrial power supplies, which are widely used in unmanned aerial vehicles, servers, industrial robots, and data centers. It has been reported that Google and Microsoft consume more than 1120 and 600 GWh annually [1]. *LLC* converters have gained popularity owing to their capability to effectuate primary side zero voltage switching (ZVS) as well as secondary side zero current switching [2], [3], [4], [5], as a result enabling the achievement of high efficiency.

In recent years, *LLC* converters have been moving toward high frequency, which helps to reduce the size of the passive devices and increase the overall power density [6]. Compared to Si MOSFET, gallium nitride (GaN) has a faster turn-on speed and smaller gate charge total (Q_g), making it more suitable for high-frequency and high-efficiency applications [7], [8], [9]. Generally, synchronous rectification (SR) and planar transformer designs are two of the most important aspects to achieve high *LLC* efficiency in high-current applications.

A. SR in High-Current Applications

The SR strategies for low-voltage and high-current applications are mainly divided into two types: drain-to-source v_{ds} sensing methods and sensorless methods.

For the drain-to-source v_{ds} sensing method, it mainly collects the voltage of the SR body diode to adjust the on-time of the SR [10]. However, due to the package parasitic inductance, the high *dv/dt* and *di/dt* caused by fast switching can generate voltage spikes and ringing [11]. In [12], an auxiliary circuit was added to filter out the noise caused by the parasitic inductance. Integrating complex v_{ds} sampling circuit into integrated circuit (IC) is a good way to save printed circuit board (PCB) space [13]. However, a large portion of duty cycle is easily lost in the analog chips, so an approach is proposed in [14] to adjust the SR on-time using a ripple counter to minimize the body diode on-time. In [15] and [16], considering SR parasitic capacitance v_{ds} method is proposed using the extra circuit, which improves the SR on-time accuracy. Although the drain-to-source v_{ds} sensing method is being improved, the IC still occupies PCB space.

With the development of research, many modeling methods considering SR parasitic capacitance have been studied. In [17], the extended SR turn-on time is proposed to regulate the light-load voltage. In [18] and [19], the ZVS process and guidelines of the circuit are provided. The SR method improved efficiency by the dead time regulation and better transient characteristics with

Manuscript received 17 July 2023; revised 13 December 2023; accepted 7 February 2024. Date of publication 19 February 2024; date of current version 20 March 2024. This work was supported in part by the National Natural Science Foundation of China under Grant 52377164, in part by the Natural Science Foundation of Anhui Province under Grant 2308085QE179, and in part by the Outstanding Youth Fund of Anhui Natural Science under Grant 2108085J24. Recommended for publication by Associate Editor F. Costa. *(Corresponding author: Haoran Li.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3366884.

Digital Object Identifier 10.1109/TPEL.2024.3366884

TABLE I
COMPARISONS OF LOW-VOLTAGE HIGH-CURRENT SR ALGORITHMS

Detailed method for considering SR capacitance	Frequency	Additional loss	Circuit complexity	Algorithm complexity	Efficiency of full load
IC v_{ds} sensing method [15]	467 kHz	Medium	Medium	None	High
v_{ds} sensing method to use comparator [16]	507 kHz	Medium	High	None	Medium
Extended SR turn-on time [17]	550 kHz	None	Low	High	Medium
ZVS process mechanism [18]	490 kHz	None	Low	High	-
ZVS analysis and design [19]	80 kHz	None	Low	High	Low
Dead time regulation [20]	98 kHz	Medium	Medium	Medium	Medium

the instantaneous drain voltage information [20]. The existing references mainly use the SR parasitic capacitor to analyze the circuit state instead of calculating the SR on-time.

Furthermore, a method is proposed in [21] that the SR on-time only takes into account the frequency variations. The adaptive regulation of the driving signal is achieved by establishing a mathematical model and adjusting the duty cycle of SR in real time according to the switching frequency and load conditions [22]. Since the equation for the SR calculation time derived by this method is extremely complex, a simplified algorithm for second-order fitting is proposed in [23]. In [24], a mathematical model was developed in the frequency domain to calculate the on-time of the SR. However, the formula obtained remains complex.

Table I summarizes the characteristics of the above SR methods. While various SR techniques offer distinct advantages, there is ample opportunity for further enhancement.

B. Planar Transformer Design

On the one hand, SR algorithms can effectively enhance the efficiency of *LLC* converters. On the other hand, the design of magnetic components also plays a critical role in boosting the power density of the converter.

In [25], a structure with multiple transformers to form a matrix transformer was proposed, which helps to reduce the secondary current stress of a single transformer. However, these designs still have the problem of complex structure with multiple cores and there is a room for efficiency improvement. In [26] and [27], the litz-wire winding is used to design high-frequency resonant inductors to reduce ac losses. In [28], the transformer is integrated with the resonant inductor by using an additional UI core. However, these approaches add excess losses by using an extra UI core and take up extra PCB space.

In order to solve this problem, the integrated transformer structure with controlled-leakage inductance is proposed in [29], but the transformer ratio is 1. In [30], a transformer loss model is proposed and a four-post magnetically integrated transformer is designed by using the leakage inductance as a resonant inductor, and the terminal loss and core loss are obviously reduced. To further shrink the core size and increase the power density of the converter, the design method of 1/4-turn high-frequency transformer was explored in [31]. A similar concept was used in [32] for a 1 kW *LLC* converter. To reduce the PCB loss, the partially interleaved PCB planar transformer is used [33]. Termination design and optimization of high-current PCB-winding matrix transformer is proposed in [5]. A method is presented to create a modular magnetic structure suitable for a wide range of voltage by integrating the matrix inductor with the structure [34].

TABLE II
KEY DESIGN SPECIFICATIONS

Parameters	Specifications
Input voltage	370–390 V
Output voltage/current	28 V/53.5 A
Rated power	1.5 kW
Output efficiency (at full load)	≥97%
Size (L×W×H)	63.1 mm×60.6 mm×12.7 mm

Although the magnetic integration method is helpful to improve the power density, the ac loss is increased due to the large winding loss in low-voltage and high-current applications. The conventional PCB or Litz wire is hardly used because the PCB or Litz wire current carrying capacity is limited. The method by stacking PCB or increasing numbers of Litz wire will increase the converter volume largely and decrease the power density.

In this article, the SR algorithm based on charge conservation is proposed, which allows online adjustment of the SR conduction time to improve the *LLC* efficiency and avoid the effect of high *dv*/*dt*. Moreover, a design for the planar transformer is presented using the secondary-parallel multiple interleaved copper foil winding structure, which reduces the dc resistance and ac resistance significantly.

The rest of the article is organized as follows. Section II specifies the existing issues in the state of the art. Section III presents the advantages of SR control and planar transformer design. The proposed SR model is analyzed in Section IV. The four candidate planar transformers are analyzed and the most suitable structure is adopted in Section V. Section VI provides the experimental results. Finally, Section VII concludes the article.

II. CHALLENGES FOR 1.5 KW *LLC* CONVERTER

A. Requirements and Specifications

The key design specifications are given in Table II. From Table II, the output voltage is required to be regulated at 28 V within a range of 370–390 V. The size of the converter is 63.1 mm × 60.6 mm × 12.7 mm and the output rated power is 1500 W, which makes the converter power density of 524 W/in^3. The full load efficiency is more than 97%. These requirements pose a serious challenge to the design of the *LLC* converter.

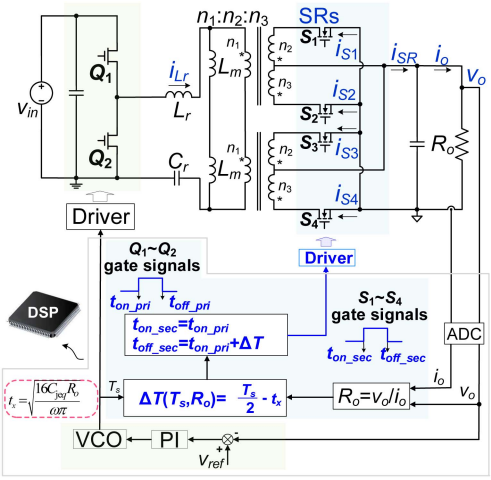


Fig. 1. Proposed *LLC* SR control based on charge conservation.

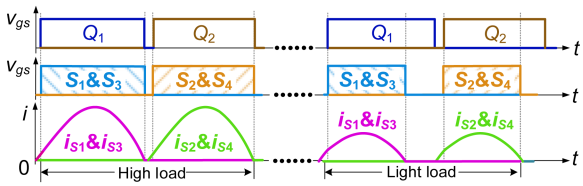


Fig. 2. Waveforms of the *LLC* converter at resonant frequency.

B. Challenges of High Efficiency and High Power Density

In low-voltage and high-current applications, *LLC* converter has huge challenges, such as accurate drive of SR, winding losses, and termination losses. The method of detecting high-frequency v_{ds} using external circuits is prone to losing the SR duty cycle, which limits efficiency improvement.

Although PCB planar transformers reduce the size of magnetic components to increase power density, the PCB current carrying capacity is limited. A low-cost approach to reducing current density by stacking PCBs is exceeded by the required height of the converter. Therefore, it is necessary to propose the *LLC* converter with high efficiency and high power density.

III. Proposed SR Algorithm and Secondary-Parallel Multiple Interleaved Transformer Design

A. Proposed SR Algorithm Based on Charge Conservation

Fig. 1 illustrates the proposed *LLC* SR control and Fig. 2 displays the proposed SR control waveforms. i_{S1}, i_{S2}, i_{S3}, and i_{S4} are the SR current. t_{on_pri} and t_{off_pri} are the turn-on and turn-off moments of the GaN, respectively. t_{on_sec} and t_{off_sec} are the opening and closing moments of the SR, respectively.

The proposed SR method requires the sampling signals of output dc voltage and current to calculate the SR on-time in the digital signal processor (DSP). The turn-on time of SR is consistent with the turn-on time of the primary GaN devices, whereas the SR turn-off instant is based on the calculated conduction time from the proposed SR.

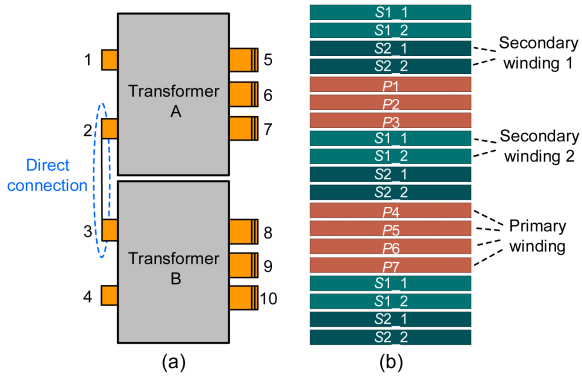


Fig. 3. Secondary-parallel multiple interleaved copper foil transformer. (a) Transformer connection structure. (b) Single transformer winding.

The conventional v_{ds} detection method uses the parasitic capacitances to estimate SR on-time in [15] and [16], which occupies the extra PCB areas and easily operates falsely due to high *dv/dt*. In addition, compared with the complicated SR on-time equation method [22], the proposed method is simple to implement and calculates the SR on-time with the SR parasitic capacitance.

B. Proposed Secondary-Parallel Multiple Interleaved Copper Foil Planar Transformer Design

The design of an isolated high-current output dc–dc converter has been a huge challenge, mainly due to the huge conduction loss, termination loss, and ac loss on the secondary side of the transformer. Fig. 3 depicts the structure of the proposed secondary-parallel multiple interleaved transformer design.

In Fig. 3(a), the termination 1–4 is connected to the primary side winding and the termination 5–10 is connected to the secondary side winding. The two transformers are connected in series on the primary winding and in parallel on the secondary winding. Compared to using a single transformer, this structure effectively reduces the current stress on the secondary side of the transformer and reduces the conduction loss. The dashed circle in Fig. 3(a) indicates direct connection without power transfer through the PCB, which decreases the termination loss.

Fig. 3(b) displays the structure of the single transformer winding. The ratio of the single transformer is 7:2:2, with secondary winding 1 and secondary winding 2 being the transformer's secondary windings. *P*1–*P*7 denote the primary winding. *S*1_1, *S*1_2, *S*2_1, and *S*2_2 denote the secondary winding. To reduce the secondary side dc conduction resistance, the transformer uses the copper foil winding and the secondary winding is connected in parallel with three layers of copper foil. Furthermore, the primary and secondary windings are interleaved to decrease transformer ac resistance, so that reducing the ac loss.

It is different from the conventional PCB planar transformer used in high-output current applications [30]. The proposed planar transformer adopts multiple interleaved copper foil windings in parallel, which effectively reduces the dc loss and ac loss of the winding.

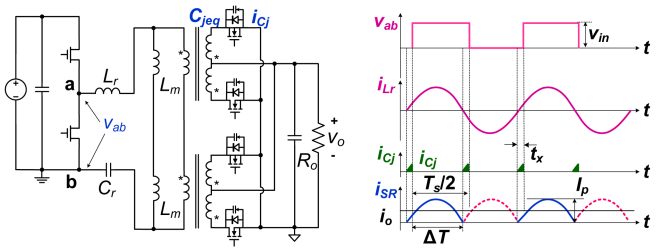


Fig. 4. *LLC* converter and waveforms. (a) Topology. (b) Waveforms.

C. Advantages of the Proposed SR and Transformer Design

The benefits of the proposed SR scheme and transformer design are as follows.

1) The proposed SR scheme achieves accurate conduction time without sampling high-frequency signals of v_{ds} and greatly avoids the effect of high *dv*/*dt* for the SR on-time.
2) The design of the planar transformer is proposed by using secondary-parallel multiple interleaved copper foil winding, which largely reduces the dc resistance and ac resistance.
3) By using the proposed SR algorithm and planar transformer design, the *LLC* converter achieves high efficiency and high power density.

IV. Proposed SR Calculation Modeling

By building the proposed SR mathematical model, the SR on-time is calculated to improve the *LLC* efficiency. Due to the advantage of high-precision digital control, the SR on-time is implemented precisely to reduce conduction loss.

A. Proposed SR Calculation Modeling Based on Charge Conservation

Fig. 4 shows the topology and operating waveforms of the *LLC* converter. In order to simplify the derivation, the following assumptions are used.

1) In the half cycle, the rectifier waveform period of the *LLC* converter is $T_s/2$ and the charging current is an ideal delta wave.
2) The power devices, transformers, resonant inductor, resonant capacitors, and passive devices in the *LLC* converter are ideal. The dead time is also ignored to simplify analysis.

In Fig. 4, ΔT is the SR conduction time, T_s is the switching period, C_{jeq} is the parasitic capacitance, and i_{Cj} is the SR charging current of the parasitic capacitor.

The expression of the current waveform on the rectifier side is

$$i_{SR}(t) = I_p \sin(\omega t) \quad 0 \le t \le \Delta T \tag{1}$$

where I_p is the peak current on the rectifier side. ω is angular frequency, $\omega = \pi/\Delta T$. ΔT is the conduction time for the current to flow through the SR MOSFET. I_p can be calculated from

$$\int_0^{\Delta T} i_{SR}(t)dt = i_o \Delta T \tag{2}$$

$$I_p = \pi i_o/2 \tag{3}$$

where i_o is the output current. The charge stored during the charging of the capacitor is

$$Q = C_{jeq} v_{jeq} \tag{4}$$

$$v_{jeq} = 2v_o \tag{5}$$

where v_{jeq} is the SR MOSFET voltage and C_{jeq} is the parasitic capacitance. Assuming that the charging current is an ideal delta wave, it can be deduced as

$$0.5\pi i_o \int_0^{t_x} \sin(\omega t)dt = 4C_{jeq} v_o. \tag{6}$$

t_x is the conduction time when the SR current flows through the MOSFET body diode. Since $t_x << T_s$, $\sin(\omega t)$ is approximately equal to ωt. Thus, it is

$$0.25\pi i_o \omega t_x^2 = 4C_{jeq} v_o. \tag{7}$$

t_x can be simplified as

$$t_x = \sqrt{16C_{jeq} R_o/(\pi\omega)} \tag{8}$$

where R_o is the equivalent output load. The SR conduction time can be deduced as

$$\Delta T = T_s/2 - t_x. \tag{9}$$

Fig. 5 shows the comparisons of SR conduction time. The digital SR driver scheme in [22] is consistent with the simulation times at 630 and 710 kHz. For the proposed algorithm, the maximum conduction time tolerance is only 2.9% (corresponding to 20 ns) at 630 kHz. Therefore, the proposed algorithm achieves accurate SR conduction time and optimizes the on-time of SR body diode.

TABLE III
Comparisons of Consumed CPU Cycles

	[22]		Proposed method	
Types	Number	CPU cycles	Number	CPU cycles
Addition	2	2	0	0
Subtraction	1	1	1	1
Multiplication	24	48	3	6
Division	4	96	2	48
Root	2	56	1	28
Total period		203		**83**

B. Execution Time Analysis in DSP

The proposed control scheme is implemented using the Texas Instrument (TI) TMS320F280049C, a DSP with a clock master frequency f_{clk} up to 100 MHz.

Table III shows the comparisons of the consumed central processing unit (CPU) cycles. The execution cycle for different operations in the DSP is determined based on [36]. The values presented in Table III correspond to the ideal case. Based on

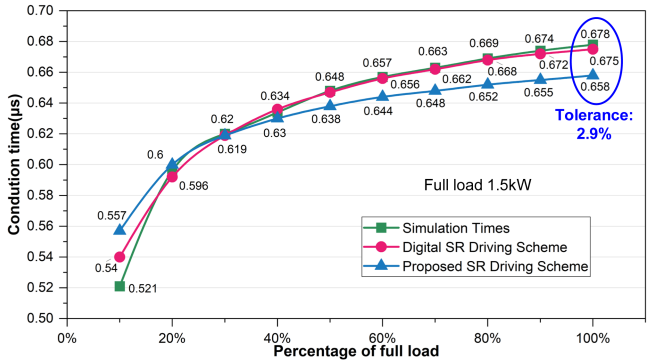


Fig. 5. SR on-time comparisons at $v_o = 28$ V. (a) $f_s = 630$ kHz. (b) $f_s = 710$ kHz.

Table III, the proposed algorithm reduces the DSP computation cycles by 59.1% compared to [22], which demonstrates the simplicity of the proposed algorithm.

C. Soft Start-Up Strategy

The soft start-up is an important process in *LLC* converter control. In this article, the pulsewidth modulation duty cycle is gradually increased for soft start-up.

Using fundamental harmonic approximation analysis, *LLC* circuit can be equivalent to a low-pass filter. When the switching frequency is equal to the resonant frequency, the change of v_{ab} with duty cycle D is calculated as

$$v_{ab}(t) = \frac{v_{in}}{2\pi}\sum_{n=1}^{\infty}\frac{1-(-1)^n}{n} \times\left[\cos n\pi\left(\frac{1-D}{2}\right)-\cos n\pi\left(\frac{1+D}{2}\right)\right]. \times \sin(n\omega t) \tag{10}$$

Considering only the fundamental wave, the above formula can be equivalent to

$$v_{ab}(t) = \frac{v_{in}}{\pi}\left(\cos\frac{1-D}{2}\pi-\cos\frac{1+D}{2}\pi\right)\sin\omega t = (v_{in}/\pi)H(D)\sin\omega t \tag{11}$$

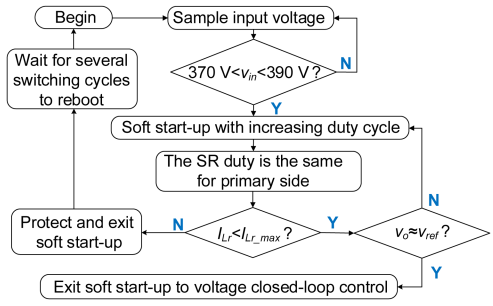


Fig. 6. Flowchart of soft start-up control.

where $H(D)$ is a function of the variable D, denoted as H. The resonant current can be written as

$$i_{Lr}(t) = v_{ab}(t)/Z(j\omega) = I_{Lr}\sin(\omega t+\varphi) \tag{12}$$

where I_{Lr} represents the resonant current peak value, φ is the phase, and $Z(j\omega)$ is the equal impendence of the resonant tank.

The relation between input power and input power is

$$\int_0^{\Delta T} v_o i_o dt = \eta\int_0^{\Delta T} v_{ab}(t)i_{Lr}(t)dt \tag{13}$$

where η is the efficiency. Based on (11)–(13), it is obtained that

$$I_{Lr} = \frac{4\pi\omega\Delta T}{\eta H v_{in}\left[\sin(\varphi)-\sin(2\omega\Delta T+\varphi)+2\omega\Delta T\cos(\varphi)\right]}v_o i_o = f(H)P_o \tag{14}$$

where P_o is the output power and $f(H)$ is a function of the variable H. Therefore, I_{Lr} can be controlled by controlling the D.

Fig. 6 shows the flowchart of soft start-up control. If the resonant current exceeds the maximum value $I_{Lr\_\max}$, the soft start-up is exited for protection. When output voltage v_o approaches the output rated voltage v_{ref}, the soft start-up is exited for voltage closed-loop control.

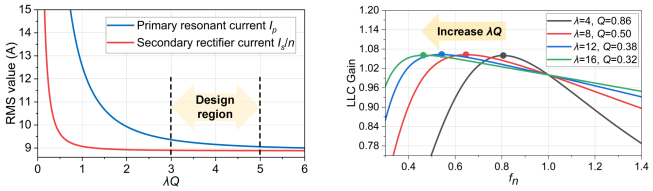
V. Secondary-Parallel Multiple Interleaved Copper Foil Planar Transformer and Inductor Design

By theoretical calculation, the core type is adopted. Four alternative transformer copper foil winding interleaved structures are proposed through theoretical analysis. The parallel multiple interleaved winding structure has the lower winding loss than others in Maxwell.

A. Calculation of Resonant Parameters

With a resonant frequency of 650 kHz, the calculated maximum and minimum gains are 1.059 and 1.005, respectively. Because the required gain is small, a larger λ can be chosen to minimize turn-off losses. Based on [34], the rms values of primary resonant current I_p and SR current I_s are obtained

$$I_p = \frac{1}{4\sqrt{2}}\frac{v_o}{nR_o}\sqrt{\frac{4\pi^2}{(\lambda Q)^2}+4\pi^2} \tag{15}$$



(a) (b)

Fig. 7. Influence of λQ. (a) Impact of λQ on primary and secondary rms current. (b) λ and Q combinations to achieve the 1.06 peak gain.

$$I_s = \frac{\sqrt{2}\sqrt{3}}{24\pi}\frac{v_o}{R_o}\sqrt{(5\pi^2-48)\frac{4\pi^2}{(\lambda Q)^2}+12\pi^4}. \quad (16)$$

From (15) and (16), I_p and I_s are related to the product of λQ. Fig. 7(a) shows the relationship between λQ and *LLC* rms current. The lower λQ increases the circulating energy in the resonant tank. The larger λQ should be chosen to reduce the effective value of the primary side and secondary side current. However, the large λQ makes the peak gain move to the low frequency, which increases the difficulty of frequency modulation, as shown in Fig. 7(b). Therefore, the λQ should be chosen at the knee point. The L_m is chosen as 25 μH and L_r is chosen as 2.7 μH.

B. Design of Copper Foil Planar Transformer Core

To minimize the core loss while satisfying converter size requirements, it is necessary to achieve the lower resonant frequency. The transformer can be designed as follows.

1) Transformer Turns Ratio: Since it is a half-bridge structure, the transformer turns ratio is

$$n = v_{in}/2v_o. \quad (17)$$

From (17), the single transformer ratio n is 7:2:2.

2) Transformer Core Design: The effective core area A_e is dominant in the transformer design. Radius r of the central leg of the core can be determined as

$$r = \sqrt{nv_o/(8\pi B_{\max} N_p f_s)} \quad (18)$$

where N_p is the number of turns on the transformer primary side. The EC28L was selected as the core for this design with a column core radius of 6.2 mm. The core material is DMR51 from Dongyang Magnetics Enterprise Group Company (DMEGC). From Fig. 8, the core loss is 1.5 W at the magnetic density of 60 mT with the maximum switching frequency of 710 kHz, which meets the design requirements.

C. Proposed Secondary-Parallel Multiple Interleaved Winding Design

The dc loss and ac loss of transformer winding are closely related to the thickness and distribution of the winding. Four winding distributions are designed and analyzed in Maxwell to select the optimal winding structure.

1) Calculation of Winding Thickness: To determine the appropriate winding thickness for the transformer, the skin depth needs to be calculated based on the converter resonant frequency

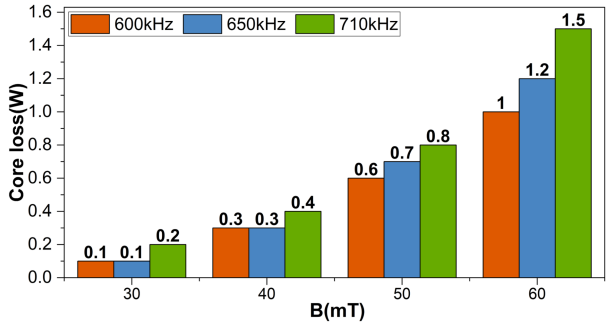


Fig. 8. Transformer core losses at different magnetic density.

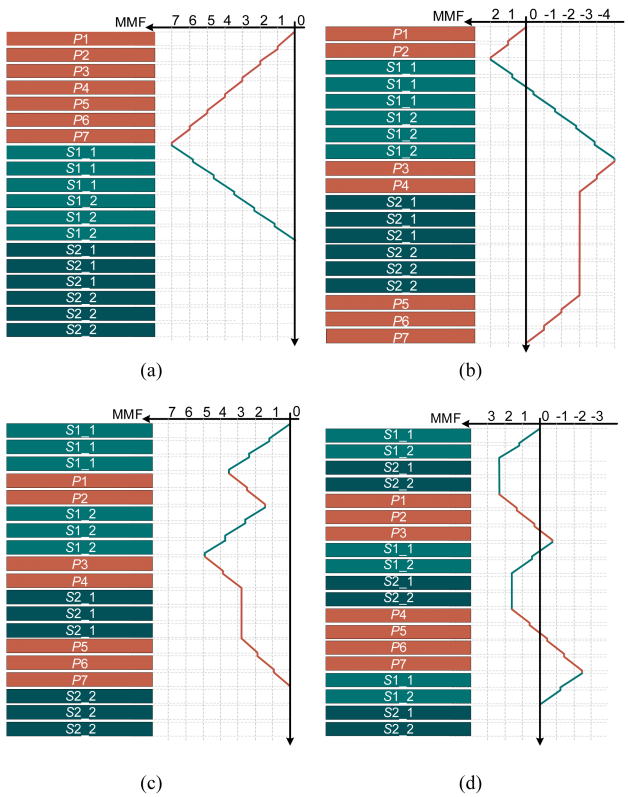


Fig. 9. Four candidates of winding interleaved and MMF analysis. (a) Case A. (b) Case B. (c) Case C. (d) Case D.

of 650 kHz using

$$\delta = \sqrt{\rho/(\pi\mu_0\mu_r f_s)} \quad (19)$$

where ρ denotes the resistivity of the material. Typically, the transformer winding is less than twice the skin depth. Thus, the copper foil winding with 0.2 mm thickness is selected.

2) Four Candidates of Interleaved Winding Structure: The interleaved winding structure can effectively reduce the magnetomotive force (MMF). However, the excessive number of interleaved primary and secondary sides may elevate the junction capacitance of the windings [33].

At this time, four winding interleaved structures were designed, as shown in Fig. 9. The primary side is seven turns winding. The secondary side is two turns with three layers in parallel. The MMF distribution is shown in Fig. 9.

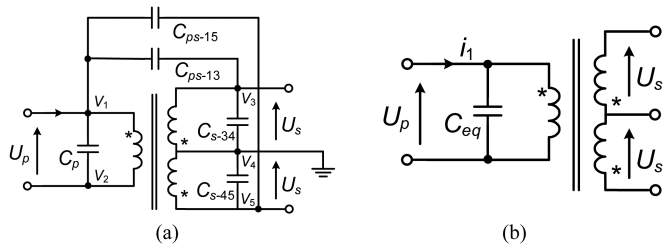


Fig. 10. Capacitance of transformer model. (a) Distribution of capacitance. (b) Equivalent circuit for primary side.

Compared with the completely noninterleaved and partially interleaved winding structures, the parallel multiple interleaved winding structure has the smallest MMF, which means that the current density distribution is more balanced. The reason that the MMF of the secondary winding is only on one side is the full wave rectification that only one secondary winding is in the on-state at the same time and the other winding is in the off-state.

Fig. 9(a) shows a completely noninterleaved winding structure, which can increase the leakage inductance and integrate the resonant inductor into the transformer, but the disadvantage is that it increases the ac loss and core loss. Fig. 9(b) and (c) shows the partial interleaved winding structure. Fig. 9(d) shows the parallel multiple interleaved winding structure.

3) Calculation of Winding Loss: The dc resistance of the copper foil winding is expressed by R_{dc}, which is related to the thickness, cross-sectional area and length of the copper.

Dowell's equation states that when a sinusoidal ac current is passed through the winding, the ac impedance consists of R_{ac_sk} and R_{ac_pro}. R_{ac_sk} and R_{ac_pro} indicate the ac resistance caused by the skin effect and proximity effect, respectively, expressed as

$$R_{ac\_sk} = \frac{\xi}{2}\frac{\sinh(\xi)+\sin(\xi)}{\cosh(\xi)-\cos(\xi)}R_{dc} \tag{20}$$

$$R_{ac\_pro} = \frac{\xi}{2}(2m-1)^2\frac{\sinh(\xi)-\sin(\xi)}{\cosh(\xi)+\cos(\xi)}R_{dc} \tag{21}$$

where $\xi = h/\delta$, h is the copper thickness and δ is the skin depth. m denotes the MMF of per layer. Therefore, the total transformer winding loss is determined by R_{ac_sk} and R_{ac_pro}.

Based on (20), (21), and Fig. 9, it can be concluded that the parallel multiple interleaved winding structure has the low power loss caused by proximity effects while the skin effect is only frequency dependent.

4) Calculation of Equivalent Parasitic Capacitance: Fig. 10(a) shows the distributed capacitance with a central tapped transformer, where C_p, $C_{s\text{-}34}$, and $C_{s\text{-}45}$ are interwinding capacitances and $C_{ps\text{-}13}$ and $C_{ps\text{-}15}$ are the capacitances between primary and secondary windings. Fig. 10(b) shows the parasitic capacitance model equivalent to the primary side.

From Fig. 10, Kirchhoff's current law is applied

$$\begin{aligned} i_1 = {} & (V_1 - V_3)j\omega C_{ps-13} + (V_1 - V_5)j\omega C_{ps-15} \\ & + V_1 j\omega C_p + N^2 V_1 j\omega C_{s-34} + N^2 V_1 j\omega C_{s-45} \end{aligned} \tag{22}$$

TABLE IV
TRANSFORMER PARASITIC CAPACITANCE PARAMETERS

Parameters	Value	Parameters	Value
C_p	86.6 pF	$C_{s\text{-}34}$	52.4 pF
$C_{s\text{-}45}$	52.5 pF	$C_{ps\text{-}13}$	34.7 pF
$C_{ps\text{-}15}$	34.7 pF	C_{eq}	164.6 pF

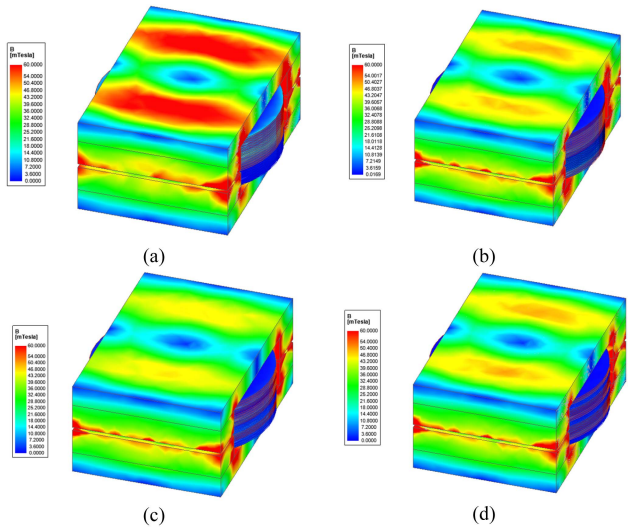


Fig. 11. Simulations of magnetic density distribution. (a) Case A. (b) Case B. (c) Case C. (d) Case D.

where N is U_s/U_p, V_1–$V_3 = V_1(1–N)$, V_1–$V_5 = V_1(1+N)$, $N = V_3/V_3$. Thus, C_{eq} is

$$\begin{aligned} C_{eq} = {} & (1-N)C_{ps-13} + (1+N)C_{ps-15} + C_p \\ & + N^2 C_{s-34} + N^2 C_{s-45}. \end{aligned} \tag{23}$$

A planar transformer model is established in Maxwell electric field. Through simulation analysis, the value of transformer parasitic capacitance is shown in Table IV. Thanks to the proposed transformer design, the parasitic capacitance C_{eq} is low.

5) Analysis of Transformer Loss in Maxwell Simulation: The transformers with four candidate winding structures were constructed in Ansys Maxwell eddy current field and the resonant frequency was set at 650 kHz. The primary current rms value I_{pri_RMS} of a single transformer is 8.1 A and the secondary current rms value I_{sec_RMS} is 20.5 A.

Fig. 11 shows the magnetic density distribution. Except for case A, the magnetic density of the other three cores is basically below 50 mT due to the high-frequency applications, which means the lower core loss.

Fig. 12 shows the transformer winding current density distribution of the primary side and secondary side. Although the current of the secondary side is up to 53 A, the current density of the secondary side is greatly reduced because the multilayer copper foil is connected in parallel. From Fig. 12, it can be obtained that the current density of the four candidates is basically below 30 A/mm^2. In particular, Case D is essentially lower than 20 A/mm^2, which is mainly benefited from the

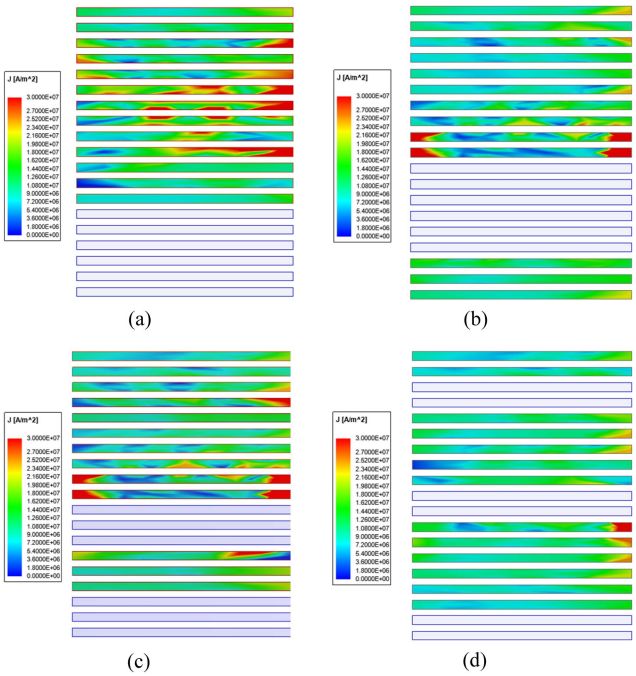


Fig. 12. Simulations of current density distribution. (a) Case A. (b) Case B. (c) Case C. (d) Case D.

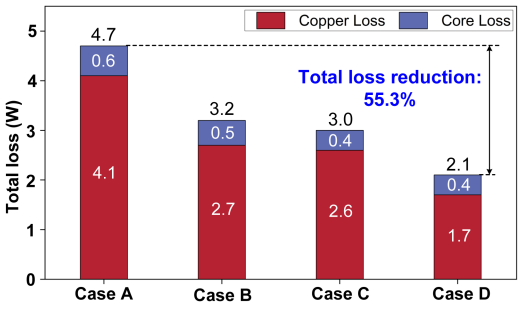


Fig. 13. Loss comparisons: $I_{pri\_RMS} = 8.1$ A, $I_{sec\_RMS} = 20.5$ A, and $f_s = 650$ kHz.

TABLE V
RESONANT INDUCTOR PARAMETERS

Parameters	Value	Parameters	Value
Core material	DMR51	L_r	2.7 μH
A_e	62.6 mm^2	N_1	6

parallel multiple interleaved winding structure making his current density distribution more uniform.

In Fig. 13, the total losses of Case A, Case B, Case C, and Case D are 4.7, 3.2, 3.0, and 2.1 W, respectively. Both winding loss and core loss of Case D is minimum. Compared with Case A, the total loss of Case D is reduced by 55.3%, which mainly benefits from the proposed winding structure.

D. Design of Copper Foil Winding Inductor

The inductor design method is similar to the transformer. Thus, the EC19.4 from DMEGC is selected as the core of

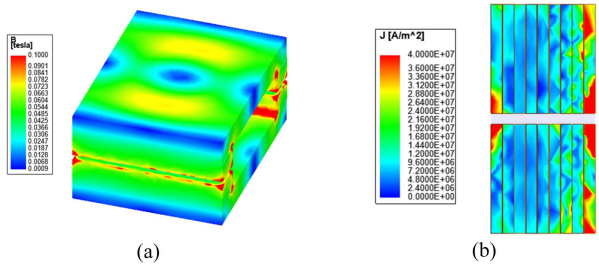
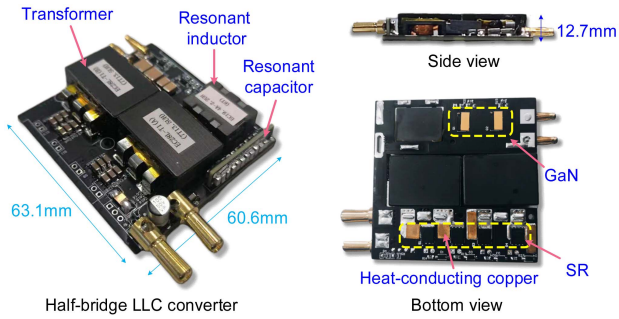
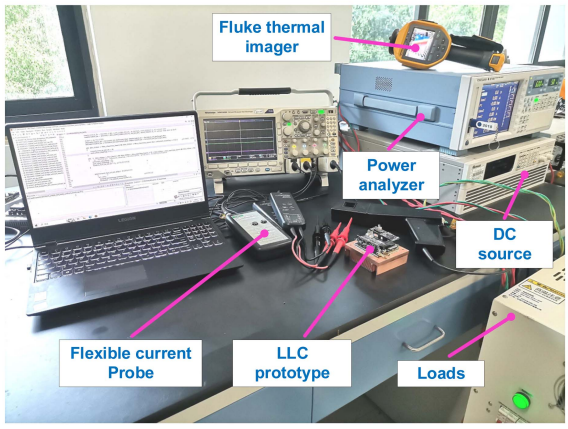


Fig. 14. Inductor simulation. (a) Magnetic density distribution. (b) Current density distribution.



(a)



(b)

Fig. 15. Prototype and platform. (a) *LLC* converter. (b) Platform.

resonant inductor. The detailed parameters are shown in Table V. N_1 is the winding turns.

The inductor model is established in the Maxwell eddy current field and the frequency is set to 650 kHz. The inductor was wrapped in three layers with 0.2 mm copper foil. Fig. 14(a) shows that the inductor flux density is basically below 70 mT and Fig. 14(b) shows that the current density is less than 30 A/mm^2. The core loss is 0.7 W and the winding loss is 2.5 W. Therefore, the inductor design meets the requirement of low loss.

VI. EXPERIMENTAL RESULTS AND DISCUSSION

A. Experimental Prototype

To validate the proposed method, a GaN *LLC* converter prototype with 650 kHz resonant frequency was built, as demonstrated in Fig. 15(a). Fig. 15(b) shows the experimental platform. The

TABLE VI
KEY PARAMETERS OF PROTOTYPE

Symbol	Parameters	Symbol	Parameters
v_{in}	370–390 V	v_o	28 V/53.5 A
L_m	25 μH	n_1:n_2:n_3	7:2:2
L_r	2.7 μH	C_r	1 nF×22 (ceramic)
C_o	100 μF+10 μF×12 (aluminum + ceramic)	C_{in}	1 μF×2 (ceramic)
T_r core	EC28L, DMR51 (DMEGC)	L_r core	EC19.4A, DMR51 (DMEGC)
Q_1–Q_2	GS66508T (GaN systems, 650 V 30 A)	S_1–S_4	ISC027N10NM6 (Infineon, 100 V, 192 A)
Primary driver	Si8271GB (SILICON LABS)	SR driver	UCC27511A (TI)

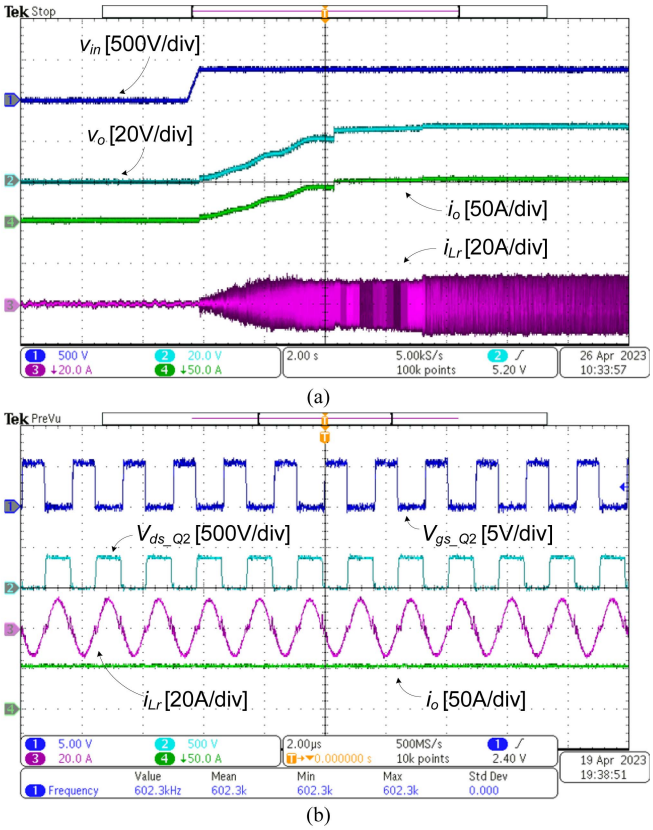


Fig. 16. *LLC* operation waveforms. (a) Soft start-up at $v_{in} = 390$ V, $P_o = 1.5$ kW. (b) Operated at $P_o = 1.5$ kW, $f_s = 602$ kHz.

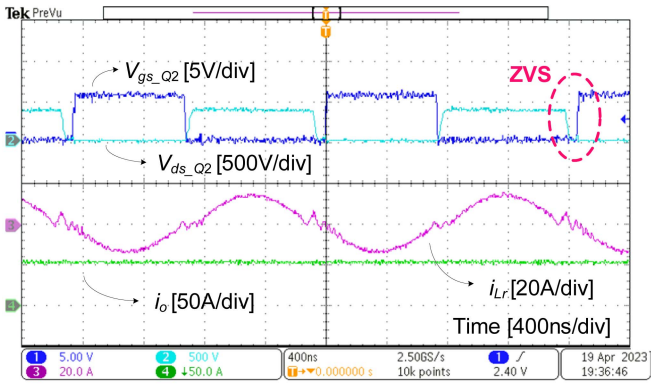


Fig. 17. ZVS characteristic at $P_o = 1.5$ kW and $v_o = 28$ V.

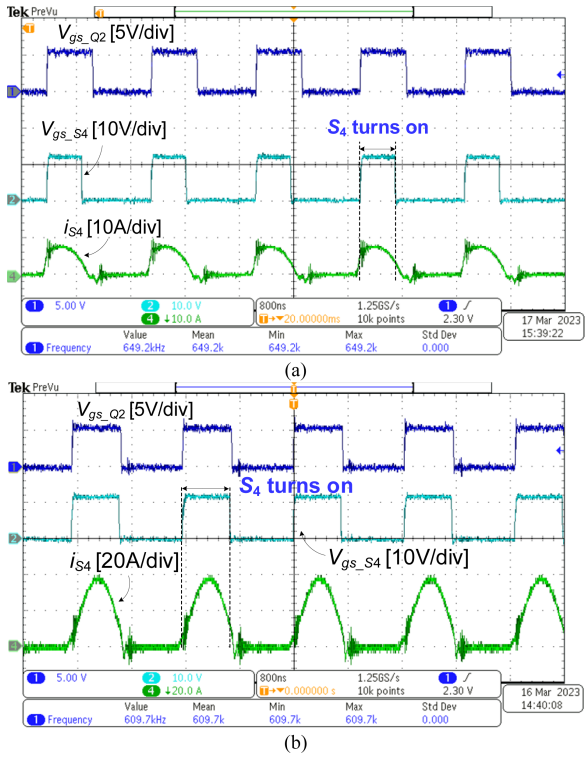


Fig. 18. SR waveforms at different loads. (a) $P_o = 0.2$ kW, $f_s = 649$ kHz. (b) $P_o = 1.5$ kW, $f_s = 610$ kHz.

prototype uses GaN systems 650-V 30-A (GS66508T) devices on the primary side. Infineon's 100-V 192-A (ISC027N10NM6) is used for the SR MOSFETs. The single transformer ratio is 7:2:2. The output voltage is required to be regulated at 28 V within a range of 370–390 V and the full load power is 1.5 kW. The detailed parameters of the prototype are given in Table VI.

B. LLC Operation Waveforms

Fig. 16 illustrates the waveforms of the prototype soft start-up and operating at full load. The resonant current reaches the rated value without overshoot from Fig. 16(a), which indicates that the converter starts steadily. The output current and resonant current reach the rated value from Fig. 16(b) and the converter runs stably at full load.

The ZVS characteristic is shown in Fig. 17. Thanks to the low parasitic capacitance of transformer structure, the prototype achieves the ZVS characteristics to maintain the high efficiency.

The SR waveforms under varying load conditions are shown in Fig. 18. From Fig. 18, the on-time of SR progressively increases with the load increment, which achieves precise control and validates the proposed SR.

Fig. 19 shows the waveforms of the load transition from 1.3 to 0.7 kW. As depicted in Fig. 19, the switching frequency varies from 613 to 625 kHz with the change in load. Thus, the proposed SR algorithm accomplishes the expected control.

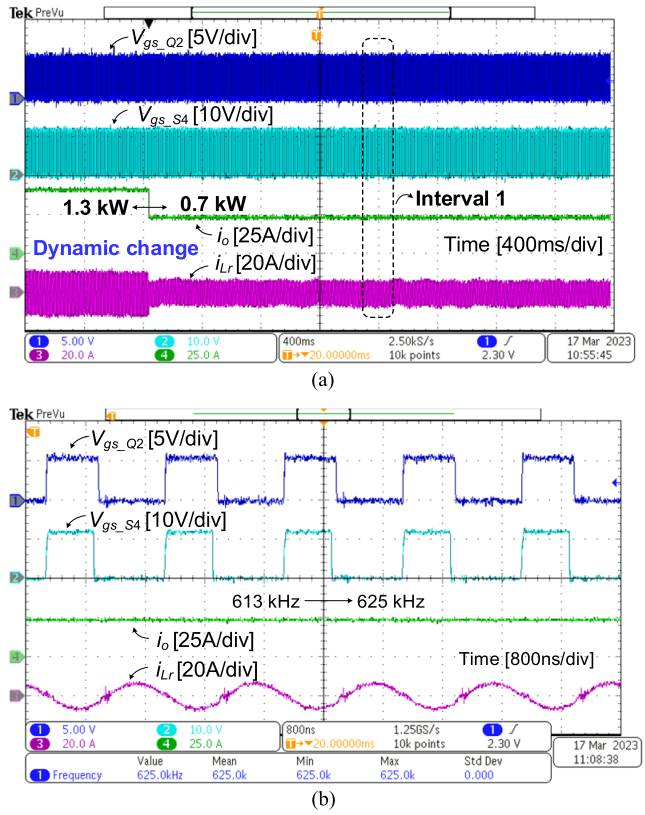


Fig. 19. Load changes. (a) Load changes from 1.3 to 0.7 kW. (b) Interval 1 is zoomed in.

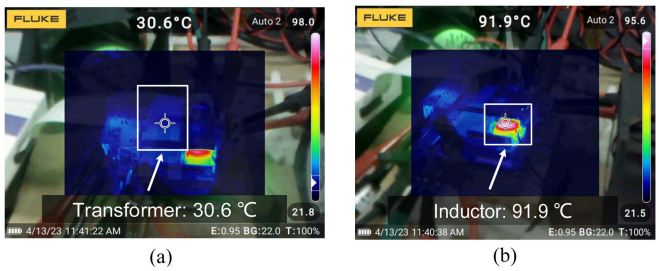


Fig. 20. *LLC* converter temperature at 1.5 kW. (a) High-frequency transformer. (b) Resonant inductor.

Fig. 20 depicts the prototype temperature distribution after 1 h of operation under forced air-cooling conditions. The transformer temperature is 30.6 °C, which indicates that the parallel multiple interleaved copper foil winding significantly reduces the loss. The resonant inductor is 91.9 °C, which means that the design of the resonant inductor is reasonable.

According to Fig. 21, the loss of a single transformer is 2.1 W, whereas the resonant inductor loss is 3.2 W, which is 52.4% higher than it. The volume of the resonant inductor is much smaller than the transformer. In addition, it resulted in a large winding loss because the MMF of the resonant inductor cannot be reduced by the distribution of the windings. Therefore, the temperature rise of the resonant inductor is higher than the transformer.

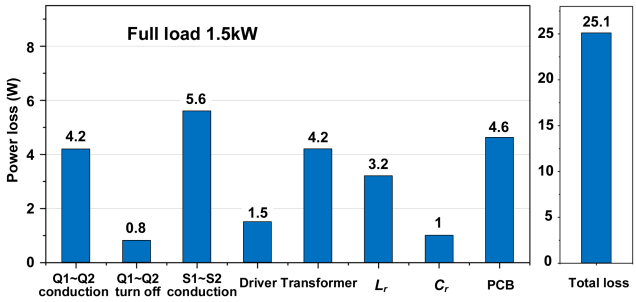


Fig. 21. Loss distribution: $v_{in} = 390$ V, $v_o = 28$ V, $P_o = 1.5$ kW, $f_s = 650$ kHz.

TABLE VII
PARASITIC RESISTANCE OF ACTUAL LAYOUT FROM Q3D

Symbol	DC_R	AC_R
R_{pri_total}	8.0 mΩ	15.9 mΩ
R_{sec_total}	2.6 mΩ	10.3 mΩ

TABLE VIII
COMPARISONS OF *LLC* CONVERTER

Ref	Frequency	Control complexity	Output voltage/ current	Power density	Efficiency
[22]	1 MHz	Complex	32 V/ 93.7 A	103 W/in^3	95.3% @3 kW
Proposed	650 kHz	Simple	28 V/ 53.5 A	**524 W/in^3**	**98.0% @1.5 kW**

C. Loss Distribution and Efficiency Comparison

Fig. 21 shows the loss distribution of the designed prototype at 1.5 kW. The transformer loss and resonant inductor loss are derived from Ansys Maxwell eddy current field and the PCB layout parasitic resistances are derived from Ansys Q3D. The PCB parasitic resistance is shown in Table VII. R_{pri_total} and R_{sec_total} indicate the total parasitic resistance of the primary power loop and secondary power loop, respectively. The total loss of the converter is 25.1 W and the efficiency is estimated to be 98.3%.

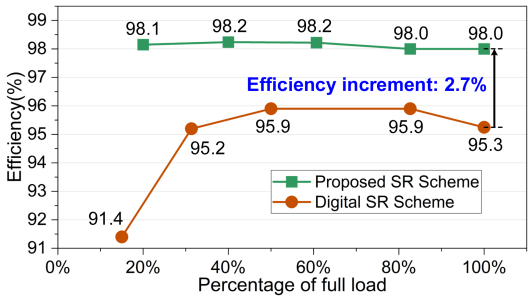
The efficiency of the digital SR scheme in [22], which is also used in low-voltage high-current applications, is compared with that of the proposed scheme under different loads in Fig. 22. The efficiency of the proposed scheme is as high as 98% at full load, which is 2.7% higher than the digital SR scheme. The efficiency curve fully illustrates the superiority of the proposed design.

Table VIII shows the comparisons of *LLC* converter with frequency, control complexity, output voltage/current, power density, and efficiency. Based on Table VIII, the prototype efficiency is up to 98% at full load and the power density is as high as 524 W/in^3, which is much higher than [22].

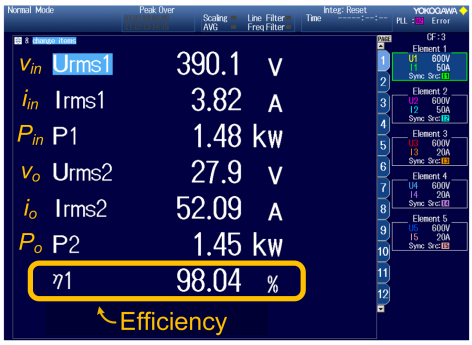
Table IX shows the comparisons of dc–dc converter. Based on Table IX, the full load efficiency of the proposed method is higher than other references. Furthermore, compared with the conventional method in [14] using the v_{ds} detection method, the proposed SR scheme is easy to implement without occupying extra PCB area and greatly avoids the effect of high dv/dt for the SR conduction time.

TABLE IX
COMPARISONS OF DC–DC CONVERTER

Ref	SR category		Transformer design			Output voltage/current	Power density	Efficiency
	Detailed information	Extra component	Winding implementation	Occupied PCB	Height			
[7]	-	-	Stacked PCB	1800 mm^2	16 mm	32 V/94 A	107 W/in^3	95.9%@3 kW
[12]	v_{ds} sensing	Filter and ICs	-	-	-	12 V/50 A	-	95.8%@0.6 kW
[14]	v_{ds} sensing	Comparator	PCB	-	-	12 V/83 A	200 W/in^3	94.2%@1 kW
[21]	From Infineon	-	Litz wires	910 mm^2	28 mm	51.5 V/64 A	66 W/in^3	97.6%@3.3 kW
[22]	Digital control	None	Stacked PCB	1800 mm^2	16 mm	32 V/93.7 A	103 W/in^3	95.3%@3 kW
[31]	-	-	Six-layer PCB	1225 mm^2	10 mm	12 V/83 A	616 W/in^3	96.5%@1 kW
[35]	From GaN systems	-	Litz wire	1176 mm^2	30 mm	54 V/55 A	146 W/in^3	97.4%@3 kW
Proposed	**Digital control**	**None**	**Copper foil**	**1064 mm^2**	**12 mm**	**28 V/53.5 A**	**524 W/in^3**	**98.0%@1.5 kW**



(a)



(b)

Fig. 22. *LLC* efficiency. (a) Prototype at $v_{in} = 390$ V, $v_o = 28$ V. (b) Full load efficiency measured by power analyzer.

VII. CONCLUSION

The SR algorithm based on charge conservation is proposed, which deduces SR on-time by calculating the time of current flowing through the SR MOSFET junction capacitor. The SR mathematical model is developed to accurately calculate the SR on-time. The turn-on times of the primary side and secondary side gate signals are the same and the SR turn-off time is equal to the turn-on time plus the calculated SR on-time. Due to the advantage of the high-resolution pulse width modulator (HRPWM), the SR on-time is implemented precisely to reduce conduction loss.

Meanwhile, the secondary-parallel multiple interleaved copper foil transformer is designed in high-output current applications. To reduce the dc resistance, the secondary side winding is connected in parallel with three layers of copper foil. The ac resistance is reduced by the winding structure of interleaved primary and secondary sides. Four interleaved winding structures were analyzed in Maxwell that the parallel multiple interleaved winding design provides a more even current density distribution and reduces the total loss by 55.3% compared to the completely noninterleaved winding design.

Compared to the conventional SR method, the proposed scheme is simple and effective, which can largely avoid the effect of high *dv*/*dt* for the SR on-time. In contrast to the conventional transformer winding design, the proposed design uses the copper foil windings and parallel multiple interleaved winding scheme, which effectively decreases the dc loss and ac loss.

A 1.5 kW GaN *LLC* converter is built. Compared to the existing method, the *LLC* efficiency is improved by 2.7% using the proposed SR scheme and transformer design. The full load efficiency is up to 98.0% with 28 V/53.5 A and the power density is as high as 524 W/in^3, which confirms the effectiveness of the proposed SR method and transformer design.

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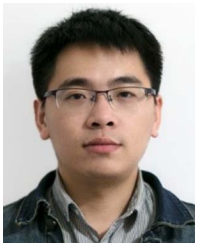

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