Efficiency-Oriented Optimized Design and Control of Hybrid FSBB–*CLLC* Converters With Partial Power Processing Capability

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***Abstract*—Combining the highly efficient *CLLC* topology with the exceedingly flexible four-switch buck–boost (FSBB) topology, this article introduces a novel hybrid FSBB–*CLLC* converter incorporating partial power processing capability. This hybrid structure utilizes FSBBs to regulate its output voltage by adjusting its duty cycle, handling a small portion of the total power, and providing a fast dynamic response. Meanwhile, the *CLLC* in the structure operates in a complete resonant state to ensure high system efficiency. By sharing a bridge arm between the FSBB and the *CLLC*, where one arm from each system serves a similar function, the number of switches utilized is significantly reduced, resulting in higher system efficiency. In addition to the structural improvements, to achieve a higher average system efficiency under different loads, this article presents an efficiency-based parameter design methodology. Furthermore, phase shift, an additional control freedom of FSBB, is employed to further enhance the system's overall efficiency; however, calculating the relationship between efficiency and phase shift can be burdensome, especially in real-time controllers. To address this issue, this article proposes a fitting-model-based maximum efficiency tracking approach to reduce calculation complexity. Ultimately, experimental results demonstrate the effectiveness of the proposed design, highlighting its enhanced performance.**

***Index Terms*—Efficiency-based parameter design, fitting model, hybrid four-switch buck–boost (FSBB)–*CLLC* converter, partial power processing (PPP), phase shift control.**

I. Introduction

As THE demand for Renewable energy sources (RESs), electric vehicles, and energy storage systems (ESSs) continues to rise, there is a growing interest in integrating these areas with dc microgrids [1], [2]. To properly realize the integration, it is necessary to achieve bidirectional voltage regulation and efficient power distribution, which are often achieved by an essential component—an isolated bidirectional dc–dc converter (IBDC) [3], as shown in Fig. 1; therefore, IBDCs have gained significant popularity.

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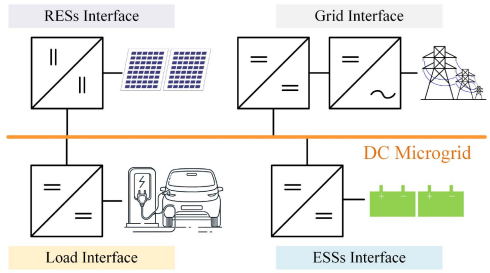
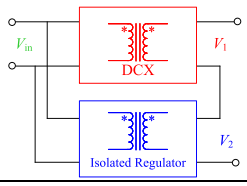
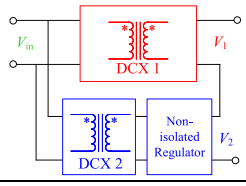
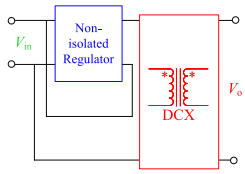
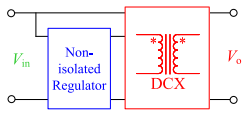


Fig. 1. Typical applications of IBDCs in microgrids.

As a promising candidate for IBDCs, *CLLC* resonant converters have drawn significant attention due to their high efficiency and wide-range soft-switching capability [4]. However, the output voltage regulation of *CLLC* converters typically relies on the pulse frequency modulation (PFM) controllers [5], resulting in several limitations. First, the system efficiency of *CLLC* converters decreases when the switching frequency deviates from the resonant frequency, particularly when the divergence is significant. In such cases, system efficiency rapidly declines due to the loss of soft switching. In addition, *CLLC* converters have a limited output voltage range [6]. Conventionally, a lower ratio between magnetizing inductance and series inductance is acquired to widen the voltage range; however, as the system efficiency and the ratio concomitantly decrease, this method would not be ideal. Furthermore, the inadequate system dynamic response, caused by changes in loop characteristics with the working state, limits the application of *CLLC* in microgrids [7]. Moreover, *CLLC* converters require synchronous rectification (SR) to minimize the conduction losses caused by high voltage drops across body diodes of the switches, especially in high output current conditions; nevertheless, the implementation of SR would inevitably increase system costs and complexity. To address the aforementioned issues and enhance system efficiency while reducing control complexity, it is recommended to operate *CLLC* converters in the dc transformer (DCX) mode [8], [9]. In this mode, the switching frequency matches the resonant frequency, enabling the utilization of an open-loop controller [10]. This approach enables the achievement of high conversion efficiency and simplifies control difficulties by leveraging the inherent soft-switching characteristics of all switches in a wide load range and utilizing the natural SR provided by the system.

TABLE I
PREVIOUSLY PROPOSED PPP-REGULATED ISOLATED DC–DC CONVERTER COMPARISON

Type	Type A (Two isolated converters)		Type B (one isolated converter)	
Topology				
Examples	[11]: FB+FB [12],[13],[14],[15],[16]:*LLC*+DAB [17]:*LLC*+FB/PP	[18]: *LLC*+Boost [19]: *CLLC*+BTI buck	[20]: Boost+SSRC [21]: buck+*LLC*	[22]: Boost+*LLC*
Number of transformers	2	2	1	1
Number of switches	⋆⋆⋆	⋆⋆⋆⋆	⋆⋆	⋆⋆
Direction	Unidirectional or bidirectional	Bidirectional	Unidirectional	Unidirectional

* FB, DAB, PP, BTI-Buck, ACF, and SSRC are short for full bridge, dual-active-bridge, push–pull, bipolar three-phase interleaved buck, active clamp flyback, and secondary-side series resonant converter, respectively.

Nonetheless, in the DCX mode, *CLLC*s' output voltage follows their input voltage. To widen the voltage gain of *CLLC*–DCX, the two-stage configurations, pulsewidth modulation (PWM)-controlled nonisolated regulator and *CLLC*–DCX cascaded structure, are commonly utilized. Nonisolated regulators such as buck [23], boost [24], buck–boost [25], etc., are normally employed due to their voltage regulating ability and simple control, yet the number of utilized switches would increase in the two-stage structure, leading to a reduced system efficiency. To address this issue, switch integration is introduced by integrating switches with similar functions. For instance, in [26] and [27], the boost and buck–boost are merged with a DCX, respectively. Although the number of semiconductor devices is reduced due to the integration, because regulators process all power, the efficiency of the two-stage system is still unsatisfactory.

As a consequence, to enhance system efficiency, the concept of partial power processing (PPP) gains much attention in numerous applications [28], [29], [30], [31], including ESSs [32], [33], photovoltaic systems [34], [35], electrified transportation systems [36], microgrids [37], [38], etc. In a PPP-regulated IBDC, which combines the advantages of regulators and DCXs, the majority of power transfers via a highly efficient DCX, whereas partial power transfers via a bidirectional regulator. Therefore, based on connection configurations and the type of regulators, the existing proposed dc–dc converter with PPP property can be classified into two types: Type A (two isolated converters) and Type B (one isolated converter), as listed in Table I.

Type A has two primary topologies. In [11], two unidirectional full-bridges (FBs) are utilized, where one becomes the master converter and the other the slave converter. Both converters operate in the discontinuous conduction mode (DCM) in this configuration, reducing output filter inductance. However, FBs offer relatively low-efficiency performance, resulting in suboptimal system efficiency. To enhance the system's overall efficiency, the resonant converter should serve as the master, transferring the main power. In [12], a hybrid DAB–DCX converter is proposed, where the main power flows through the DCX, and the DAB is employed for power flow control and output voltage regulation. In [13], to minimize the number of switches, the secondary side transformer outputs are connected to a shared full bridge. In [14], a hybrid control strategy is proposed to realize zero-voltage-switching (ZVS) operation for all switches; however, the system dynamic response is not considered since the PFM is applied to the resonant converter. In [15] and [16], a switching control method and a trajectory-switching-modulation method for this hybrid DAB–DCX are, respectively, proposed to realize fast voltage response. Furthermore, the PPP concept can also be applicable to interleaved resonant converters. In [39], a current-sharing method for the interleaved Type-A converter by adjusting the phase shift between the DCX's bridge and the auxiliary bridge is introduced. Chen et al. [40] demonstrate that effective current sharing between phases can be realized by controlling the duty cycle of the auxiliary converter. Although these novel paralleled type PPP converters in [11], [12], [13], [14], [15], [16], and [17] enhance systems' efficiency, two transformers are necessary to achieve galvanic isolation, thereby increasing the systems' complexity and reducing the power density. Another configuration of Type A involves two identical isolated converters, along with an extra nonisolated regulator for output voltage control. The utilization of the boost in [18] and the bipolar three-phase interleaved (BTI) buck in [19] leads to higher system cost and increased volume.

Contrary to Type-A PPP converters, a Type-B PPP-regulated converter employs a single isolated converter, resulting in a substantial improvement in system power density. In [20], a secondary-side series resonant converter (SSRC) is utilized as the master converter and a boost as the slave converter, which is well-suited for step-up unidirectional isolated power conversion applications. Similarly, a unidirectional postregulated *LLC* converter with a buck employing a center-tapped transformer is introduced in [21]. In [22], a novel structure is proposed by combining a regulator and a DCX in a hybrid manner; however, achieving ZVS for all switches is not satisfied in the full-load

range, which decreases the system efficiency. To reduce power losses in the nonisolated converter, a lower frequency is used in [22], which not only increases the volume of bus capacitance but also decreases power density. Besides, the previously proposed Type-B converters are all unidirectional, restricting their applications in microgrids.

Hence, a hybrid FSBB–*CLLC* converter is proposed to compensate for the drawbacks of the previously proposed converters. The focus of this research is to enhance the overall system efficiency, which is achieved through several efficiency-based approaches, including structure modification, design methodology, and control strategy. The main contributions of this article can be summarized as follows.

1) A PPP-regulated hybrid FSBB–*CLLC* converter with a limited number of power switches is introduced. By utilizing a shared bridge arm, the number of switches utilized in the converter is significantly reduced. Moreover, the converter achieves high efficiency by transferring only partial power via the FSBB.
2) An efficiency-oriented parameter design methodology that ensures ZVS for all switches across a wide load range is proposed. To obtain the overall system loss model, operation modes and expressions are derived. Then, the optimal inductances are calculated considering different load conditions to acquire a higher average system efficiency.
3) To further boost system efficiency, the phase shift of FSBB is precisely controlled. Through an investigation of the relationship among input voltage, output current, and duty cycle, the optimal phase shift of the FSBB is determined. Consequently, a system control strategy based on a three-polynomial fitting model is proposed to achieve real-time tracking of the maximum efficiency.

The rest of this article is organized as follows. Section II presents the system structure and theoretical analysis. Section III introduces the parameter design methodology. Section IV discusses the control strategy for the proposed structure. Section V validates the proposed design and control methods through experiments. Finally, Section VI concludes this article.

II. System Modeling

A. System Configuration

The hybrid FSBB–*CLLC* configuration, as illustrated in Fig. 2, consists of two topologies: an FSBB and a *CLLC* resonant converter. In Fig. 2, the FSBB is composed of four MOSFETs, namely Q_1, Q_2, S_1, and S_2, while the *CLLC* comprises eight MOSFETs S_1∼S_8. In other words, the switches S_1 and S_2 are shared by both the FSBB and the *CLLC*.

The series inductors and capacitors of the primary and secondary sides in the *CLLC*–DCX are denoted by L_{ri} and C_{ri}, respectively, where $i = 1, 2$. The FSBB possesses an inductance denoted as L_b, while L_m denotes as the magnetizing inductance of the *CLLC* transformer, and the turns ratio of the transformer is denoted by n. The input and output voltages are V_{in} and V_o, respectively. i_L signifies the current flowing through L_b, while

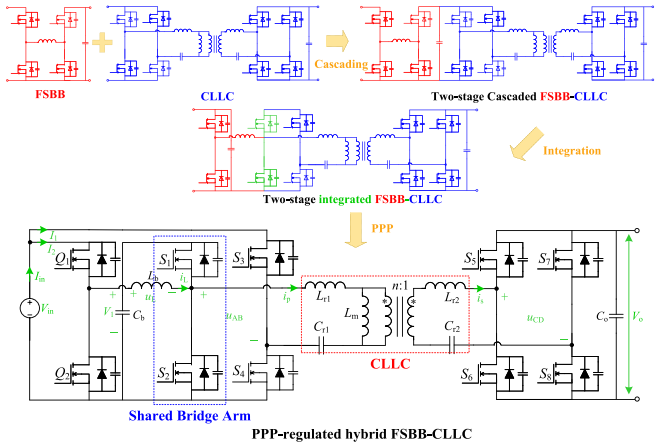


Fig. 2. Derivation process and structure of the proposed system.

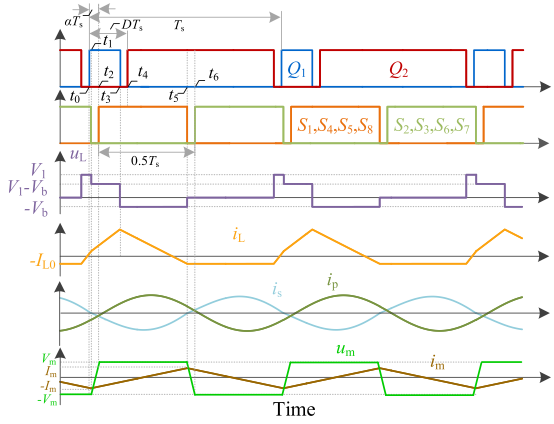


Fig. 3. Operation principles of the proposed system.

i_p and i_s correspond to the primary- and secondary-side currents of the *CLLC*, respectively.

The operation waveforms of the system are displayed in Fig. 3. All switches operate at the frequency f_s. The *CLLC* converter is controlled in an open-loop manner with a resonant frequency of $f_r = f_s$. The output voltage is regulated by adjusting the duty cycle D (as one control freedom) of switch Q_1(and $(1 - D)$ for Q_2), and the detailed analyses of this control strategy are presented in subsequent sections. Therefore, the duty cycles of Q_1 and Q_2 become variable, and the duty cycles of S_1∼S_8 remain constant at 0.5.

There is another control freedom in the system, which is the phase shift α between (Q_1, Q_2) and (S_1∼S_8). This phase shift impacts the current in the inductance L_b, and subsequently, affects the system's performance. A comprehensive analysis of this effect is provided in the following sections.

B. PPP Property

The output voltage of an FSBB can be expressed as

$$V_1 = \frac{D}{1 - D'} V_{in} \tag{1}$$

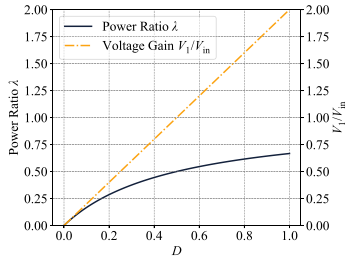


Fig. 4. Power ratio λ and voltage gain V_1/V_{in} with duty cycle D.

where D and D' are the duty cycles of the left and right arm in an FSBB, respectively, and V_1 is the output voltage of an FSBB. Since the right arm in the proposed structure is shared with the *CLLC* converter, this results in a fixed duty cycle D' of 0.5 and allows deriving the voltage gain as

$$V_1 = 2DV_{\text{in}}. \tag{2}$$

In this hybrid structure, main power should transfer via *CLLC*, while partial power should transfer via the combination of FSBB and *CLLC* (FSBB+*CLLC*). The power ratio λ is defined as the ratio between the partial power P_{FSBB} and the total system transferred power. Considering the hybrid integrated implementation and assuming no power losses in the system, the power ratio can be given as

$$\lambda = \frac{P_{\text{FSBB}}}{P_{\text{in(o)}}} = \frac{V_{\text{in}}I_1}{V_{\text{in}}I_{\text{in}}} = \frac{I_1}{I_1 + I_2} \tag{3}$$

where $P_{\text{in(o)}}$ are the input and output power of the system, and I_1 and I_2 are the input currents of FSBB+*CLLC* and *CLLC*, respectively.

Based on the power conservation law, the following equation is satisfied.

$$V_{\text{in}}I_1 = V_1I_2. \tag{4}$$

Thus, substituting (2) and (4) into (3), the power ratio can be rewritten as

$$\lambda = \frac{1}{1 + V_{\text{in}}/V_1} = \frac{2D}{2D + 1}. \tag{5}$$

Therefore, Fig. 4 can be depicted according to (2) and (5), which illustrated the relationship among duty cycle, the voltage gain of the FSBB, and power ratio. The power ratio λ increases as the duty cycle D increases, indicating the FSBB processes much power with an increased duty cycle, yet the increased power ratio leads to a decrease in the overall efficiency. When $D = 1$ is ideally applied to the FSBB, $\lambda = 2/3$ is obtained, causing the PPP converter's function to mimic a two-stage converter, reducing the overall system efficiency. Moreover, the FSBB operates in the step-down mode when $D < 0.5$ and in the step-up mode when $D > 0.5$. Consequently, the system efficiency of the hybrid FSBB–*CLLC* converter is higher when the FSBB operates in step-down mode than in step-up mode.

C. Operation Principles

The operation principles and key waveforms of the hybrid FSBB–*CLLC* system are illustrated in Fig. 3. To further analyze the system's operation characteristics, the detailed equivalent circuits in one switching period are described, as shown in Fig. 5.

1) Mode 1 (Before t_0): During a dead-time zone, both Q_1 and Q_2 are switched OFF. In this subinterval, the current i_{L} is negative, discharging Q_1's junction capacitance while charging Q_2's junction capacitance. Consequently, the voltage across Q_2's capacitance reaches the input voltage V_{in}, achieving ZVS in Q_1. Throughout this mode, the switches S_2, S_3, S_6, and S_7 remain in the ON-state.

2) Mode 2 ($[t_0, t_1)$): At time t_0, Q_1 achieves ZVS-ON. Since the input voltage is applied to the inductance L_{b}, the current i_{L} can be described by

$$i_{\text{L}}(t) = -I_{\text{L0}} + \frac{V_{\text{in}}}{L_{\text{b}}}(t - t_0). \tag{6}$$

3) Mode 3 ($[t_1, t_2)$): In this mode, the switches S_2, S_3, S_6, and S_7 turn OFF. The positive current i_{L} and the negative current i_{p} discharge the capacitance of S_1 while charging the capacitance of S_2. Once the voltage across the capacitance of S_2 reaches the output voltage of FSBB V_1, the ZVS conditions for S_1 are satisfied. Besides, the energy stored in the magnetizing inductance L_{m} charges or discharges the capacitances of the switches S_3, S_6, and S_7. If this process is completed before t_2, ZVS can be achieved for the switches S_4, S_5, and S_8.

4) Mode 4 ($[t_2, t_3)$): At time t_2, S_1, S_4, S_5, and S_8 realize ZVS-ON, while Q_1 remains in the ON-state. The current i_{L} can be expressed as

$$i_{\text{L}}(t) = i_{\text{L}}(t_2) + \frac{V_{\text{in}} - V_1}{L_{\text{b}}}(t - t_2). \tag{7}$$

5) Mode 5 ($[t_3, t_4)$): At time t_3, Q_1 turns OFF. During this subinterval, the current i_{L} becomes positive, charging Q_1's junction capacitance while discharging Q_2's junction capacitance. Subsequently, the voltage across Q_2's capacitance decreases to zero, achieving ZVS in Q_2. In this mode, the switches S_1, S_4, S_5, and S_8 remain in the ON-state.

6) Mode 6($[t_4, t_5)$): At time t_4, Q_2 enters the ZVS-ON state, with S_1 remaining ON. The current i_{L} can be derived as

$$i_{\text{L}}(t) = i_{\text{L}}(t_4) + \frac{-V_1}{L_{\text{b}}}(t - t_4). \tag{8}$$

7) Mode 7 ($[t_5, t_6)$): In this mode, the switches S_1, S_4, S_5, and S_8 turn OFF. The negative current i_{L} and positive current i_{p} charge the capacitance of S_1 while discharging the capacitance of S_2. When the voltage across S_2's capacitance drops to zero, the ZVS conditions for S_2 are met. Simultaneously, the energy stored in the magnetizing inductance L_{m} charges or discharges the capacitances of the switches S_4, S_5, and S_8. If this process is completed before t_6, ZVS can be achieved for the switches S_3, S_6, and S_7.

8) Mode 8 (After t_6): At time t_6, S_2, S_3, S_6, and S_7 achieve ZVS-ON, whereas Q_2 remains ON. The current i_{L} is expressed

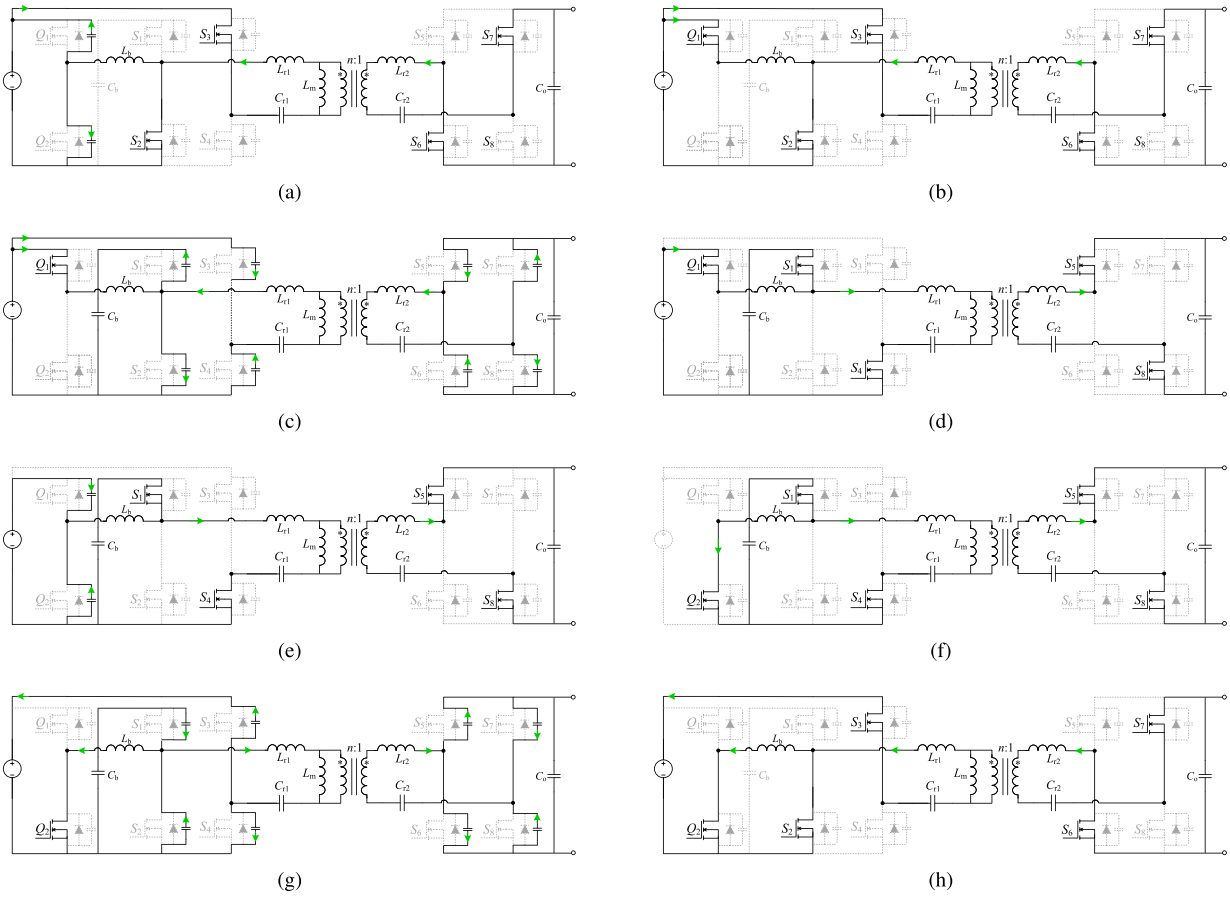


Fig. 5. Detailed waveforms. (a) Before t_0. (b) $[t_0, t_1)$. (c) $[t_1, t_2)$. (d) $[t_2, t_3)$. (e) $[t_3, t_4)$. (f) $[t_4, t_5)$. (g) $[t_5, t_6)$. (h) After t_6.

as

$$i_{\mathrm{L}}(t) = -I_{\mathrm{L0}}. \tag{9}$$

D. Quantitative Analysis

According to the analyses in the previous section, the time intervals can be simplified as $t_0 = 0$, $t_2 = \alpha T_{\mathrm{s}}$, $t_4 = DT_{\mathrm{s}}$, and $t_6 = 0.5T_{\mathrm{s}} + \alpha T_{\mathrm{s}}$.

Therefore, the inductance current $i_{\mathrm{L}}(t)$ can be rewritten as

$$i_{\mathrm{L}} = \begin{cases} -I_{\mathrm{L0}} + \frac{V_{\mathrm{in}}}{L_{\mathrm{b}}} t & (0, \alpha T_{\mathrm{s}}) \\ i_{\mathrm{L}}(\alpha T_{\mathrm{s}}) + \frac{V_{\mathrm{in}} - V_1}{L_{\mathrm{b}}}(t - \alpha T_{\mathrm{s}}) & (\alpha T_{\mathrm{s}}, DT_{\mathrm{s}}) \\ i_{\mathrm{L}}(DT_{\mathrm{s}}) + \frac{-V_1}{L_{\mathrm{b}}}(t - DT_{\mathrm{s}}) & (DT_{\mathrm{s}}, (0.5+\alpha)T_{\mathrm{s}}) \\ -I_{\mathrm{L0}} & ((0.5+\alpha)T_{\mathrm{s}}, T_{\mathrm{s}}) \end{cases}. \tag{10}$$

Relying on the current continuity in adjacent time intervals, the currents at αT_{s} and DT_{s} can be derived as

$$\begin{cases} i_{\mathrm{L}}(\alpha T_{\mathrm{s}}) = -I_{\mathrm{L0}} + \frac{V_{\mathrm{in}}}{L_{\mathrm{b}}} \alpha T_{\mathrm{s}} \\ i_{\mathrm{L}}(DT_{\mathrm{s}}) = -I_{\mathrm{L0}} + \frac{V_{\mathrm{in}}}{L_{\mathrm{b}}} DT_{\mathrm{s}} - \frac{V_1}{L_{\mathrm{b}}}((D-\alpha)T_{\mathrm{s}}). \end{cases} \tag{11}$$

Hence, to determine I_{L0} in (10), the input power equation of FSBB is established, which can be expressed as

$$P_{\mathrm{FSBB}} = V_{\mathrm{in}} I_1 = V_{\mathrm{in}} \frac{\int_0^{T_{\mathrm{s}}} i_{\mathrm{L}} dt}{T_{\mathrm{s}}}. \tag{12}$$

Substituting (5), (10), and (11) into (12), the undetermined I_{L0} can be derived as

$$I_{\mathrm{L0}} = \frac{DT_{\mathrm{s}} V_{\mathrm{in}} \Phi - 2L_{\mathrm{b}} P_{\mathrm{o}} \lambda - \alpha^2 T_{\mathrm{s}} V_1 V_{\mathrm{in}}}{2DL_{\mathrm{b}} V_{\mathrm{in}}} \tag{13}$$

where $\Phi = D(V_{\mathrm{in}} - V_1) + 2\alpha V_1$.

Based on the volt-second balance of the magnetizing inductance L_{m}, the voltage across the inductance in the positive period can be expressed as

$$V_{\mathrm{m}} = \frac{V_{\mathrm{in}} + V_1}{2}. \tag{14}$$

Therefore, the voltage that crosses the inductance L_{m} is given by

$$u_{\mathrm{m}} = \pm V_{\mathrm{m}}. \tag{15}$$

Since the operation frequency of a *CLLC* is the same as its resonant frequency, the unity gain of a *CLLC* converter can be acquired, which means that the output voltage is V_{m}/n. By substituting (2) and (14), the voltage gain in forward mode can be derived as

$$G_{\mathrm{f}} = \frac{V_{\mathrm{o}}}{V_{\mathrm{in}}} = \frac{nV_{\mathrm{m}}}{V_{\mathrm{in}}} = \frac{2D+1}{2n}. \tag{16}$$

TABLE II
VOLTAGE STRESSES OF THE SWITCHES

Switch	Voltage stress
Q_1,Q_2,S_3,S_4	$V_{\rm in}$
S_1,S_2	$2DV_{\rm in}$
S_5,S_6,S_7,S_8	$(2D+1)/(2n)V_{\rm in}$

Similarly, the voltage gain in the backward mode is given as

$$G_{\rm b} = \frac{2n}{2D+1}. \tag{17}$$

The current in the magnetizing inductance $L_{\rm m}$ [9] can be calculated as

$$i_{\rm m}(t) = -I_{\rm m} + \frac{V_{\rm m}}{L_{\rm m}}t \tag{18}$$

where $I_{\rm m} = V_{\rm m}T_{\rm s}/(4L_{\rm m})$.

Therefore, the currents in the primary and secondary sides of the transformer can be expressed as follows [4]:

$$\begin{cases} i_{\rm p}(t) = \frac{\pi}{2}\frac{P_{\rm o}}{V_{\rm o}}\sin(2\pi f_{\rm s}t) + i_{\rm m}(t) \\ i_{\rm s}(t) = \frac{n\pi}{2}\frac{P_{\rm o}}{V_{\rm o}}\sin(2\pi f_{\rm s}t). \end{cases} \tag{19}$$

Besides, the voltage stress on the switches can also be determined based on its operation principles, as shown in Table II.

III. EFFICIENCY-ORIENTED PARAMETERS DESIGN

In the previous section, the currents and voltages in this hybrid PPP converter are computed, which provides valuable guidance for its design process. By considering the voltage and current limitations, appropriate power semiconductor devices can be selected. However, there are additional parameters that require careful design: the inductance $L_{\rm b}$ in FSBB and the resonant parameters in the resonant tank of the *CLLC* topology.

A. Output Power Requirements

The inductance $L_{\rm b}$ is a critical power link in FSBB, significantly influencing the maximum output power of the hybrid FSBB–*CLLC* system. Therefore, the boundary inductance $L_{\rm b}$ should allow the maximum output power of FSBB to be greater than the required power. According to (5), (12), and (13), to fulfill the basic output power requirement, the inductance $L_{\rm b}$ should satisfy

$$L_{\rm b} \le \frac{D\left(-2\alpha^2 - D^2 + (2\alpha+0.5)D\right)V_{\rm in}^2 T_{\rm s}}{2(1-D)\lambda P_{\rm o}}. \tag{20}$$

B. ZVS Conditions

ZVS is highly desirable as it helps minimize switching losses and enhances the overall efficiency of the hybrid converter. Designing for ZVS involves selecting appropriate values for the inductance $L_{\rm b}$ in the FSBB and the inductance $L_{\rm m}$ in the *CLLC* resonant tank. Therefore, these parameters must be chosen diligently to ensure ZVS conditions are met under various operating conditions and load variations.

Based on the previous analyses, achieving ZVS for S_1 and S_2 is relatively easier than for Q_1 and Q_2. This is due to the combined effect of the current $i_{\rm L}$ flowing through both FSBB and the resonant current $i_{\rm p}$, which provides the necessary charging current for ZVS of S_1, allowing the voltage across its junction capacitance to charge to V_1. Similarly, these currents provide the requirements for ZVS of S_2, allowing the voltage to discharge to 0. The ZVS realization for S_1 and S_2 benefits from a strong charging/discharging current, ensuring an adequate energy supply for ZVS. Therefore, once ZVS is achieved for Q_1 and Q_2, ZVS for S_1 and S_2 can also be achieved.

For Q_1 and Q_2, the ZVS condition is satisfied when the energy stored in $L_{\rm m}$ is greater than the energy stored in $C_{\rm oss}$. This condition can be expressed as

$$\frac{1}{2}L_{\rm b}i_{\rm L}^2(0) \ge \frac{1}{2}C_{\rm oss}V_{\rm in}^2. \tag{21}$$

By substituting (10) and (13) into (21), the constraint for $L_{\rm b}$ is derived as

$$L_{\rm b} \le \frac{\sqrt{C_{\rm oss}V_{\rm in}^2\left(C_{\rm oss}V_{\rm in}^2 + 2\Psi\right)} + C_{\rm oss}V_{\rm in}^2 + \Psi}{2I_{\rm o}^2} \tag{22}$$

where $\Psi = (-2\alpha^2 - 2D^2 + 4\alpha D + D)I_{\rm o}T_{\rm s}V_{\rm in}$.

To achieve ZVS for the switches in the *CLLC* topology, the magnetizing inductance $L_{\rm m}$ should satisfy [9]

$$L_{\rm m} < \frac{(1-2f_{\rm s}t_d)t_d}{8\left(C_{\rm oss} + C_{\rm oss}/n^2\right)f_{\rm s}} \tag{23}$$

where t_d is the deadtime and $C_{\rm oss}$ is the junction capacitance.

By properly selecting the values of $L_{\rm b}$ and $L_{\rm m}$, the hybrid converter can achieve ZVS for the switches, leading to a significant reduction in switching losses. Consequently, $L_{\rm b}$ should simultaneously satisfy (5) and (23) to realize output power and ZVS requirements.

C. System Efficiency

$L_{\rm b}$ and $L_{\rm m}$ play a crucial role in determining the proposed converter's current characteristics. By altering the values of these parameters, system efficiency will also vary accordingly. Consequently, to achieve the highest average efficiency, it is essential to carefully design the passive device parameters. To obtain the highest average efficiency, the system loss model is established first, which can be divided into several parts

$$P_{\rm loss} = P_{\rm co} + P_{\rm sw} + P_{\rm T} + P_{\rm RC} \tag{24}$$

where $P_{\rm co}$ is the conduction losses, $P_{\rm sw}$ is the switching losses, $P_{\rm T}$ is the inductances and transformer losses, and $P_{\rm RC}$ is the resonant capacitance losses.

First, the conduction loss of all switches can be expressed as

$$\begin{cases} P_{\rm co(Q1,Q2)} = I_{\rm Q}^2 R_{\rm ds(on)} \\ P_{\rm co(S1,S2)} = I_{\rm S}^2 R_{\rm ds(on)} \\ P_{\rm co(S3,S4)} = I_{\rm p}^2 R_{\rm ds(on)} \\ P_{\rm co(S5,S6,S7,S8)} = 2I_{\rm s}^2 R_{\rm ds(on)} \end{cases} \tag{25}$$

where $R_{\mathrm{ds(on)}}$ is the ON-resistor of an MOSFET, which can be found in MOSFET's datasheet, and

$$\begin{cases} I_{\mathrm{Q}} = \sqrt{\frac{1}{T_{\mathrm{s}}}\int_0^{T_{\mathrm{s}}} i_{\mathrm{L}}^2 dt}, I_{\mathrm{S}} = \sqrt{\frac{1}{T_{\mathrm{s}}}\int_0^{T_{\mathrm{s}}} (i_{\mathrm{p}} - i_{\mathrm{L}})^2 dt} \\ I_{\mathrm{p}} = \sqrt{\frac{1}{T_{\mathrm{s}}}\int_0^{T_{\mathrm{s}}} i_{\mathrm{p}}^2 dt}, I_{\mathrm{s}} = \sqrt{\frac{1}{T_{\mathrm{s}}}\int_0^{T_{\mathrm{s}}} i_{\mathrm{s}}^2 dt}. \end{cases} \tag{26}$$

Since all the switches in the hybrid converter can achieve ZVS, switching losses mainly arise from the energy dissipated during the switching transitions when switches turn OFF, which can be calculated as

$$P_{\mathrm{sw}} = \frac{V_{\mathrm{GS}}}{V_{\mathrm{DS,ref}}} E_{\mathrm{off}} f_{\mathrm{s}} \tag{27}$$

where $V_{\mathrm{DS,ref}}$ is the reference drain–source voltage, and E_{off} is the turn-OFF energy per switching cycle of an MOSFET. The gate–source voltage V_{GS} of the switches are listed in Table II.

The total loss P_{T} in the inductors and the transformer of the proposed structure can be divided into two parts: copper loss P_{cu} and core loss P_{core}. The copper loss P_{cu} can be calculated as

$$P_{\mathrm{cu}} = I_{\mathrm{Q}}^2 R_{\mathrm{r,avg1}} + I_{\mathrm{p}}^2 R_{\mathrm{r,avg2}} \tag{28}$$

where $R_{\mathrm{r,avg1}}$ and $R_{\mathrm{r,avg2}}$ are the equivalent ac resistance of the inductance and the transformer, respectively.

The core loss P_{core}, using the Steinmetz equation, can be computed as

$$P_{\mathrm{core}} = P_{\mathrm{v}} V_{\mathrm{e}} \tag{29}$$

where P_{v} is the relative core losses, and V_{e} is the effective magnetic volume.

The capacitance loss can be represented as the sum of losses in the two resonant capacitors

$$P_{\mathrm{RC}} = \left(\frac{I_{\mathrm{p}}^2}{2\pi C_{\mathrm{r1}}} + \frac{I_{\mathrm{s}}^2}{2\pi C_{\mathrm{r2}}} \right) T_{\mathrm{s}} \tan\delta \tag{30}$$

where the dissipation factor $\tan\delta$ can be obtained from the capacitor datasheet.

Therefore, the system's efficiency can be calculated as

$$\eta = \frac{P_{\mathrm{o}}}{P_{\mathrm{o}} + P_{\mathrm{loss}}}. \tag{31}$$

Subsequently, the optimal inductances, L_{bo} and L_{mo}, that realize a higher system efficiency can be acquired through the derivation of (31), which can be expressed as

$$\begin{cases} \frac{\partial \eta}{\partial L_{\mathrm{b}}} = 0 \Rightarrow L_{\mathrm{bo}} \\ \frac{\partial \eta}{\partial L_{\mathrm{m}}} = 0 \Rightarrow L_{\mathrm{mo}}. \end{cases} \tag{32}$$

However, obtaining the general expressions of L_{bo} and L_{mo} are challenging due to the complexity of (32). To analyze the system efficiency with respect to the inductance L_{b} and L_{m} considering different load conditions, the system efficiency needs to be plotted as a function of L_{b} and L_{m}, as shown in Fig. 6.

From the analysis presented in Fig. 6(a), it can be observed that the optimal inductance L_{bo} as loads get lighter. Specifically, for full load, L_{bo} should be lower than 30 μH, whereas for light loads, L_{bo} reaches 80 μH. To maximize the average system efficiency and ensure output power and ZVS requirements,

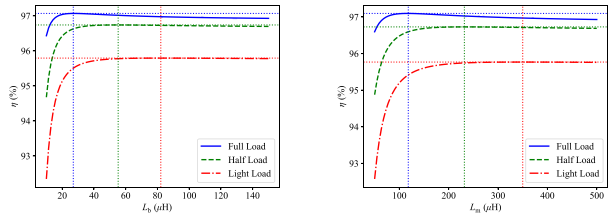


Fig. 6. System efficiency versus inductances. (a) L_{b}. (b) L_{m}.

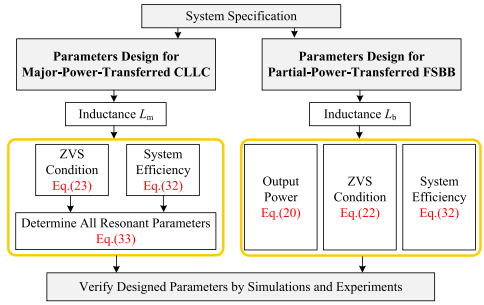


Fig. 7. Principles of choosing the parameters L_{b} and L_{m}.

the inductance L_{b} is selected as 40 μH. Similarly, the optimal inductance L_{mo} also increases with decreasing loads, as depicted in Fig. 6(b). Therefore, to achieve a higher efficiency and ZVS, the value of L_{m} is set to 200 μH. Since the *CLLC* operates in a resonant state, other resonant parameters should satisfy

$$\begin{cases} L_{\mathrm{r1}} = n^2 L_{\mathrm{r2}} \\ C_{\mathrm{r1}} = \frac{C_{\mathrm{r2}}}{n^2} = \frac{1}{4\pi^2 f_{\mathrm{s}}^2 L_{\mathrm{r1}}}. \end{cases} \tag{33}$$

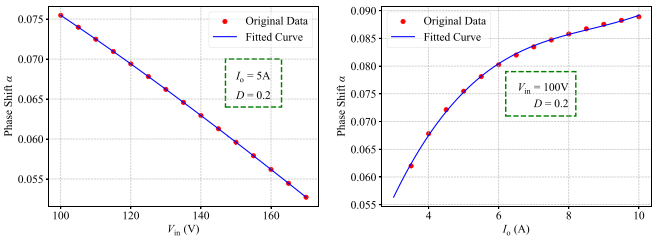
Ultimately, the overall process of choosing the most appropriate inductances is illustrated and summarized in Fig. 7.

IV. Controller Design

According to the previous analysis, it is evident that the output voltage is related to the duty cycle D and is not affected by the phase shift α. However, the phase shift does have an impact on the current in the converter, which can lead to fluctuation in system efficiency. Therefore, to achieve the highest efficiency in the system, it is necessary to find the optimal phase shift α_{o}. Thus, by taking the derivative of η with respect to α and setting it to zero, the optimal phase shift α_{o} that minimizes power loss can be determined. Then, the optimal phase shift α_{o} can be calculated as

$$\frac{\partial \eta}{\partial \alpha} = 0 \Rightarrow \alpha_{\mathrm{o}} = f(V_{\mathrm{in}}, I_{\mathrm{o}}, D). \tag{34}$$

However, obtaining the symbolic solution of α_{o} using professional mathematical software is challenging due to the presence of nonlinear trigonometric terms. Furthermore, implementing such a solution in a real-time controller with limited computational capabilities can be even more difficult. Therefore, to address this issue, by utilizing numerical optimization algorithms,



(a) (b)

Fig. 8. Two-dimensional fitted curve of the phase shift. (a) Phase shift versus input voltage. (b) Phase shift versus output current.

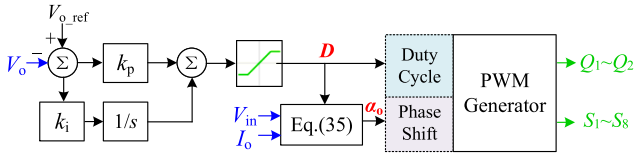


Fig. 9. Proposed system controller.

a fitting tool is employed to find the α_o that results in the lowest power loss. The basic steps are as follows:

1) *Collect the data:* Calculate α_o using professional mathematical software, such as MATLAB, Mathematica, etc.
2) *Set up the equation:* In this article, considering the fitting performance and calculation difficulty, a three-order polynomial fitting equation is used, shown as follows:

$$\begin{aligned}\alpha_o \approx\ & p_{000} + p_{100}V_{in} + p_{010}I_o + p_{001}D \\ & + p_{200}V_{in}^2 + p_{110}V_{in}I_o + p_{101}V_{in}D + p_{020}I_o^2 \\ & + p_{011}I_oD + p_{002}D^2 + p_{300}V_{in}^3 + p_{210}V_{in}^2I_o \\ & + p_{201}V_{in}^2D + p_{120}V_{in}I_o^2 + p_{111}V_{in}I_oD \\ & + p_{102}V_{in}D^2 + p_{030}I_o^3 + p_{021}I_o^2D + p_{012}I_oD^2 \\ & + p_{003}D^3 \end{aligned} \tag{35}$$

where $p_{xyz}(x, y, z = 0, 1, 2, 3)$ are coefficients of the three-order polynomial.

3) *Perform the curve fitting:* Use a curve fitting algorithm to fit α_o using mathematical software and find the optimal values for the coefficients.
4) *Evaluate the fitted results:* Fig. 8 shows the original data and fitted curve, in which the original data points are located on or close to the fitted curve, confirming the accuracy of the fitting model.

By employing this fitting approach, the need for a symbolic solution is circumvented, and instead, a numerical approximation is used. This numerical approximation can be easily implemented in microcontroller units, with minimized computational burdens, enabling practical real-time controls.

By combining the real-time calculated α_o, a fitting-model-based maximum efficiency tracking control strategy is proposed, as depicted in Fig. 9. Two control freedoms, namely the duty cycle D and the phase shift α, are utilized to control the system.

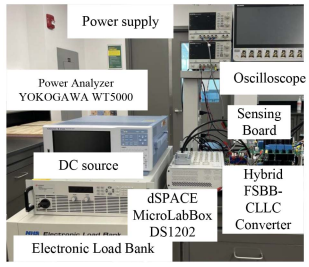
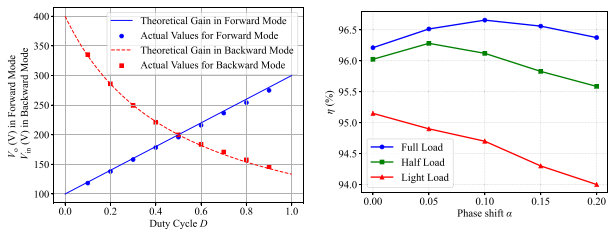


Fig. 10. Experimental setup.

TABLE III
SYSTEM SPECIFICATIONS

Parameters	Symbols	Designed values
Input voltage	V_{in}	$120-250$ V
Rated output voltage	V_o	150 V
Transformer turns ratio	n	1:1
Magnetizing inductance	L_m	200 μH
FSBB inductance	L_b	40 μH
CLLC series inductances	L_{r1}, L_{r2}	15 μH, 15 μH
CLLC series capacitances	C_{r1}, C_{r2}	168.9 nF, 168.9 nF
Capacitances	C_{in}, C_b, C_o	270 μF
Switching frequency	f_s	100 kHz



(a) (b)

Fig. 11. Tested curves. (a) Voltage gain versus duty cycle D. (b) Efficiency with different phase shifts and loads.

The output voltage is regulated using a proportional-integral (PI) controller. Simultaneously, the optimal phase shift α_o is calculated based on the real-time values of D, input voltage, and output current. The phase shift α is then adjusted accordingly. Overall, this control strategy optimizes the system's efficiency by dynamically adjusting both the duty cycle and phase shift to track the maximum efficiency.

V. EXPERIMENT AND DISCUSSION

A. Experimental Setup and Results

To verify the proposed hybrid system, a 1-kW hybrid PPP-regulated FSBB–*CLLC* converter is established, as shown in Fig. 10. The detailed system parameters are listed in Table III. The dSPACE MicroLabBox DS1202 is used to control the hybrid FSBB–*CLLC* converter. In this prototype, SiC MOSFETs C3M0065100 K (Cree) are utilized as the main switches, which are driven by gate driver UCC5350 (TI).

First of all, the voltage gain characteristics of the proposed structure are measured and compared to the theoretical results at an input or output voltage of 200 V, as shown in Fig. 11(a).

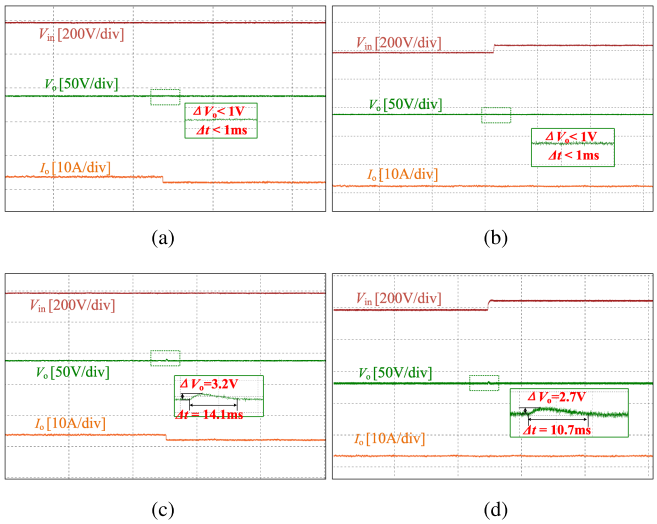


Fig. 12. System dynamic responses of the proposed structure compared to a single *CLLC* converter. (a) Load transitions from 800 to 500 W in the FSBB–*CLLC* converter. (b) Input voltage variations from 200 to 250 V in the FSBB–*CLLC* converter. (c) Load transitions from 800 to 500 W in the *CLLC* converter. (d) Input voltage variations from 200 to 250 V in the *CLLC* converter.

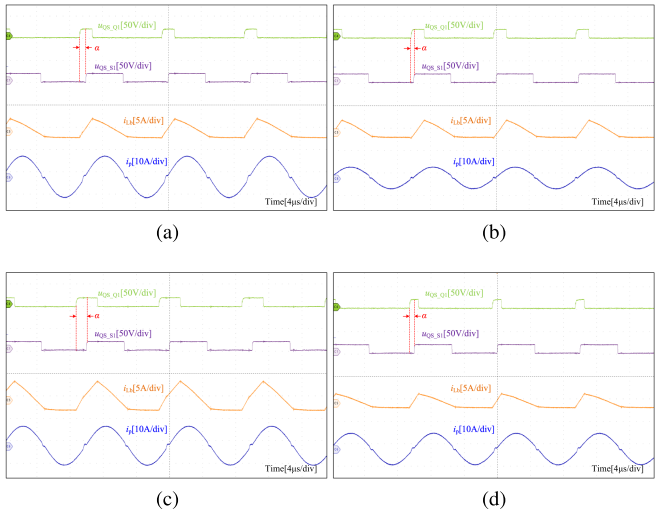


Fig. 13. Detailed waveforms when the FSBB–*CLLC* operates in step-down mode. (a) Output power is 1 kW. (b) Output power is 500 W. (c) Input voltage is 200 V. (d) Input voltage is 250 V.

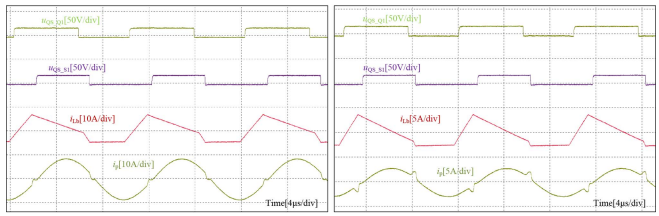


Fig. 14. Detailed waveforms when the FSBB–*CLLC* operates in step-up mode. (a) Output power is 700 W. (b) Output power is 200 W.

The practical voltage gain results match the theoretical results well, verifying the gain analysis of the hybrid converter. Then, the relationship between system efficiency and the phase shift α, under different loads, is evaluated, and the experimental results are depicted in Fig. 11(b). It shows that the highest efficiency is obtained in different phase shifts with different loads. At full loading, the optimal phase shift α_o is between 0.05 and 0.15; at half loading, α_o is between 0 and 0.1; and at light loading, α_o is between 0 and 0.05. Besides, the system's efficiency decreases as a load becomes lighter. These results show great consistency with the previous analyses, proving the system efficiency can be enhanced by adjusting the phase shift α.

Subsequently, the proposed system control strategy is validated by comparing to the PFM-controlled single *CLLC* converter, which is shown in Fig. 12. In Fig. 12(a) and (c), the system dynamic responses of the hybrid FSBB–*CLLC* converter and the single *CLLC* converter are presented, respectively, when the load steps from 800 to 500 W. Fig. 12(a) shows that the overshoot and settling time is limited when load steps, illustrating that the output voltage of the hybrid converter can be simply and accurately regulated by a PI controller. Contrary to the PWM-controller converter, the dynamic response of the PFM-controlled *CLLC* converter is unsatisfactory. The output voltage overshoot increases to 3.2 V, and the settling time extends to 14.1 ms. Similarly, the dynamic response when the input voltage jumps from to 250 V is also tested, as shown in Fig. 12(b) and (d). The transient response results of the proposed structure illustrate that the overshoot and settling time are limited; however, a notable increase in voltage overshoot (2.7 V) and settling time (10.7 ms) is observed in the single *CLLC*. Therefore, by employing the proposed converter, fast dynamic response performance can be achieved, which is beneficial to microgrids.

The detailed waveforms when loads are 1 kW or 1000 W, not 1 W and input voltages are 200 and 250 V are recorded in Fig. 13. It shows that the phase shift α changes with load and input voltage conditions. When the load changes, the phase shift alters according to system operation conditions. Besides, Fig. 13 indicates that the phase shift in the heavier load (1 kW) is larger than that in the lighter load. Similarly, when the input voltage increases, the phase shift and duty cycles change accordingly. Fig. 14 reveals similar results as Fig. 13 under the condition when the proposed hybrid converter operates in the step-up mode. And Fig. 15 shows that all the switches can realize ZVS-ON with appropriately designed system parameters.

In addition, the bidirectional mode transition waveforms are recorded in Fig. 16. The mode transition waveforms for this hybrid FSBB–*CLLC* converter are examined under specific conditions: $V_{in} = 200V$ and $V_o = 150V$. In this scenario, the converter functions in step-down mode when power flows from the primary- to the secondary side, and in step-up mode when the flow direction reverses from the secondary- to the primary-side. Observations indicate that the converter, utilizing a fixed-frequency PWM-controlled FSBB and open-loop controlled *CLLC*–DCX, manages to achieve automatic and smooth transitions between modes. In this process, the duty cycle D is accurately adjusted to track the reference voltage,

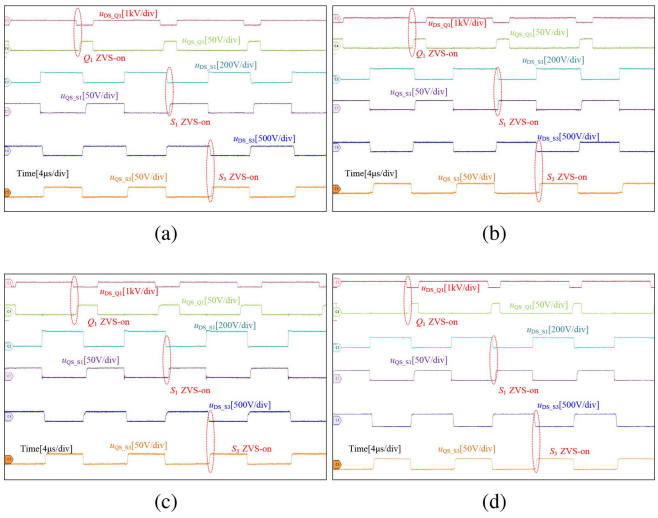


Fig. 15. ZVS conditions. (a) Output power is 1kW. (b) Output power is 500 W. (c) Input voltage is 200 V. (d) Input voltage is 250 V.

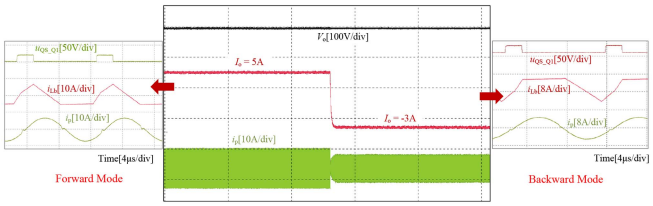


Fig. 16. Bidirectional modes transition.

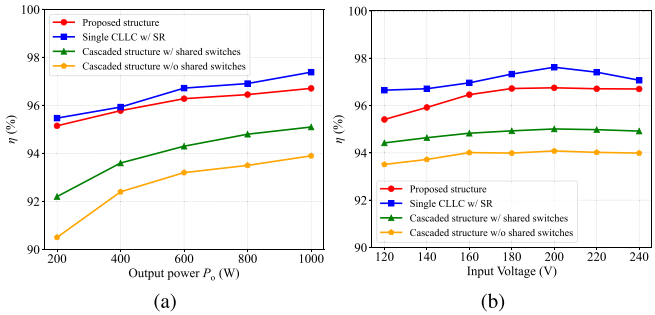


Fig. 17. Efficiency comparisons. (a) With different output power. (b) With different input voltage.

and negligible voltage/current overshoot is observed, verifying that the proposed structure possesses rapid mode transition capability.

Finally, the system efficiency comparison results among the proposed hybrid converter, a single *CLLC*, and cascaded FSBB–*CLLC* converters with/without shared switches are depicted in Fig. 17. The results in Fig. 17(a) illustrate that the peak efficiency of the proposed hybrid structure is 96.7%, and the overall system efficiency is larger than 95% in lighter load. In Fig. 17(b), it can be seen that the system efficiency of the proposed structure is relatively lower when $V_{\text{in}} < 150$ V. This is due to the FSBB–*CLLC* converter operating in the step-up mode, where much power is transferred via the FSBB. The cascaded converters obtain a relatively lower efficiency because of the two-stage structure. And the PFM-controlled single *CLLC* employing the SR technique, which utilizes the fewest power switches, achieves higher efficiency. Moreover, the peak efficiency of the proposed hybrid converter is lower than the single *CLLC* converter when it operates in the DCX mode. This is intuitive since partial power is transferred via the FSBB, leading to extra losses. Besides, the power density of the hybrid FSBB–*CLLC* would also decline because of the extra power devices and passive components.

The peak efficiency of the hybrid FSBB–*CLLC* converter can be improved by designing smaller inductances L_{b} and L_{m}, as illustrated in Fig. 6. The chosen parameters in this article aim to optimize the overall average efficiency across various loads. In essence, selecting smaller inductances maximizes peak efficiency, while opting for larger inductances prioritizes higher average efficiency. Moreover, to enhance the efficiency of the *CLLC*–DCX, Cao and Dong [41] introduce a trapezoidal current modulation method, which effectively reduces the root-mean-square current in the resonant tank, resulting in decreased total conduction loss. Incorporating this method into the proposed hybrid FSBB–*CLLC* converter can further enhance the system's overall efficiency.

B. Benefits of the Proposed PPP FSBB–CLLC Converter Compared to the Single CLLC Converter

The novel hybrid PPP FSBB–*CLLC* configuration brings several benefits to the system, as illustrated as follows.

1) *Fast dynamic response performance:* Based on Fig. 12, the proposed FSBB–*CLLC* converter demonstrates faster voltage tracking ability compared to a single *CLLC* converter. This is because the frequency characteristics of a single *CLLC* alter across the operating point, and the PFM controller has to trade low bandwidth for loop stability over a wide range of operations, making it challenging for a single *CLLC* to achieve fast dynamic performance. Moreover, while control strategies for the resonant converters are limited and complex, advanced control methods for the PWM converters have been developed over the decades. Implementing these methods can further enhance the dynamic performance of the proposed structure, making it suitable for utilization in microgrids.
2) *Reduced system control complexity:* In a PFM-controlled single *CLLC* converter, to reduce the power loss due to the high voltage drop of the SiC MOSFET body diode, it is necessary to implement SR on the rectifier-side MOSFETs. To address the issue, voltage/current sensing-based SR methods were proposed to improve the system efficiency; nevertheless, extra high-bandwidth sensors and conditioning circuits are always required, leading to increased control complexity and cost in high-frequency applications. For the proposed hybrid converter, however, the *CLLC*–DCX can realize natural SR, and only the dc voltage and current are sensed in the control loop, which significantly decreases the control complexity compared to a single *CLLC* converter.

3) *Smooth modes transit capability:* According to Fig. 16, the proposed hybrid converter is capable of smoothly transitioning between bidirectional modes. However, for a single *CLLC* converter, due to the presence of SR, mode switching typically involves initially shutting down in one direction, and then, starting up in the other direction, making an automatic and smooth mode transition challenging.
4) *Simplified modularization ability:* The Input-series-output-parallel (ISOP)-connected converter system, where multiple converter modules are in series at the input and in parallel at the output, proves beneficial for high-input voltage applications due to reduced voltage stress on power switches. Employing a single *CLLC* as the modular, the parameters mismatch of resonant tanks in practice will lead to inconsistent power-sharing and necessitate complicated control methods. In [42], it was verified that due to the unity voltage gain of DCX, despite parameter variations and the ease of ensuring identical nonisolated converters, the ISOP converter system can realize effective power sharing even with unmatched parameters. Similar to this two-stage converter, the proposed hybrid converter also fulfills these criteria, allowing it to simplify control requirements.

VI. Conclusion

In conclusion, this article presents a hybrid FSBB–*CLLC* converter that combines the high efficiency of a *CLLC* with the flexibility of an FSBB. The FSBB effectively regulates the system's output voltage by adjusting duty cycles and handling a small portion of the total power, resulting in a fast dynamic response. Simultaneously, the *CLLC* operates in a complete resonant state, ensuring high system efficiency. By utilizing a shared bridge arm, the converter significantly reduces the number of switches employed, resulting in a more streamlined design. The design process prioritizes efficiency by optimizing critical converter parameters and attaining ZVS, thereby enhancing the overall performance of the system. In addition, utilizing phase shift as an additional control freedom in the FSBB topology enhances the system efficiency. Moreover, to reduce the calculation complexity in real-time controllers, a fitting-model-based optimal control approach is proposed. Ultimately, experimental results validate the efficacy of the proposed design, demonstrating its improved performance in terms of high efficiency and enhanced dynamic responses.

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