Direct Power Flow Controller With Continuous Full Regulation Range

Chong Yao and Youjun Zhang

***Abstract*—In order to enhance power flow control in power transmission, a new simplified structure of direct power flow controller with continuous full regulation range (F-DPFC) was proposed. It has only one-stage power conversion and comprises of a three-phase transformer in parallel and a three-phase transformer in series with grid, three single-phase full-bridge ac units, and a three-phase filter. Compared with the previous DPFC, the proposed one dispenses with two complex three-phase selection switches, which are connected to a high-voltage grid directly, and replaces buck-type ac units with full-bridge-type ac units. Then, the limit of its duty cycle is extended from [0, 1] to [−1, 1], providing a continuous 360° adjustment range of compensation voltage. Within a large complete zone replacing six separate zones, the proposed F-DPFC can regulate the amplitude and phase angle of grid node voltage, respectively and simultaneously, and the active and reactive power flow in the grid can be controlled smoothly and effectively. The new structure is easy to achieve modular expansion and enables it to operate under high-voltage and power conditions. Its structure and operational principle were analyzed in detail, and a prototype was developed. The experimental results verified the feasibility and the correctness of the theoretical analysis.**

***Index Terms*—Compensation voltage, direct power flow controller (DPFC), grid voltage, phase regulation, power transmission.**

I. INTRODUCTION

HOW to control the power flow quickly and accurately in power transmission systems is always the key to improve power grid quality and energy transfer efficiency. Power flow in power system includes active power flow and reactive power flow (P_R, Q_R), and they are functions of the line impedance (X), the magnitudes of the sending-end voltage and the receiving-end voltage (U_{Sm}, U_{Rm}), and the phase angle difference between the two voltages (θ), as illustrated in (1), when the line is represented in its most simplified form as reactance [1], [2], [3], [4], [5]. Therefore, the flexible ac-transmission system (FACTS), which can adjust one or more ac-transmission system parameters to increase the stability of power system, is widely used [6], [7], [8].

The FACTS devices can be connected to the transmission line in different ways, such as series, parallel, or series–parallel integration. The shunt FACTS devices [9], [10] are used to control transmission voltage and power, and reduce losses, among which static var compensator [11], [12] and static synchronous compensator (STATCOM) [13], [14], [15] are used widely. STATCOM is applied to ac power transmission based on a voltage-source converter [16], providing a reactive power supply to the grid. Typically, it is installed on power grids experiencing power factor and voltage regulation issues. The main features of STATCOM systems are fast response time, small footprint, and excellent dynamic characteristics under different operating conditions

$$\begin{cases} P_R = \frac{U_{Sm}U_{Rm}}{2X}\sin\theta \\ Q_R = \frac{U_{Sm}U_{Rm}\cos\theta - {U_{Rm}}^2}{2X}. \end{cases} \tag{1}$$

The series FACTS devices [17], [18] include static synchronous series compensator (SSSC) [19], [20], thyristor-controlled series capacitor [21], and gate-controlled series capacitor [22]. These devices are connected in series to the power system and change the equivalent reactance and resistance of the circuit to achieve voltage regulation and power compensation, thereby improving the stability and reliability of the power system. However, they cannot control active and reactive power flow independently and simultaneously.

The unified power flow controller (UPFC) [23], [24], [25], [26], composed of SSSC, STATCOM, and dc energy storage components, is one of the most powerful and comprehensive devices in FACTS. By combining STATCOM and SSSC, UPFC can realize the function of adjusting active and reactive power flow, respectively and simultaneously. However, due to the large dc energy storage element between STATCOM and SSSC, which has a short equipment life cycle or a high number of failures and causes high maintenance cost, the further promotion of UPFC is restricted, even though it has superior control ability.

In order to remove the dc energy storage elements in the device, a new structure, namely the ac–ac converter with controllable phase and amplitude (ACCPA) [27], [28], [29], [30], was proposed. It adopts the concept of a virtual orthogonal source [28] and a two-stage structure, which not only has the functions of boosting and bucking voltage but also allows for the adjustment of the output voltage phase angle. Based on ACCPA, a new concept called direct power flow controller (DPFC), which does not contain large dc energy storage elements, was described in [8]. As shown in Fig. 1, DPFC is based on single-stage ACCPA and it replaces the boost-type ac converter in two-stage ACCPA with an output transformer to achieve the function of boosting voltage and has only a one-stage conversion circuit.

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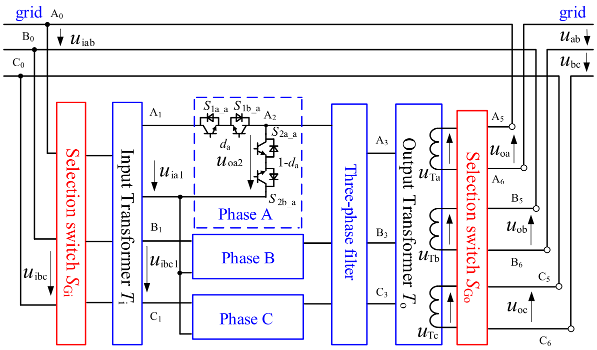


Fig. 1. DPFC with full 360° regulation zone.

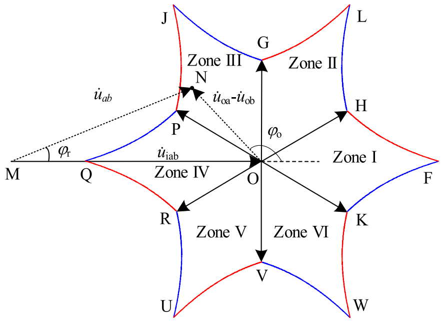


Fig. 2. Six basic regulation zones of DPFC.

TABLE I
COMPARISON BETWEEN F-DPFC AND EXISTING METHODS

Objects	Advantages of F-DPFC
Compared with STATCOM and SSSC	F-DPFC can adjust active and reactive power flow simultaneously and independently.
Compared with U PFC	F-DPFC has only one-stage conversion circuit and does not suffer from the drawbacks of high failure rates and maintenance costs caused by the presence of large dc energy storage elements in UPFC.
Compared with DPFC	F- DPFC can achieve continuous adjustment of compensation voltage within a 360° range, and its structure is simple and easy to implement modular expansion.

DPFC is able to regulate the amplitude and phase angle of output compensation voltage, respectively and simultaneously, within a 360° range and adjust active power and reactive power in the power transmission system by connecting the output compensation voltage in series to the power grid.

However, under a certain combination of selection switches S_{Gi} and S_{Go}, the DPFC can only adjust the phase of the output compensating voltage within the range of $-30°$ to $30°$. As shown in Fig. 2, the output compensating voltage adjustment range of DPFC is divided into six independent zones. The adjustment process is only carried out continuously in a separate zone and only by changing the combination of the selection switches can the output compensation voltage be adjusted from one zone to another. Because the step length for phase adjustment in selection switches is 60°, this adjustment will result in a sudden change in the output voltage. From (1), it can be seen that the discontinuity of voltage caused by the change of the combination of selection switches will lead to abrupt changes in active and reactive power flow, which is obviously not conducive to the stability of the power transmission. And due to the selection switches, it is difficult for DPFC to achieve modular expansion [31], [32], [33], which limits its application in high-voltage and high-power situations.

In order to solve the problem of discontinuous control process in DPFC and simplify the structure for modular expansion, a new structure called DPFC with continuous full regulation range (F-DPFC) was proposed in this article. F-DPFC, without the need for selection switches, allows smooth and continuous adjustment of compensating voltage within a 360° range, and then independently or simultaneously adjusts the magnitude and phase angle of the voltage at the grid nodes to control the active and reactive power flow in the transmission system. Compared with DPFC, F-DPFC replaces buck-type ac units in DPFC with full-bridge-type ac units and removes selection switches that have complex structure and high cost, owing to being connected to the high-voltage power grid directly. Furthermore, as the selection switches are removed, F-DPFC is easier to achieve modular expansion, which further broadens its application. F-DPFC also does not contain the large dc energy storage element, which is present in UPFC, and has only one-stage conversion circuit. Therefore, F-DPFC does not suffer from the drawbacks of high failure rates and maintenance costs caused by the presence of large dc energy storage elements in UPFC. The comparison between F-DPFC and existing methods is summarized in Table I. The topology and operational principle of F-DPFC were described in detail. The regulation range of output compensation voltage and relationship between adjustment range and control parameters were analyzed, and then the selection of control parameters and closed-loop control strategy were given. Finally, a prototype of F-DPFC and experimental results were shown to verify the correctness of theory and feasibility of F-DPFC.

II. TOPOLOGICAL STRUCTURE AND OPERATIONAL PRINCIPLE

A. Topological Structure

The structure of F-DPFC is shown in Fig. 3. Similar to DPFC, F-DPFC also contains a three-phase transformer in parallel and a three-phase transformer in series with grid. It takes the place of buck-type ac units in DPFC with full-bridge-type ac units and removes selection switches.

The input terminals of transformer T_i are connected in parallel with the power grid and the output terminals of the transformer T_o are connected in series with the power grid. Fig. 4 shows the connection mode of input transformer winding and output transformer winding. In this article, T_i and T_o are connected in a Δ/Yn11 type to cancel out the third harmonic currents and voltages. The possible connection type can also be Δ/Yn1, Δ/Yn3, Δ/Yn5, Δ/Yn7, or Δ/Yn9, with the same operating principle for different connection types. Each secondary winding of transformer T_i is connected to the input terminal of a

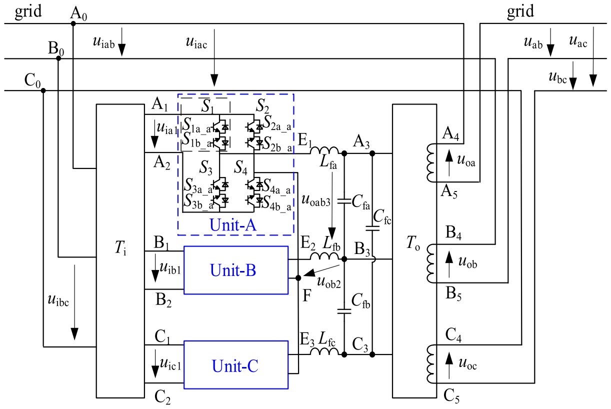


Fig. 3. Basic topological structure of the F-DPFC.

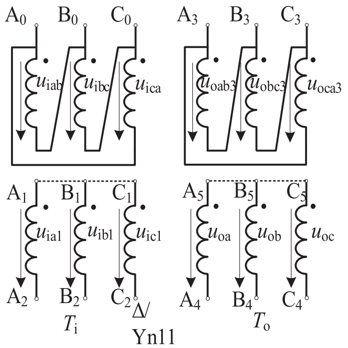


Fig. 4. Connection mode of input transformer and output transformer.

full-bridge-type ac unit. As shown in Fig. 3, one output terminal of each full-bridge-type ac unit is connected to the same point, defined as point F, and the other output terminal is connected to the input terminal of transformer T_o through a three-phase output filter.

B. Operational Principle

To facilitate analysis, we assume the following.

1) Original grid voltage is sinusoidal with angular frequency ω ($=2\pi f$, where f is its frequency) and u_{iab}, u_{ibc}, and u_{ica} are the original line voltages.
2) Circuit components are ideal and low-frequency voltage drop across the inductor L_{fx} ($x = a, b, c$, where x is the name of phase in lowercase letter) is not taken into account.
3) T_i and T_o are of Δ/Yn11-type connection group with turn ratios N_i and N_o. It should be noted that points A_1, B_1, and C_1 or A_5, B_5, and C_5 are not connected together, and the secondary windings of T_o are separately connected with the power transmission line in series.

Then, u_{ia1}, u_{ib1}, and u_{ic1}, the secondary voltage of T_i, and the input voltages of buck units in Fig. 3, and d_a, d_b, and d_c, and the duty ratio of the buck units, are given as follows:

$$\begin{cases} u_{ia1} = \frac{u_{iab}}{N_i} = \frac{U_{imL}}{N_i}\sin\omega t = U_{im}\sin\omega t \\ u_{ib1} = \frac{u_{ibc}}{N_i} = \frac{U_{imL}}{N_i}\sin(\omega t - 120^\circ) = U_{im}\sin(\omega t - 120^\circ) \\ u_{ic1} = \frac{u_{ica}}{N_i} = \frac{U_{imL}}{N_i}\sin(\omega t + 120^\circ) = U_{im}\sin(\omega t + 120^\circ) \end{cases} \tag{2}$$

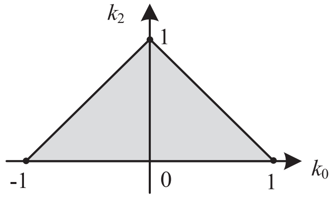


Fig. 5. Value range of k_0 and k_2.

$$\begin{cases} d_a = k_0 + k_2\sin(2\omega t + \beta_2) \\ d_b = k_0 + k_2\sin[2(\omega t - 120^\circ) + \beta_2] \\ d_c = k_0 + k_2\sin[2(\omega t + 120^\circ) + \beta_2] \end{cases} \tag{3}$$

where U_{imL} and U_{im} are the amplitudes of u_{iab} and u_{ia1}, respectively, β_2 is the phase angle of the ac component of d_a based on u_{ia1}, and the parameters k_0 and k_2 are constants and k_2 is nonnegative.

In unit-A of Fig. 3, when switch unit S_1 is always on and switch unit S_3 is always off, and switch units S_2 and S_4 are alternately on, the output voltage varies within 0–1 times the input voltage u_{ia1}, that is, $0 < d_a < 1$. When switch unit S_3 is always on and switch unit S_1 is always off, and switch units S_2 and S_4 are alternately on, the output voltage varies within -1 to 0 times the input voltage u_{ia1}, that is, $-1 < d_a < 0$. Therefore, we can get $-1 \le d_a \le 1$ and further know that $k_0 + k_2 \le 1$ at $0 \le k_0 \le 1$, or $k_0 - k_2 \ge -1$ at $-1 \le k_0 \le 0$. The value range of k_0 and k_2 is shown in Fig. 5.

After most high-frequency components are filtered out, u_{ox2}, the output voltage of the buck unit (between points X_3 and F in Fig. 3, where $X = A, B, C$ and X is the name of phase in uppercase letter), is obtained, which contains the fundamental and third harmonic components

$$\begin{cases} u_{oa2} = d_a u_{ia1} \\ \quad = U_{im}\sin\omega t\,[k_0 + k_2\sin(2\omega t + \beta_2)] \\ u_{ob2} = d_b u_{ib1} \\ \quad = U_{im}\sin(\omega t - 120^\circ)\,[k_0 + k_2\sin(2\omega t - 240^\circ + \beta_2)] \\ u_{oc2} = d_c u_{ic1} \\ \quad = U_{im}\sin(\omega t + 120^\circ)\,[k_0 + k_2\sin(2\omega t + 240^\circ + \beta_2)]. \end{cases} \tag{4}$$

Simplified

$$\begin{cases} u_{oa2} = U_{im}\left[k_0\sin\omega t + \frac{1}{2}k_2\sin(\omega t + \beta_2 + 90^\circ) \right. \\ \qquad \left. -\frac{1}{2}k_2\cos(3\omega t + \beta_2)\right] \\ u_{ob2} = U_{im}\left[k_0\sin(\omega t - 120^\circ) + \frac{1}{2}k_2\sin(\omega t + \beta_2 - 30^\circ) \right. \\ \qquad \left. -\frac{1}{2}k_2\cos(3\omega t + \beta_2)\right] \\ u_{oc2} = U_{im}\left[k_0\sin(\omega t + 120^\circ) + \frac{1}{2}k_2\sin(\omega t + \beta_2 + 210^\circ) \right. \\ \qquad \left. -\frac{1}{2}k_2\cos(3\omega t + \beta_2)\right]. \end{cases} \tag{5}$$

Since T_o is of Δ/Y-type connection group with turn ratio N_o, the third harmonic signals in u_{oa2}, u_{ob2}, and u_{oc2} cancel each other out, and only the fundamental voltage components u_{oa3}, u_{ob3}, and u_{oc3} have remained. It can be seen that F-DPFC can only operate when there is at least two-phase grid balance. One can obtain the voltages u_{oab3}, u_{obc3}, and u_{oca3}

$$\begin{cases} u_{oa3} = U_{im}\big[k_0 \sin\omega t + \frac{1}{2}k_2 \sin(\omega t + \beta_2 + 90^\circ)\big] \\ \quad = U_{om}\sin(\omega t+\varphi_1) \\ u_{ob3} = U_{im}\big[k_0\sin(\omega t - 120^\circ) \\ \quad + \frac{1}{2} k_2 \sin(\omega t+\beta_2-30^\circ)\big] \\ \quad = U_{om}\sin(\omega t+\varphi_1-120^\circ) \\ u_{oc3} = U_{im}\big[k_0\sin(\omega t+120^\circ) \\ \quad +\frac{1}{2} k_2\sin(\omega t+\beta_2+210^\circ)\big] \\ \quad = U_{om}\sin(\omega t+\varphi_1+120^\circ)\end{cases} \tag{6}$$

$$\begin{cases} u_{oab3} = u_{oa3} - u_{ob3} = \sqrt{3}U_{om}\sin(\omega t+\varphi_1+30^\circ) \\ u_{obc3} = u_{ob3} - u_{oc3} = \sqrt{3}U_{om}\sin(\omega t+\varphi_1-90^\circ) \\ u_{oca3} = u_{oc3} - u_{oa3} = \sqrt{3}U_{om}\sin(\omega t+\varphi_1+150^\circ) \end{cases} \tag{7}$$

where U_{om} is the amplitude of the fundamental voltage component u_{oa3}, and φ_1 is the phase angle of the fundamental voltage component u_{oa3}.

Here, φ_1 and U_{om} would be given as follows:

$$\varphi_1 = \begin{cases} \arctan\frac{k_2\cos\beta_2}{2k_0-k_2\sin\beta_2} & (2k_0-k_2\sin\beta_2>0) \\ \arctan\frac{k_2\cos\beta_2}{2k_0-k_2\sin\beta_2}+\pi & (2k_0-k_2\sin\beta_2<0) \\ \frac{\pi}{2} \quad (2k_0-k_2\sin\beta_2=0 \text{ and } \cos\beta_2>0) \\ -\frac{\pi}{2} \quad (2k_0-k_2\sin\beta_2=0 \text{ and } \cos\beta_2<0) \end{cases} \tag{8}$$

$$\begin{aligned} U_{om} &= U_{im}\sqrt{\frac{{k_2}^2}{4}+{k_0}^2-k_0k_2\sin\beta_2} \\ &= \frac{U_{imL}}{N_i}\sqrt{\frac{{k_2}^2}{4}+{k_0}^2-k_0k_2\sin\beta_2}. \end{aligned} \tag{9}$$

One can obtain the compensation phase voltages of grids u_{oa}, u_{ob}, and u_{oc}

$$\begin{cases} u_{oa} = \frac{\sqrt{3}U_{om}}{N_o}\sin(\omega t+\varphi_1+30^\circ) \\ u_{ob} = \frac{\sqrt{3}U_{om}}{N_o}\sin(\omega t+\varphi_1-90^\circ) \\ u_{oc} = \frac{\sqrt{3}U_{om}}{N_o}\sin(\omega t+\varphi_1+150^\circ). \end{cases} \tag{10}$$

Then, the compensation line voltages of grids u_{oab}, u_{obc}, and u_{oca} are obtained

$$\begin{cases} u_{oab} = u_{oa} - u_{ob} = \frac{3U_{om}}{N_o}\sin(\omega t+\varphi_1+60^\circ) \\ u_{obc} = u_{ob} - u_{oc} = \frac{3U_{om}}{N_o}\sin(\omega t+\varphi_1-60^\circ) \\ u_{oca} = u_{oc} - u_{oa} = \frac{3U_{om}}{N_o}\sin(\omega t+\varphi_1+180^\circ). \end{cases} \tag{11}$$

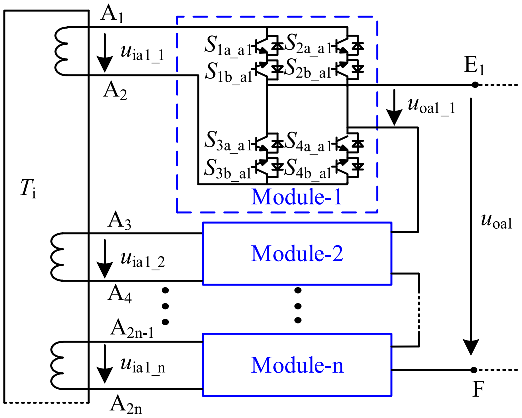


Fig. 6. Structure of A-phase modular expansion.

The regulated grid line voltages u_{ab}, u_{bc}, and u_{ca} are as follows:

$$\begin{cases} u_{ab} = u_{iab} + u_{oab} = u_{iab} + (u_{oa} - u_{ob}) \\ \quad = U_{mL}\sin(\omega t+\varphi_r) \\ u_{bc} = u_{ibc} + u_{obc} = u_{ibc} + (u_{ob} - u_{oc}) \\ \quad = U_{mL}\sin(\omega t+\varphi_r-120^\circ) \\ u_{ca} = u_{ica} + u_{oca} = u_{ica} + (u_{oc} - u_{oa}) \\ \quad = U_{mL}\sin(\omega t+\varphi_r+120^\circ) \end{cases} \tag{12}$$

where U_{mL} and φ_r are the amplitude and phase angle of u_{ab}, and here, U_{mL} and φ_r would be given as follows:

$$\begin{aligned} \varphi_r &= \arctan\frac{\frac{3U_{om}}{N_o}\sin(\varphi_1+60^\circ)}{U_{imL}+\frac{3U_{om}}{N_o}\cos(\varphi_1+60^\circ)} \\ &= \arctan\frac{3U_{om}\sin(\varphi_1+60^\circ)}{N_oU_{imL}+3U_{om}\cos(\varphi_1+60^\circ)} \end{aligned} \tag{13}$$

$$U_{mL} = \sqrt{\begin{aligned} &\left[U_{imL}+\frac{3U_{om}}{N_o}\cos(\varphi_1+60^\circ)\right]^2 \\ &+\left[\frac{3U_{om}}{N_o}\sin(\varphi_1+60^\circ)\right]^2 \end{aligned}}. \tag{14}$$

From (8) and (9), we know that U_{om} and φ_1 are controlled by three parameters k_0, k_2, and β_2, and so are U_{mL} and φ_r.

C. Expansion of Circuit Modular Structure

Due to material constraints, the voltage stress of power electronic device cannot be significantly increased. Therefore, modular expansion is an effective way for circuit structures to be suitable for high-voltage and high-power applications. Here is an introduction to the modular expansion structure.

Compared with the previous structure, the modular structure increases the number of the secondary windings of T_i and the full-bridge ac circuits of each phase. The output terminals of the full-bridge ac circuits for each phase are connected in series, and the input terminals are connected to the secondary windings of the three-phase multiwinding transformer, respectively. The A-phase conversion unit of modular structure is shown in Fig. 6.

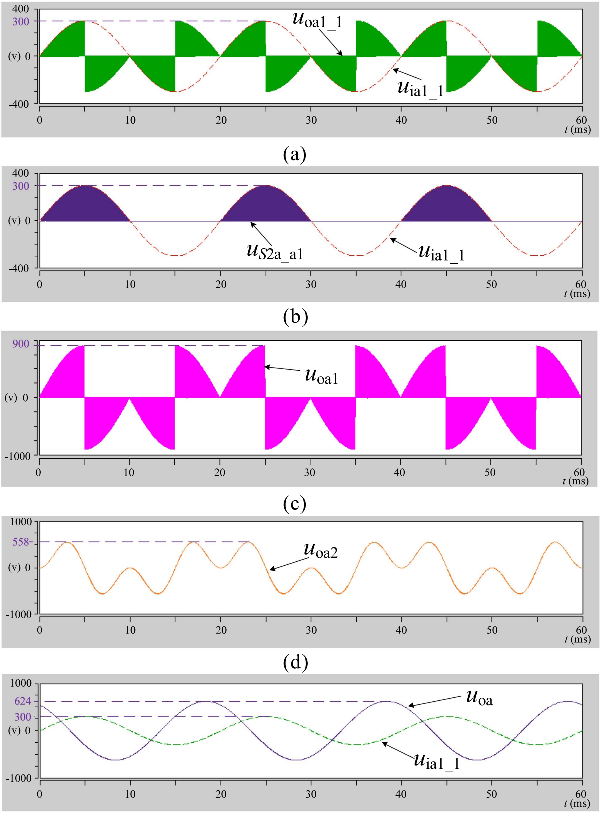


Fig. 7. Simulation results of F-DPFC with modular expansion. (a) u_{ia1_1} and u_{oa1_1}. (b) u_{S2a_a1}. (c) u_{oa1}. (d) u_{oa2}. (e) u_{ia1_1} and u_{oa}.

To verify the feasibility of the modular structure, simulation verification is conducted for the F-DPFC with modular expansion. In the simulation experiment, the number of modules in each phase of the structure is set to 3, and T_o is of Δ/Yn11 type with turn ratio 1. The input voltage of each module is the same, with an amplitude of 300 V, and parameters $k_0 = 0$, $k_2 = 0.8$, and $\beta_2 = 90°$ are set, which can also be others. The input voltage u_{ia1_1} and the unfiltered output voltage u_{oa1_1} of module-1 are shown in Fig. 7(a). It can be seen that u_{ia1_1} is the amplitude envelope curve of the high-frequency pulse signal u_{oa1_1}. In Fig. 7(b), u_{S2a_a1} is the voltage stress across the switch tube S_{2a_a1} in module-1. It can be seen that the switch tube S_{2a_a1} maintains a conducting state during half of the u_{ia1_1} period and performs a switching action during the other half of time. The voltage stress of the switch tube at the time of disconnection is the input voltage of the module. Since each module has the same control law and is connected in series at the output end, the voltage signal u_{oa1} is obtained in Fig. 7(c), which is the sum of the output voltages of each module in A-phase and also three times the magnitude of voltage u_{oa1_1}. By filtering out higher harmonic components, the voltage u_{oa2}, as shown in Fig. 7(d), containing the fundamental wave and the third harmonic wave, is obtained. Then, after offsetting the third harmonic, the output compensation voltage u_{oa} is finally obtained in Fig. 7(e). By substituting the values of k_0, k_2, and β_2 into (8), (9), and (10), one can get $\varphi_1 + 30° = 120°$ and $\sqrt{3}U_{om}/N_o = 207.85$ V, which are the phase angle of u_{oa} leading u_{ia1_1} and approximately the one-third magnitude of u_{oa} in Fig. 7(e), respectively. Therefore, the simulation results not only demonstrate the feasibility of the modular structure but also validate the correctness of the theoretical analysis presented. And it can be seen that the modular expansion enables F-DPFC to be applied in high-voltage and high-power situations using low-voltage devices.

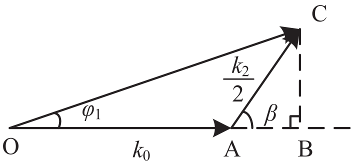


Fig. 8. Schematic diagram of compensation voltage synthesis.

III. ADJUSTMENT RANGE AND CONTROL STRATEGY

A. Range of Grid Compensation Voltage

For the convenience of analysis, take A-phase as an example. We can simplify the A-phase in (6) to the following formula:

$$k_d = \frac{u_{oa3}}{U_{im}} = k_0 \sin \omega t + \frac{1}{2} k_2 \sin(\omega t + \beta) \tag{15}$$

where $\beta = \beta_2 + 90°$, and k_d is a vector with the same phase as u_{oa3}.

The compensation voltage synthesis diagram is shown in Fig. 8. In the diagram, the vector OC represents u_{oa3}/U_{im}, and the vectors OA and AC represent the voltage components $k_0 \sin\omega t$ and $0.5k_2 \sin(\omega t + \beta)$. If $0 < \varphi_1 < 90°$, the following can be obtained:

$$\begin{cases} |\overrightarrow{AB}| = \cos\beta \cdot |\overrightarrow{AC}| = \frac{k_2 \cos\beta}{2} \\ |\overrightarrow{BC}| = \sin\beta \cdot |\overrightarrow{AC}| = \frac{k_2 \sin\beta}{2} \\ |\overrightarrow{OB}| = |\overrightarrow{OA}| + |\overrightarrow{AB}| = k_0 + \frac{k_2 \cos\beta}{2}. \end{cases} \tag{16}$$

Then, one can obtain φ_1 and $|k_d|$

$$\begin{aligned} \varphi_1 &= \arctan \frac{|\overrightarrow{BC}|}{|\overrightarrow{OB}|} = \arctan \frac{|\overrightarrow{BC}|}{|\overrightarrow{OA}| + |\overrightarrow{AB}|} \\ &= \arctan \frac{k_2 \sin\beta}{2k_0 + k_2 \cos\beta} \\ &= \arctan \frac{k_2 \cos\beta_2}{2k_0 - k_2 \sin\beta_2} \\ |k_d| &= \frac{|u_{oa3}|}{U_{im}} = |\overrightarrow{OC}| = \sqrt{|\overrightarrow{OB}|^2 + |\overrightarrow{BC}|^2} \\ &= \sqrt{\left(k_0 + \frac{k_2 \cos\beta}{2}\right)^2 + \left(\frac{k_2 \sin\beta}{2}\right)^2} \\ &= \sqrt{\frac{{k_2}^2}{4} + {k_0}^2 + k_0 k_2 \cos\beta} \end{aligned} \tag{17}$$

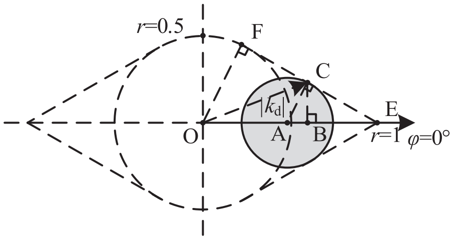


Fig. 9. When k_0 is a fixed value, the adjustment range of compensation voltage.

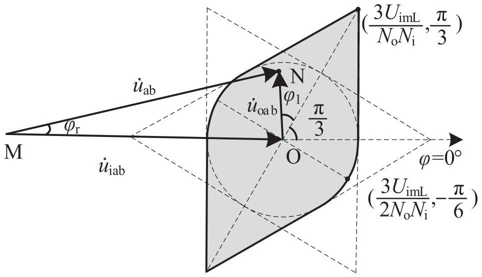


Fig. 10. Total adjustment range of compensation voltage.

$$= \sqrt{\frac{{k_2}^2}{4} + {k_0}^2 - k_0 k_2 \sin\beta_2}. \tag{18}$$

The expression for φ_1 and $|u_{oa3}|$ over the entire range can be derived by similar deduction, as shown in (8) and (9).

By combining the value range of k_0 and k_2, we can further obtain the total adjustment range of compensation voltage. Establish polar coordinates, as shown in Fig. 9. Obviously, when $k_0 = 0$, the adjustment range is a circle with point O as the center and 0.5 as the radius. When $k_0 = 1$, the adjustment range is at point $E\,(1, 0°)$. Make the tangent line of circle O through point E and the tangent point is F, where $\angle EOF = 60°$. When $0 < k_0 < 1$, assuming $OA = k_0$, as shown in Fig. 10, the adjustment range of the compensation voltage is a circle with point A as the center and AC as the radius. One knows that $AC_{\max} = 0.5(1-k_0)$ and $AE = 1-k_0$. In the right triangle ACE, we know $\angle ACE = 90°$ and $2AC = AE$. One can obtain $\angle CEA = 30°$ and $\angle FEO = 30°$, that is, points F, C, and E are on the same straight line. The adjustment range of compensation voltage for other zones can be obtained in the same way. If T_i and T_o are Δ/Yn11-type connection group, the total compensation voltage adjustment range is shown in Fig. 10, and that of other combination methods is also shown in it. The only difference between them is the phase difference and the working principle of them is the same, so it will not be discussed here. Through u_{oab}, not only the phase angle φ_r of u_{ab} can be adjusted to lead or lag but also the amplitude U_{mL} of u_{ab} can be larger or smaller than the amplitude U_{imL} of u_{iab}.

B. Influence of Control Parameters on Adjustment Range

Since k_2 is a nonnegative number and the relationship between k_2 and k_0 is shown in Fig. 5, only the influence of k_0 on the amplitude and phase of the output voltage is analyzed here.

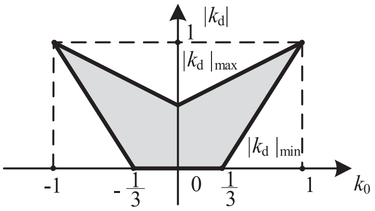


Fig. 11. Relationship between the regulation range of $|k_d|$ and k_0.

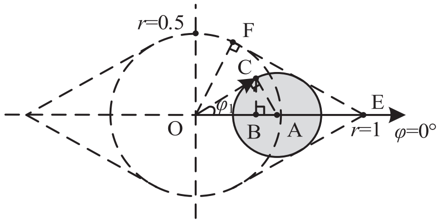


Fig. 12. Compensation voltage regulation range.

1) The relationship between the adjustable range of $|k_d|$ and k_0.

It can be seen from Fig. 9 that the extreme value points of adjustable voltage amplitude are the two intersections of the circle A and the line $\varphi = 0°$ or 180°, and the adjustment range is the circle based on point A as center and $0.5(1-k_0)$ as the radius. When the adjustable range does not include the origin O, we can get

$$\begin{cases} |k_d|_{\max} = k_0 + \frac{k_2}{2} = \frac{1+k_0}{2} \\ |k_d|_{\min} = k_0 - \frac{k_2}{2} = \frac{1-k_0}{2} \end{cases} \quad \left(\frac{1}{3} < k_0 < 1\right). \tag{19}$$

If the adjustable range includes the origin O, one can obtain $|OC|_{\min} = 0$. When $-1 < k_0 < 0$, the situation is similar. Fig. 11 shows the relationship between the regulation range of $|k_d|$ and k_0.

2) The relationship between the adjustable range of φ_1 and k_0.

When the compensation voltage phase angle takes the extreme value and $0 < k_0 < 1$, the relationship between φ_1 and k_0 is shown in Fig. 12. At this time, $k_2 = 1-k_0$, $OA = k_0$, and $2AC = 1-k_0$. We can get

$$\begin{cases} \varphi_1 \in \left[-\arcsin\frac{1-k_0}{2k_0}, \arcsin\frac{1-k_0}{2k_0}\right], \frac{1}{3} < k_0 < 1 \\ \varphi_1 \in [0, 2\pi], 0 < k_0 < \frac{1}{3}. \end{cases} \tag{20}$$

When $-1 < k_0 < 0$, the situation is similar to $0 < k_0 < 1$. The relationship between the regulation range of φ_1 and k_0 is shown in Fig. 13.

C. Control Strategy

1) Selection of Initial Parameters: Known from (5), the value of k_2, where $k_2 \geq 0$, affects the magnitude of the third harmonic voltage in F-DPFC and it should be taken as small as possible for the stability of grid. A reasonable parameters selection strategy is

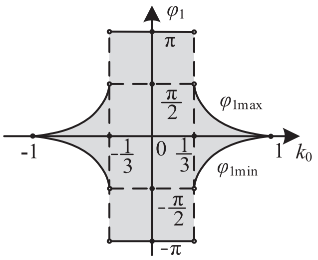


Fig. 13. Relationship between the regulation range of φ_1 and k_0.

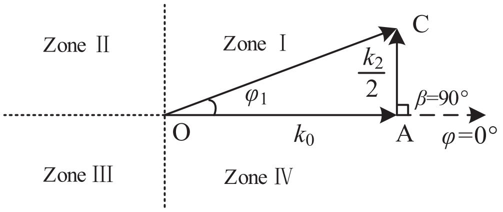


Fig. 14. Compensation voltage vector synthesis under optimal control.

proposed below and the compensation voltage vector synthesis is shown in Fig. 14.

From Fig. 8 and (15), in order to minimize the value of k_2, the vector AC should be perpendicular to the vector OA, that is, $\beta = 90°$ or $-90°$. From Fig. 14, the adjustment range of compensation voltage is divided into four zones. The phase adjustment ranges of the four zones are (0°, 90°), (90°, 180°), (180°, 270°), and (270°, 360°), and one knows that $k_0 > 0$ and $\beta = 90°$ in zone I, $k_0 < 0$ and $\beta = 90°$ in zone II, $k_0 < 0$ and $\beta = -90°$ in zone III, and $k_0 > 0$ and $\beta = -90°$ in zone IV. The value of k_0 and k_2 can be obtained based on the expected amplitude and phase of the output compensation voltage. The specific process is given as follows.

Taking A-phase as an example, we assume that the input voltage of the buck unit be u_{ia1}, where $u_{ia1} = U_{im}\sin\omega t$ and U_{im} is the amplitude of u_{ia1}. T_o is of Δ/Yn11-type connection group with turn ratio N_o. If the reference of output compensation voltage u_{oa} is $U_{\text{ref}}\sin(\omega t + \varphi_{\text{ref}})$, where U_{ref} is the amplitude of u_{oa} and φ_{ref} is the phase angle of u_{oa} leading u_{ia1}, according to the compensation voltage vector synthesis in Fig. 14 and (10), the value of k_0 and k_2 can be obtained as follows:

$$\begin{cases} k_0 = \frac{N_o U_{\text{ref}}}{\sqrt{3}U_{im}}\cos\left(\varphi_{\text{ref}} - 30^\circ\right) \\ k_2 = 2\left|\frac{N_o U_{\text{ref}}}{\sqrt{3}U_{im}}\sin\left(\varphi_{\text{ref}} - 30^\circ\right)\right|. \end{cases} \tag{21}$$

When the compensation voltage is required to be in zone I or II, let $\beta = 90°$, and when the compensation voltage is required to be in zone III or IV, let $\beta = -90°$.

It should be noted that the adjustment range of output compensation voltage synthesized based on the above control strategy is slightly smaller than the total compensation voltage adjustment range analyzed previously, and the range is a rhombus formed by connecting the four intersection points of the edge of total adjustment range and coordinate axis. When the required output adjustment point is outside the range, we can obtain the value range of k_0, k_2, and β based on the previous analysis. As this area is small and there will be a certain margin during operation, we will not discuss it in detail here.

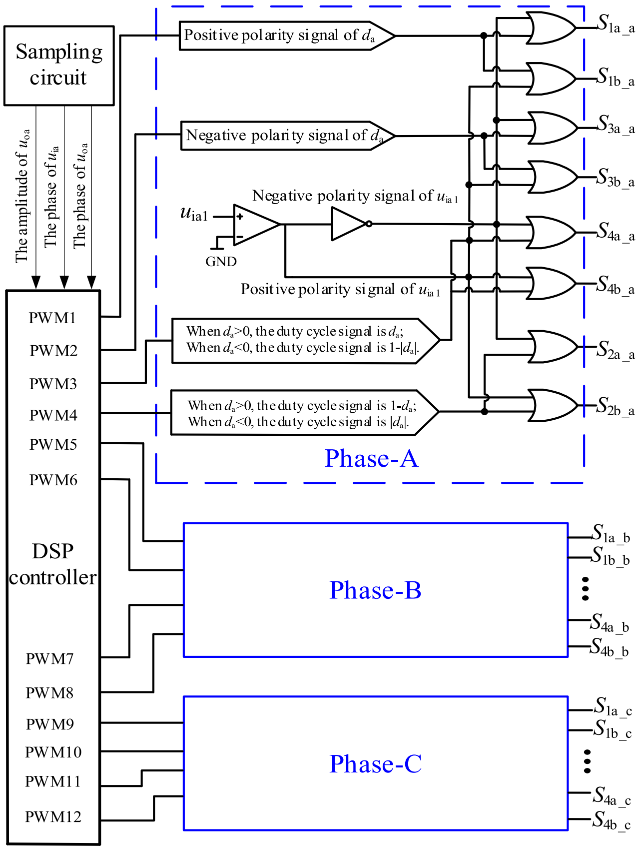


Fig. 15. Control block diagram.

2) Closed-Loop Control Strategy: The control block diagram is shown in Fig. 15. By using a sampling circuit, the amplitude of u_{oa} and the phase of the u_{oa} and u_{ia1} are obtained. In the DSP processor, the measured signals are compared with the reference signals, and the parameters are adjusted to synthesize a new duty cycle signal. In the A-phase, the first arm of the full-bridge buck ac unit is controlled by the positive and negative polarity signal of the duty cycle d_a, while the second arm is controlled by the absolute value of d_a and its complementary signal. When $d_a > 0$, the switch unit S_1 is always on, S_3 is always off, and the duty cycle signal of S_4 is d_a, while the duty cycle signal of S_2 is $1-d_a$. When $d_a < 0$, the switch unit S_3 is always on, S_1 is always off, and the duty cycle signal of S_2 is $|d_a|$, while the duty cycle signal of S_4 is $1-|d_a|$. Then, the signals of the four switch units are combined with the positive and negative polarity signals of u_{ia1} through a logical "OR" operation to obtain the signals of each switching tube.

The control objects of F-DPFC are the amplitude and phase angle of the output voltage. First, the initial values are assigned to the parameters k_0, k_2, and β. During the control process, phase closed loop is performed first, followed by an amplitude closed loop. φ_{o1}, which is the phase angle of u_{oa} leading u_{ia1}, and U_{o1}, which is the amplitude of u_{oa}, are obtained by sampling. Then, by comparing them with reference phase angle

φ_{ref} and voltage amplitude U_{ref}, the parameters k_0 and k_2 are continuous adjusted to generate a new duty cycle signal. If k_0 or k_2 is 0, the control process is simple because there is only one parameter that needs to be adjusted, so this condition will not be discussed here.

In Fig. 14, it is evident that $\beta = 90°$ or $-90°$, and when φ_{o1} is not equal to φ_{ref}, we can increase or decrease φ_{o1} by adjusting the values of k_2 or k_1 so as to make φ_{o1} equal to φ_{ref}. Once φ_{o1} becomes equal to φ_{ref}, the ratio of k_2 to k_0 is calculated, and constantly adjust the values of k_0 and k_2 according to this ratio to ensure that U_{o1} is equal to U_{ref}. One complete adjustment cycle in detail is given as follows.

1) *The phase closed loop:* When $\varphi_{o1} > \varphi_{\text{ref}}$, if $k_0 > 0$ and $\beta = 90°$, or $k_0 < 0$ and $\beta = -90°$, k_2 decreases and $|k_0|$ increases, and if $k_0 < 0$ and $\beta = 90°$, or $k_0 > 0$ and $\beta = -90°$, k_2 increases and $|k_0|$ decreases. When $\varphi_{o1} < \varphi_{\text{ref}}$, if $k_0 > 0$ and $\beta = 90°$, or $k_0 < 0$ and $\beta = -90°$, k_2 increases and $|k_0|$ decreases, and if $k_0 < 0$ and $\beta = 90°$, or $k_0 > 0$ and $\beta = -90°$, k_2 decreases and $|k_0|$ increases. When the absolute value of the difference between φ_{o1} and φ_{ref} is maintained within a small range Δ, the ratio k_r of k_2 to k_0 is saved at this time and the phase closed loop is completed.
2) *The amplitude closed loop:* When $U_{o1} > U_{\text{ref}}$, if $k_0 > 0$, k_0 decreases, and if $k_0 < 0$, k_0 increases. When $U_{o1} < U_{\text{ref}}$, if $k_0 < 0$, k_0 decreases, and if $k_0 > 0$, k_0 increases. Then, k_2 is obtained based on the saved ratio k_r of k_2 to k_0. This is done until the amplitude closed loop is finished.

The flowchart is shown in Fig. 16. It should be noted that, in the amplitude closed loop, in order to improve control precision, when $0 < |k_r| < 1$, that is $|k_0| > k_2$, we obtain k_2 by adjusting k_0, and when $|k_r| > 1$, that is $|k_0| < k_2$, we obtain k_0 by adjusting k_2. The "start" and "finish" are the beginning and end of a cycle rather than the adjustment process.

In this article, the TMS320F2812 chip in DSP is used for closed-loop control. After receiving the digital signal of the output voltage, the main factors affecting the parameter adjustment time are the data sampling rate, processing delay, and the running time of the control algorithm. The TMS320F2812 is a high-performance DSP chip with a maximum system clock frequency of 150 MHz, capable of fast data processing and computation. Considering that the main purpose of the experiment is to verify the correctness of the control strategy, a fixed step size is used to adjust the parameters, and the sampling frequency is 50 Hz. Due to the fact that data processing and program execution time are in the microsecond range, the parameter adjustment time can be approximately equal to the system's sampling period, and the parameter adjustment time is about 20 ms.

Due to the fact that the control parameters in digital control vary by step size, continuous changes cannot be achieved as in analog circuits. This will inevitably bring errors and affect the control accuracy of the system. Taking into account factors, such as clock frequency and switching frequency, 500 points were set for the ac component of d_a to be taken within one sinusoidal period when programming, with a corresponding step size of 0.72° for parameter β_2. According to (8) and (9), the phase adjustment step size $\Delta\varphi_1$ and amplitude adjustment step size ΔU_{om} generated by the changes in control parameters k_0, k_2, and β_2 are given as follows:

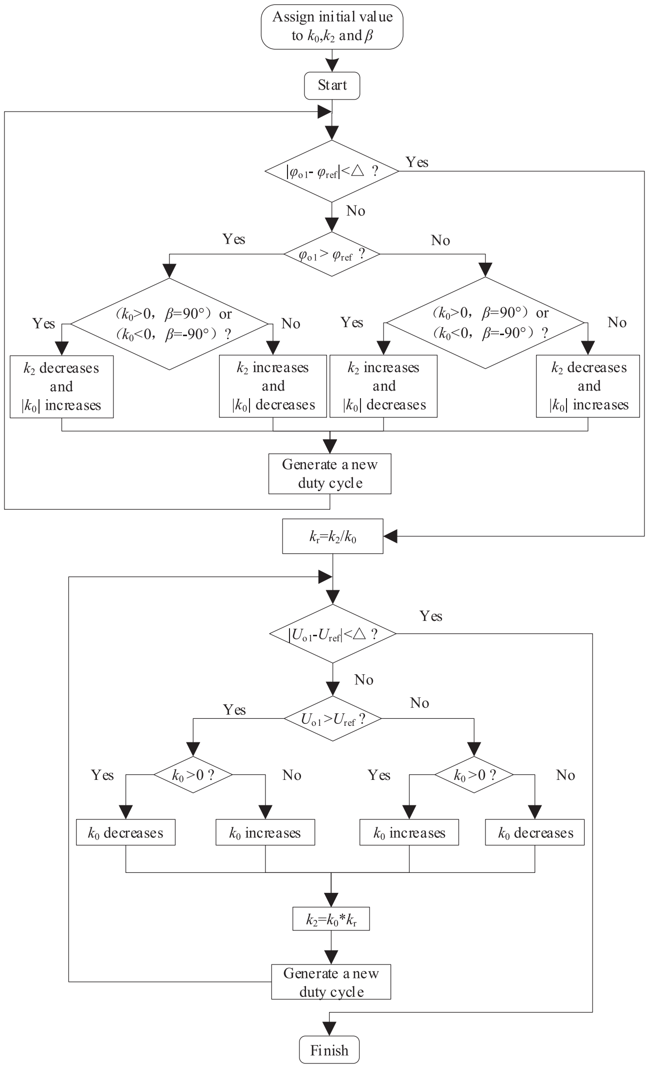


Fig. 16. Closed-loop logic flowchart.

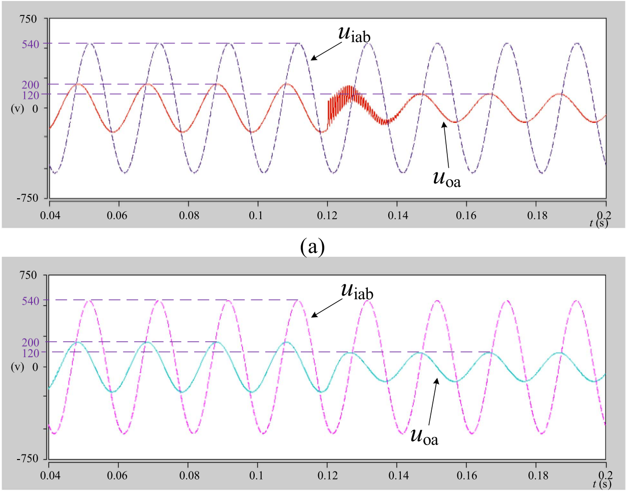
$$\begin{cases} \Delta\varphi_1 = \frac{\partial\varphi_1}{\partial k_0}\Delta k_0 + \frac{\partial\varphi_1}{\partial k_2}\Delta k_2 + \frac{\partial\varphi_1}{\partial\beta_2}\Delta\beta_2 \\ \Delta U_{om} = \frac{\partial U_{om}}{\partial k_0}\Delta k_0 + \frac{\partial U_{om}}{\partial k_2}\Delta k_2 + \frac{\partial U_{om}}{\partial\beta_2}\Delta\beta_2. \end{cases} \tag{22}$$

Through control strategies, taking zone I in Fig. 14 as an example, it can be seen that β is always 90°, where $\beta = \beta_2 + 90°$ and can get

$$\begin{cases} \varphi_1 = \arctan\frac{k_2}{2k_0} \\ U_{om} = U_{im}\sqrt{{k_0}^2 + \left(\frac{k_2}{2}\right)^2}. \end{cases} \tag{23}$$

Since the sum of k_0 and k_2 remains constant during the phase closed-loop process, let $k_0 + k_2 = a$, which means $k_2 = a - k_0$, where a is a constant and $0 \le a \le 1$. Then, one can obtain

$$\Delta\varphi_1 = \frac{d\left(\arctan\frac{a-k_0}{2k_0}\right)}{dk_0}\Delta k_0 = -\frac{2a}{4{k_0}^2 + (a-k_0)^2}\Delta k_0. \tag{24}$$



(a)

(b)

Fig. 17. Circuit simulation results. (a) DPFC. (b) F-DPFC.

In this article, Δk_0 and Δk_2 are set to 0.001. Since $0 \leq k_0 \leq a$, when $a = 1$, the range of $d\varphi_1/dk_0$ is [−2.5, −0.5]. Therefore, the range of $|\Delta\varphi_1|$ is [0.0005, 0.0025], that is [0.0286°, 0.1432°]. Similarly, when $a = 0.5$, the range of $|\Delta\varphi_1|$ is [0.001, 0.005], that is [0.0572°, 0.2863°]. When $a = 0.2$, the range of $|\Delta\varphi_1|$ is [0.0025, 0.0125], that is [0.143°, 0.716°]. From (24), it can be seen that, as the value of a increases, where $0 \leq a \leq 1$, the precision of the phase-locked loop control also increases. Since $a > 0.2$ in most operating conditions, setting $\Delta k_0 = 0.001$ and $\Delta k_2 = 0.001$ can meet the requirement of the system's phase closed-loop control.

From the control strategy, it can be seen that, in the amplitude closed-loop process, when adjusting k_0, the ratio of k_0 to k_2 remains constant and k_0 is larger than k_2. Therefore, let $k_2 = bk_0$, where $0 \leq k_0 \leq 1$, b is a constant and $0 < b < 1$. Then, one can obtain

$$\Delta U_{om} = \frac{d\left(U_{im}\sqrt{{k_0}^2 + \frac{b^2{k_0}^2}{4}}\right)}{dk_0}\Delta k_0 = U_{im}\sqrt{1 + \frac{b^2}{4}}\Delta k_0. \tag{25}$$

Therefore, the range of ΔU_{om} is about ($0.001U_{im}$, $0.0011U_{im}$). Similarly, when adjusting k_2, the value of k_2 is larger than k_0 and the range of ΔU_{om} is same.

It can be seen that setting Δk_0 and Δk_2 to 0.001 can meet the requirements of experimental accuracy.

D. Comparison of F-DPFC and DPFC

To demonstrate the superiority of F-DPFC over DPFC, a set of circuit simulation comparative experiments was conducted. Among them, the original power grid line voltage u_{iab} is 540 V, and T_i and T_o are of Δ/Yn11-type connection group with turn ratio of 1. The simulation result is shown in Fig. 17. Before 0.12 s, the amplitude of the output compensation voltage u_{oa} of both F-DPFC and DPFC is 200 V, and the phase is leading u_{iab} by 60°. After 0.12 s, the amplitude of the output compensation voltage u_{oa} of both F-DPFC and DPFC is adjusted to 120 V, and the phase is leading u_{iab} by 90°. Since DPFC can only adjust the phase of the output compensation voltage within the range of 0°–60° when T_i and T_o are of Δ/Yn11 type, it can only change the combination of the selection switches to achieve the above-mentioned change of u_{oa}. This leads to the disturbance of DPFC in Fig. 17(a) at 0.12 s, while F-DPFC can be achieved by adjusting parameters without such disturbance, as shown in Fig. 17(b). It can be seen that, compared with DPFC, F-DPFC can continuously and smoothly adjust the compensation voltage within the range of 360°, which is more conducive to the stability of energy transmission in the power grid.

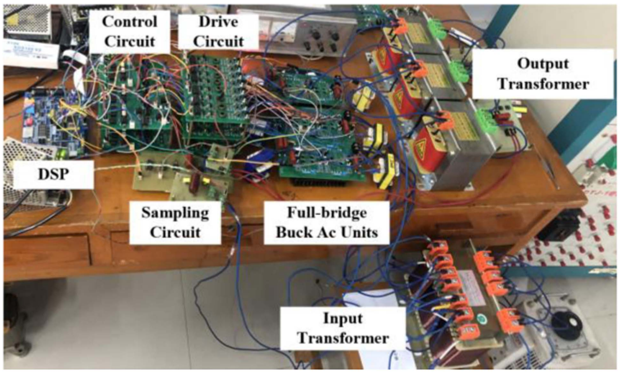


Fig. 18. F-DPFC prototype.

TABLE II
EXPERIMENTAL SPECIFICATIONS

Specification	Value
Amplitude of original grid line voltage: U_{imL}	$200\sqrt{2}$ V
Frequency of grid voltage: f	50 Hz
Switching frequency: f_s	25 kHz
Turn ratio of the input transformer T_i: N_i	200/70
Turn ratio of the output transformer T_o: N_o	220/127
Output filter inductance: L_{fa}=L_{fb}=L_{fc}	0.66 mH
Output filter capacitor: C_{fa}=C_{fb}=C_{fc}	4.4 μF
Switch device	IRFP460A
DSP IC	TMS320F2812

IV. EXPERIMENTAL RESULTS

In order to verify the correctness of the working principle and the feasibility of the closed-loop control strategy, the lower power prototype (considering the experimental purpose and conditions), as shown in Fig. 18, is established. T_i and T_o are of Δ/Yn11-type connection group. To observe the third harmonic voltage, a small capacitor is connected in parallel at the output of each full-bridge-type ac unit. Table II lists its specifications.

To verify that the output compensation voltage of F-DPFC can be adjusted within a 360° range, four sets of experiments were conducted with output compensation voltage phases within (0°, 90°), (90°, 180°), (180°, 270°), and (270°, 360°), corresponding to zones I, II, III, and IV, respectively. The experimental results are as follows.

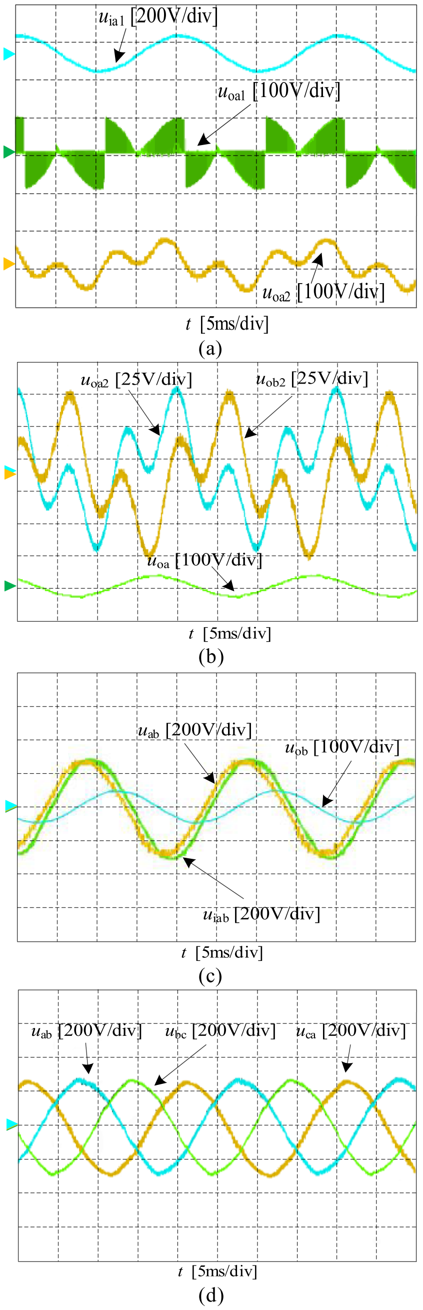


Fig. 19. Experimental waveforms of F-DPFC in zone I when $k_0 = 0.32$, $k_2 = 0.58$, and $\beta = 90°$. (a) u_{ia1}, u_{oa1}, and u_{oa2}. (b) u_{oa2}, u_{ob2}, and u_{oa}. (c) u_{ab}, u_{iab}, and u_{ob}. (d) u_{ab}, u_{bc}, and u_{ca}.

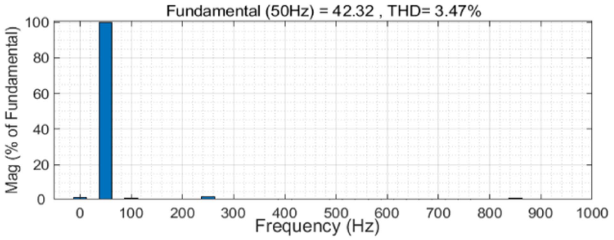


Fig. 20. Fast Fourier transform (FFT) analysis of u_{oa} when $k_0 = 0.32$, $k_2 = 0.58$, and $\beta = 90°$.

In zone I, theoretical analysis shows that $0 < k_0 < 1, 0 < k_2 < 1$, and $\beta = 90°$. Therefore, let parameters $k_0 = 0.32$, $k_2 = 0.58$, and $\beta = 90°$, and Fig. 19 shows the experimental waveforms of F-DPFC.

The input voltage u_{ia1} and output voltages u_{oa1} (between point E_1 and point F in Fig. 3) and u_{oa2} (between point A_3 and point F in Fig. 3) of A-phase buck ac unit in F-DPFC are shown in Fig. 19(a). Among them, u_{ia1} is modulated by the A-phase buck ac unit with a duty cycle of d_a. u_{oa1} is a high-frequency pulse sequence, and u_{ia1} is its amplitude envelope curve. Most of the high-frequency components of u_{oa1} are filtered by L_{fa} to obtain u_{oa2}. u_{oa2} has not only the fundamental voltage component but also the third harmonic voltage component and a small number of high-frequency components.

The experimental waveforms of voltages u_{oa2} and u_{ob2}, which include the third harmonic components and fundamental components, and the voltage u_{oa}, the compensated output voltage of A-phase, are shown in Fig. 19(b). The phase difference between u_{oa2} and u_{ob2} is 120°, where the third harmonic component is the same and the fundamental component phase difference is 120°. Therefore, by offsetting the third harmonic, the output compensation voltage u_{oa} can be obtained, where $u_{oa} = N_o(u_{oa2} - u_{ob2})$.

The experimental waveforms of the original grid line voltage u_{iab}, B-phase output compensation voltage u_{ob}, and the regulated grid line voltage u_{ab} are shown in Fig. 19(c). One knows that $u_{ab} = u_{iab} + u_{oa} - u_{ob}$. With the help of Code Composer Studio Software and DSP simulator, it is easy to observe variables. As can be measured from Fig. 19(c), u_{ob} lags the u_{iab} by 48.1°. We can get that u_{oa} leads the u_{ia1} by 71.9°, as u_{oa} leading u_{ob} by 120°, and u_{ia1} and u_{iab} having the same phase. The amplitude of u_{ia1} is 99.3 V, while the amplitude of u_{oa} is 43.8 V, which is 0.440 times that of u_{ia1}. The calculated values should be 72.2° and 0.432. u_{ab} leads u_{iab} by 9.6°, with an amplitude of 270.6 V. The measured value is close to the calculated value of 9.01° and 273.8 V. We can see that under the open-loop control, the difference between the measured value and the calculated value is very small.

The experimental waveforms of regulated grid line voltages u_{ab}, u_{bc}, and u_{ca}, where $u_{ab} = u_{iab} + u_{oa} - u_{ob}$, $u_{bc} = u_{ibc} + u_{ob} - u_{oc}$, and $u_{ca} = u_{ica} + u_{oc} - u_{oa}$, are shown in Fig. 19(d), and the amplitude of u_{ab}, u_{bc}, and u_{ca} is 270.6 V. u_{iab} is compensated by u_{oa} and u_{ob} to obtain u_{ab}. u_{ab} and u_{iab} have different phases and amplitudes. u_{ab}, u_{bc}, and u_{ca} have a phase difference of 120° and are positive-sequence symmetric. In general, the original grid line voltages u_{iab}, u_{ibc}, and u_{ica} are symmetrical, which obviously mean that compensation phase voltages u_{oa}, u_{ob}, and u_{oc} must be symmetrical. Fig. 20 shows the voltage u_{oa} range for the first 20 harmonics when $k_0 = 0.32$, $k_2 = 0.58$, and $\beta = 90°$, and the THD of u_{oa} is 3.47%.

The experimental waveforms of regulated grid line voltages u_{ab}, u_{bc}, and u_{ca}, where $u_{ab} = u_{iab} + u_{oa} - u_{ob}$, $u_{bc} = u_{ibc} + u_{ob} - u_{oc}$, and $u_{ca} = u_{ica} + u_{oc} - u_{oa}$, are shown in Fig. 19(d), and the amplitude of u_{ab}, u_{bc}, and u_{ca} is 270.6 V. u_{iab} is compensated by u_{oa} and u_{ob} to obtain u_{ab}. u_{ab} and u_{iab} have different phases and amplitudes. u_{ab}, u_{bc}, and u_{ca} have a phase difference of 120°

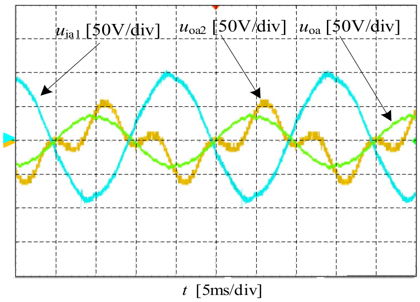


Fig. 21. Experimental waveforms of F-DPFC in zone II when $k_0 = -0.33$, $k_2 = 0.50$, and $\beta = 90°$.

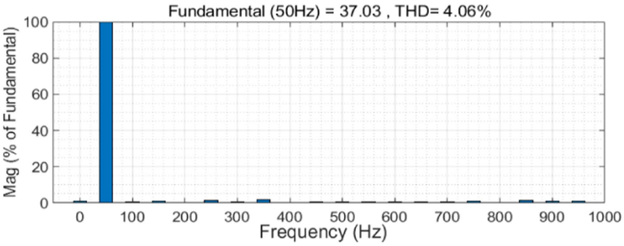


Fig. 22. FFT analysis of u_{oa} when $k_0 = -0.33$, $k_2 = 0.50$, and $\beta = 90°$.

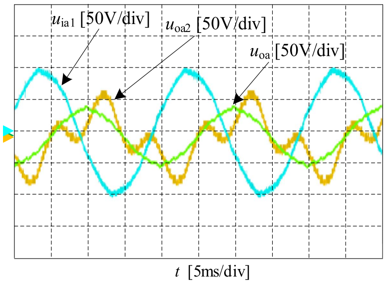


Fig. 23. Experimental waveforms of F-DPFC in zone III when $k_0 = -0.36$, $k_2 = 0.58$, and $\beta = -90°$.

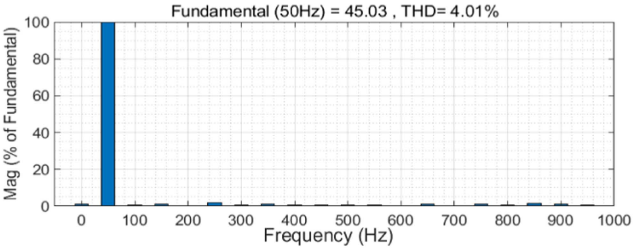


Fig. 24. FFT analysis of u_{oa} when $k_0 = -0.36$, $k_2 = 0.58$, and $\beta = -90°$.

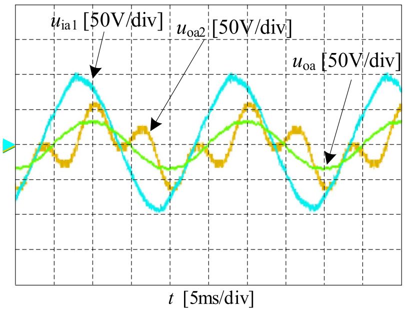


Fig. 25. Experimental waveforms of F-DPFC in zone IV when $k_0 = 0.21$, $k_2 = 0.58$, and $\beta = -90°$.

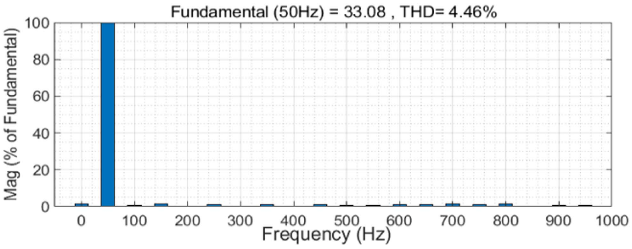


Fig. 26. FFT analysis of u_{oa} when $k_0 = 0.21$, $k_2 = 0.58$, and $\beta = -90°$.

and are positive-sequence symmetric. In general, the original grid line voltages u_{iab}, u_{ibc}, and u_{ica} are symmetrical, which obviously mean that compensation phase voltages u_{oa}, u_{ob}, and u_{oc} must be symmetrical. Fig. 20 shows the voltage u_{oa} range for the first 20 harmonics when $k_0 = 0.32$, $k_2 = 0.58$, and $\beta = 90°$, and the THD of u_{oa} is 3.47%.

In zone II, theoretical analysis shows that $-1 < k_0 < 0$, $0 < k_2 < 1$, and $\beta = 90°$. Therefore, let parameters $k_0 = -0.33$, $k_2 = 0.50$, and $\beta = 90°$, and the experimental waveforms of u_{ia1}, u_{oa2}, and u_{oa} are shown in Fig. 21. The u_{oa} leads u_{ia1} by 173.8° and the amplitudes of u_{ia1} and u_{oa} are 94.9 V and 39.7 V, respectively. The calculated values of u_{oa} are 172.9° and 39.2 V, which are basically the same as the measured values. Fig. 22 shows the voltage range u_{oa} for the first 20 harmonics when $k_0 = -0.33$, $k_2 = 0.50$, and $\beta = 90°$, and the THD of u_{oa} is 4.06%.

In zone III, theoretical analysis shows that $-1 < k_0 < 0$, $0 < k_2 < 1$, and $\beta = -90°$. Therefore, let parameters $k_0 = -0.36$, $k_2 = 0.58$, and $\beta = -90°$, and the experimental waveforms of u_{ia1}, u_{oa2}, and u_{oa} are shown in Fig. 23. The u_{oa} lags u_{ia1} by 112.5° and the amplitudes of u_{ia1} and u_{oa} are 99.3 V and 46.8 V, respectively. The calculated values of u_{oa} are 111.1° and 45.9 V, which are basically the same as the measured values. Fig. 24 shows the voltage range u_{oa} for the first 20 harmonics when $k_0 = -0.36$, $k_2 = 0.58$, and $\beta = -90°$, and the THD of u_{oa} is 4.01%.

In zone IV, theoretical analysis shows that $0 < k_0 < 1$, $0 < k_2 < 1$, and $\beta = -90°$. Therefore, let parameters $k_0 = 0.21$, $k_2 = 0.58$, and $\beta = -90°$, and the experimental waveforms of u_{ia1}, u_{oa2}, and u_{oa} are shown in Fig. 25. The u_{oa} lags u_{ia1} by 24.8° and the amplitudes of u_{ia1} and u_{oa} are 96.9 V and 34.7 V, respectively. The calculated values of u_{oa} are 24.1° and 35.8 V, which are basically the same as the measured values. Fig. 26 shows the voltage range u_{oa} for the first 20 harmonics when $k_0 = 0.21$, $k_2 = 0.58$, and $\beta = -90°$, and the THD of u_{oa} is 4.46%.

On the basis of the above experiments, another four groups of experiments were carried out. The experimental results are shown in Table III, where φ_1 represents the phase angle of u_{oa} leading u_{ia1} and k_a represents the ratio of the amplitude of u_{oa} to

TABLE III
EXPERIMENTAL RESULTS

Parameter settings			Calculated		Measured(*)	
k_0	k_2	β	φ_1	k_a	φ_1*	k_a*
0.64	0	90°	30.0°	0.64	29.8°	0.637
0.32	0.58	90°	72.2°	0.432	71.9°	0.440
0	0.8	90°	120°	0.4	120.1°	0.396
−0.33	0.50	90°	172.9°	0.413	173.8°	0.418
−0.64	0.14	−90°	−143.7°	0.634	−144.6°	0.629
−0.36	0.58	−90°	−111.1°	0.462	−112.5°	0.471
0.07	0.85	−90°	−50.6°	0.431	−50.1°	0.434
0.21	0.58	−90°	−24.1°	0.369	−24.8°	0.358

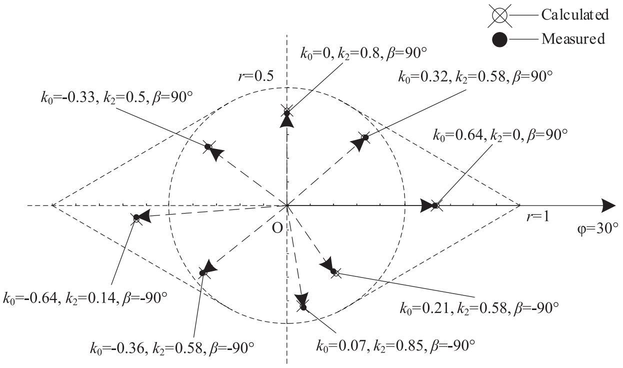
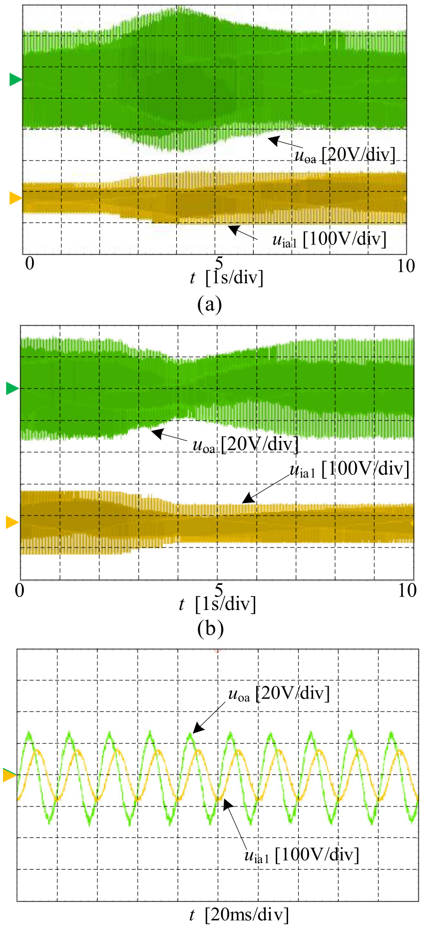


Fig. 27. Experimental results and calculated results.

u_{ia1}. In order to present the experimental results more clearly, all eight sets of data are displayed within the compensation voltage adjustment range, as shown in Fig. 27, and it should be noted that the initial phase of the polar axis is 30°. It can be seen that the error between the measured value and the calculated value is very small.

The closed-loop control strategy of the system is verified below. In order to stabilize the closed-loop control quickly and reduce the oscillation caused by the excessive change of the control parameters, the initial control parameters of the closed-loop control should be consistent with the open-loop control parameters under ideal conditions. In this experiment, an autotransformer is used to change the amplitude of u_{ia1} to simulate the input voltage disturbance to confirm the feasibility of the closed-loop control strategy. The experimental results are shown in Fig. 28. Let the amplitude of u_{oa} and the phase angle of u_{oa} leading u_{ia1} be 32 V and 75°.

As shown in Fig. 28(a), F-DPFC is in a steady state within the range of 0–2 s, the amplitude of u_{ia1} and u_{oa} are 49.5 V and 31.8 V, respectively. Within the range of 2–4 s, the amplitude of u_{ia1} is increased to 80.3 V, and the amplitude of u_{oa} is also increased. F-DPFC performs the closed-loop parameter adjustment and enters steady state after 7 s, at which time the amplitude of u_{oa} is measured to be 31.7 V. As can be seen from Fig. 28(b), F-DPFC can still adjust parameters to achieve amplitude closed-loop control when the input voltage is reduced. In Fig. 28(c), u_{oa} always leads u_{ia1} by 75° during the closed-loop regulation. Therefore, the closed-loop control strategy is feasible.



(a)

(b)

(c)

Fig. 28. Closed-loop experimental waveform of F-DPFC. (a) u_{ia1} and u_{oa}. (b) u_{ia1} and u_{oa}. (c) u_{ia1} and u_{oa}.

Considering the purpose of the experiment and the existing equipment conditions, the experiment was conducted at a low-voltage level. If the application is to be extended to high-voltage conditions, this can be achieved not only through modular expansion but also by increasing the voltage withstand level of semiconductor devices. In addition, considerations must be given to the cooling system, electromagnetic compatibility, insulation, and other designs. In addition, as the switching frequency increases, it leads to an increase in power loss and a decrease in efficiency. Therefore, in specific design, it is necessary to select appropriate components based on frequency requirements to balance power consumption and performance requirements.

It can be seen that the experimental results are basically consistent with the theoretical analysis, which verifies the correctness and feasibility of the theory in this article.

V. CONCLUSION

In this article, a new concept called DPFC with continuous full regulation range (F-DPFC) was proposed. F-DPFC inherits the advantages of DPFC and UPFC and can achieve the regulation of active and reactive power flow in the power grid. F-DPFC simplifies the structure of DPFC and achieves full range continuous regulation. Compared with UPFC, F-DPFC has only one-stage conversion circuit and low maintenance cost because dc energy storage elements are not contained. The structure of F-DPFC is simple to achieve modular expansion and enables it to operate under high-voltage and power conditions. The operational principle and control strategy of F-DPFC were presented and analyzed in detail, and the prototype and experimental results verify the correctness and feasibility of the concept of F-DPFC.

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