# Design of High-Efficiency Microwatt RF Energy Harvesting System

Lanyu Li and Yanfeng Jiang, *Senior Member, IEEE*

***Abstract*—A radio frequency energy harvesting (RFEH) system can harvest and utilize radio frequency (RF) energy in the natural environment. The fully integrated circuit of the RFEH system with the ultralow power consumption is designed and implemented in this article, including the receiving antenna, matching circuit, RF-dc rectifier circuit, and power management unit. The key parameters are calculated and simulated, and the power consumption model of the system is established. Optimization of the power consumption is conducted. The overall power conversion efficiency of the microwatt-level RFEH system is 31.77%, which has potential application in fields, such as wireless energy transmission and portable device power supply. The circuit is designed and implemented based on Taiwan semiconductor manufacturing company limited (TSMC) CMOS 0.18-$\mu$m technology.**

***Index Terms*—Power conversion efficiency (PCE), power management unit (PMU), radio frequency energy harvesting (RFEH), receiving antenna, RF-dc rectifier.**

## I. Introduction

RADIO frequency (RF) energy harvesting technology can convert radio signals in the surrounding environment into the harvested electrical energy. At present, research on radio frequency energy harvesting (RFEH) system has made significant progress [1]. Based on the electromagnetic induction of radio waves, the RFEH system receives radio signals and converts them into dc power. The research on the RFEH system includes antenna design, energy conversion circuit design, energy management, and power transmission [2].

In recent years, RFEH technology has undergone rapid development, with obvious improvements in the energy level and the harvesting efficiency. Nowadays, RFEH system can be commonly used for self-powered low-power device and wireless sensor node. In [3], the RFEH system can provide dc current for wireless Internet of Things (IoT) devices. Installing infrared sensors on IoT sensing nodes, such as smart homes, can automatically control the switch of corridor light [4]. Sensor nodes applied to human LAN can assist in monitoring health status and predicting disease occurrence [5]. In [6], the RFEH system is used in power implanted biomedical devices, eliminating the need for frequent battery replacement surgeries and alleviating patient pain. The RFEH system can also be used to collect data, such as temperature, mineral content, and soil moisture. In [7], the receiving antenna, smart meter, and LCD display are connected and powered by the wireless RFEH system. The RFEH technology is also involved in the applications of optical detectors, remote base station weather prediction, and military monitoring.

Efforts have been reported to design a fully integrated RFEH system [8], [9], [10], [11]. Currently, there are some works on the adoption of multiband RFEH, which is considered as a promising solution to improve the practicality and efficiency of the harvesting system [8], [12], [13], [14], [15]. Current state-of-the-art multiband RFEH adopting CMOS technology requires the integration of nonmonolithic aids, such as transmission line impedance matching network and antenna codesign to match the RF-dc rectifier [8], [12], [13], [14], [15]. A fully integrated solution is desirable without constraints in the reliance on external components. In this article, to investigate the fully integrated solution, a single-band RFEH system, which can be fully integrated, is designed and implemented.

For the application of RF harvesting systems, it tends to be developed toward smaller and lighter with more multifunctional. Antenna is moving from external to internal and very sensitive to size and function. For antennas to satisfy the requirements of the current market, they must be compact with smaller size. High-performing antennas with simple structures are focused. One candidate is the planar inverted-F antenna (PIFA). A PIFA is composed of a ground plane, radiation plane, feed line, and short pin. Because it operates at a resonant length of $\lambda/4$, it is highly conductive to a small and lightweight design, and thus well suited for use as an internal antenna [16], [17].

In the designed RFEH system, the matching circuit is necessary for circuit startup and maximum power transmission. An impedance transformation network that converts the input impedance of the antenna into the matching impedance of the rectifier for the maximum power transmission is required. A shunt-inductor power-matching network between the antenna and the voltage rectifier is employed to resonate out the capacitive part of the input impedance of the antenna. At the same time, the impedance imaginary part coefficients of the antenna and the rectifier circuit can be adjusted accordingly [18], [19].

There are different types of matching networks, such as L-network [11], transformer matching network [18], and

Manuscript received 28 September 2023; revised 28 December 2023; accepted 20 January 2024. Date of publication 29 January 2024; date of current version 20 March 2024. This work was supported in part by Leading Technology Pre-Research Project (XD23008, Wuxi Industrial Innovation Research Institute and Jiangsu JITRI IC Application Technology Innovation Center), in part by the National Natural Science Foundation of China under Grant 61774078, and in part by the Natural Science Foundation of Jiangsu Province (BK20210453). Recommended for publication by Associate Editor S. K. Panda. *(Corresponding author: Yanfeng Jiang.)*

The authors are with the Department of Electrical Engineering, Advanced Technology Institute, Jiangnan University, Wuxi 214122, China (e-mail: 6201922007@stu.jiangnan.edu.cn; jiangyf@jiangnan.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3359973.

Digital Object Identifier 10.1109/TPEL.2024.3359973

Chebyshev matching network [20]. The Chebyshev network can provide wideband matching but increases parasitic losses due to a larger number of passive components [20], [21]. The transformer matching provides compact sizing but requires a large turn ratio and high mutual inductance [18]. The L-network offers a more compact size with fewer passive components, reducing parasitic losses. It also has a straightforward design process [13], [19], [22], [23], [24], [25], [26], [27], [28]. The performance of the receiving antenna in the RFEH system is crucial. High gain and miniaturized antennae are highly required by the RFEH system. The RF signal is very low, stochastically scattered across multiple frequency bands. The tradeoff between the high gain and miniaturization is quite challenging. In this article, an L-type high-pass matching circuit is adopted in the system. The relevant design is shown in Section III.

The performance of the rectifier circuit in the RFEH system is important. The RF-dc rectifier circuit should have low-threshold loss, high output voltage, and high-power conversion efficiency (PCE) performance. In order to reduce the threshold voltage of the rectifier device, the external power source is always needed [29]. To get rid of the external power, a number of threshold voltage compensation techniques for the rectifier have been proposed in order to increase the efficiency of the RF energy harvesters. Schottky diodes [29] or HSMS diodes [30] are used to implement the rectifier circuit. The drawbacks of these techniques are high cost caused by the additional fabrication steps and integration with the standard CMOS-integrated circuits. The active threshold voltage compensation method proposed in [31] requires an external battery, which is inconvenient for application or maintenance. The scheme proposed in [32] uses auxiliary transistors to control the gate-source voltage of the rectifying devices. A differential dual-path CMOS rectifier described in [33] employs an adaptive control circuit to control both high-power path and low-power path over extending input power range. However, the power efficiency is always degraded by the parasitic capacitances of the multiple paths. A hybrid threshold voltage employs P-channel metal-oxide-semiconductor (PMOS) transistors as rectifying devices in rectifier's stages except in the first stage in order to eliminate the need of N-channel metal-oxide-semiconductor (NMOS) triple-well transistors [34]. A dual-band rectifier is reported in [35] to implement an internal threshold voltage compensation technique. A differential cross-coupled rectifier [36] can compensate the threshold voltage of the rectifying devices and suppress the leakage current. A self-biasing circuit in [37] provides dc biasing voltage by using an off-chip impedance resistive network.

In order to improve the output voltage level of RF-dc voltage doubling rectifier circuit, several or even dozens of stages of rectifier circuit structure are usually required. However, external power supply and multilevel structure could increase the reverse leakage current of the rectifier device, causing a decrease in PCE. In this article, a novel synchronous self-threshold voltage doubling rectifier circuit is proposed, showing high power efficiency and high output voltage. The details are listed in Section V.

Based on the designed RFEH system, an appropriate voltage should be provided as the power supply for the IoTs system, in which specific voltages are required for the microcontrollers, sensors, and wireless communication modules. In this sense, voltage limiting is required in RFEH system to ensure the long-term reliability of the circuit [38], [39], [40]. Valenta and Durgin [30] show achievements on triband ambient RF energy harvesting system. In the proposed system, the voltage monitor with a novel structure is proposed, with the merits of ultralow power consumption ($<0.021\ \mu$W) and small layout area ($0.37\ \text{mm}^2$). It shows potential applications in IoTs' systems.

In this article, the hysteresis control circuit combined with low dropout (LDO) is adopted for the voltage divider. One of the benefits of the hysteresis control is that it can provide high-voltage protection. At the same time, the limiting voltage can be adjusted for various applications by varying the divider ratio. The LDO regulator is designed in this article to filter out the ripple and provide a stable output voltage for external loading.

For the ultralow power operation system, self-start of the RFEH system is one of the prerequisites for design. At the microwatt power level, the system's operating voltage is at a very low level. However, if the input power is nonsufficient, the circuit cannot be operated successfully. Therefore, it is necessary to reduce the startup threshold of the RFEH system and reduce system power loss. The so-called "cold-start" technology is adopted in the RFEH system for reliable start-up operation with low-level power [41]. Recently, a ring oscillator-based cold-start system has aroused much interest in the energy harvesting system. Because of the delicate power supply characteristics and the vulnerability to MOS device noise, the ring oscillator for the cold start is studied intensively.

In order to smooth the vibration of the ring oscillator and make it suitable for the integration in the standard CMOS technology, researchers attempted to use intrinsic transistors to construct the oscillator [41]. In 2015, Ashraf and Masoumi [42] proposed a complete energy harvesting power supply for implantable pacemakers. A forward body bias strategy was used to reduce the startup voltage of the ring oscillator, allowing the circuit to be started at 60 mV. However, the ring oscillator cannot be operated on the process corners. Dezyani et al. [43] proposed a new process-tolerant inverter unit for the ring oscillator. This method does not need postfabrication or trimming, and is compatible with the standard CMOS technology. With an input voltage as low as 60 mV, the harvesting system can be operated with 4.5-$\mu$W output power. Bose and Johnston [44] proposed a modified ring oscillator architecture with triple-stacked inverter delay elements, in which the oscillator can be started as low as 50 mV.

A fully integrated RFEH system is designed in this article.

The rest of this article is organized as follows. Section II describes the structure of the proposed RFEH system and the functions of each module. Section III introduces the receiving antenna and the matching circuit. Section IV provides the circuit of synchronous self-threshold compensation voltage doubling rectifier circuit. Section V introduces the designed power management unit (PMU) for maximum power transmission. Finally, Section VI concludes this article.

## II. Proposed RFEH System

Fig. 1 illustrates the overall structure diagram of the RFEH system, showing the specific energy conversion process of RF-dc

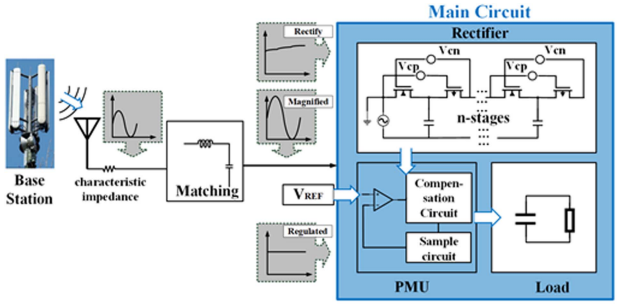



Fig. 1. Schematic of the RFEH system.

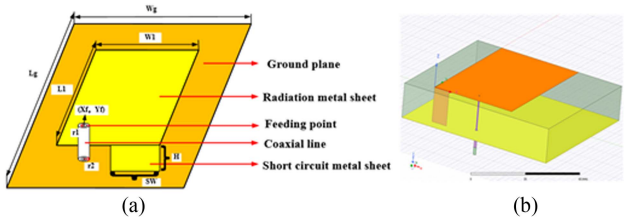



Fig. 2. Structure of the proposed PIFA. (a) Theoretical model. (b) HFSS model.

and the output voltage waveforms of the key nodes. The whole system is divided into five parts, including the receiving antenna, the matching circuit, the rectifier, the PMU, and the subsequent energy storage application module.

As shown in Fig. 1, the antenna can be used to collect RF energy in the environment. The harvested RF signal would be transmitted into the matching circuit for the impedance transformation. The matching circuit can ensure the maximum power transmission between the receiving antenna and the rectifier circuit, minimizing transmission loss as much as possible. The rectifier circuit can convert the ac signal into dc signal, where performance directly determines the efficiency and the sensitivity of the system. The electrical signal from the rectifier circuit is stabilized by the energy management unit (PMU) to achieve end-to-end maximum power transmission. Finally, the transmitted energy is stored or directly supplied to the application load.

There are four main parameters to evaluate the performance of the RFEH system, including the PCE, the sensitivity, the dynamic range of input signal, and the output voltage. This article focuses on optimizing the PCE of the RFEH system. PCE is generally defined as the ratio of output dc power ($P_{\mathrm{OUT}}$) to input RF power ($P_{\mathrm{IN}}$). In this article, the overall PCE is determined by the product of the antenna efficiency $\mathrm{PCE}_{\mathrm{an}}$, the rectification circuit efficiency $\mathrm{PCE}_{\mathrm{rec}}$, the matching circuit efficiency $\mathrm{PCE}_m$, and the PMU efficiency $\mathrm{PCE}_p$

$$\mathrm{PCE} = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}} = \mathrm{PCE}_{\mathrm{an}} \times \mathrm{PCE}_{\mathrm{rec}} \times \mathrm{PCE}_m \times \mathrm{PCE}_p. \quad (1)$$

## III. Receiving Antenna and Matching Circuit

### A. Receiving Antenna

The PIFA shows the merits of high gain, high efficiency, and small size, which is commonly used as the receiving antenna in the global system for mobile communication (GSM) 900 band. The PIFA is an improved microstrip rectangular antenna [45], with its basic structure, as shown in Fig. 2. The meanings of the key parameters are listed in Table I.

As shown in Fig. 2, the radiating metal sheet is parallel to the grounding plane (reflecting surface), while they are short connected by the short-circuit metal sheet. The purpose of the short-circuit metal sheet is to reduce the sensitivity of the antenna to ground so that the PIFA antenna can be resonated at $\lambda/4$ points for better load matching. The coaxial feeding is used in the PIFA antenna. The feeding point of the coaxial line is determined by the impedance matching of the subsequent rectification circuit.

TABLE I
Lists of Key Parameters of PIFA Antenna

| Parameters | Parameter Meaning |
|---|---|
| H | Height |
| $L_1$ | Radiant metal sheet length |
| $W_1$ | Radiant metal sheet width |
| $X_g$ | X coordinate of the vertex of the grounding plane |
| $Y_g$ | Y coordinate of the vertex of the grounding plane |
| $L_g$ | Length of grounding plane |
| $W_g$ | Width of grounding plane |
| $X_f$ | X-axis center coordinates of the coaxial line |
| $Y_f$ | Y-axis center coordinates of the coaxial line |
| $X_s$ | Distance from short-circuit metal sheet to the upper edge of radiation metal sheet |
| SW | Width of short-circuit metal sheet |
| $r_1$ | Inner core radius of coaxial feeder |
| $r_2$ | Coaxial feeder outer diameter |

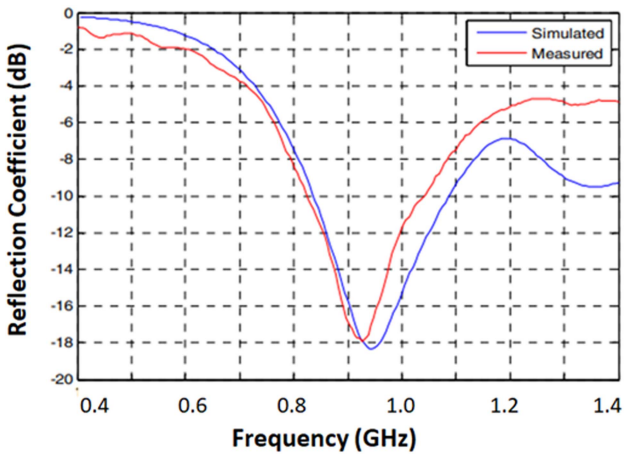



Fig. 3. $S_{11}$ parameter of the PIFA antenna.

The coaxial feeding can achieve the collaborative design of impedance matching circuit and rectification circuit, showing good voltage standing wave ratio (VSWR) parameter results.

The insulating media is added between the radiating metal sheet and the grounding plane. The selection of insulation materials is critical. If the dielectric constant of the insulation layer is high, the size of the PIFA antenna can be reduced. However, the medium with a smaller dielectric constant can generate better radiation.

An optimization process is conducted on the antenna design. Fig. 3 shows the waveform of optimized $S_{11}$ parameters, including the simulation and the measurement results. It shows that $S_{11} = -29$ dB at 900 MHz. The antenna design meets

the bandwidth requirements of GSM 900, with a bandwidth of 130 MHz (840–970 MHz) for $S_{11}<-10$ dB.

The antenna shows the maximum gain of 3.2 dBi vertically above the radiating metal plate ($m1$). The antenna efficiency can be represented by the following equation:

$$\mathrm{PCE_{an}} = \frac{P_o}{P_R} = \frac{P_R - P_r}{P_R} \tag{2}$$

where $P_R$ is the input power, $P_o$ is the antenna output power, and $P_r$ is the power reflected by the antenna. $P_r$ can be calculated by the VSWR coefficient of the antenna, and the ratio $k$ of the reflected voltage to the incident voltage can be determined by VSWR. $k^2$ is the percentage of $P_r$ in $P_R$.

The relationship between $k$ and VSWR is given as follows:

$$\mathrm{VSWR} = \frac{1+k}{1-k}. \tag{3}$$

Based on the simulation results, at the center frequency of 900 MHz, VSWR = 0.6.

With the results of VSWR and (2) and (3), it can be calculated that $k=-1/4$ (The negative value indicates the opposite phase), and the reflected power accounts for 1/16 of the input power. Therefore, the efficiency of the PIFA is $\mathrm{PCE_{an}} = 93\%$. It is necessary to calculate the equivalent collection voltage $V_{\mathrm{RF}}$ of the PIFA antenna to determine the input voltage of the matching circuit and prepare for the design of subsequent circuits. According to (4), the RF power collected by the antenna can be calculated as $P_{\mathrm{in}} = -6$ dBm. The conversion of power values is given as follows:

$$P(\mathrm{dBm}) = 10\mathrm{lg}\left(\frac{P\,(\mu\mathrm{W})}{1\,(\mu\mathrm{W})}\right). \tag{4}$$

It can be concluded that the energy harvested by the antenna is approximately 251 $\mu$W.

Assuming the antenna's reactance $Z_{\mathrm{ant}} = R_{\mathrm{ant}} + jX_{\mathrm{ant}}$, and the input reactance $Z_{\mathrm{in}} = R_{\mathrm{in}} + jX_{\mathrm{in}}$, the equivalent voltage value $V_{\mathrm{RF}}$ can be obtained from the following equation:

$$P_{\mathrm{in}} = \frac{1}{2}\,\mathrm{Re}\left(V_{\mathrm{in}}^{*}\cdot i_{\mathrm{in}}\right) \tag{5}$$

$$P_{\mathrm{in}} = \frac{1}{2}\,\mathrm{Re}\left(\frac{V_{\mathrm{RF}}^2\left(R_{\mathrm{in}} - jX_{\mathrm{in}}\right)}{\left|Z_{\mathrm{ant}} + Z_{\mathrm{in}}\right|^2}\right) \tag{6}$$

$$P_{\mathrm{in}} = \frac{1}{2}\,\frac{V_{\mathrm{RF}}^2\cdot R_{\mathrm{in}}}{\left(R_{\mathrm{ant}} + R_{\mathrm{in}}\right)^2 + \left(X_{\mathrm{ant}} + X_{\mathrm{in}}\right)^2} \tag{7}$$

$$P_{\mathrm{in}} = \frac{V_{\mathrm{RF}}^2}{8R_{\mathrm{in}}}\left(1 - \left|\frac{Z_{\mathrm{in}} - Z_{\mathrm{ant}}^{*}}{Z_{\mathrm{in}} + Z_{\mathrm{ant}}}\right|^2\right) \tag{8}$$

where $V_{\mathrm{in}}$ is the peak voltage at the matching circuit's input, and $i_{\mathrm{in}}$ is the peak current flowing between the antenna and the matching circuit. $V_{\mathrm{RF}}$ is the peak source voltage that would be observed if there is no load on the antenna. With the power available from the antenna being

$$P_{\mathrm{in}} = \frac{V_{\mathrm{RF}}^2}{8R_{\mathrm{in}}} \tag{9}$$

$$V_{\mathrm{RF}} = \sqrt{8{*}R_{\mathrm{in}}{*}P_{\mathrm{in}}} = 300\ \mathrm{mV}. \tag{10}$$

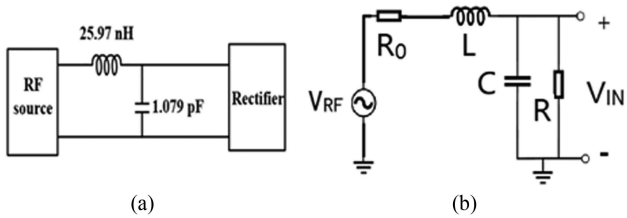



Fig. 4. *LC* matching circuit structure. (a) L-type high-pass matching circuit. (b) Equivalent blocking diagram of the matching circuit.

### B. Matching Circuit

Power matching and gain boosting can be achieved simultaneously by inserting a passive impedance transformation network consisting of a spiral inductor and a metal–insulator–metal capacitor between the antenna and the multiplier, as shown in Fig. 4(a) [18]. The functionality of the impedance transformation network is twofold: First, to provide matching impedance to the antenna in order to maximize the power transmission from the antenna to the rectifier at the carrier frequency, and second, to resonate at the carrier frequency such that the voltage at the output of the impedance transformation network is maximized.

Fig. 4(b) shows the equivalent block diagram of the L-type high-pass matching circuit. In the figure, $R_O = 50\ \Omega$, which is the characteristic impedance of the antenna. $R$ denotes the equivalent input resistance of the rectifier circuit, $L$ and $C$ denote the inductance and capacitance of the matching circuit, $V_{\mathrm{RF}}$ denotes the RF voltage harvested by the antenna, and $V_{\mathrm{IN}}$ denotes the matched input voltage of the rectifier circuit.

The relationship between $V_{\mathrm{RF}}$ and $V_{\mathrm{IN}}$ can be derived by

$$V_{\mathrm{IN}} = V_{\mathrm{RF}}\frac{\frac{1}{j\omega C}\|R}{\frac{1}{j\omega C}\|R + R_O + j\omega L}. \tag{11}$$

Passive amplification is the optimal voltage gain when maximum power transfer occurs, which enhances the sensitivity of the system at the matched desired frequency. To achieve the matching, the impedance of the antenna and the *LC* matching network needs to be in complex conjugate with the rectifier's impedance, when the source and the load resistances are equal, and the imaginary components are conjugate [18]. As shown in Fig. 4(b), the following conditions should be satisfied:

$$R_0 = \frac{\mathrm{R}}{1+\omega^2R^2C^2} \tag{12}$$

$$L = \frac{R^2C}{1+\omega^2R^2C^2}. \tag{13}$$

The Smith impedance chart is shown in Fig. 5(a). Fig. 5(b) shows the simulation and the measurement results of $S_{11}$ parameter. It can be seen that the L-type high-pass matching circuit can make the entire circuit resonance at 900 MHz, achieving the effect of maximum power transmission. After verifying the theoretical values through simulation, the results, as shown in Fig. 6, are obtained. The matched circuit can amplify the small RF signal voltage from 300 mV to 1.04 V, which is greater than the threshold voltage of the rectifier transistor and can be used to start the rectifier circuit effectively.

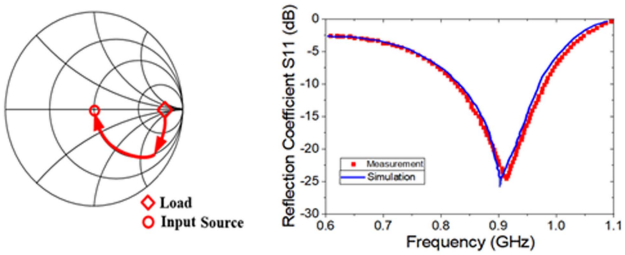



Fig. 5. Simulation and measurement results of the matching circuit. (a) Smith chart. (b) $S_{11}$ parameters, including both simulation and measurement results.

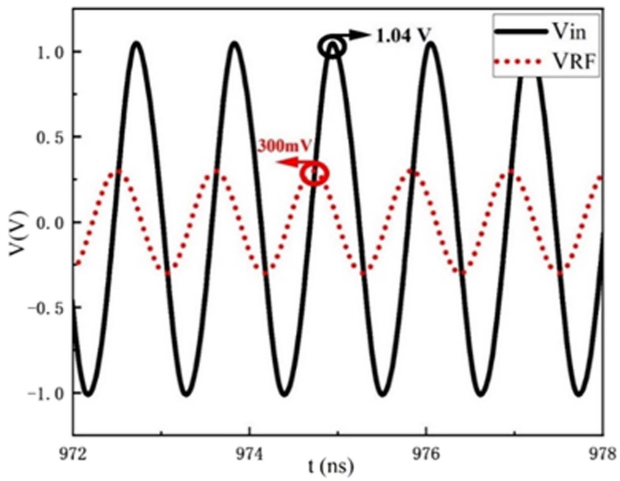



Fig. 6. Signal amplification results of impedance matching circuit.

## IV. Synchronous RF-DC Rectifier

Fig. 7 shows the iterative process of the synchronous threshold compensation RF-dc rectifier circuit [46]. Based on the traditional rectifier, as shown in Fig. 7(a), two voltage adjustable self-threshold compensation modules are provided to compensate NMOS2 and PMOS2 transistors, as shown in Fig. 7(b). The voltage sharing structure enables the circuit to obtain the accurate compensation values under low RF input voltage and power, reducing the equivalent conduction threshold loss of the rectifier circuit. However, the compensation voltage of this structure is obtained by copying $V_c$ from the current mirror. This could cause a sharp increase in reverse leakage current during the sleep duty, which would degrade the PCE.

In order to control the operation time of the threshold voltage compensation, the circuit in Fig. 7(c) is designed with two switches $M_{N2}$ and $M_{P2}$, which control the threshold compensation modules 1 and 2, separately. The periodic operation of the switching transistors can suppress the reverse leakage current of rectifying transistors during nonoperating periods. However, the compensation voltages in the structure are provided by an external supply, affecting the circuit's PCE.

Fig. 7(d) shows the circuit diagram of the proposed synchronous self-threshold compensation RF-dc rectifier circuit [46]. In the structure, no external voltage bias is needed. The input voltage $V_{\rm IN}$ is directly connected with the switching transistor, meaning that the working state of the switch transistor is periodically changed with the input signal. The two rectifying transistors are synchronized with the operation of the switching transistors, effectively reducing reverse leakage current.

The synchronous rectifier can be serially connected in multilevel mode to achieve higher output voltage, as shown in Fig. 7(e). The number of stages in the rectifier circuit is a key parameter for the RF energy harvesting, and the optimal point should be determined to obtain the maximum PCE. As the number of stages of the rectifier circuit increases, the gain of the output dc level and the voltage multiplication reaches the optimal point. In addition, as the number of stages increases, the peak of PCE shifts toward higher power values. In this article, the three-level rectifier circuit is used to provide power for subsequent circuits.

The operating states of the switching transistors and the impacts on the steady-state voltages of the voltage doubling capacitors are summarized in Table II. The input signal is used to control the periodic operation of the switching transistor to generate threshold compensation voltage, to achieve voltage doubling, and to obtain higher voltage with less loss.

The results of the proposed rectifier circuit are shown in Fig. 8. Fig. 8(a) shows the process corner results of the output voltage of the synchronous self-threshold compensation voltage doubling rectifier circuit without load. The output voltage reaches 1.9 V, with the error less than 0.16 V.

The specific parameters should be optimized to achieve the maximum PCE under fixed input power and loads. Fig. 8(b) shows the influences of the load impedances and the input power values on the output voltage. The adopted loads are based on the typical values of RFEH sensor nodes, RFID nodes, and test nodes, with storage capacitors of 10 pF. As shown in Fig. 8(b), the larger the load, the higher the output voltage could be.

The influence of input power and load value on PCE of the rectifier is shown in Fig. 8(c). There is an optimal load value and input power value for the maximized PCE value. With the condition of $P_{\rm in} = -6$ dBm, the PCE is maximized when there is an optimal load of 80 kΩ. Taking into account the peak PCE value and the output voltage, at the fixed input power of −6 dBm, the load impedance is determined to be 80 kΩ, and the load capacitance is 10 pF.

Fig. 8(d) shows the simulation results of the output voltage of four circuits [see Fig. 7(a), (b), (d), and (e)]. Consistent with theoretical analysis, for a fixed load of 80 kΩ, through iterative optimization, the peak output voltage changes from 1.1 V ($V_{\rm out2}$) to 1.4 V ($V_{\rm out4}$), with a voltage ripple range of 0.0021–0.0075 V. The PCE values of the iterative rectifiers are shown in Fig. 8(e).

The reverse leakage current waveform of the rectifier transistor is shown in Fig. 8(f). The leakage current of PMOS2 is greater than 70 $\mu$A, which would deteriorate the circuit efficiency. Compared with the circuit, as shown in Fig. 7(b), the leakage current only occurs during the transient period of reverse input signal change. Therefore, the designed rectifier can suppress the reverse leakage current efficiently, with 16.24 $\mu$A and 15.24 $\mu$A in an alternate manner. During nonoperating time, the rectifier transistor can be considered completely closed.

For the circuit structure, as shown in Fig. 7(d), the compensation voltage simulation results are shown in Fig. 8(f). When the

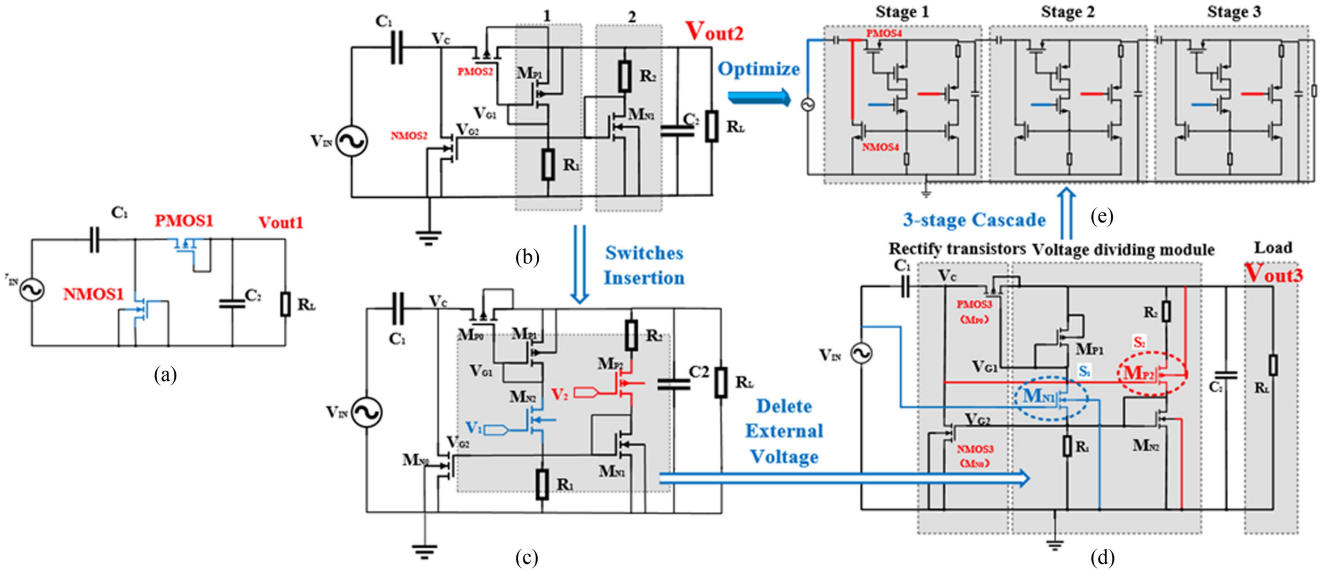



Fig. 7. Proposed rectify circuit with the iterative process. (a) Traditional voltage doubling rectifier circuit. (b) First conceptual design with the dividing resistances. (c) Second improvement with the added external supplied switches. (d) Proposed circuit diagram with the synchronous switching threshold compensation. (e) Three-stage RF-DC rectifier circuit.

TABLE II
MOS SWITCHES AND THEIR EFFECTS ON CAPACITOR VOLTAGE UNDER STEADY STATE

| Switching states | Loop current | $V_C$ | $S_1$ ($M_{N1}$) | $S_2$ ($M_{P2}$) | $C_1$ | $C_2$ | $V_{out3}$ |
|---|---|---|---|---|---|---|---|
| 1 | $I_{in} < 0$ | $V_{IN} - V_{THn}$ | off | on | charging | - | 0 |
| 2 | $I_{in} > 0$ | $2V_{IN} - V_{THn}$ | on | off | discharging | charging | $2V_{IN} - V_{thn} - \lvert V_{thp}\rvert + V_{G1}$ |
| 3 | $I_{in} < 0$ | $V_{IN} - V_{THn}$ | off | on | - | discharging | $2V_{IN} - V_{thn} - \lvert V_{thp}\rvert + V_{G1} + V_{G2}$ |

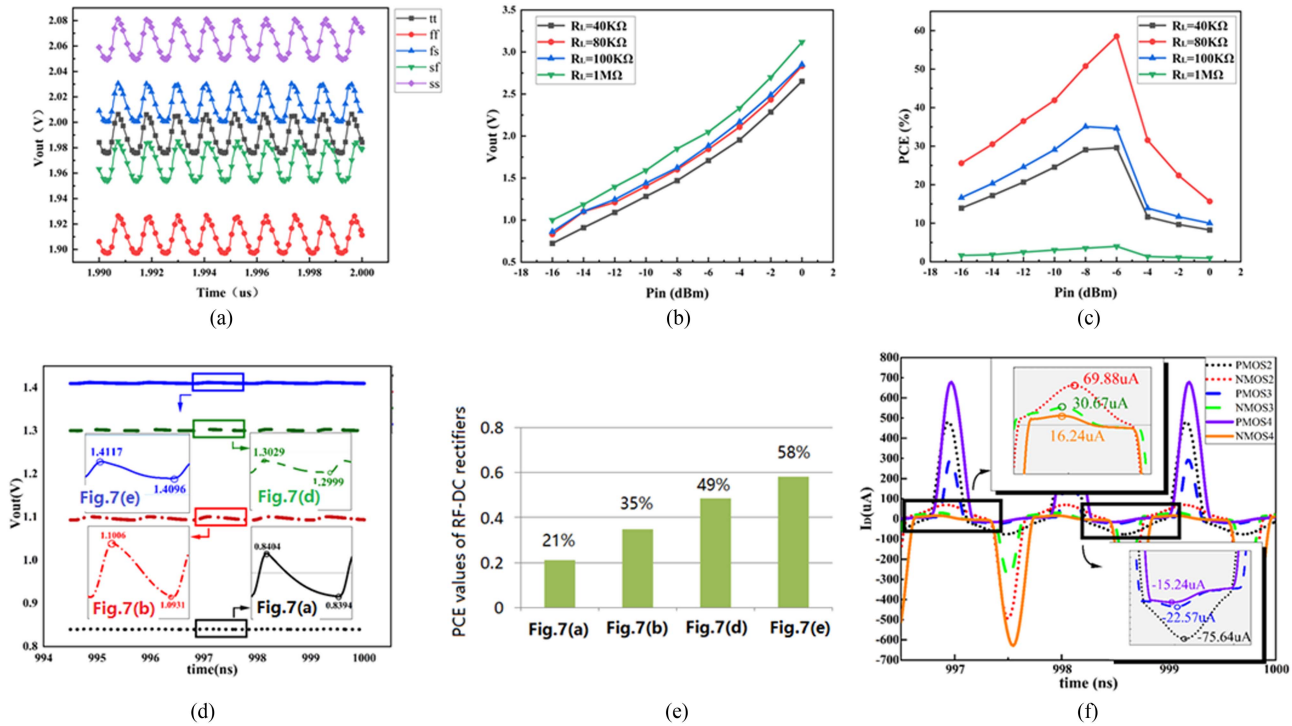



Fig. 8. (a) Process corners simulation of output voltage. (b) Relationship between output voltage $V_{out}$ and input power $P_{in}$. (c) Impact of input power and load resistance on PCE. (d) Four key output voltages. Insets show the zoom-in curves for clear observation. (e) PCE values of the iterative rectifiers. (f) Comparison of the reverse leakage currents of the rectifying transistors. In the figure, PMOS2/NMOS2 in Fig. 7(b), PMOS3/NMOS3 in Fig. 7(d), and PMOS4/NMOS4 in Fig. 7(e).

TABLE III
POWER CONSUMPTION OF THE COMPONENTS IN THE PROPOSED RF-DC RECTIFIER [SEE FIG. 7(D)]

| Components | Power Consumption (μW) |
|---|---|
| $S_1(M_{N1})$ | 2.53 |
| $S_2(M_{P2})$ | 2.41 |
| $C_1$ | 0.5 |
| $C_2$ | 0.5 |
| $R_1$ | 5 |
| $R_2$ | 3 |
| $R_L$ | 24.85 |

input signal is in a negative period, the rectifier transistor $M_{N0}$ is in the operating region, with a threshold voltage of 0.47 V. $V_{G2}$ plays an important role in reducing the effective threshold voltage of $M_{N0}$. As shown in the figure, the peak value of $V_{G2}$ is 0.52 V, which can compensate the forward conduction loss of $M_{N0}$. Similarly, the peak value of the compensation voltage $V_{G1}$ generated by $M_{P1}$ is 0.57 V, which can effectively compensate the threshold loss of $M_{P0}$. During the periodic switching period of the rectifier transistor, two compensation voltages $V_{G1}$ and $V_{G2}$ can compensate the forward conduction threshold voltage of $M_{P0}$ and $M_{N0}$ to be close to zero.

The synchronous self-threshold voltage doubling rectifier circuit designed in this article shows the highest PCE and output voltage.

The calculation method for the rectification circuit's PCE is given as follows:

$$\mathrm{PCE} = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}} = \frac{\mathrm{DCpower}}{\mathrm{RFpower}} = \frac{\frac{1}{T}\int v_{\mathrm{out}} \cdot i_{\mathrm{out}} dt}{\frac{1}{T}\int v_{\mathrm{in}} \cdot i_{\mathrm{in}} dt} \tag{14}$$

in which

$$P_{\mathrm{IN(RF)}} = \frac{1}{T}\int_0^T V_{\mathrm{IN}}(t) \times I_{\mathrm{IN}}(t)\, dt = \frac{V_m I_m}{2}\ (1 - \cos 2\omega_0 t)$$

$$= 42.75\ \mu\mathrm{W} \tag{15}$$

$$P_{\mathrm{OUT}} = \frac{V_{\mathrm{OUT}}^2}{R_L} = 24.85\ \mu\mathrm{W} \tag{16}$$

$$\mathrm{PCE} = \frac{P_{\mathrm{IN}} - P_{\mathrm{loss}}}{P_{\mathrm{IN}}} \times 100\% = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}} \times 100\% \approx 58\%. \tag{17}$$

Based on the calculated results, the power consumptions of each component in the proposed RF-dc rectifier [as shown in Fig. 7(d)] are shown in Table III.

The power consumptions of $R_1$ and $R_2$ are 5 $\mu$W and 3 $\mu$W, separately, corresponding to 13% and 8% of the overall power consumption of the RF-dc rectifier. The pie chart clearly shows the percentages of the components, as shown in Fig. 9. Although there are power consumptions on $R_1$ and $R_2$, the power efficiency of the rectifier can be 58%, which is compatible with the other published results [47], [48], [49], [50], [51], [52], [53]. Table IV depicts the comparison results of the key parameters of the RF-dc rectifiers. It can be seen that the leakage current is 16 $\mu$A. The effective threshold voltage is near zero.

Fig. 10(a) depicts the rectifier's simulated and measured reflection coefficient at different input power levels from −40 to +10 dBm, with the step of 2.5 dBm. Reasonable agreement between simulation and measurement results is achieved at 900 MHz. Moreover, the simulation and the measurement reflection coefficients at the GSM frequency band are shown in Fig. 10(b). In order to demonstrate the impedance matching bandwidth of the rectifier at desired frequency bands, the corresponding power level to the minimum reflection coefficient is chosen as the input power [−5 dBm at 900 MHz based on Fig. 10(a)]. It shows the fractional bandwidth of 21% at the GSM band. It can be observed that the proposed rectifier has an acceptable impedance matching.

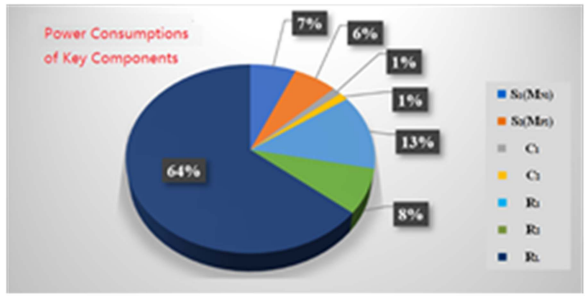



Fig. 9. Pie chart of power consumption of the components in the proposed RF-DC rectifier, as shown in Fig. 7(d).

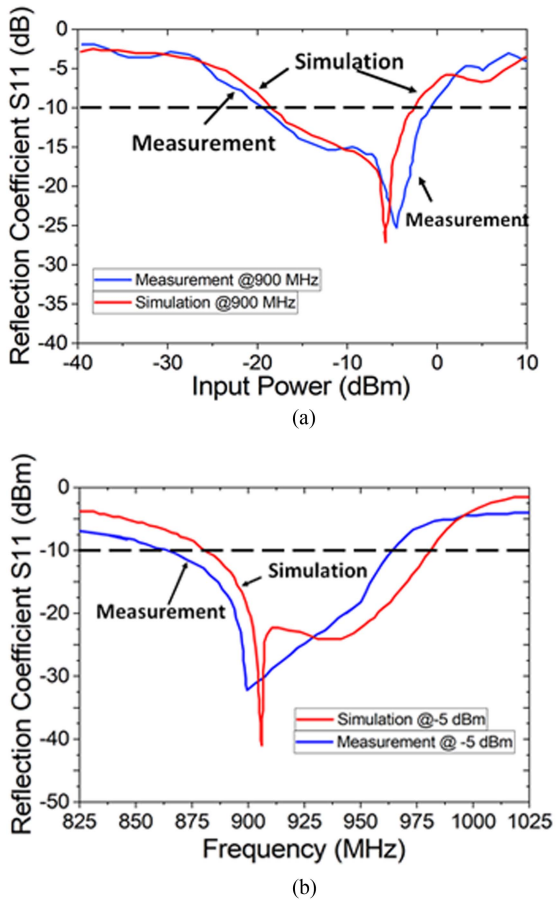



Fig. 10. Reflection coefficient of the proposed synchronous rectifier. (a) Different input RF power levels from −40 to +10 dBm. (b) Different frequency band at −5 dBm.

TABLE IV
COMPARISON OF THE KEY PARAMETERS OF THE RF-DC RECTIFIERS

| Parameters | [48] | [49] | [50] | [51] | [52] | [53] | [54] | This work |
|---|---|---|---|---|---|---|---|---|
| Technology node(nm) | 350 | 180 | 250 | 130 | 180 | 180 | 180 | 65 |
| Frequency(MHz) | 13.56 | 13.56 | 915 | 915 | 902 | 902 | 902 | 900 |
| Number of Stages | 1 | 5 | 3–5 | 6 | NA | NA | NA | 3 |
| Input voltage/Power | 1.5–2 V | –8.86 dBm | 2 V | 800 mV | –8 dBm | 63.25 mV | 6 dBm | 300 mV |
| Output voltage(V) | 2–3.6 | 2.71 | 0.6 | 1.8 | 3 | 1.2 | 3 | 1.4 |
| Load(KΩ) | 100 | 80 | 1000 | 1000 | 1000 | 1000 | 5 | 80 |
| Leakage Current (μA) | NA | 139 | 50 | NA | NA | NA | NA | 16 |
| Effective Threshold Voltage (V) | 0.7 | 0.229 | NA | NA | NA | 0.4 | NA | 0.05 |
| PCE(%) | 70 | 56 | 29 | 27 | 33 | 41 | 46 | 58 |

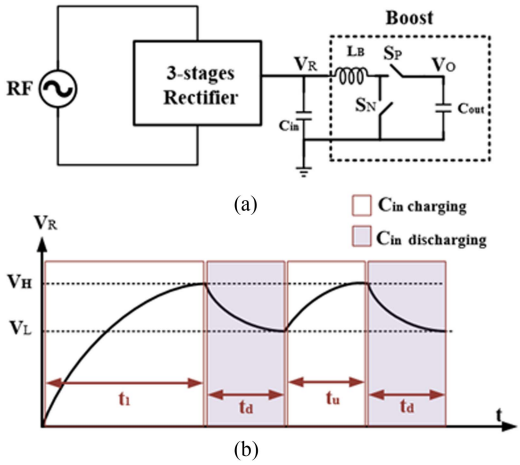



Fig. 11. (a) Schematic of the connection between rectifier and boost circuit. (b) Working voltage of storage capacitor $C_{\rm in}$.

## V. POWER MANAGEMENT UNIT

The RFEH system requires PMU to control and optimize the power supply, especially in the scenario of low power and low voltage [10]. There is an obvious power discrepancy between the environmental RF source and the load network node. The PMU is needed between the energy source and the electrical appliance. The electrical output by the rectifier circuit can be stabilized by the PMU, achieving end-to-end maximum power transmission.

The design of the PMU can be divided into two parts. The first part is the impedance matching between the rectifier circuit and the PMU in order to effectively charge the storage capacitor and achieve maximum PCE. The second part is the power transmission to the storage capacitor, which converts dc to dc for the target application.

The PMU has three fundamental characteristics, including boost voltage, high output accuracy of dc voltage, and maximum power transmission. Therefore, the PMU is designed based on the boost circuit and combined with LDO for voltage stabilization. The schematic of the connection with the three-level rectifier circuit, storage capacitor $C_{\rm in}$, and the boost circuit is shown in Fig. 11(a). The output energy of the rectifier circuit is stored by the capacitor $C_{\rm in}$ with the voltage $V_R$. $V_R$ would act as the power supply for all subsequent circuits. The boost circuit can raise the output voltage of the reduced rectifier circuit back to the usable range. When the rectifier output is used as a power supply for bandgap and oscillation, LDO is needed to stabilize the output ripple.

Fig. 11(b) shows the working voltage of the storage capacitor $C_{\rm in}$. Before the rectifier circuit reaches stable operation, its output voltage $V_R$ continues to rise in an initial period of time. $t_1$ is the charging time of the three-level rectifier to the storage capacitor $C_{\rm in}$ during the power ON period. When the voltage value on $C_{\rm in}$ exceeds the threshold voltage $V_H$, $C_{\rm in}$ begins to be discharged, and the PMU starts working. When $C_{\rm in}$ voltage is decreased to the low threshold $V_L$, the charging process is started. $t_d$ is the discharge time of $C_{\rm in}$ after the boost circuit stabilizes. $t_u$ is the charging time of $C_{\rm in}$ after stabilization.

The PMU duty cycle $D$ can be determined based on changes in $V_R$

$$D = 1 - \frac{V_R}{V_O}. \tag{18}$$

### A. Overall Structure of PMU

The top-level circuit of the PMU is shown in Fig. 12. The circuit is based on the boost structure, including the startup circuit, bandgap reference circuit, voltage detecting circuit, main clock generation circuit, logic control circuit, LDO circuit, and overvoltage protection circuit. The entire system has no external power supply. The bandgap reference circuit provides $V_{\rm REF}$ for the system. Control signals Ctr and EN are generated by the logic control circuit.

As shown in Fig. 12, the voltage $V_R$ is divided by the MOS divider. The voltage sensor $\rm VS_1$ is used to sense and compare the node voltages $\rm in_1$ and $V_{\rm REF}$. The output result is processed by a logic control circuit to generate Ctr signal. The Ctr signal is used to control the switching between the start circuit and the main clock generation circuit. When $V_R$ is lower than $V_{\rm REF}$, the startup is turned ON to provide initial bias for the PMU. As $V_R$ is gradually higher than $V_{\rm REF}$, the startup is disabled, and the clock generation circuit is enabled. At this time, the system operates during the first $t_d$, and subsequently stabilizes, as shown in Fig. 11(b), allowing $C_{\rm in}$ to be charged/discharged.

With the occurrence of the voltage drop in $V_R$, the boost circuit is used to obtain $V_p$, which is then divided by the voltage divider structure to generate $\rm in_2$. The voltage sensor $\rm VS_2$ is used

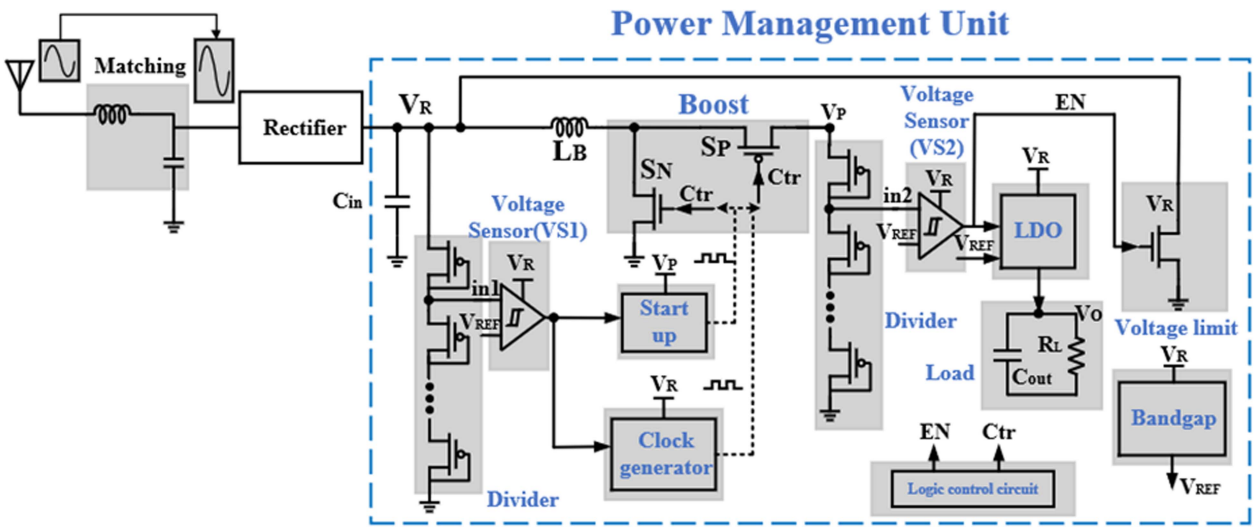
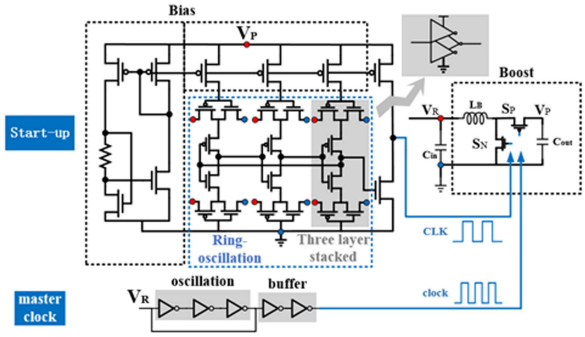


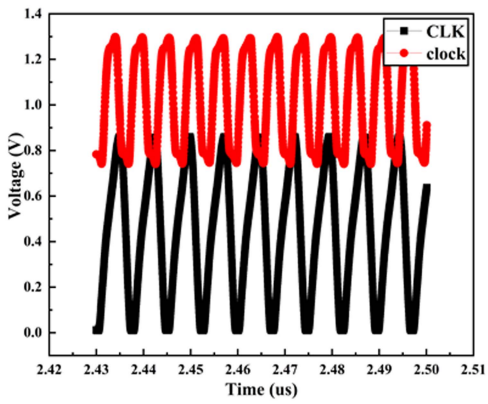

Fig. 12. Overall circuit structure of the designed PMU.

to compare between $in_2$ and $V_{\mathrm{REF}}$, generating a control signal EN, which is used to determine the switching status of LDO and overvoltage protection circuit. The LDO is used to stabilize the voltage and to supply the power. The overvoltage protection transistors are used to limit the output voltage below 2.5 V, suppressing possible large leakage current and protecting the normal operation of the system.

In the traditional boost circuit, with the control of the main clock signal's 50% duty cycle, in addition to storing charges on the inductor $L_B$, a portion of energy is wasted on the switch $S_N$. In order to utilize the wasted energy to improve the conversion efficiency of the system, there are generally two methods: increasing energy conversion rate and reducing energy loss. The former changes the structure of the NMOS part on the basis of a traditional boost circuit, combines it with the voltage detecting module, and uses this positive half-cycle energy to generate control signals for the system, thereby improving energy conversion efficiency. The latter utilizes the control signal of the main circuit to generate a clock with an adjustable duty cycle [47], which shortens the time for NMOS conduction and greatly suppresses the power consumption. In the PMU proposed in this article, a design method combining voltage detecting circuit and boost circuit is adopted. The output of the voltage detecting circuit is used to control the opening and closing of the starting circuit and the main circuit, improving energy utilization efficiency and thereby improving the PCE of the PMU.




(a)




(b)

Fig. 13. (a) Starting circuit and master clock generation circuit of the designed PMU. (b) Simulation results of start-up circuit clock CLK and master clock.

### B. Start-Up Circuit and the Master Clock Circuit

Before the circuit starts working, the output voltage $V_R$ of the rectifier circuit is zero, and all subsequent circuits powered by $V_R$ are in a dormant state. The output voltage $V_P$ of the PMU is zero, and the clock signal cannot be generated. But the output zero potential is the stable state of the system. If there is no starting circuit, the entire system cannot work. The startup circuit enables the system to resume from undervoltage locking. As shown in Fig. 13(a), the starting circuit is improved based on a ring oscillator, using a three-layer stacked ring oscillator. It can increase the amplitude of the clock signal CLK while ensuring the oscillation speed so that the charges of the capacitor $C_{\mathrm{out}}$ can be accumulated quickly. The power-insensitive bias circuit in Fig. 13(a) is used to suppress the possible influences of the frequency and the power on the starting circuit.

As shown in Fig. 13(b), with the provided input voltage, the starting circuit can generate CLK signal around 140 MHz, with low voltage of 0 V and high voltage of 0.9 V. The power supply voltage of the main clock signal is higher than $V_O$. The oscillation frequency is 180 MHz. The voltage of the clock is between 0.7 and 1.3 V.

The starting circuit is powered by the output voltage $V_P$ instead of $V_R$. It is because, as mentioned earlier, $V_R$ has a significant voltage drop when supplying power to subsequent circuits. If it is used as the power source, it not only further reduces $V_R$ but also does not meet the input voltage requirements of the ring oscillator, which can cause the failure of the starting circuit. In addition, the time for $V_R$ reduction cannot be accurately predicted and controlled, and the starting circuit only works for a short period of time when the rectifier circuit begins to accumulate charges. Using $V_R$ power supply may even lead to logic errors.

Regardless of whether the front-end rectifier circuit reaches a stable state or whether the starting circuit of the PMU is turned ON, as long as the rectifier circuit starts working, there is charge accumulation in $C_{\text{in}}$. The initial state CLK is low, $S_N$ is OFF, and $S_P$ is ON. When the rectifier circuit and boost circuit are matched, the boost circuit transfers the charge on $C_{\text{in}}$ through the $S_P$, causing the charge to accumulate at the output end, gradually increasing $V_o$. The starting circuit can start working when the $V_o$ is as low as 0.3 V and can generate CLK with a duty cycle of 50%. CLK signal provides the boost circuit an initial voltage value, which can charge the switching capacitor $C_{\text{in}}$ and storage capacitor $C_{\text{out}}$ so that they can respond quickly when the working clock signal of the main circuit arrives.

As the output voltage of the rectifier circuit gradually increases, the starting circuit would be disabled when the value is higher than $V_{\text{REF}}$. Therefore, the working time of the startup circuit is only a few microseconds. The three-level three-layer stacked ring connection is adopted in this article, which can ensure the completion of the oscillation of the starting circuit in a short time, and quickly stabilize CLK with a high-voltage level.

After the startup circuit is closed, the main clock circuit begins to work. The main circuit is connected in a loop by a three-level inverter and processed by two buffers for waveform stabilization. The frequency of the clock is higher than CLK because its power source is $V_R$. As $V_R$ increases, the frequency of the voltage-controlled oscillator also increases.

### C. CMOS Bandgap Circuit

The bandgap reference circuit for the reference voltage source used in subsequent voltage detecting circuit and voltage stabilizing circuit is designed based on CMOS technology [48]. An improved voltage reference circuit is shown in Fig. 14(a). In the first stage startup circuit, $M_1$ is constantly turned ON, and a path from $V_R$ to $V_{\text{REF}}$ is constructed in the startup circuit to prevent the degradation of the bandgap reference circuit. A current mirror is composed of $M_2$ and $M_3$, which replicates the current of $M_1$. The input voltages $V_1$ and $V_2$ of the second stage are intercepted internally in the circuit, and the output terminal

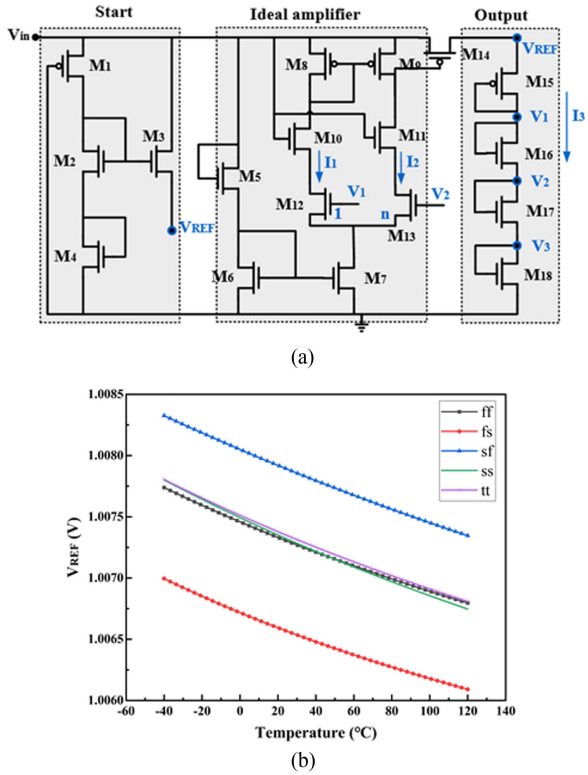



Fig. 14. (a) Schematic of CMOS bandgap reference circuit. (b) Simulation results of $V_{\text{REF}}$ on different process corners, including *ff, fs, sf, ss,* and *tt*.

is connected to $M_{14}$ to replicate the reference current. The third output stage $M_{15}$–$M_{18}$ is a voltage divider, and the required reference voltage can be obtained by changing the appropriate width/length ratios of the transistors. The number of transistors can be changed based on the concrete requirement. The input transistor of the ideal differential amplifier biases $M_{12}$ and $M_{13}$ in the subthreshold region of 1: $n$. With $M_{10}$ and $M_{11}$ current mirror loads, the currents of the two input transistors are equal, so $I_1 = I_2$. Therefore, the parameter relationship between $M_{12}$ and $M_{13}$ can be expressed as follows:

$$I_0 \exp\left(\frac{V_{\text{GS12}}}{V_T}\right) = nI_0 \exp\left(\frac{V_{\text{GS13}}}{V_T}\right). \tag{19}$$

The negative temperature coefficient voltage of the bandgap reference circuit is provided by the gate-source voltage $V_{\text{GS18}}$ of $M_{18}$, and the positive temperature degree voltage is constructed by the gate-source voltage difference $\Delta V_{\text{GS}}$ of $M_{12}$ and $M_{13}$

$$\Delta V_{\text{GS}} = V_{\text{GS12}} - V_{\text{GS13}} = V_T \ln\frac{nI_0}{I_1} - V_T \ln\frac{I_0}{I_2} = V_T \ln n \tag{20}$$

in which $V_{\text{GS12}} - V_{\text{GS13}} = V_1 - V_2 = V_{\text{DS16}} = V_{\text{GS16}}$.

$V_{\text{REF}}$ can be obtained by

$$\begin{aligned} V_{\text{REF}} &= V_{\text{DS15}} + V_{\text{DS16}} + V_{\text{DS17}} + V_{\text{DS18}} \\ &= V_{\text{GS18}} + I_3 \left(R_{\text{on15}} + R_{\text{on16}} + R_{\text{on17}}\right). \end{aligned} \tag{21}$$

$R_{\text{on}}$ is the conduction resistance of the MOS transistor, $R_{\text{on}} = 1/\sqrt{\mu_p C_{\text{ox}} \frac{W}{L} I_3}$, $I_3 = \frac{V_T \ln n}{R_{\text{on16}}}$, so $V_{\text{REF}}$ can also be represented

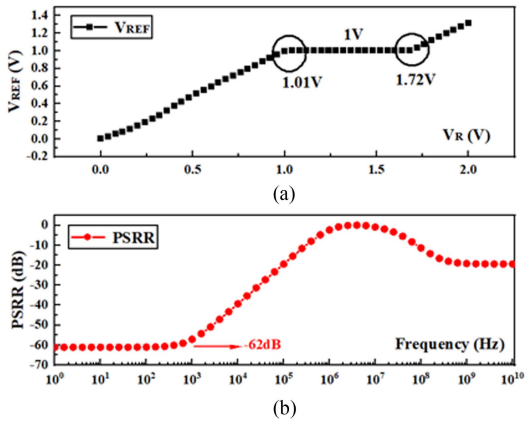



Fig. 15. (a) Variation of reference voltage with input. (b) PSRR simulation of bandgap reference circuit.

as follows:

$$V_{\mathrm{REF}} = V_{\mathrm{GS18}} + \frac{V_T \ln n}{R_{\mathrm{on16}}}\left(R_{\mathrm{on15}} + R_{\mathrm{on16}} + R_{\mathrm{on17}}\right)$$
$$= V_{\mathrm{GS18}} + V_T \ln n\left(1 + \frac{R_{\mathrm{on15}}}{R_{\mathrm{on16}}} + \frac{R_{\mathrm{on17}}}{R_{\mathrm{on16}}}\right)$$
$$= V_{\mathrm{GS18}} + V_T \ln n\left(1 + \frac{(W/L)_{16}}{(W/L)_{15}} + \frac{(W/L)_{16}}{(W/L)_{17}}\right). \quad (22)$$

The simulation results of $V_{\mathrm{REF}}$ of the bandgap circuit changing with temperature at different process corners are shown in Fig. 14(b). $V_{\mathrm{REF}}$ variation is within 0.002 V under different process corners and within 0.01 V with the temperature range of $-40\sim120$ °C.

Fig. 15(a) shows the simulation results at *tt* process corner at 27 °C (top). The bandgap circuit can provide reference voltage $V_{\mathrm{REF}} = 1$ V within the range $V_R = 1.01$–$1.72$ V. As shown in Fig. 15(b), the power supply ripple rejection (PSRR) at low frequency is $-62$ dB, showing good power noise suppression ability. The static current of the bandgap circuit is 300 nA, meeting the low-power consumption requirement.

### D. Voltage Detecting Circuit

The essence of PMU voltage detecting characteristics is reflected by a comparator, which compares the monitored voltage with $V_{\mathrm{REF}}$ to obtain the voltage detection results. At this point, the voltage on the capacitor $C_{\mathrm{in}}$ fluctuates between $V_L$ and $V_H$, so the detecting circuit needs to be sensitive to the voltages at these two endpoints. Possible oscillation at the output of the comparator should be avoided. Therefore, the voltage detecting circuit is composed of a hysteresis comparator.

The threshold voltages $V_H$ and $V_L$ of a hysteresis comparator are the result of the interaction between the feedback resistor and the divider resistor, and both input and output voltages have an impact on the threshold. In the design of hysteresis comparator with the hysteresis effect, the voltage divider should be included. Also, the positive feedback should be added to introduce the input and the output voltages on the threshold together. To address the issue of high-power consumption in traditional hysteresis comparators, the resistors are replaced by the diode-connected MOSFETs (as shown in the voltage divider structure in Fig. 12) to achieve the goal of reducing static power consumption. The hysteresis comparator is designed based on this voltage divider structure.

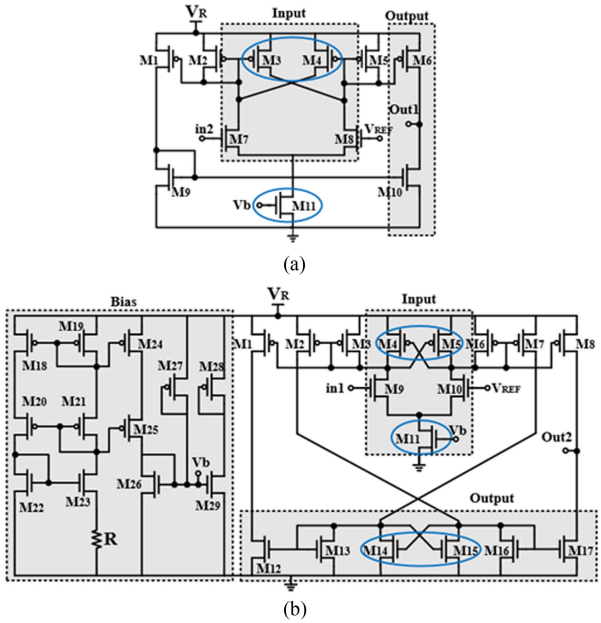



Fig. 16. Hysteresis comparator design. (a) $VS_1$ circuit. (b) $VS_2$ circuit.

As shown in Fig. 11, there is a significant variation of the voltage on the capacitor $C_{\mathrm{in}}$. It is necessary to sense the changing rate of the voltage in a target manner. When the voltage detecting circuit $VS_1$ is used to monitor the rise rate of $V_R$, it shows low-speed and low-power consumption. When $VS_1$ is used to monitor the drop rate of $V_R$, the changing rate of voltage on $C_{\mathrm{in}}$ is accelerated, and the comparator needs to have high-speed performance at this stage. Therefore, the balance between the power consumption and the response speed is needed. When $VS_2$ is in a stable state, no speed requirement on $VS_2$ is needed, while the low-power consumption should be considered.

Fig. 16(a) shows the circuit diagram of the hysteresis comparator $VS_1$. There are two feedback loops. The first is current-series-negative-feedback brought by the tail current source $M_{11}$. The second is the voltage formed by $M_4$ and $M_3$ cross-coupling connection. So, its response speed is faster than $VS_2$, but its power consumption is higher than $VS_1$.

Fig. 16(b) shows the circuit schematic of the hysteresis comparator $VS_2$. The input stage and the output stage are connected in a cross-coupling manner. $M_{18}$–$M_{29}$ form the bias circuit of the comparator, providing a bias voltage $V_b$ for the tail current $M_{11}$. This voltage is not affected by the working state of other transistors and can constantly bias $M_{11}$ in the saturation region. By controlling the aspect ratio and gate-source voltage of $M_{11}$, the input current can be controlled, thereby reducing the power consumption. $VS_2$ has three feedback paths.

1) Current-series-negative feedback by tail current source $M_{11}$.

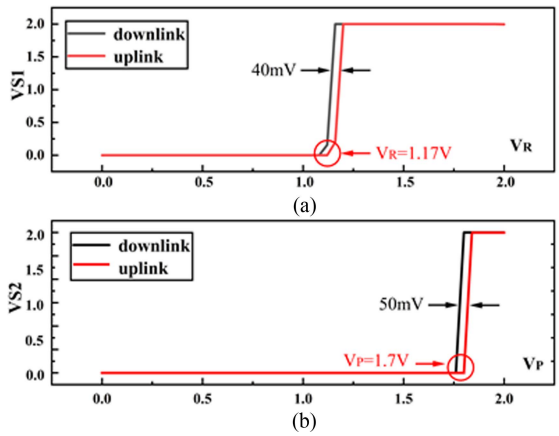



Fig. 17. Simulation results of hysteresis comparators. (a) VS1. (b) VS2.

TABLE V
RIPPLE REQUIREMENTS OF LOAD CIRCUIT FOR POWER SUPPLY VOLTAGE

| Load type | Ripple | Examples |
|---|---|---|
| Digital circuit | 0.3000~0.4000 V | Digital switching circuits, memory |
| General analog circuit | < 0.1000 V | Amplifiers, comparators |
| Accurate analog circuit | < 0.0010 V | ADC and DAC |

2) Voltage-parallel-positive feedback by $M_4/M_5$ cross-coupling connection.
3) Voltage-parallel-positive feedback by $M_{14}/M_{15}$ cross-coupling connection.

The hysteresis simulation results of the voltage detecting circuits are shown in Fig. 17. The comparator has a hysteresis of 40 mV. The working current of $VS_1$ is as low as 2 $\mu$A. As shown in Fig. 17(b), the comparator flips at $V_P = 1.7$ V in $VS_2$, while its response speed is slower than $VS_1$.

### *E. Voltage Stabilizing Circuit*

The power supply voltage on the load node is varied in the range of 1–3 V. To stabilize the voltage, an LDO circuit is integrated to suppress the output voltage ripple of the PMU. Table V presents the ripple requirements for power supply voltages.

In order to be applicable for portable RF harvesting system, low-power consumption, fast transient response, and easy integration are the main characterizations of LDO regulator. In the design, the structure with a single-stage operational amplifier is adopted. Its stability is improved by the transconductance enhancement circuit, and the transient speed at low static current is optimized by conversion rate enhancement circuit.

Fig. 18 shows the designed LDO, which mainly consists of five parts. The first part is a single-stage error amplifier (EA) with a single output to increase the loop gain and the stability of the regulator. The second part is the conversion rate enhancement circuit (SRE), which enhances the load regulation ability. The output of SRE is connected to $M_{\mathrm{PASS}}$ in the third part, in which large-sized PMOS transistors are used as power transistors to obtain large output resistance. The fourth part is a transconductance enhancement circuit ($G_m$ cell) [49], implemented by transistors $M_L$ and $M_H$. $M_{N10}$–$M_{P10}$ corresponds to the fifth part, which deals with the large current during the transient response of the $G_m$ cell.

With SR $= I_{SS}/C_{\mathrm{PASS}}$, the conversion rate SR of LDO is directly proportional to the tail current $I_{SS}$. Two PMOS current mirrors are adopted to increase the bias current and also enlarge the input voltage range. However, the larger the bias current, the more power is consumed. EA can be biased by adjusting the mirror ratios of $M_{N1}$–$M_{P4}$, $M_{N10}$, and $M_{N12}$ to generate appropriate currents in order to compromise the performance of design conversion rate and power consumption.

In order to improve the transient response rate and achieve stability at fast speed, it is necessary to increase the EA bandwidth. The bias circuit and the output of EA are connected to the $M_{P4}$ and $M_{N5}$ of SRE, respectively, while the output of SRE circuit is connected to the gate of $M_{\mathrm{PASS}}$. $M_{P7}$ can accelerate the charging speed of $M_{\mathrm{PASS}}$ gate capacitor, causing a rapid increase in $M_{\mathrm{PASS}}$ gate voltage and a rapid decrease in $V_O$. Similarly, if $V_O$ decreases, SRE undergoes two reverse changing, which can ultimately maintain the stability of the output voltage.

Without a large off-chip output capacitor, system stability and transient response are degraded. The transconductance enhancement circuit can effectively solve the problem. The transconductance enhancement circuit has two units: a negative difference compensation module ($G_{mL}$) and a positive difference compensation module ($G_{mH}$). During the transient response process, regardless of the size relationship between $V_O$ and $V_{\mathrm{REF}}$, a large current from any $G_m$ cells can quickly charge or discharge the gate capacitor. Therefore, even if the static current is very low, the SR can be improved, no longer limited by the traditional amplifier constant current sources. The output transient current at $G_{mL}$ is used to discharge the large gate capacitor of the $M_{\mathrm{PASS}}$, while at $G_{mH}$, it is used to charge the gate capacitor, accelerating the processing speed of excess current flowing through the power transistor. The $G_m$ cells are connected by a current summation circuit with power transistor cross coupling, achieving high conversion rate in the positive and negative directions, improving transient response, while greatly reducing the static power consumption of the system [49], [50].

The voltage buffer circuit provides dynamic bias voltage to the current mirror by detecting changes in the system output voltage, in order to improve the transient response speed of LDO. The output of the $G_m$ cell is connected to the voltage buffer circuit, generating loop feedback voltage $V_{\mathrm{FB}}$. $V_{\mathrm{FB}}$ is transmitted into EA to form negative feedback, allowing the circuit to respond to changes in load current based on the feedback loop of EA. $M_{N12}$ and $M_{P9}$ act as push–pull output stage, which can sum up the output currents to amplify the changes in the output signal. The single-stage amplifier has the ability to drive the source output. The push–pull output stage provides more current at the output of the EA to charge or discharge the gate of the power transistor during transient response with fast stability time.

There are two compensation methods in the LDO topology, including active feedforward and transconductance enhancement. SRE implements feedforward compensation technology by placing the main pole at extremely low frequencies and the output pole at high frequencies. With zero compensation

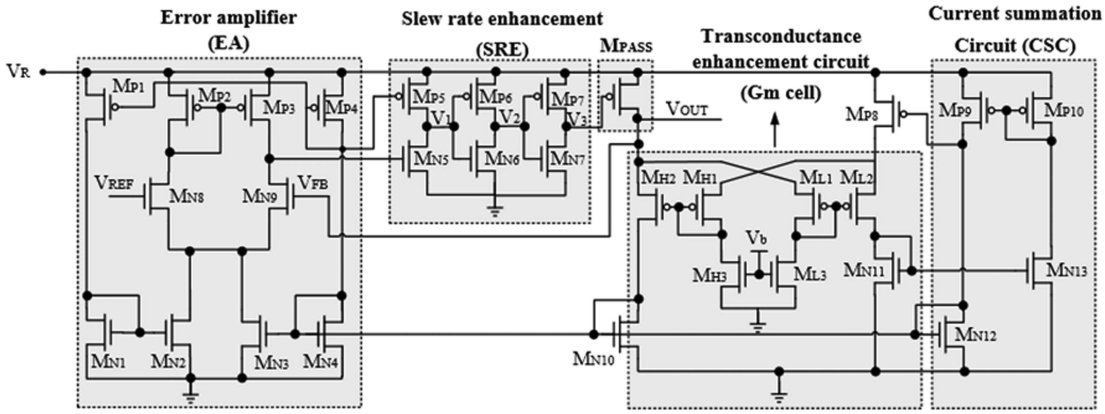



Fig. 18. Schematic of the designed LDO circuit.

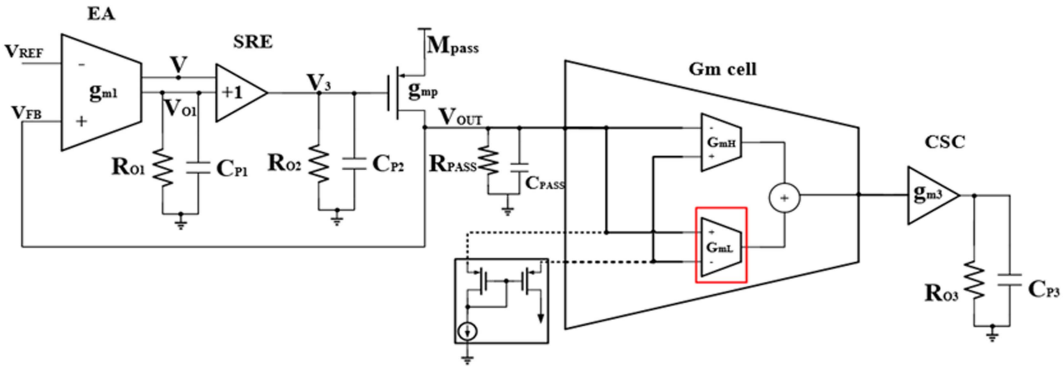



Fig. 19. Small-signal equivalent circuit of LDO.

technology and two current mirrors, a left half-plane zero offset pole is generated to reduce the influence of nonmain poles, thereby improving the stability and power suppression ability of the voltage regulator.

The small-signal equivalent model of the LDO regulator is shown in Fig. 19. The output impedance of EA is $R_{\mathrm{O1}} = (\frac{1}{g_{m(N8)}} || \frac{1}{g_{m(P4)}})$. Its output terminal has the first main pole $P_1 = \frac{1}{R_{o1} C_{P1}}$.

The second main pole $P_2$ is located at the output of LDO, mainly depending on the gate capacitance size of $M_{\mathrm{PASS}}$. The source of the transistor in the $G_m$ cell is directly connected to the output of LDO, causing the open-loop output resistance to be changed from $R_{\mathrm{PASS}}$ to $(R_{\mathrm{PASS}} || \frac{1}{G_{mH}})$. It means LDO has smaller open-loop output resistance over a wide range of required load currents [51]. The second main pole $P_2 = \frac{1}{C_{p2} R_{\mathrm{OUT}}}$ (where $R_{\mathrm{OUT}} = R_{\mathrm{PASS}} || \frac{1}{G_{mH}} || R_{O2}$) is still at the high frequency, being away from the low-frequency pole.

Fig. 20 shows the loop stability results of LDO with the load current from 1 $\mu$A to 8 mA without the fixed load. The gain intersection GX and the phase intersection PX are at lower frequencies, and the phase margin is about 77°. With full load ($I_{\max} = 8$ mA), the loop gain is increased. The intersections of GX and PX move to high frequency, while the phase margin is still 62°. The transconductance enhancement circuit ensures the stability of LDO at full load.

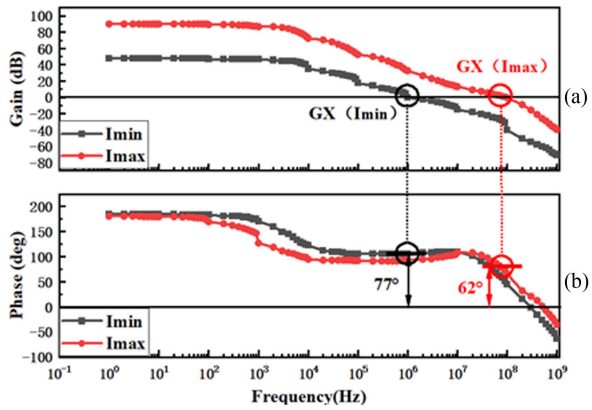



Fig. 20. Loop frequency response. (a) Loop gain. (b) Phase of LDO under no-load ($I_{\min}$) and full-load ($I_{\max}$) conditions.

Fig. 21 shows the transient results of LDO. When the rising time of $I_{\mathrm{load}}$ is 1 $\mu$s, the overshoot voltage of LDO is 0.03 V, and the transient time is 1 $\mu$s. When the current is changed in the opposite direction, the change of the output voltage is 0.3 V, with the transient time 1 $\mu$s.

PSRR of LDO is shown in Fig. 22. When $I_{\mathrm{load}} = 8$ mA, the PSRR is $-52$ dB. When $I_{\mathrm{load}} = 1$ $\mu$A, PSRR $= -56$ dB. The static current of LDO is 3 $\mu$A, calculated by $I_Q = I_{\mathrm{IN}} - I_{\mathrm{OUT}}$.

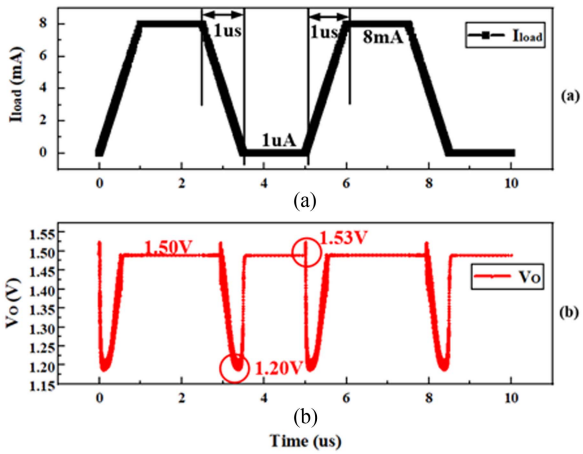



Fig. 21. Load transient response. (a) Load current with time. (b) Transient response of output voltage.

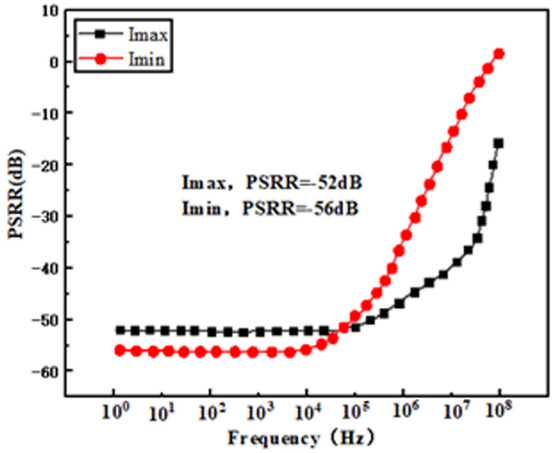



Fig. 22. PSRR results of LDO.

### F. Logic Control Circuit

The logic circuit is used to control the working status and consequences of the startup circuit, the main clock signal, LDO, and the overvoltage protection circuit. Table VII presents the logic function. Ctr = 0 and 1 represents $in_1 < V_{REF}$ and $in_1 > V_{REF}$, respectively. EN = 0 and 1 represents $in_2 < V_{REF}$ and $in_2 > V_{REF}$, respectively.

From Table VII, it can be seen that

$$A = \overline{\text{Ctr}}$$

$$B = \text{Ctr} \times \overline{\text{EN}}$$

$$C = \text{Ctr} \times \text{EN}.$$

The corresponding logical relationship is shown in Fig. 23.

The basic gate circuit is shown in Fig. 24, including XOR and NXOR gates. The transient simulation results of the logic gate are shown in Fig. 25. Fig. 25(a) shows $\overline{\text{Ctr}} \times \overline{\text{EN}}$, and Fig. 25(b) shows $\text{Ctr} \times \overline{\text{EN}}$. The simulation results of the logic circuit are shown in Fig. 25(c), showing that the logic circuit can meet the functions in Table VI.

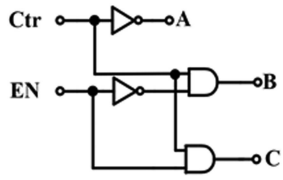



Fig. 23. Logic circuit diagram of PMU.

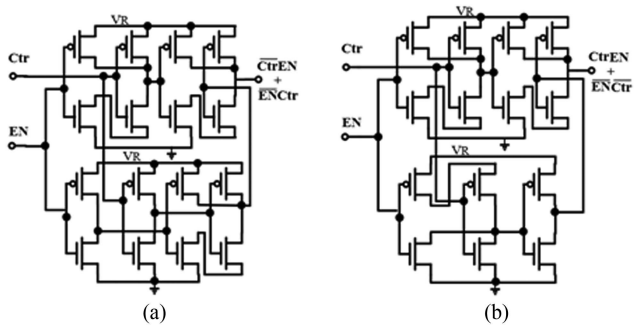



Fig. 24. Logic gate circuit used in this article. (a) XOR gate. (b) NXOR gate.

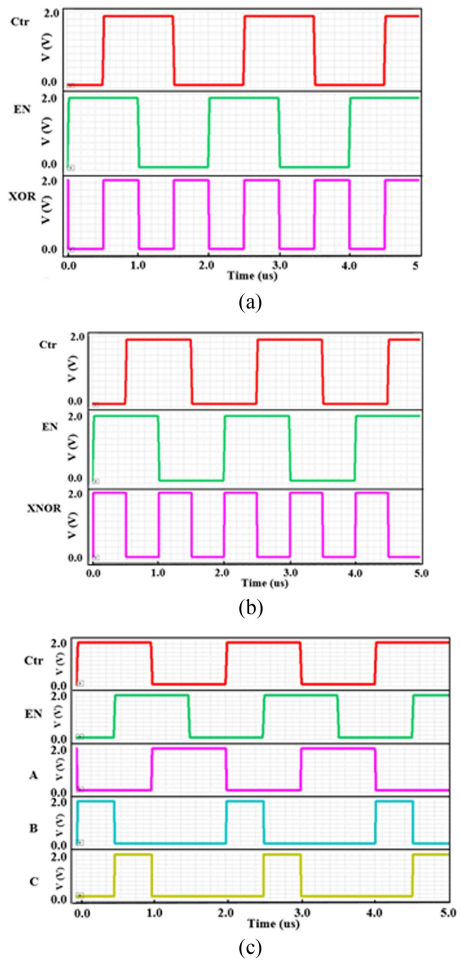



Fig. 25. Transient simulation results of logic circuits. (a) XOR. (b) NXOR. (c) Overall logic results.

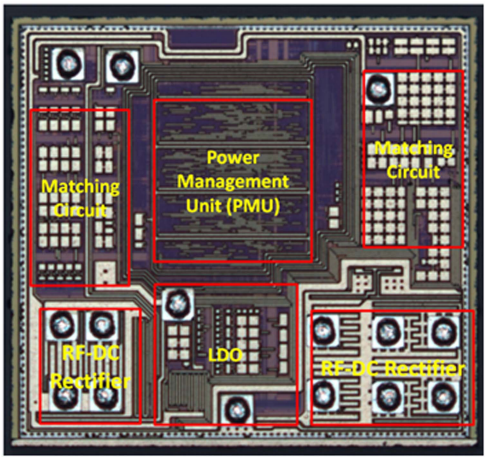



Fig. 26. Layout photo of the designed RFEH circuit.

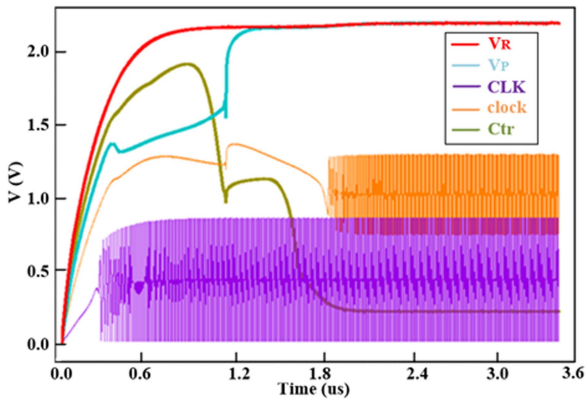



Fig. 27. PMU control signals and the key nodes' voltages.

TABLE VI
LOGIC FUNCTION OF THE CONTROL CIRCUIT

| Ctr | EN | Start-up circuit (A) | Clock and LDO (B) | Overvoltage protection transistor (C) |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |

The waveform of $V_P$ is shown in Fig. 28. It can be seen that under no-load conditions, the voltage ripple of the boost is 0.02 V. As shown in Fig. 29, when EN is at a high level, the boost circuit cannot turn ON, so the transistor SP is not working. $V_P$ is at a low level. The boost circuit is in the stand-by mode. When EN is low, $V_R$ is transmitted to $V_P$ through the boost and the LDO is turned ON at this time. At this stage, the boost circuit is working in a lossless transmission mode.

The output performance of the PMU module is shown in Fig. 30. LDO can be turned ON when the input voltage $V_P$ is higher than 0.3 V. When the input voltage continuously increases, the output $V_O$ of LDO can also be increased accordingly. When $V_P$ exceeds 1.5 V, the circuit output voltage stabilizes at 1.5 V.

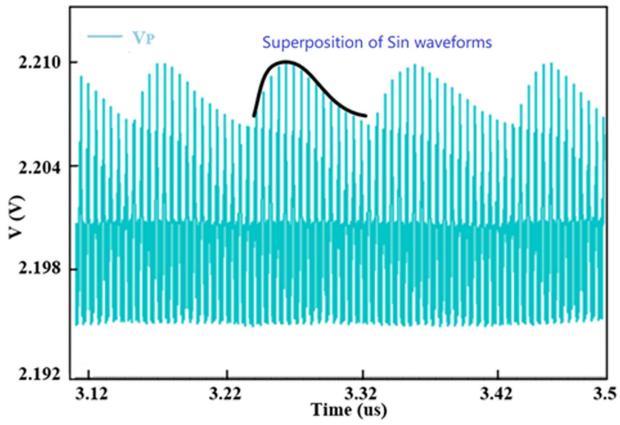



Fig. 28. Output of $V_p$ in PMU controller.

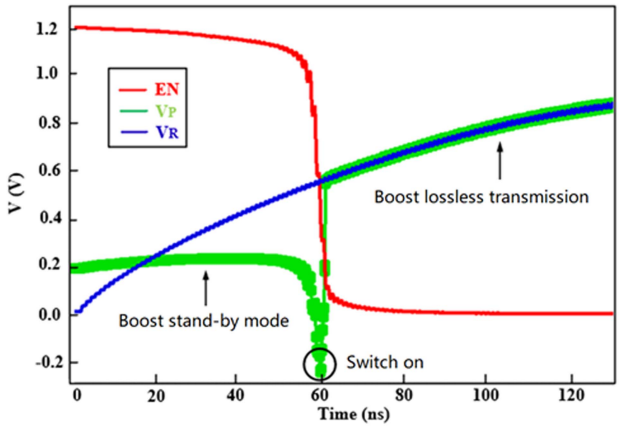



Fig. 29. Logic control signal and output voltages in PMU module.

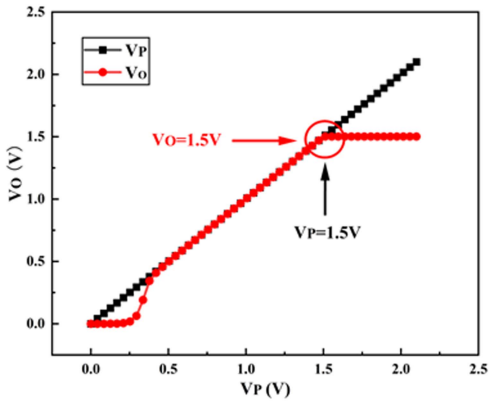



Fig. 30. Output voltage of PMU module.

In Table VII, the key properties of the designed PMU in this article are listed and compared with the other PMUs in the literature [13], [14], [54], [55]. It can be seen the designed PMU shows wide tunable voltage gain (0.1–8), less consumed power ($< 1\ \mu$W), and wider output voltage (0.2–2 V).

Fig. 31 shows the output voltage of RFEH system. The PMU obtains an output voltage $V_O$ with a ripple of <0.001 V [as shown in Fig. 31(a)]. Fig. 31(b) shows that the variation of the PMU output voltage is less than 0.2 mV with different frequencies in

TABLE VII
KEY PROPERTIES OF THE DESIGNED PMU IN RFEH SYSTEM AND COMPARISON WITH PRIOR ARTS

| Parameter | [13] | [14] | [55] | [56] | This work |
|---|---|---|---|---|---|
| **Technology(nm)** | 65 | 130 | 180 | Discrete | 180 |
| **PMU Type** | AEM3094 0 PMU | Asyn. SC | SC | Switched -L | Cold-start with LDO |
| **PMU integration** | No | Yes | Yes | No | Yes |
| **Frequency** | 2.45 GHz | 2.4 GHz | 400 MHz | 2.45 GHz | 900 MHz |
| **Startup voltage(V)** | 0.38 V | 0.2 V | 1.2 V | NA | **0.3** |
| **Output voltage(V)** | >2.2 V | 0.4-1.2V | 1.2 V | 0-14 V | 1.5 |
| **Static current** | NA | NA | NA | NA | 300 nA |
| **Achieved voltage gain** | NA | 1.73 | <1 | 1.3 | 0.1~8 |
| **PMU working range** | >–19 dBm | >–20 dBm | –12 to –1 dBm | NA | **>–21.5 dBm** |
| **PMU consumed power** | >1 μW | 28-405 nW | 35 μW | >47μW | **<1 μW** |
| **PMU $V_{DD}$** | >1.2 V | 0.3-1.0 V | >1.2 V | > 3.0 V | **0.2-2 V** |

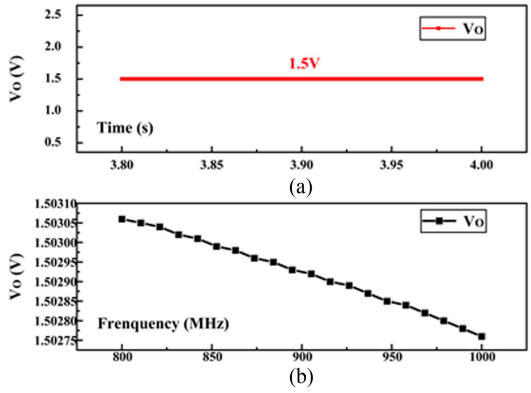



Fig. 31. Output voltage $V_O$ of RFEH system. (a) Ripple of $V_O$. (b) Variation of $V_o$ with different frequencies in the range of 800 MHz–1 GHz.

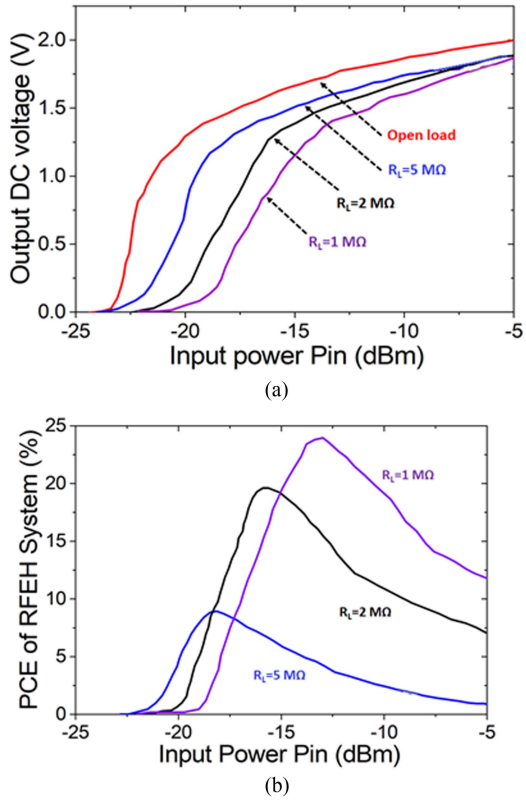



Fig. 32. Measured results of the designed RFEH system. (a) Output DC voltage versus input power $P_{\text{in}}$ with different load resistance values. (b) PCE of RFEH system with different load resistance values. ($C_L = 57$ nF and $f =$ 900 MHz, CW input).

the range of 800 MHz–1 GHz. Fig. 32(b) shows the PCE values versus input powers. The maximum PCE value is 23.8% with the load resistance of 1 MΩ at input power −13.2 dBm.

The designed whole RFEH system is tested with a single-tone continuous wave (CW) 50-Ω source with a nominal frequency of 900 MHz. Fig. 32 shows the measured results of the fabricated RFEH system. The load capacitor is 57 nF, and the load resistance is varied to get different output results. Fig. 32(a) shows the measured output voltage versus input power with different load resistances. The RFEH system shows a low input threshold power. With the input power −22.5 dBm, it can provide a 1-V output voltage with an open-load scenario. With the load resistance of 1 MΩ, it can provide the nominal output voltage of 1.2 V with an input power of −15 dBm.

The total power consumption and the conversion efficiency of the RFEH system can be calculated, as shown in Table VIII. The PCE calculation of the RFHE system can be obtained from (1). The overall conversion efficiency of the system is 31.77%

$$\begin{aligned}\text{PCE}_{\text{RFEH}} &= 93\% \times 95\% \times 58\% \times 62\% \\ &= 31.77\%. \end{aligned} \tag{23}$$

There exists an obvious discrepancy between the theoretical PCE value and the measured ones [58], [59]. The impedance matching is one of the key issues. The impedance of the RFEH system depends on various parameters, such as input power level, operating frequency, load impedance, rectifier stage, and PMU topology. Maximum power transfer can only be obtained when the load impedance of each stage is well matched with the

TABLE VIII
POWER CONSUMPTION AND CONVERSION EFFICIENCY OF EACH MODULE

| | Antenna | Matching | Rectifier | PMU |
|---|---|---|---|---|
| **Loss** | 75 mV | Nearly 0 | 13.94 μW | 9.52 μW |
| **PCE** | 93% | 95% | 58% | 62% |

TABLE IX
PERFORMANCE SUMMARY AND COMPARISON OF RFEH SYSTEM WITH PREVIOUS WORKS

| | **Sensitivity** | **Power** | **Matching network** | **Rectifier** | **Technology** | **Frequency** | ***A. Spiral size* (μm ×μm )** | **Layout area ($mm^2$ )** |
|---|---|---|---|---|---|---|---|---|
| This work | **–22.5dBm** | 2 μW | On-Chip LC | 3-stage synchronous rectifier | 0.18 μm | 900 MHz | **180 ×180** | **0.25** |
| [19] | –14.1dBm | 2 μW | On-chip LC | 2-stage multiplifier | 0.18 μm | 900 MHz | 455×455 | **0.45** |
| [26] | –12.6dBm | 1μW | Off-chip LC | 3-stage full-wave rectifier | 5 μm SOI | 2.45GHz | NA | **0.50** |
| [11] | –12dBm | 2μW | On-chip stacked transformer | Dual half-wave rectifier | 0.18 μm | 3.85GHz | 230×230 | **NA** |
| [12] | –11dBm | 7.3μW | **Two on-chip LC for each frequency** | **Reconfigura ble Dickson** | **0.13**μm | 1.8GHz/2.1G Hz | **500 ×350** | **NA** |
| [22] | –20dBm | **8.5**μW | **Tri Band on-chip LC** | **Cross-couple differential drive** | **65 nm** | **0.9, 1.9, 2.4 GHz** | **400×600** | **0.37** |

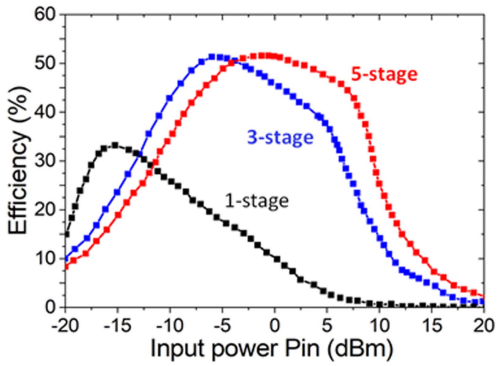



Fig. 33. Relationship between input power $P_{\text{in}}$ and rectifier's efficiency with different rectifier's stages.

next stage. For this reason, there is an optimum load impedance for each input power level and operating frequency. So, the RFEH system should be designed by optimization on the load to achieve the highest PCE.

To consider the matching between the rectifier and the PMU module, optimization should be made for higher power transmission. As shown in Fig. 8(c), the peak PCE reaches 58% with an optimal load of 80 kΩ on a single-stage rectifier. While the rectifier is connected with the followed PMU, the peak PCE would be suppressed. To optimize the matching property at this stage, multiple stages of the rectifier would be adopted. The number of stages is a critical parameter for RF energy harvesting, which should be determined optimally to obtain the maximum value of dc–dc PCE.

Fig. 33 shows the relationship between input power $P_{\text{in}}$ and the rectifier's efficiency with variable stages of the rectifier. As the number of voltage multiplier stages increases from 1 to 5, the output dc voltage level and the voltage gain of the voltage multiplier increase up to the optimal point. The number of voltage multiplier stages should be at the optimal point for the maximum dc–dc PCE. In the designed RFEH system, three stages of the synchronous rectifier are adopted, as shown in Fig. 7(e).

As shown in Fig. 33, as the number of voltage multiplier stages increases, the peak of PCE moves toward the higher power value. Fig. 33 depicts the effect of the number of stages on the PCE. The peak of PCE shifts from the lower power to the higher power region while the number of voltage multiplier stages increases. The operation of the large number of voltage multiplier stages in the low-power level environment may reduce the PCE.

Table IX presents the performance summary of the designed RFEH system. The comparison with the prior arts is also listed, especially including the full integration results [11], [12], [19], [22], [26].

## VI. RESULTS OF RFEH

The layout of the designed RFEH, including the matching circuits, the RF-DC rectifiers, and the PMU, is shown in Fig. 26, based on TSMC CMOS 0.18$\mu$m technology. The area of the layout is 0.25 $mm^2$ (0.5 mm*0.5 mm). The matching inductor is implemented using M6 of TSMC 0.18$\mu$m six-metal CMOS technology with thick-metal options. The thickness of the spiral, the dielectric constant of the substrate, and the distance between the spiral and the substrate, are provided by TSMC [57], [58].

## VII. CONCLUSION

The RFEH system is designed and implemented in this article. The key components, including the receiving antenna, the matching circuit, the RF-dc rectifier circuit, and PMU, are designed, separately. The overall simulation is conducted to testify the application of the RFEH system, showing promising PCE, as well as the stability and the robust of the controlling circuit.

For possible full integration of the RFEH system, PIFA antenna operating in the GSM 900 frequency band is designed to meet the requirements of compact size and high gain. The *LC* matching circuit structure is adopted to achieve impedance matching between the antenna and the rectifier circuit. The self-threshold compensation voltage doubling rectifier circuit is proposed, showing near-zero threshold voltage and suppressed leakage current.

The PMU is designed for the power management, providing high-precision voltage stabilization. An improved startup circuit is proposed to address the possible degeneracy problem of PMU in a zero output state. A CMOS bandgap reference circuit is designed to address the issues of high-resistance power consumption and high output reference voltage in traditional bandgap reference circuits. An improved nonresistance hysteresis comparator is designed to address the issue of high-power consumption by resistors in the traditional voltage detecting circuits. A power consumption model for PMU is established based on the parameter requirements for maximum power transmission. It shows that the starting circuit can be turned ON when the input is only 0.3 V. The static current of the bandgap reference circuit is 300 nA and can output a stable reference voltage of 1 V.

The PCE of the microwatt-level RF energy harvesting system in this article is 31.77%, which has the potential application value in fields, such as wireless energy transmission and portable device power supply.

## REFERENCES


[1] W. Zhao, P. Gadfort, K. Bhanushali, and P. D. Franzon, "RF-only logic: An area efficient logic family for RF-power harvesting applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 1, pp. 406–418, Jan. 2018, doi: 10.1109/tcsi.2017.2715321.

[2] S. K. Divakaran, D. D. Krishna, and Nasimuddin, "RF energy harvesting systems: An overview and design issues," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 29, no. 1, 2019, Art. no. e21633, doi: 10.1002/mmce.21633.

[3] H. S. Vu, N. Nguyen, N. Ha-Van, C. Seo, and M. T. Le, "Multiband ambient RF energy harvesting for autonomous IoT devices," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 12, pp. 1189–1192, Dec. 2020, doi: 10.1109/lmwc.2020.3029869.

[4] H.-K. Ra, S. Jeong, H. J. Yoon, and S. H. Son, "SHAF: Framework for smart home sensing and actuation," in *Proc. IEEE 22nd Int. Conf. Embedded Real-Time Comput. Syst. Appl.*, 2016, Paper 258.

[5] W. Sun, Y. Ge, Z. Zhang, and W.-C. Wong, "An analysis framework for interuser interference in IEEE 802.15.6 body sensor networks: A stochastic geometry approach," *IEEE Trans. Veh. Technol.*, vol. 65, no. 10, pp. 8567–8577, Oct. 2016, doi: 10.1109/tvt.2015.2502324.

[6] D. Tamilarasi, P. Ramesh, R. Krishnamoorthy, C. Bharatiraja, and T. Jayasankar, "Design of radio frequency integrated circuit for RF to DC power converter for bio-medical application," *Mater. Today, Proc.*, vol. 45, pp. 2139–2144, 2021, doi: 10.1016/j.matpr.2020.09.733.

[7] J. Bito, S. Kim, M. Tentzeris, and S. Nikolaou, "Ambient energy harvesting from 2-way talk-radio signals for smart meter and display applications," in *Proc. IEEE Antennas Propag. Soc. Int. Symp.*, 2014, pp. 1353–1354.

[8] C.-H. Li, M.-C. Yu, and H.-J. Lin, "A compact 0.9-/2.6-GHz dual-band RF energy harvester using SiP technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 7, pp. 666–668, Jul. 2017, doi: 10.1109/LMWC.2017.2711506.

[9] G. Papotto, F. Carrara, and G. Palmisano, "A 90-nm CMOS threshold-compensated RF energy harvester," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 1985–1997, Sep. 2011, doi: 10.1109/JSSC.2011.2157010.

[10] M. A. Abouzied, K. Ravichandran, and E. Sánchez-Sinencio, "A fully integrated reconfigurable self-startup RF energy-harvesting system with storage capability," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 704–719, Mar. 2017, doi: 10.1109/JSSC.2016.2633985.

[11] N. Soltani and F. Yuan, "A high-gain power-matching technique for efficient radio-frequency power harvest of passive wireless microsystems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 10, pp. 2685–2695, Oct. 2010, doi: 10.1109/TCSI.2010.2048770.

[12] A. C. C. Chun, H. Ramiah, and S. Mekhilef, "Wide power dynamic range CMOS RF-DC rectifier for RF energy harvesting system: A review," *IEEE Access*, vol. 10, pp. 23948–23963, 2022, doi: 10.1109/ACCESS.2022.3155240.

[13] P. Xu, D. Flandre, and D. Bol, "Analysis, modeling, and design of a 2.45-GHz RF energy harvester for SWIPT IoT smart sensors," *IEEE J. Solid-State Circuits*, vol. 54, no. 10, pp. 2717–2729, Oct. 2019, doi: 10.1109/JSSC.2019.2914581.

[14] Z. Zeng, S. Shen, B. Wang, J. J. Estrada-López, R. Murch, and E. Sánchez-Sinencio, "An ultra-low-power power management circuit with output bootstrapping and reverse leakage reduction function for RF energy harvesting," in *Proc. IEEE/MTT-S Int. Microw. Symp.*, 2020, pp. 1059–1062.

[15] S. Nagaveni, P. Kaddi, A. Khandekar, and A. Dutta, "Resistance compression dual-band differential CMOS RF energy harvester under modulated signal excitation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 11, pp. 4053–4062, Nov. 2020, doi: 10.1109/TCSI.2020.3006156.

[16] Y. X. Guo, M. Y. W. Chia, and Z. N. Chen, "Miniature built-in multiband antennas for mobile handsets," *IEEE Trans. Antennas Propag.*, vol. 52, no. 8, pp. 1936–1944, Aug. 2004.

[17] D.-G. Kang and Y. Sung, "Compact hexaband PIFA antenna for mobile handset applications," *IEEE Antennas Wireless Propag. Lett.*, vol. 9, no. 11, pp. 1127–1130, Nov. 2010, doi: 10.1109/LAWP.2010.2095407.

[18] W. X. Lian et al., "A fully-integrated CMOS dual-band RF energy harvesting front-end employing adaptive frequency selection," *IEEE Access*, vol. 11, pp. 74121–74135, 2023, doi: 10.1109/ACCESS.2023.3296145.

[19] A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, and F. De Flaviis, "Power harvester design for passive UHF RFID tag using a voltage boosting technique," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 6, pp. 1089–1097, Jun. 2007.

[20] Y. Wang, J. Zhang, Y. Chen, J. Ren, and S. Ma, "A 4.5-W, 18.5–24.5-GHz GaN power amplifier employing Chebyshev matching technique," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 31, no. 2, pp. 233–242, Feb. 2023, doi: 10.1109/TVLSI.2022.3225967.

[21] S.-K. Li, P. Guo, D. Yi, and M.-C. Tang, "Ultra-wideband 3-way equal-power divider based on multi-section Chebyshev matching method," in *Proc. IEEE MTT-S Int. Microw. Workshop Ser. Adv. Mater. Processes RF THz Appl.*, 2021, pp. 320–322, doi: 10.1109/IMWS-AMP53428.2021.9643931.

[22] J. K. Yong et al., "A fully integrated CMOS tri-band ambient RF energy harvesting system for IoT devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 12, pp. 4705–4718, Dec. 2023, doi: 10.1109/TCSI.2023.3304664.

[23] Z. Liu, Y.-P. Hsu, B. Fahs, and M. M. Hella, "An RF-DC converter IC with on-chip adaptive impedance matching and 307-μw peak output power for health monitoring applications," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 26, no. 8, pp. 1565–1574, Aug. 2018, doi: 10.1109/TVLSI.2018.2822120.

[24] A. Mohan and S. Mondal, "An impedance matching strategy for micro-scale RF energy harvesting systems," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 68, no. 4, pp. 1458–1462, Apr. 2021, doi: 10.1109/TCSII.2020.3036850.

[25] M. A. Abouzied and E. Sánchez-Sinencio, "Low-input power-level CMOS RF energy-harvesting front end," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 11, pp. 3794–3805, Nov. 2015, doi: 10.1109/TMTT.2015.2479233.

[26] P.-H. Chen et al., "0.18-V input charge pump with forward body biasing in startup circuit using 65nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, 2010, pp. 1–4, doi: 10.1109/CICC.2010.5617444.

[27] M. A. Karami and K. Moez, "Systematic co-design of matching networks and rectifiers for CMOS radio frequency energy harvesters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 3238–3251, Aug. 2019, doi: 10.1109/TCSI.2019.2902506.

[28] Z. Hameed and K. Moez, "Design of impedance matching circuits for RF energy harvesting systems," *Microelectron. J.*, vol. 62, pp. 49–56, Apr. 2017, doi: 10.1016/j.mejo.2017.02.004.

[29] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-μW minimum RF input power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1608, Oct. 2003.

[30] C. R. Valenta and G. D. Durgin, "Harvesting wireless power: Survey of energy-harvester conversion efficiency in far-field, wireless power transfer systems," *IEEE Microw. Mag.*, vol. 15, no. 4, pp. 108–120, Jun. 2014.

[31] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2005, pp. 34–51.

[32] Z. Hameed and K. Moez, "A 3.2 V×15 dBm adaptive threshold-voltage compensated RF energy harvester in 130 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 948–956, Apr. 2015.

[33] Y. Lu et al., "A wide input range dual-path CMOS rectifier for RF energy harvesting," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 64, no. 2, pp. 166–170, Feb. 2017.

[34] Z. Hameed and K. Moez, "Hybrid forward and backward threshold-compensated RF-DC power converter for RF energy harvesting," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 4, no. 3, pp. 335–343, Sep. 2014.

[35] D. Khan et al., "A CMOS RF energy harvester with 47% peak efficiency using internal threshold voltage compensation," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 6, pp. 415–417, Jun. 2019.
[36] M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips, and W. A. Serdijn, "Co-design of a CMOS rectifier and small loop antenna for highly sensitive RF energy harvesters," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 622–634, Mar. 2014.
[37] B. Li, X. Shao, N. Shahshahan, N. Goldsman, T. Salter, and G. M. Metze, "An antenna co-design dual band RF energy harvester," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 12, pp. 3256–3266, Dec. 2013.
[38] A. K. Moghaddam, J. H. Chuah, H. Ramiah, J. Ahmadian, P.-I. Mak, and R. P. Martins, "A 73.9%-efficiency CMOS rectifier using a lower DC feeding (LDCF) self-body-biasing technique for far-field RF energy harvesting systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 992–1002, Apr. 2017.
[39] A. K. Moghaddam, A. C. C. Choo, H. Ramiah, and K. K. P. Churchill, "A self-protected, high-efficiency CMOS rectifier using reverse DC feeding self-body-biasing technique for far-field RF energy harvesters," *AEU-Int. J. Electron. Commun.*, vol. 152, Jul. 2022, Art. no. 154238.
[40] H. Yi, J. Yin, P.-I. Mak, and R. P. Martins, "A 0.032-mm$^2$ 0.15-V three-stage charge-pump scheme using a differential bootstrapped ring-VCO for energy-harvesting applications," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 65, no. 2, pp. 146–150, Feb. 2018, doi: 10.1109/TCSII.2017.2676159.
[41] M. B. Machado, M. C. Schneider, and C. Galup-Montoro, "On the minimum supply voltage for MOSFET oscillators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 2, pp. 347–357, Feb. 2014.
[42] M. Ashraf and N. Masoumi, "A thermal energy harvesting power supply with an internal startup circuit for pacemakers," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 1, pp. 26–37, Jan. 2016.
[43] M. Dezyani, H. Ghafoorifard, S. Sheikhaei, and W. A. Serdijn, "A 60 mV input voltage, process tolerant start-up system for thermoelectric energy harvesting," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 10, pp. 3568–3577, Oct. 2018.
[44] S. Bose and M. L. Johnston, "A stacked-inverter ring oscillator for 50 mV fully-integrated cold-start of energy harvesters," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2018, pp. 1–5.
[45] M. Arrawatia, M. S. Baghini, and G. Kumar, "Broadband bent triangular omnidirectional antenna for RF energy harvesting," *IEEE Antennas Wireless Propag. Lett.*, vol. 15, no. 4, pp. 36–39, Apr. 2016, doi: 10.1109/lawp.2015.2427232.
[46] L. Li and Y. Jiang, "Design of synchronous RF-DC rectifier for energy harvesting system," *Int. J. Electron.*, vol. 111, no. 3, pp. 442–464, 2024, doi: 10.1080/00207217.2022.2164076.
[47] H. Raben, J. Borg, and J. Johansson, "Improved efficiency in the CMOS cross-connected bridge rectifier for RFID applications," in *Proc. 18th Int. Conf. Mixed Des. Integr. Circuits Syst.*, 2011, pp. 334–339.
[48] X. Han, Z. Zhang, Y. Tan, G. Xie, and Z. Cheng, "A 13.56 MHz low-voltage RF-DC rectifier with controlled vth cancellation technique," in *Proc. IEEE Int. Symp. Radio Freq. Integr. Technol.*, 2014, pp. 1–3.
[49] P. T. Theilmann, C. D. Presti, D. J. Kelly, and P. M. Asbeck, "A $\mu$m complementary bridge rectifier with near zero turn-on voltage in SOS CMOS for wireless power supplies," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 9, pp. 2111–2124, Sep. 2012.
[50] Z. Wu, Y. Zhao, Y. Sun, H. Min, and N. Yan, "A self-bias rectifier with 27.6% PCE at -30 dBm for RF energy harvesting," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2021, pp. 1–5.
[51] D. Khan et al., "An efficient reconfigurable RF-DC converter with wide input power range for RF energy harvesting," *IEEE Access*, vol. 8, pp. 79310–79318, 2020.
[52] Q. Cui, C. Zhang, Y. Guo, Y. Zhang, Y. Zhang, and F. Yuan, "A 1.8 V output RF energy harvester at input available power of −20 dBm," in *Proc. IEEE 3rd Int. Conf. Integr. Circuits Microsyst.*, 2018, pp. 33–37.
[53] D. Khan et al., "A 2.45 GHz high efficiency CMOS RF energy harvester with adaptive path control," *Electronics*, vol. 9, no. 7, 2020, Art. no. 1107.
[54] S.-H. Lin, C.-Y. Kuo, S.-Y. Lu, and Y.-T. Liao, "A high-efficiency power management IC with power-aware multi-path rectifier for wide-range RF energy harvesting," in *Proc. IEEE MTT-S Int. Microw. Symp.*, 2017, pp. 304–306.
[55] S. Fan et al., "A 2.45-GHz rectifier-booster regulator with impedance matching converters for wireless energy harvesting," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3833–3843, Sep. 2019.
[56] L. Xia, J. Cheng, N. E. Glover, and P. Chiang, "0.56 V, –20 dBm RF-powered, multi-node wireless body area network system-on-a-chip with harvesting-efficiency tracking loop," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1345–1355, Jun. 2014, doi: 10.1109/jssc.2014.2305074.
[57] Z. Zhang, X. Xin, R. Chuai, and M. Han, "An ultra-low power off chip capacitor-less LDO with high transient response," *J. Phys., Conf. Ser.*, vol. 2209, 2022, Art. no. 012002.
[58] T. Y. Man, P. K. T. Mok, and M. Chan, "A high slew-rate push-pull output amplifier for low-quiescent current low-dropout regulators with transient-response improvement," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 54, no. 9, pp. 755–759, Sep. 2007, doi: 10.1109/tcsii.2007.900347.
[59] M. Moradian Boanloo and M. Yavari, "A low-power high-gain low-dropout regulator for implantable biomedical applications," *Circuits, Syst., Signal Process.*, vol. 40, no. 3, pp. 1041–1060, 2020, doi: 10.1007/s00034-020-01520-9.

**Lanyu Li** was born in Henan, China, in 1998. She received the B.S. degree in microelectronics science and engineering and the M.S. degree in integrated circuit engineering under the supervision of Prof. Y. Jiang from Jiangnan University, Wuxi, China, in 2020 and 2023, respectively.

She is currently working with Wuxi Taihu University, Wuxi, China. Her main research direction is integrated circuit design.

**Yanfeng Jiang** (Senior Member, IEEE) was born in Jilin, China, in 1972. He received the B.S. degree in electrical engineering from Southeast University, Nanjing, China, in 1993, and the Ph.D. degree in microelectronics from Lanzhou University, Lanzhou, China, in 2000.

He is currently a Full Professor with Jiangnan University, Wuxi, China. His research interests include integrated circuit design, MEMS, power semiconductor devices, and magnetic devices.