Design and Analysis of Reconfigurable Resonant Converter With Ultrawide Output Voltage Range

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***Abstract*—In this article, a reconfigurable isolated dc/dc converter is proposed suitable for a wide output voltage range of 180–1500 V for efficient onshore charging in maritime applications. The proposed circuit concept can also fulfill the requirements of other heavy-duty battery charging applications, especially those operating within the shore environment—such as straddle carriers, forklifts, reach stackers, and terminal tractors. The circuit topology consists of two interleaved *LLC* resonant converters each connected to a three-winding transformer. Through the use of additional circuitry, the topology can be adapted to operate at peak efficiency in three output voltage ranges. Furthermore, the topology is able to alleviate the current and voltage stresses on the semiconductor devices in comparison to the conventionally employed *LLC* resonant converters. The operation of the circuit is explained and its steady-state model is developed. In order to validate the performance of the converter, an 11-kW prototype is designed, tested, and analyzed. The experimental results attest that the proposed reconfigurable resonant converter is able to achieve an extremely wide output voltage range while maintaining a high power transfer efficiency.**

***Index Terms*—Electromobility, isolated dc–dc converter, power conversion, reconfigurability, resonant converter.**

I. Introduction

THE maritime transportation industry has increasingly embraced dc-based distribution systems in recent years. This shift is driven by several factors such as the elimination of additional ac/dc conversion stages in propulsion drives, the seamless integration of dc-based energy sources such as battery packs, fuel cells, and solar arrays, as well as the development of fast and reliable solid-state breakers [1]. This makes the adoption of dc distribution more favorable for the maritime sector in its efforts to curb greenhouse gas emissions. Therefore, dc architecture is being adopted more commonly on board, particularly in battery-powered water taxis, boats, and ferries [2], [3]. An onshore charging framework for such a vessel is shown in Fig. 1, which features a dc shore bus. The availability of a dc bus at the shore is useful for incorporating distributed energy sources at the shore and helps in reducing the peak power demand from the grid. The onshore batteries are charged slowly throughout the day and discharged quickly once the boat arrives at the shore for charging. It is pertinent to mention that there is often a separate converter located on board to charge the battery from its main dc bus while the shore-to-vessel (S2V) dc/dc converters shown in Fig. 1 are used to feed power into the bus. They adjust the output voltage to match the bus voltage of the incoming boat to deliver energy to the onboard system. However, in different battery-powered vessels, the onboard bus voltages can differ significantly from one another resulting in an extremely wide voltage range [typically within the low-voltage (LV) dc range of under 1500 V]. Therefore, charging infrastructure manufacturers often need to set up dedicated stations for individual vessels and also for other electric transportation systems operating around the shore environment. This is due to the inherent limitation of conventional dc/dc converters to operate stably and efficiently over a wide voltage range making the design of a multifunctional converter challenging.

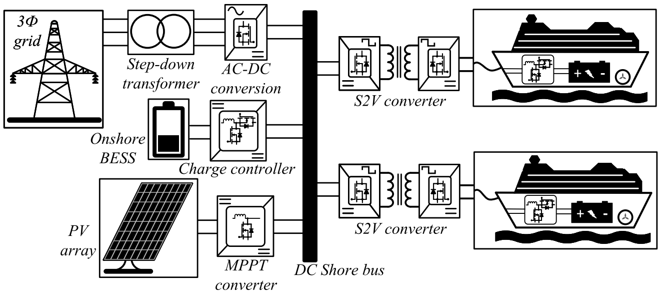

Fig. 1. S2V power electronics framework with an onshore DC bus; the high charging power often necessitates the use of onshore BESS.

The design of wide output voltage range dc/dc converters has been the subject of extensive research in power electronics for various applications. In recent years, there has been an impetus

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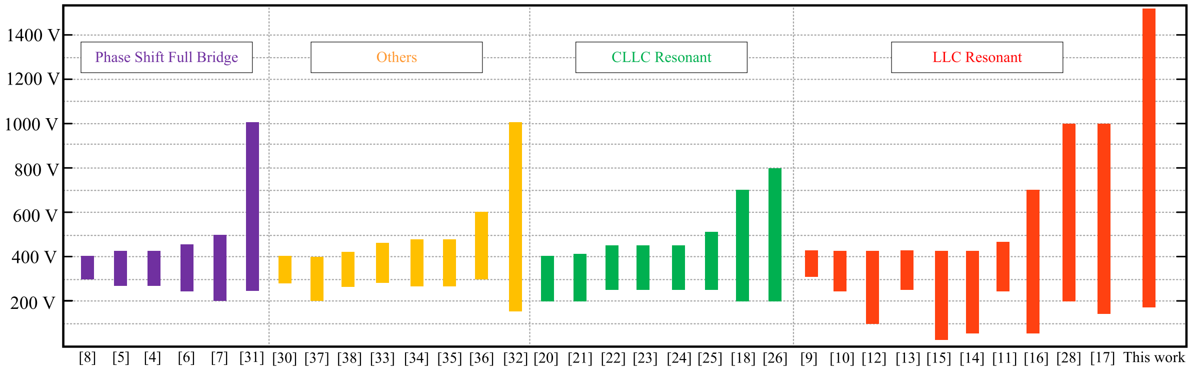


Fig. 2. Overview of output voltage ranges for various DC–DC converters reported in the literature for wide voltage applications in recent years; some common themes are not repeated and only studies with experimental designs and maximum voltages of at least 350 V are listed.

for the development of public high-power fast-charging stations for electric cars capable of operating over a wide range of output voltage to facilitate charging of different vehicles, including heavy-duty ones, which may have different battery voltage classes and charging profiles. Fig. 2 summarizes a survey of the available literature on isolated dc/dc converters researched for electric vehicle (EV) charging applications and their applicable voltage ranges. It can be seen that the most commonly used back-end topologies used in EV charging are the phase-shift full-bridge (PSFB) and the series resonance-based converters. Both circuit technologies can operate with phase-shift control of their H-bridge converter, which can reach their highest efficiency when operating at the highest output voltage. However, as the phase-shift control angle between the bridge legs increases or the output voltage decreases, the efficiency of the converter will decline because of the increased circulating reactive power. In order to make the topology efficient over a wider range, several topological and control modifications have been proposed [4], [5], [6], [7], [8].

Resonant power converters (RPCs) have also garnered significant attention in research due to their high peak efficiency, which is attributed to low switching losses resulting from zero-voltage switching (ZVS) and zero-current switching (ZCS). Typically, in the most common topology that is the *LLC* converter, pulse-frequency modulation (PFM) is employed to control the RPCs and a wide output voltage variation implies a wide frequency variation, which can lead to a suboptimal design for magnetics, poor overall efficiency, and EMI issues. Several methods have been proposed for improving the efficiency with wider voltage regulation for *LLC* RPCs [9], [10], [11], [12], [13], [14], [15]. A commonly employed method in EV chargers is the change of input dc-link voltage while keeping the RPC voltage gain unchanged and thereby operating it at peak efficiency. However, this is not possible in the onshore charging interface shown in Fig. 1 as the shore dc bus voltage is fixed and other power converters connected to it are optimized for that specific voltage. An alternative approach is to operate the resonant converter at peak efficiency and incorporate an additional buck stage for catering to the voltage variation while the resonant converter only provides isolation and unity voltage gain [16], [17]. However, additional circuitry and dependence of the efficiency on the buck stage emerge as two limiting factors for a wide operating range. The implementation of phase-shift modulation (PSM) in conjunction with PFM enables a more flexible voltage-gain performance and narrower switching frequency range albeit at the expense of an increase in circulating losses and control complexity [18], [19]. Employing phase shifts for efficiency improvement is further explored in *CLLC* converters where the presence of multiple active bridges allows for a more complex control scheme involving multiple phase shifts [20], [21], [22], [23], [24], [25], [26]. In RPCs, the output voltage is always linearly dependent on the turns ratio of the isolating transformer. Modifying the effective turns while switching the converter near the resonant frequency is, therefore, a natural approach to maximize efficiency. This approach has been carried out in [27], [28], and [29] through the use of reconfiguring tap changers on the secondary side. However, eradicating a certain number of turns reduces the flux linkage, the effective window area, and copper utilization on the secondary side, thereby derating the transformer and the system severely. Some other approaches include using additional active semiconductor devices, multiport transformers, cascaded or interleaved architectures, etc. [30], [31], [32], [33], [34], [35], [36], [37], [38]. However, among these variants of full-bridge and resonant converters, no work demonstrates a wide output voltage range that goes up to 1500 V, as shown in Fig. 2.

In order to increase the return on investment, fast charger manufacturers are incentivized to maximize the compatibility of their products with different vehicle classes. In Norway, Kempower and Evoy have deployed fast-charging stations in harbor areas that can be used for charging cars as well as boats while other commercial solutions such as the ABB Terra, EVBox Troniq, and Porsche Charge Box are also compatible with different EVs. However, these solutions use conventional power converter topologies and, therefore, perform suboptimally over different output voltages, which serve as the motivation for this work.

The authors first introduced the circuit concept in [39] and this article analyzes the *LLC*-based variant of the proposed converter, which can otherwise be configured as a PSFB or any of the commonly used RPCs with a cascaded or interleaved primary side. The converter is designed to operate at a peak efficiency for output voltages of 375, 750, and 1500 V without derating the converter power. The topology uses an interleaved

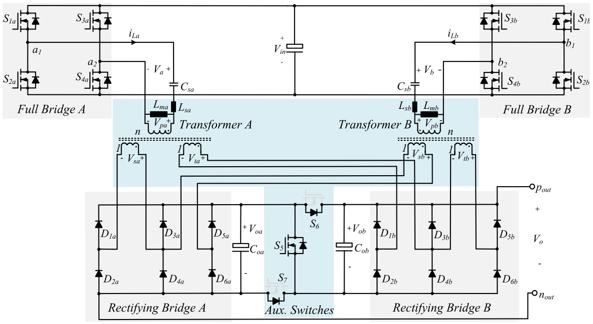


Fig. 3. Circuit topology of the proposed resonant converter comprising two interleaved full bridges with reconfigurability enabled using a double three-winding transformer structure and auxiliary switches.

structure on the primary sides of three-winding transformers and three-legged diode bridges on the secondary sides, which can be reconfigured in series or parallel using three auxiliary low-frequency switches. This design allows for the utilization of more reliable semiconductor devices with lower voltage and current ratings while ensuring good efficiency across a broad output voltage range. The contribution of this work is summarized as follows.

1) The operation and principle of the proposed reconfigurable resonant converter (RRC) are detailed. Moreover, other potential variants of the topology are identified, highlighting their advantages and drawbacks.
2) A steady-state model explaining the operation and behavior of the converter is derived and used in the design of the converter prototype and its magnetics.
3) The performance of the topology is experimentally verified on an 11-kW prototype, which is operated in a wide voltage range (180–1500 V) and compared with the performance of a conventional *LLC* RPC.
4) Additional modifications to potentially improve the efficiency of the converter even further in the future are identified.

The rest of this article is organized as follows. Section II explains the operation and working principle of the topology. In Section III, the converter model is developed. The design guidelines for the converter are detailed in Section IV. The experimental results are presented in Section V. Finally, Section VI concludes this article.

II. TOPOLOGY AND PRINCIPLE OF OPERATION

The circuit topology of the proposed RRC is presented in Fig. 3. The converter comprises of an interleaved *LLC* full bridge on the primary sides of two three-winding transformers A and B. The corresponding full-bridge MOSFETs $S_{1a} - S_{4a}$ and $S_{1b} - S_{4b}$, which are fed from the dc-bus input V_{in}, collectively form the actively switching semiconductor devices during converter operation. The secondary side of each transformer consists of a pair of three-legged diode bridges, each with a dc-side capacitance of its own. The rectifying bridges are interconnected through low-frequency auxiliary switches S_5, S_6, and S_7, which can be assembled via semiconductor technology or as mechanical power relays. The converter output is fed from the positive rail of diode bridge B and the negative rail of diode bridge A.

A. Reconfiguration of the Topology

The RRC, as depicted in Fig. 3, offers circuit reconfigurability through the auxiliary switches S_5, S_6, and S_7 on the secondary side. Turning ON of S_5 is accompanied by turning OFF of both S_6 and S_7. As a result, the left (A) and right (B) rectifying bridges are cascaded. This effectively provides voltage doubling at the output. Conversely, when S_5 is turned OFF, both S_6 and S_7 are turned ON, configuring the left and right rectifying bridges in parallel and providing current doubling at the output. Furthermore, the three-legged rectifying bridge can be utilized to connect the two secondary sides and the two tertiary sides of the transformers in series or in parallel with each other, respectively. This configuration leads to an equivalent circuit that again doubles the output voltage or current, depending on the mode selected. Achieving this requires aligning the phase-shift (in-phase or antiphase) of the primary-side parallel full-bridges with respect to each other. The different possible configurations are further explained in Fig. 4.

1) *Mode I [see Fig. 4(a)]:* In this mode, S_5 is ON while S_6 and S_7 are OFF. H-bridges A and B are operated in-phase, that is, during the positive half-cycle when S_{1a} and S_{4a} are ON, then S_{1b} and S_{4b} are also ON [Mode I (+)]. In this scenario, when the primary-side bridges are in phase, the secondary diodes D_{2a} and D_{5a}, as well as D_{2b} and D_{5b}, are effectively connected in series through transformer windings (assuming identical capacitor currents). Consequently, the load voltage V_o is four times the magnitude of the voltage across any of the secondary windings. Similarly, during the negative half-cycle, the complementary semiconductor devices conduct on each leg of the H-bridge and rectifying bridge [Mode I (-)]. This condition corresponds to the maximum voltage that can be obtained at the output terminals.
2) *Mode II [see Fig. 4(b)]:* In this mode, S_5 is turned OFF while S_6 and S_7 are ON. Under this condition, when H-bridges A and B are operated in-phase, during the positive half-cycle [Mode II (+)], the secondary diodes D_{5a} and D_{2a} are connected in series and the resulting combination is paralleled with the series connection of D_{5b} and D_{2b}. Therefore, the load voltage V_o is twice the magnitude of the voltage across any of the secondary windings. This condition leads to a current and voltage doubling effect at the output.
3) *Mode III [see Fig. 4(c)]:* Similar to Mode I, here S_5 is ON while S_6 and S_7 are OFF. However, the H-bridges A and B are now switched antiphase, that is, the positive half-cycle of A when S_{1a} and S_{4a} are ON coincides with the negative half-cycle of B where S_{2b} and S_{3b} are ON [Mode III (+)]. The resulting circuit leads to the conduction of one of the diodes in each leg of the secondary circuit with the central diode in each rectifying bridge carrying twice the current of noncentral legs. The load voltage V_o in this case

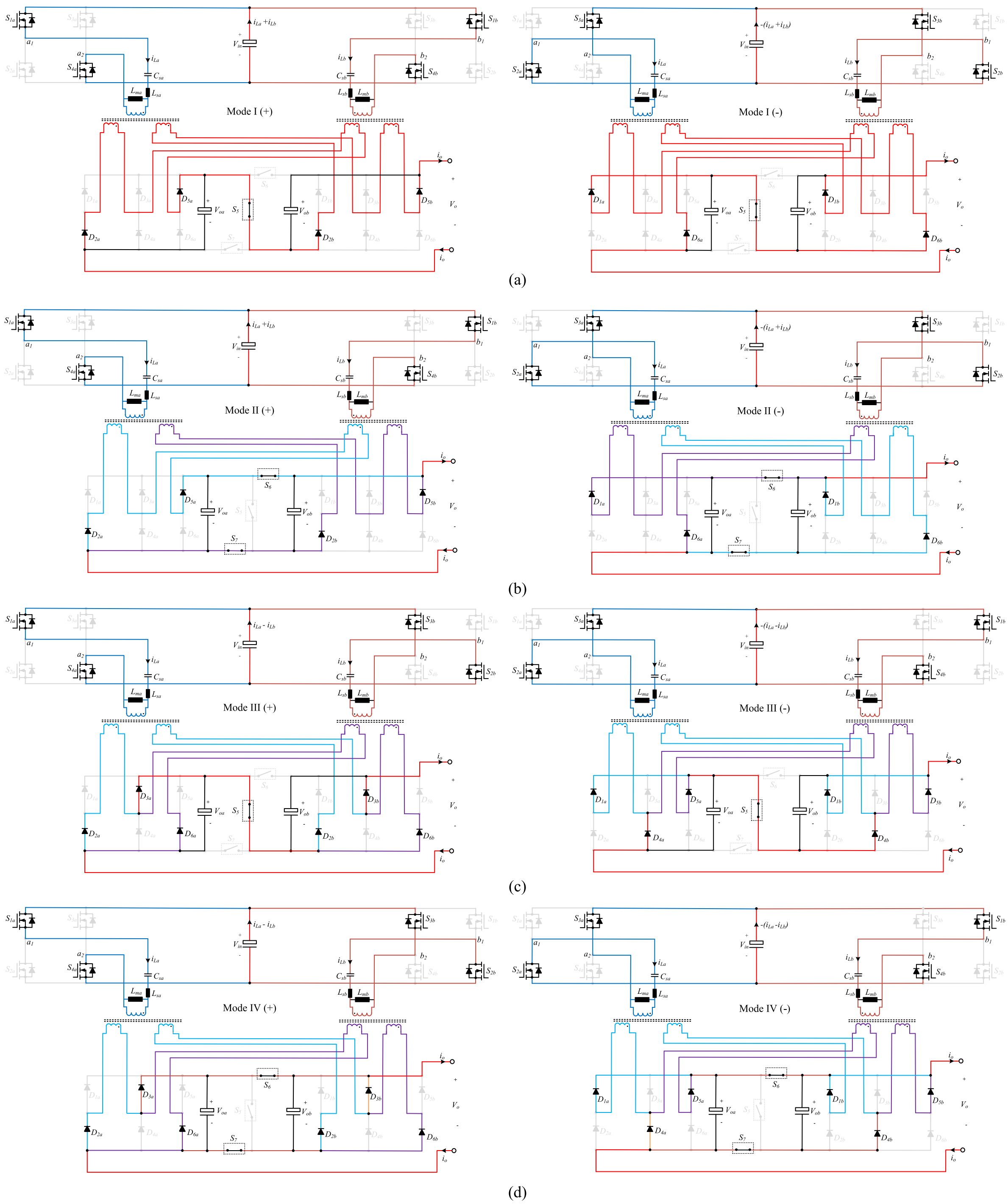


Fig. 4. Operating modes of the proposed converter for positive (+) and negative half-cycles (-) illustrating the effect of primary-side bridge synchronization and auxiliary switch selection on the equivalent connection of secondary-side windings with respect to the output terminals. (a) Mode I: Voltage quadrupling mode with all four windings in series. (b) Mode II: Voltage and current doubling under in-phase operation of the H-bridges. (c) Mode III: Voltage and current doubling under antiphase operation. (d) Mode IV: Current quadrupling mode with all four windings in parallel under antiphase operation of the H-bridges.

is also twice the magnitude of the voltage across each secondary winding. Therefore, this configuration serves as a redundancy for Mode II for voltage and current doubling.

4) *Mode IV [see Fig. 4(d)]:* Similar to Mode II, here S_5 is OFF while S_6 and S_7 are ON while the H-bridges operate in phase opposition similar to Mode III. The resulting circuit leads to the conduction of one of the diodes in each leg of the secondary circuit and the auxiliary switches ensure that all windings are now paralleled with each other. Therefore, the load voltage V_o equals the magnitude of the voltage across each secondary winding. This configuration leads to a current quadrupling effect at the output and leads to the minimum output voltage among all four modes.

The reconfiguration through modes I–IV allows voltage/current amplification at the output terminals by a factor of up to four. The voltage amplification results in a current decrease. Thus, the winding currents and voltages do not change making the circuit reconfiguration power invariant at the output. Ideally, the capacitor voltages V_{oa} and V_{ob} evenly split the output voltage V_o. Therefore, the blocking voltages across the output capacitance, diodes, and auxiliary switches are always half of the output voltage. It can also be observed that the currents in central leg diodes (D_{3a}, D_{4a}, D_{3b}, D_{4b}) are twice the value of current in other diodes during Modes II and IV. This can be compensated by using two hard-paralleled diodes for each one in the central leg allowing the use of eight identical diodes on each secondary-side bridge. On the primary sides, the voltages and currents are always evenly shared between the H-bridges. Furthermore, it is important to admit that in a conventional *LLC* RPC, the presence of a load is paramount to prevent overvoltage at the output due to its inherent current source behavior. In the case of the proposed RRC, this condition is extended to also include the state of auxiliary switches since it is necessary to have either the series switch or the parallel switches ON for delivering current to the load. The use of diodes as parallel auxiliary switches caters to this issue at the expense of additional power losses.

B. *Other Variations of the Topology*

The proposed circuit concept can theoretically be used in any of the commonly used full-bridge-based isolated dc/dc converters. Therein, when the converter is fed from a higher voltage, the primary-side full bridges can be cascaded instead of being paralleled. The reconfiguration circuit remains the same and the operating modes also do not change. However, the current stresses in that case on all the primary-side components are naturally doubled while the voltage stresses on the MOSFETs are halved. Since the topology is aimed to be used in LV, high-current charging systems, the cascading on the primary side is not as favorable as interleaving, as the current stresses can be quite high. Moreover, one or both of the primary side H-bridges can be operated in half-bridge mode by clamping the low-side MOSFET of one leg to the negative rail. This is a commonly employed practice in full-bridge-based converters and can result in the creation of additional voltage ranges [40]. For example, if the converters are operating in phase and the auxiliary switch S_5 is ON, clamping one of the converters to half-bridge mode can result in a voltage tripling effect instead of quadrupling, thereby providing an intermediate operational region. Since each of the H-bridges is connected through the three-winding transformer to both rectifying bridges, the converter can also be operated partially by switching just one of the H-bridges. Naturally, these interventions reduce the voltage and power capability of the converter but can prove to be beneficial for high-efficiency operation at light load. These variations present natural redundancies in the proposed topology but lead to unequal power sharing between the modules, which can adversely affect the reliability of the converter due to asymmetrical degradation and therefore are not considered further in this work.

III. STEADY-STATE CONVERTER MODEL

Conventionally, the converter output of *LLC* RPCs is regulated through PFM, PSM, or a hybrid control combining the variation of frequency with that of phase shift. The latter is also known as dual control (DC). Therein, in the simplest method of employing DC, there may be a switchover condition, based on a predefined maximum switching frequency or a duty cycle that serves as a point of transition from PFM to PSM or vice versa [41]. Optimization of DC for use of different semiconductor technology in the two legs such that one leg exhibits ZVS turn-ON and the other exhibits ZCS turn-OFF for an overall reduction of losses is also possible [19], [42]. Another approach is to develop a steady-state control polynomial relating operating frequency and duty cycle to always minimize the circulating current required for achieving ZVS turn-ON in both legs [43]. In the proposed RRC, any of these schemes can be used once the steady-state converter model is developed.

A. *Converter Operation With PFM*

For the RRC, if the phase shift between the bridges is limited to in-phase and antiphase operation, a linear FHA-based model, as shown in Fig. 5, can be used as an equivalent circuit to derive the gain characteristics with PFM. The effect of changing the state of auxiliary switches and the phase shift between the primary-side bridges is incorporated by the varying effective turns ratio n_{eff}, which can alter the effective output voltage and current. Furthermore, since the currents in the primary-side bridges are shared evenly, the power delivered by each bridge, and in turn, the effective quality factor (Q) is halved. This is reflected in the equivalent circuit where the tank impedances are paralleled and collectively feed the entire load. This effectively results in the same Q as the actual circuit and does not alter the resonant frequency. With these modifications and under the assumption of identical tank parameters ($C_{sa} = C_{sb} = C_s$, $L_{sa} = L_{sb} = L_s$, and $L_{ma} = L_{mb} = L_m$), FHA can be employed to evaluate the converter output voltage for a given switching frequency (f_{sw})

$$V_o = \frac{V_{\text{in}}}{n_{\text{eff}}} \frac{1}{\sqrt{\left(1 + \frac{1}{\lambda} - \frac{1}{\lambda f_n^2}\right)^2 + Q^2 \left(f_n - \frac{1}{f_n}\right)^2}} \tag{1}$$

wherein the parameters are defined as follows:

$$n_{\text{eff}} = \begin{cases} n/4 & \text{for Mode I} \\ n/2 & \text{for Mode II and III} \\ n & \text{for Mode IV} \end{cases} \tag{2}$$

$$\text{Effective total ac resistance,} \quad R_{\text{ac}} = \frac{8V_o^2}{\pi^2 P_{\text{load}}} \tag{3}$$

$$\text{Reflected resistance to each tank,} \quad R_{\text{ref}} = \frac{8n_{\text{eff}}^2 V_o^2}{\pi^2 P_{\text{load}}/2} \tag{4}$$

$$\text{Quality factor,} \quad Q = \frac{\pi^2 \sqrt{L_s/C_s}}{8n_{\text{eff}}^2} \frac{P_{\text{load}}/2}{V_o^2} \tag{5}$$

$$\text{Resonant frequency,} \quad f_r = \frac{1}{2\pi\sqrt{L_s C_s}} \tag{6}$$

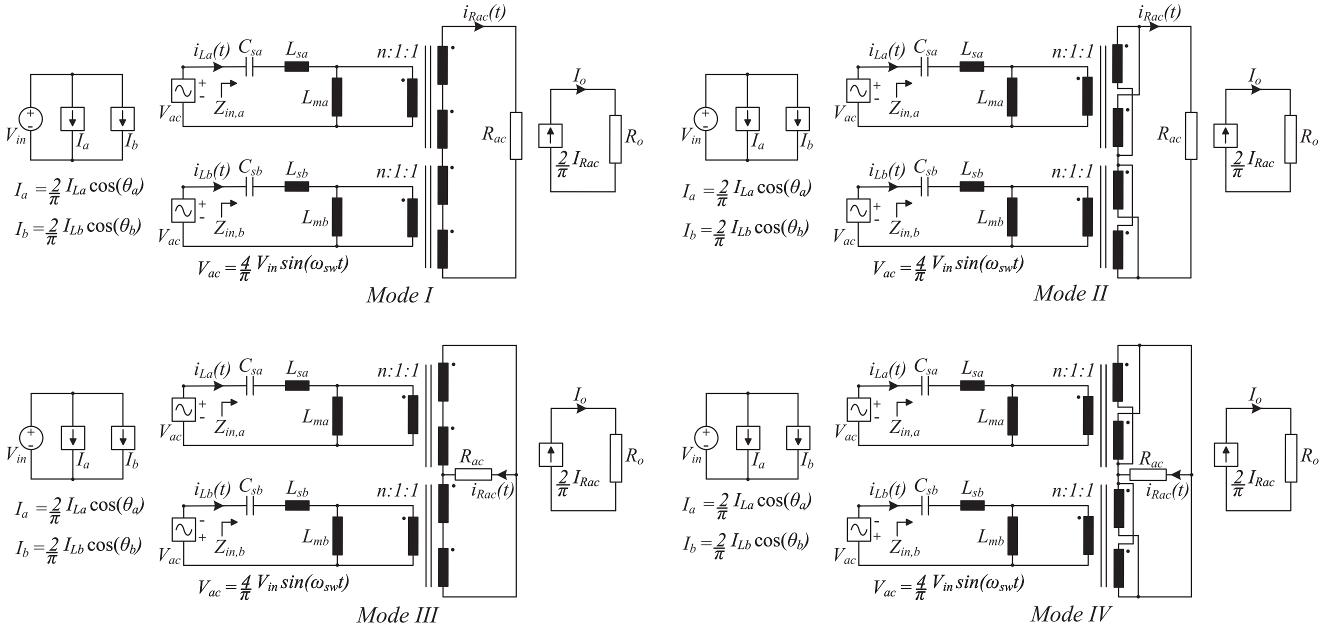


Fig. 5. FHA-based steady-state equivalent circuit for PFM of the proposed converter.

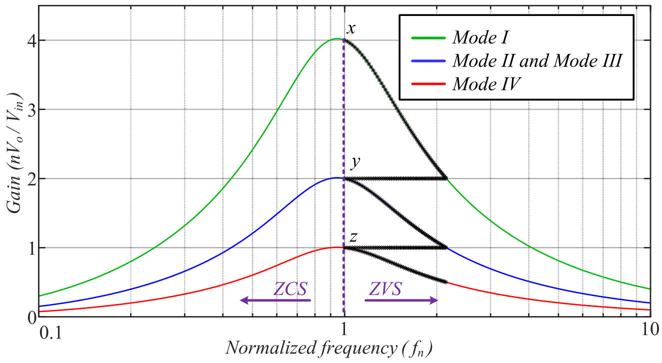


Fig. 6. RRC voltage-gain variation with PFM for different modes with $\lambda = 10$; the three curves correspond to an identical $Q = 1$ for the resonant tanks.

$$\text{Normalized frequency,}\quad f_n = \frac{f_{\text{sw}}}{f_r} = \frac{\omega_{\text{sw}}}{\omega_r} \tag{7}$$

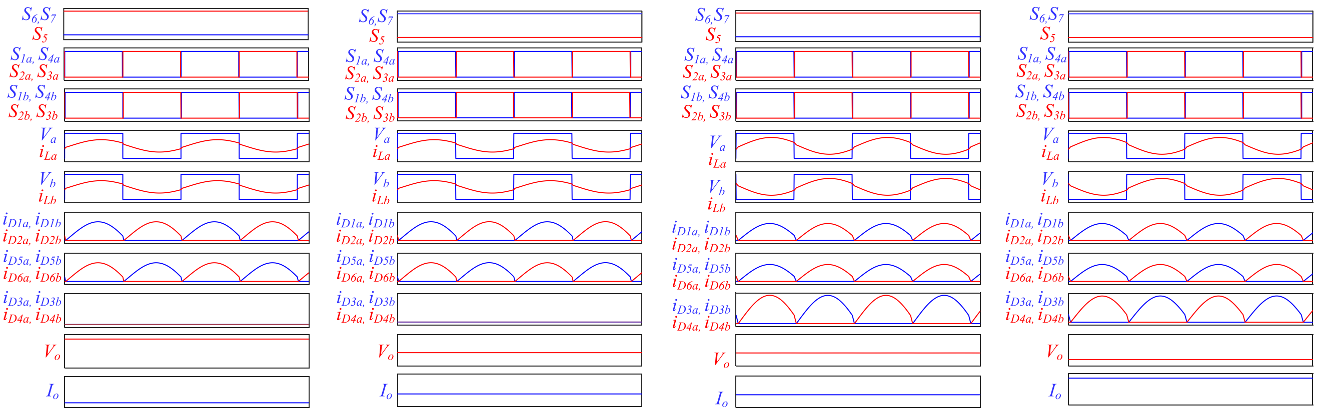
$$\text{Inductance ratio,}\quad \lambda = \frac{L_m}{L_s}. \tag{8}$$

The effect of circuit reconfigurability on the converter gain can be analyzed through (1). This is illustrated in Fig. 6, which plots the voltage-gain characteristics of the RRC converter, for an inductance ratio, $\lambda = 10$. With the other parameters unchanged, a smaller λ would lead to narrower gain curves, higher peak voltage, and easier regulation. Nevertheless, it also leads to a higher magnetizing current, circulation losses, and concerns regarding closed-loop stability. For the proposed RRC, the dependence of voltage output on the operating mode yields a much narrower frequency band for a wide voltage range compared to a conventional *LLC* converter, which can operate in only one mode. As previously mentioned, the circuit transformation is power invariant and avoids derating of the converter. This is indicated by points x, y, and z, which can result in different voltages across the output terminals while keeping the winding currents and voltages unchanged. It follows that their corresponding curves effectively impose the same quality factor on the H-bridge resonant tanks, thereby making the frequency regulation of the three curves similar. The operating waveforms of the RRC for different operating modes are shown in Fig. 7 wherein the voltage and current amplification can be observed on the basis of phase shift and state of auxiliary switches.

With PFM, it is desired to operate the converter in the region where the slope of the gain curve is negative. For all loads, this is achieved by operating the converter at switching frequencies greater than the resonant frequency. This ensures that both the resonant tanks drive an inductive impedance, which is one of the necessary conditions to enable ZVS turn-ON in the H-bridge MOSFETS, the other pertains to the timely discharge of MOSFET capacitances during commutation and will be discussed later. The average input current $(I_a + I_b)$ is a function of the effective input impedance angles θ_a and θ_b, which are reflective of the fundamental power factor angles and dictate the circulating current flow in the circuit. When the H-bridges are operated just above the resonant frequency, the magnetizing and series reactances ensure the flow of the required inductive fundamental currents. The FHA approach is quite accurate as long as the response of the tanks to the fundamental component of switched voltages is greater than the response to the harmonics, which holds true for continuous conduction mode operation [44], [45].

B. Converter Operation With PSM and DC

When operating in phase shift or DC mode, the converter generates output voltages in the two inverter networks that form quasi-square waves. The diagonal switches of each H-bridge (e.g., S_{1a} and S_{4a}) are phase-shifted leading to a controllable



(a) (b) (c) (d)

Fig. 7. Steady-state waveforms ($f_n = 1$) for different modes showing voltage/current amplification. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. The H-bridge output voltages V_a and V_b for Mode III and Mode IV show the antiphase operation relative to the in-phase operation for Mode I and Mode II. In addition, the output voltage V_o being quadrupled in Mode I and its doubling in (Mode II and Mode III) and output current (I_o) quadrupling (Mode IV) is evident in the waveforms.

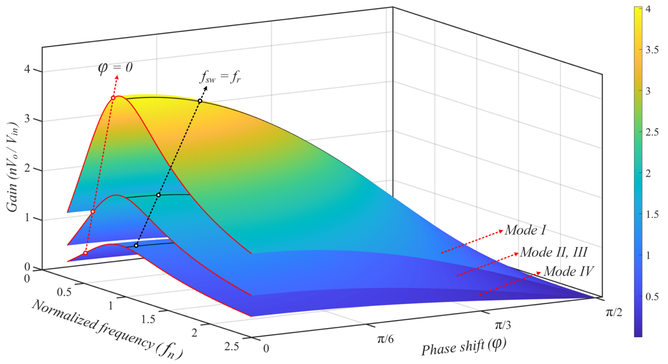


Fig. 8. Voltage-gain characteristics of the RRC with DC under various modes.

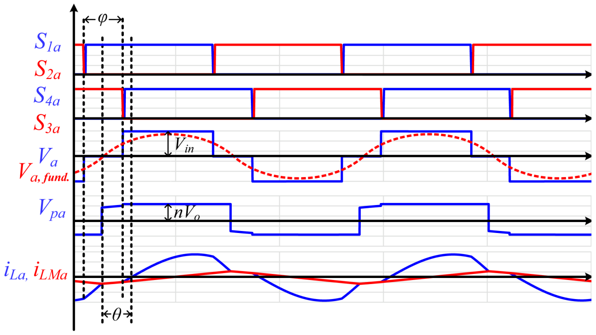


Fig. 9. Variation of ZVS boundaries with switching frequency and phase shift.

duty cycle for the inverter output voltage. With an increase in the phase-shift angles ϕ_a and ϕ_b, for in-phase and antiphase operation ($\phi_a = \phi_b = \phi$), the reduced equivalent duty cycle (D) leads to an attenuation of the fundamental component, and in turn, the voltage output

$$V_o = \frac{V_{\text{in}}}{n_{\text{eff}}} \frac{\sin(D\pi/2)}{\sqrt{\left(1+\frac{1}{\lambda}-\frac{1}{\lambda f_n^2}\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}} \tag{9}$$

wherein $D = 1 - (|\phi|/\pi)$ and the other parameters are defined as before. The variation of converter gain with ϕ and f_n is shown via the surface plot in Fig. 8. Owing to the dependence of frequency regulation on loading conditions, employing PSM or DC under light load is a common approach to overcome the otherwise slow regulation. This is further enhanced by the reconfiguration of RRC narrowing down the phase and frequency ranges.

As previously stated, an equivalent inductive ac impedance is necessary in PFM-regulated RRC for achieving ZVS operation. Under PSM or DC, this soft-switching criterion is modified. Since the inclusion of a phase shift ϕ delays the turn-ON of two devices in the lagging leg, an excessive phase shift can lead to the loss of ZVS. This is illustrated in Fig. 9, where ZVS turn-ON of S_{4a} is achieved as the zero crossing of i_{La} occurs after S_{4a} is turned ON. Assuming identical tank parameters ($\theta_a = \theta_b = \theta$), it is clear that the following constraint must be met for ZVS:

$$\frac{\phi}{2} < \theta \tag{10}$$

where θ refers to the phase angle of impedance $Z_{in,a}$ in Fig. 5, which is computed as

$$\theta = \tan^{-1}\left(\frac{C_s L_s \omega_{\text{sw}}^2 - 1}{C_s R_{\text{ref}} \omega_{\text{sw}}} + \frac{\left(C_s L_m \omega_{\text{sw}}^2 + C_s L_s \omega_{\text{sw}}^2 - 1\right) R_{\text{ref}}}{C_s L_m^2 \omega_{\text{sw}}^3}\right). \tag{11}$$

Plugging expressions (4)–(8) into (11), the impedance angle can be rewritten as

$$\theta = \tan^{-1}\left(\frac{f_n^4 \lambda^2 Q^2 - f_n^2 \lambda^2 Q^2 + f_n^2 \lambda + f_n^2 - 1}{f_n^3 \lambda^2 Q}\right). \tag{12}$$

The increase in phase shift attenuates the fundamental component of the tank input voltage but does not alter the fundamental power factor angle θ. Thus, even when driving an inductive load, a sufficiently high value of ϕ can lead to loss of ZVS. On the other hand, variation of switching frequency or load demand at

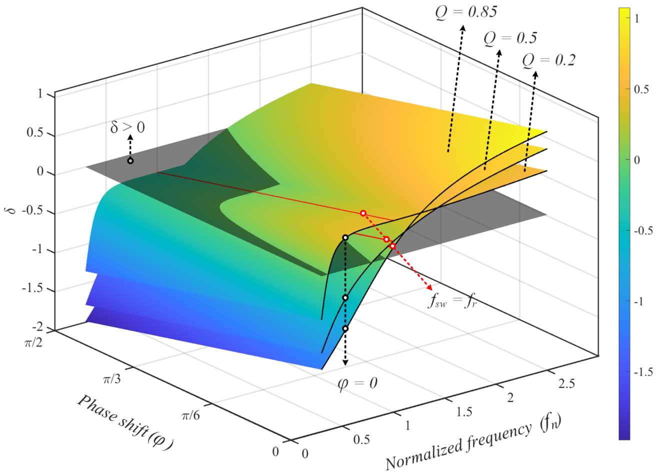


Fig. 10. Steady-state operation of H-bridge A under varying frequency and phase shift when the two bridges are operating in-phase.

the output changes the equivalent impedance and thereby the allowable phase shift for ZVS. This dependence is illustrated in Fig. 10 for $\lambda = 10$, where (10) and (12) are used to identify a boundary on the ZVS characteristics. Therein δ defined as $\theta - (\phi/2)$ must be greater than zero for ZVS. For low Q, δ is positive even for frequencies well below the series resonant frequency, which is consistent with *LLC* RPC behavior of exhibiting ZVS. Furthermore, at higher loading ($Q = 0.85$), owing to a lower equivalent ac resistance, δ is relatively larger for higher frequencies as the highly inductive tank dominates the overall impedance, resulting in a more lagging current. Therefore, when DC is employed, for a given shift, ZVS turn-ON for a higher Q is possible for a relatively lower switching frequency. It is evident that increasing just the operating frequency leads to more circulating energy and losses while increasing only the phase shift can lead to loss of ZVS. Thus, it is intended to keep δ slightly greater than zero during operation at minimum switching frequency. The FHA-based model assumes a purely resistive network on the secondary side ignoring the effects of the diode capacitances. Since these capacitances need to discharge every time the diode has to conduct, in reality, there is a phase difference between the secondary-side fundamental voltage and the corresponding current, with the current leading the voltage [46]. Depending on the diode specifications and converter design, a look-up table or frequency-phase control law can be implemented to automate the choice of operating f_{sw} and ϕ and minimize the real-time computational burden [43]. In this work, a look-up-table-based approach as shown in Fig. 11 is employed for controlling the RRC.

It is pertinent to mention that when ϕ is nonzero, the equivalent model proposed in Fig. 5 is altered. The fundamental ac voltage component (V_{ac}), the average input currents (I_a, I_b), and the output current (I_o) vary according to the phase shift. Furthermore, it can be seen in Fig. 9 that, in the presence of a phase shift, when the inverter voltage is zero, the primary current equals the magnetizing current. Thus, the secondary winding operates in DCM in the presence of a sufficiently large ϕ. For a given design, the operating frequency and the value of ϕ dictate whether the secondary winding operates in CCM or DCM. Accordingly, the equivalent model of the rectifier network and average output current magnitude change [47].

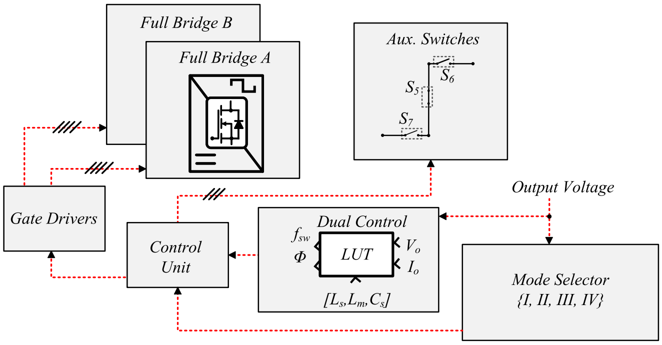


Fig. 11. Mode selection and control logic for the RRC.

TABLE I
SYSTEM PARAMETERS

Parameter	Value
Input voltage, V_{in}	600 V
Output voltage, V_{out}	180 V–1500 V
Maximum Output power, $P_{\text{out,max}}$	11 kW
Resonant Frequency, f_r	32 kHz
Full load quality factor, Q_{rated}	0.85

IV. SYSTEM STUDY AND DESIGN

The performance of the converter is validated through PLECS simulations and an 11-kW PCB prototype. The input and output voltages, resonant parameter values, and transformer turn ratios are identical in the two studies. The system parameters are shown in Table I. A 600 V input voltage is chosen based on typical dc bus voltage fed from a 230-V LV ac grid. Such a dc voltage makes the onshore bus compliant with common battery storage systems from Samsung, Toshiba, Panasonic, etc. [48].

In the simulation studies, the switching and conduction losses are obtained using PLECS thermal models derived from the semiconductor datasheets while the losses in magnetics are calculated analytically. Therein, the core losses are computed using the improved Generalized Steinmetz Equation neglecting the relaxation losses occurring during constant core flux periods when DC is employed. The average core loss per unit volume can be calculated as

$$P_v = \frac{1}{T_s} \int_0^{T_s} k_i \left| \frac{dB}{dt} \right|^{\alpha_c} (\Delta B)^{\beta_c - \alpha_c} \, dt \tag{13}$$

$$\text{where } k_i = \frac{k_c}{2\pi^{(\alpha_c - 1)} \int_0^{2\pi} |\cos\theta|^{\alpha_c} \, 2^{\beta_c - \alpha_c} \, d\theta}. \tag{14}$$

The parameters k_c, α_c, and β_c are the Steinmetz parameters while ΔB is the peak-to-peak flux density. The winding losses are estimated using the well-known Dowell's equations [49]. The losses in other passive components are calculated based on the datasheet-obtained equivalent series resistances at the corresponding operating frequencies. For the experimental prototype, end-to-end efficiency is measured using the Yokogawa WT500

Power Analyzer. In the subsequent analysis, power consumption in the control unit and auxiliary power supplies (approximately 10 W throughout the operating range) and in the six cooling fans (500 mW each) are neglected.

A. Turns Ratio Calculation

The selection of turns ratios in the two transformers is dictated by (1) for Mode I, which for an input of 600 V should yield a maximum voltage of 1500 V at the resonant frequency. Considering a 2.5% margin accounting for voltage drops due to nonideality, value of the turns ratio can be computed as

$$n = \frac{4V_{\text{in}}}{1.025V_{\text{out}}} \approx 1.561. \tag{15}$$

B. Resonant Tank Selection

When the converter is operated at 1500 V for an 11-kW load, the reflected resistance to each bridge is computed from (2) and (4) for Mode I. For a rated-load Q of 0.85 and choosing a resonant frequency of 32 kHz, the total series inductance and capacitance in each tank can be computed from (5) and (6) as

$$L_s = \frac{Q_{\text{rated}}}{2\pi 32\,000} \times \frac{8n_{\text{eff}}^2 V_o^2}{\pi^2 P_{\text{out,max}}/2} = 213.5\,\mu\text{H} \tag{16}$$

$$C_s = \frac{1}{(2\pi 32\,000)^2} \times \frac{1}{L_s} = 115.05\,\text{nF}. \tag{17}$$

The series inductance primarily comprises the externally added inductance (L_e) and the transformer leakage referred to as the primary (L_{lkg}). The external inductors are assembled using Ferrite 3C95 E64/10/50 and I64/5/50 cores and 600-strand AWG 41 Litz wire. For a peak current (I_m) and a peak flux density B_m, the required turns and airgap length are computed as

$$N = \frac{L_e I_m}{B_m A_c} \tag{18}$$

$$l_{\text{air}} \approx \frac{L_e I_m^2 \mu_o}{B_m^2 A_c}. \tag{19}$$

The FHA-approximated voltage stress across the tank capacitance is QV_{ac}, which determines the choice of capacitors. The resonant tank consists of paralleled 1-nF KEMET PHE450PA4100JR05 metalized polypropylene film capacitors (chosen due to a low dissipation factor) to collectively yield a 114 nF capacitance. This small deviation from the calculated value of C_s would result in a marginal increase in the resonant frequency and is therefore compensated by adjusting the inductance. Paralleling smaller capacitors enables the reduction of rms currents and, in turn, losses for each capacitor while also keeping the design flexible to finely alter the tank parameters.

C. Transformer Assembly

Based on the iterative process described in [50], an optimum selection of core size and number of stacks is made constrained by the material availability. Due to the presence of a tertiary winding and added insulation layer, a low window utilization factor of 0.35 is assumed. Each transformer consists of two stacked EE65/32/27 Ferrite N87 cores. A current density of 5 A/mm^2 is allowed and 600-strand AWG 41 Litz wire is used for the windings. The maximum operating flux density (B_{op}) is chosen to be 55% of B_{sat} of the core material. A classical winding arrangement in the form of primary–secondary–tertiary is used with no interleaving to maximize the fill factor. The resulting leakage inductance (L_{lkg}) forms a part of the total tank inductance (L_s). In *LLC* RPCs, it is customary to have an airgap in order to have a sufficiently large magnetizing current, which is required to charge/discharge the MOSFET capacitances (C_{oss}) during dead time and passive states [50]. The required number of turns, the value of magnetizing inductance, and the length of airgap are calculated as

$$N_{\text{pri}} = \frac{V_{\text{in}}}{4 \times B_{op} \times n_{\text{stack}} \times A_c \times f_r} \tag{20}$$

$$N_{\text{sec}} = N_{\text{ter}} = \frac{N_{\text{pri}}}{n} \tag{21}$$

$$L_m \leq \frac{t_d}{16 \times C_{oss} \times f_r} \tag{22}$$

$$l_{\text{air}} \approx \frac{N_{\text{pri}}^2 \times \mu_o \times A_c}{L_m}. \tag{23}$$

For the chosen MOSFETs, C_{oss} at 600 V is directly available from the datasheet and estimation of this nonlinear capacitance is not required. The resulting values for primary and secondary turns after rounding off are 26 and 16, respectively, while the airgap is chosen to have a magnetizing inductance of 1.2 mH.

D. Filter Capacitor and Auxiliary Switch Selection

In a conventional *LLC* RPC, a single-stage capacitive filter is often used, which determines the peak-to-peak voltage ripple. In the RRC, the operating mode further influences the magnitude of the ripple. Assuming a ripple-free load current I_o, the expression for the peak-to-peak ripple can be approximated using FHA as

$$\Delta V_{\text{pp}} \approx \frac{0.106 \times I_o}{f_{\text{sw}} \times C_{\text{eq}}}. \tag{24}$$

The factor I_o/C_{eq} inherently varies for different modes giving rise to different ripple voltage magnitudes. Due to the action of auxiliary switches, the equivalent capacitance C_{eq} is $2C_o$ in Modes II and IV while it becomes $0.5C_o$ in Modes I and III. The rated load current (I_o) on the other hand is maximum in Mode IV twice that of Modes II and III and four times the magnitude in Mode I. Consequently, under rated power, Mode II offers the lowest voltage ripple magnitude while Mode III exhibits the highest. Since Modes II and III offer the same voltage range; therefore, Mode II also exhibits one-fourth of the percentage voltage ripple as compared to Mode III. However, it can be observed from Fig. 4 that the voltage stress on the output capacitors is halved in Mode III due to the series connection by S_1. In addition, since the number of diodes and auxiliary switches in the conducting paths varies among the two modes, these two modes can exhibit different efficiencies depending on the conduction losses of respective devices chosen. Furthermore, the rms current in each capacitor is approximated by

$$I_{\text{cap,rms}} \approx \frac{P_o}{\sigma \times V_o}\sqrt{\frac{\pi^2}{8}-1}; \quad \sigma = \begin{cases} 1 & \text{for Modes I and III} \\ 2 & \text{for Modes II and IV} \end{cases}. \tag{25}$$

In the experimental prototype, the auxiliary switches are assembled using T9GV1L14-5 standard-type power relays from Potter and Brumfield. Polypropylene film capacitors B32678G4406K000 from EPCOS/TDK with a capacitance of 40 μF are used at the output. Since these are rated only for 450-V DC and the voltage ratings required are 750 V at each rectifying bridge, four of them are connected in a series–parallel combination, which further reduces the rms current in each capacitor. In addition, 39 nF MLC capacitors (2220SC393KAZ1A) from Kyocera AVX are used for high-frequency ripple filtration.

E. Semiconductor Selection

As shown in Fig. 4, the central leg diodes on the rectifier side have twice the current stress of the noncentral leg diodes. In the designed prototype, these are assembled by hard paralleling a pair of diodes identical to the ones used in the noncentral legs resulting in a total of eight diodes per rectifying bridge. Each diode must be capable of blocking 750 V in a steady state, which is half of the total output voltage in Mode I. Based on availability, IDW30G120C5B Schottky diode from Infineon is used in the rectifying bridges. The voltage stress is halved due to the presence of a series connection at the output in this mode. The MOSFETS on the primary side are required to block the 600 V dc input voltage. The SiC MOSFET C3M0065090D from Wolfspeed is used in the active H-bridges. The current ratings of these devices exhibit a significant safety margin from the steady-state values. However, during start-up and transients, the currents can shoot well beyond the full-load conditions making this margin desirable. The prototype design is summarized in Table II.

TABLE II
EXPERIMENTAL PROTOTYPE DESIGN SUMMARY

Component	Design Selection
H-bridge MOSFETS $S_{1a} - S_{4a}$, $S_{1b} - S_{4b}$	TO-247-3 G3 SiC Wolfspeed C3M0065090D (2·4x)
Rectifier Bridge Diodes $D_{1a} - D_{6a}$, $D_{1b} - D_{6b}$	TO-247-3 G5 SiC Schottky Infineon IDW30G120C5B (2·8x)
Auxiliary Switches S_5 , S_6 , S_7	SPST Standard Power Relay Potter and Brumfield T9GV5L14-5 (3x)
Output Capacitors C_{oa} , C_{ob}	Metallized polypropylene film EPCOS/TDK B32678G4406K000 (2·4x)
Resonant Capacitors C_{sa} , C_{sb}	Metallized polypropylene film KEMET PHE450PA4100JR05 (2·114x)
Resonant Inductors L_{sa} , L_{sb}	E64/10/50-I64/5/50, 600-str. AWG-41 Litz Ferroxcube Ferrite 3C95 (2·x)
Three-Winding Transformers T_a , T_b	EE65/32/27, 600-str. AWG-41 Litz EPCOS/TDK Ferrite N87 (2·x)
Control Unit	Texas Instruments F28379D launchpad
Gate Drive IC	ACPL-344JT Optocoupler (2·4x)
Voltage Sensors	LEM DVC 1000-P (2·x)
Cooling Fans	Delta Electronics ASB0305LA-D (2·3x)
Power Supply	ITECH Electronics IT6018C-1500-30

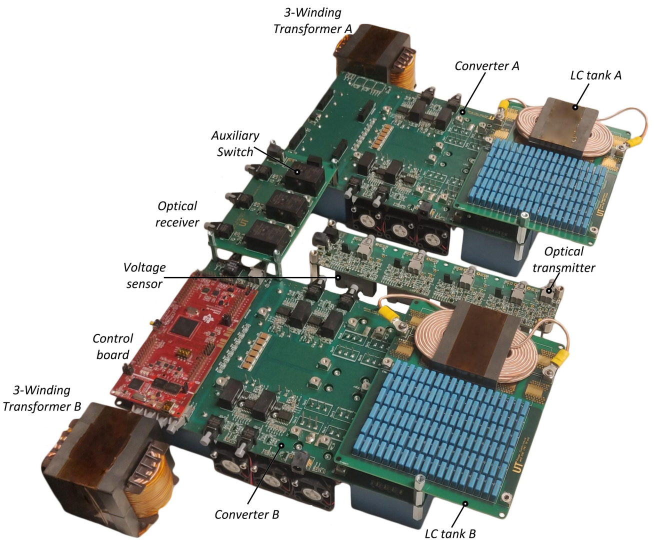
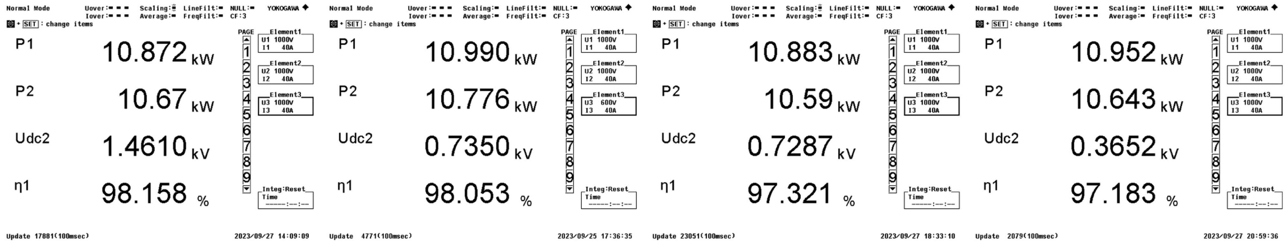


Fig. 12. 11-kW *LLC* resonant experimental DC/DC converter prototype based on SiC with dual H-bridge inverters.

V. RESULTS AND ANALYSIS

The performance of RRC is validated through the experimental prototype shown in Fig. 12 with the specifications of Table I. The converter is operated over a range of voltage and power levels in different modes. The results of end-to-end efficiency for various modes when operated at the resonant frequency are shown in Fig. 13. As previously stated, the circuit transformation in the RRC is power invariant and the converter can deliver low-current high-voltage output [see Fig. 13(a)] or an LV high-current output [see Fig. 13(d)] depending on the load demand across the terminals. The reconfiguration allows RRC to maintain excellent efficiency for extremely wide variation in the output voltage with a peak efficiency of 98.15% in Mode I (operating at resonant frequency). The steady-state waveforms under these conditions are shown in Fig. 14 where the inverter-side waveforms exhibiting the inductive characteristics and in-phase operation are shown in Fig. 14(a) while the rectifying stage exhibiting the capacitive behavior is shown in Fig. 14(b). The converter waveforms for the redundant Modes II and III are shown in Fig. 15 where the in-phase [see Fig. 15(a)] and antiphase [see Fig. 15(b)] characteristics of the two parallel bridges can be observed. There is a decrease in efficiency with reconfiguration from higher to lower voltage due to an increase in the number of conducting devices (auxiliary switches and central-leg diodes) and the current on the secondary side. This particularly occurs in Modes III and IV where the conduction losses in central-leg diodes increase the total power loss. However, as previously mentioned, these modes reduce voltage stress on the output capacitor and diodes, thereby offering a design tradeoff between Modes II and III. The antiphase operation for the current quadrupling mode, which exhibits the lowest voltage range, is illustrated in Fig. 16(a). The results corresponding to DC are presented in Fig. 16(b) for voltage quadrupling mode where $\phi = \pi/6$ rad at 40 kHz. These values ensure the ZVS



Normal Mode Uover:- - - Iover:- - - Scaling:- Average:- LineFilt:- FreqFilt:- NULL:- CF:3 YOKOGAWA
SET : change items
P1 10.872 kW
P2 10.67 kW
Udc2 1.4610 kV
η1 98.158 %
Element1 U1 1000V I1 40A
Element2 U2 1000V I2 40A
Element3 U3 1000V I3 40A
Integ:Reset Time -----:--:--
Update 17881(100msec) 2023/09/27 14:09:09

(a)

Normal Mode Uover:- - - Iover:- - - Scaling:- Average:- LineFilt:- FreqFilt:- NULL:- CF:3 YOKOGAWA
SET : change items
P1 10.990 kW
P2 10.776 kW
Udc2 0.7350 kV
η1 98.053 %
Element1 U1 1000V I1 40A
Element2 U2 1000V I2 40A
Element3 U3 600V I3 40A
Integ:Reset Time -----:--:--
Update 4771(100msec) 2023/09/25 17:36:35

(b)

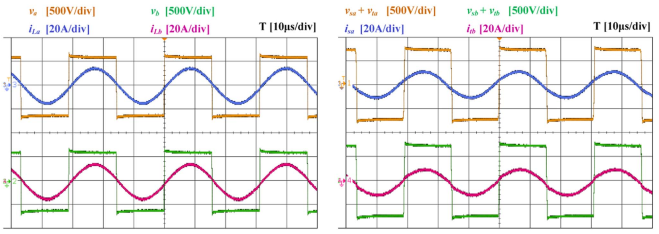
Normal Mode Uover:- - - Iover:- - - Scaling:- Average:- LineFilt:- FreqFilt:- NULL:- CF:3 YOKOGAWA
SET : change items
P1 10.883 kW
P2 10.59 kW
Udc2 0.7287 kV
η1 97.321 %
Element1 U1 1000V I1 40A
Element2 U2 1000V I2 40A
Element3 U3 1000V I3 40A
Integ:Reset Time -----:--:--
Update 23051(100msec) 2023/09/27 18:33:10

(c)

Normal Mode Uover:- - - Iover:- - - Scaling:- Average:- LineFilt:- FreqFilt:- NULL:- CF:3 YOKOGAWA
SET : change items
P1 10.952 kW
P2 10.643 kW
Udc2 0.3652 kV
η1 97.183 %
Element1 U1 1000V I1 40A
Element2 U2 1000V I2 40A
Element3 U3 1000V I3 40A
Integ:Reset Time -----:--:--
Update 2079(100msec) 2023/09/27 20:59:36

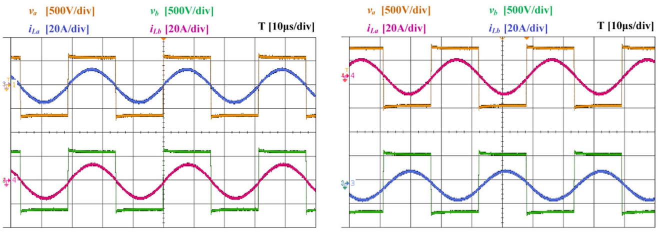
(d)

Fig. 13. Efficiency results for different voltages when the converter is operated close to the resonant frequency. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.



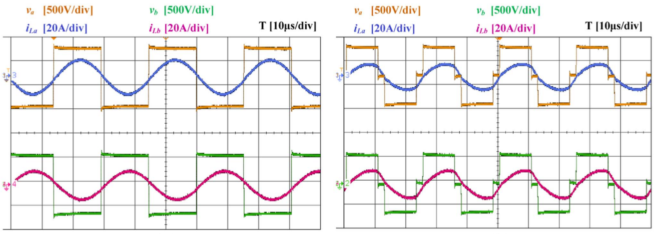
(a) (b)

Fig. 14. Experimental results showing the AC voltages and currents for Mode I (at $V_o = 1.46$ kV, $P_o = 10.67$ kW) exhibiting the in-phase operation at the resonant frequency. (a) Inverter side. (b) Rectifier side.



(a) (b)

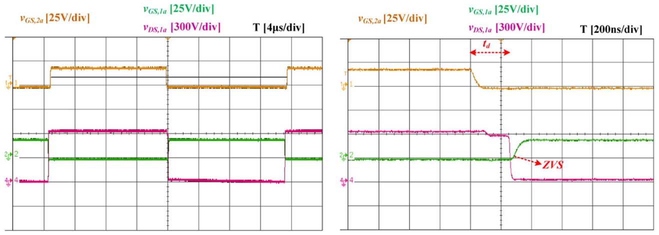
Fig. 15. Experimental results showing the steady-state waveforms. (a) Mode II operation at $V_o = 735$ V, $P_o = 10.77$ kW. (b) Mode III operation at $V_o = 728.7$ V, $P_o = 10.59$ kW.



(a) (b)

Fig. 16. Steady-state AC voltages and currents under different operating conditions. (a) Antiphase operation at the resonant frequency for Mode IV ($V_o = 365.2$ V, $P_o = 10.64$ kW). (b) Operation with DC in Mode I ($V_o = 1200$ V, $P_o = 7.2$ kW).

turn-ON of the primary-side MOSFETs without increasing the circulating current unnecessarily.



(a) (b)

Fig. 17. Switching action at the resonant frequency in RRC. (a) Switching behavior of complementary MOSFETs. (b) Zoomed-in view depicting ZVS turn-ON.

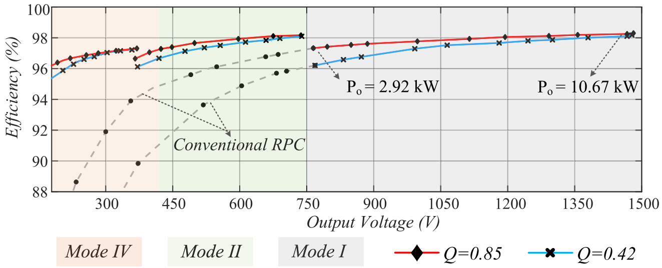


Fig. 18. Efficiency test results for the RRC prototype under various operating modes; the extension of Mode I results exhibits the characteristics of a conventional *LLC* RPC.

The ZVS mechanism of the RRC is illustrated in Fig. 17 where the converter is operated just above the resonant frequency and the gating signals are dead-timed appropriately to ensure that the high-side MOSFET is gated once the drain-to-source voltage of the low-side MOSFET is zero. The measured efficiency for the experimental prototype is shown in Fig. 18 for two values of Q wherein DC is used for voltage regulation in each operating mode. For $Q = 0.85$, the converter is able to maintain an efficiency well above 96% over the entire voltage range. When the converter is operated in Mode I throughout the voltage range (dotted line), the efficiency drops substantially. This is reminiscent of a conventional *LLC* RPC behavior and highlights the advantageous operation of the proposed converter through reconfiguration. In general, in *LLC* converters, a lower Q value makes voltage regulation with frequency modulation more difficult as the series impedance is dominated by the effective output resistance making the frequency-dependent tank reactance less effective in controlling the voltage across the output terminals. Naturally, a larger frequency band is required as the Q value is lowered due to light loading, which leads to higher turn-OFF losses, transformer core losses, and winding losses due to skin and proximity effects when normalized against

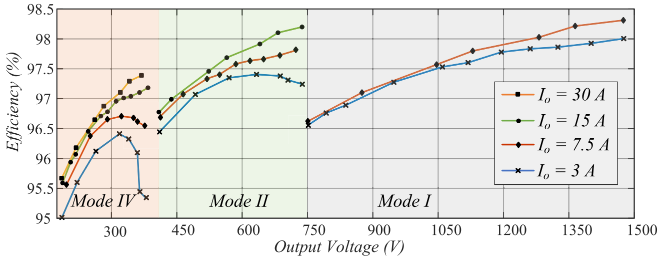


Fig. 19. Efficiency results over the complete operating range from the simulation model.

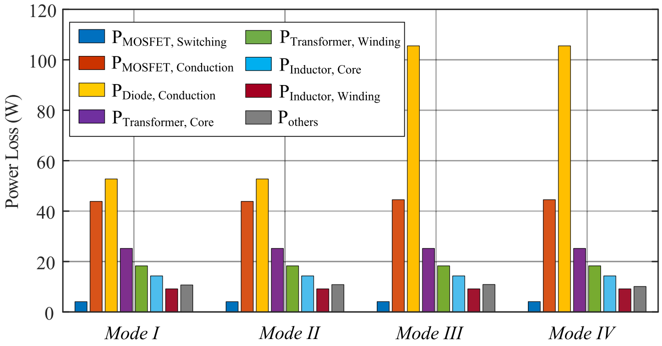


Fig. 20. Comparison of the power losses under various modes of operation.

the reduced output power. Therefore, the efficiency curve for a lower Q value trends below the efficiency curve of a higher Q value.

It is pertinent to mention that the topology is designed such that the appropriate operating mode is identified prior to converter startup and mode reconfiguration during a running operation is avoided to prevent large transients. The communication link between the onboard bus and converter can easily assist in suitable mode selection. Furthermore, as previously mentioned, the vessel usually has a dedicated charging converter for the battery onboard while the onshore converter feeds power into the main dc bus at a constant voltage making mode selection straightforward. However, loading on the bus can change during the charging process since the battery bank forms the bulk of power sink when the vessel is stationary, and depending upon the charging profile, the dc bus current can accordingly change.

Since the *LLC* can also offer a greater than unity gain under light load below the series resonant frequency, it is, therefore, possible to shift the mode boundaries toward higher voltage knowing the load demand. However, in the case of a load increase, the maximum attainable voltage decreases and the system may become nonoperational as reconfiguration cannot take place online. Therefore, the mode boundaries are set at half of the peak voltages of Modes I and II in this work.

The analytically calculated efficiency of the converter for different loading conditions over the complete voltage range is shown in Fig. 19, which exhibits the characteristics of *LLC*-based converters in each operating mode. On the other hand, Fig. 20 compares the distribution of power losses for the four operating modes at rated power. Therein, the increase in conduction loss of the diodes can be observed, which is responsible for a lower efficiency, as shown in Fig. 13. The power losses within an operating mode at the resonant frequency are compared in Fig. 21 where the switching losses are small. The advantage of the RRC is that it can operate at 375, 750, and 1500 V while incurring a small switching loss. Within an operating mode, the converter exhibits the characteristics of a conventional RPC operated with DC. It can be observed that for rated load, the diode conduction losses dominate the total power loss and inhibit a higher peak efficiency at rated power. As the loading decreases, the transformer core loss, which is independent of the current demand, forms the primary source of power loss. Therefore, if better peak and overall efficiency are desired, synchronous rectification (at the cost of lower reliability), and the choice of core material are two directions to explore. Moreover, for better light-load efficiency, operating just one of the parallel H-bridges is a potential choice that would reduce the core loss albeit at the expense of increased copper losses and uneven semiconductor degradation.

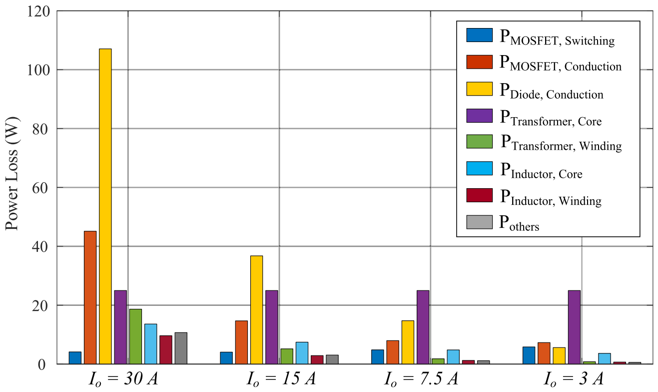


Fig. 21. Distribution of losses for different loading conditions (Mode IV operation at 365 V).

VI. CONCLUSION

In this study, an extremely wide output voltage range resonant converter is proposed, which can find applicability in systems where a multifunctional dc/dc converter is desired, such as EV charging stations, universal power supplies, and onshore charging interfaces for battery-based boats. The proposed converter makes use of a reconfigurable structure, which allows it to operate in different voltage ranges without derating the converter. By employing an interleaved structure on the primary side and an adaptable secondary side, the converter also alleviates the voltage and current stresses on the semiconductors allowing usage of lower-rated devices for higher voltage and current output. A steady-state equivalent model is developed, which aids in the design of an 11-kW experimental prototype built for validating the converter operation in a voltage range of 180–1500 V. The RRC dc/dc converter prototype exhibits a peak efficiency of 98.15% and is able to maintain excellent efficiencies over the entire voltage range. At low output voltages (180–750V), the measured efficiencies range from 96% to 98.1%, when Mode IV and Mode II are operational. On the other hand, conventional RPC that extends Mode I throughout the range suffers from poorer efficiencies between 88.5% and 97%. Furthermore, additional operating modes are identified, which through asymmetrical converter switching can create additional peak efficiency points within the full output voltage range and thereby further enhance the overall efficiency.

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