Buck Converter With Load Adaptive Losses and 256x Sub-mW Load Transient Response Time of 0.8 ms Using Synchronous Control

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***Abstract*—The authors propose a pulse-frequency modulation based buck converter that uses synchronous control. The controller clock continuously tracks twice the switching frequency through internal control that employs a primary clock. The system responds to 256x load rise transients within four switching periods using synchronous control to have fine output voltage attributes with a 27 nF-capacitor at output. Zero current switching in $\leq$10 ns is achieved using an active diode (AD). Employment of the AD ensures nonoverlap conduction of the switches in the buck converter. The analog AD-controller operates bias-free and the power consumed by it scales with switching frequency. As the average switching frequency is proportional to load, the losses in the main controller and AD-controller scale with load that improves the efficiency at light load. The system fabricated in 180 nm CMOS technology for 1.2 V output voltage, enhances the state-of-the-art transient response rate in synchronous mode (to 2.6–657 μA in 812.8 μs) for limiting the voltage droop to 7 mV. Peak efficiency achieved is 94.8% at 788 μW output. Efficiency >80% is obtained for the minimum output power levels of 12.4 μW and 1.75 μW at primary clocks of 1.25 MHz and 1.25/32 MHz, respectively.**

***Index Terms*—Active diode (AD), buck converter, dynamic clock controller (DCC), efficiency, light load, load transient response, pulse-frequency modulation (PFM), synchronous control, voltage droop, zero current switching (ZCS).**

I. Introduction

PULSE-frequency modulation (PFM) based dc–dc converters operated in discontinuous conduction mode, scale the converter losses with load and improve the efficiency η at light load [1], [2], [3]. However, PFM–based operation does not ensure the scaling of the controller quiescent power with load. As this controller power is relatively significant at smaller power levels, the light load-η of PFM–based converters is largely dictated by the controller losses [4], [5].

While employing techniques to improve the light load-η, it is also of importance to ensure that the other performance traits of the dc–dc converter are not compromised. The following are the desirable features of a dc–dc converter.

1) Fine regulation and low ripple of output voltage.
2) Very high (>90%) η at the higher range of load.
3) High (>80%) η at light load.
4) Fast transient response.
5) Minimum voltage droop [6] at the transients.
6) Small inductor L and small output capacitor C_o.

Prior works on asynchronously controlled buck converters [2], [4], [7], [8], [9], have demonstrated η at sub-mW load. Asynchronous control uses a continuous time comparator for voltage regulation. To improve η at light load, the PFM-based converter in [7] works in the retention mode, which uses subthreshold region of operation for a few controller blocks, disables unused controller blocks and also, works at a low switching frequency. The comparator of the PFM-based buck converter in [4] is provided a low bias current at light load, which in turn also reduces the switching frequency and active duty of the dynamic-biased comparator for zero current switching (ZCS). These strategies in [4] and [7] help to reduce the switching related and controller losses at light load. The works [4], [7] that reduce the switching frequency at light load to a value lower than that demanded by PFM operation, compromise on the output voltage ripple and regulation characteristics [7]. Work in [8] using single-bound hysteresis control has shown fast load transient response, along with a high η at sub-mW load. However, superior light load-η as compared to these asynchronously controlled converters [2], [4], [7], [8], [9], is shown to be provided by synchronously controlled PFM-based dc–dc converters.

Dc–dc converters having synchronous control [3], [5], [6], [10], [11], [12], [13], [14] use clocked comparator for output voltage regulation. These have an inherently higher light load-η, due to the lower power consumption by the clocked comparator (as compared to a continuous time comparator), with a consequently lower controller power. The converters also provide low ripple at the output voltage due to the high voltage gain of the clocked dynamic comparators [5].

While a high-frequency clock for the synchronous controller can provide fast transient response [6], it increases the

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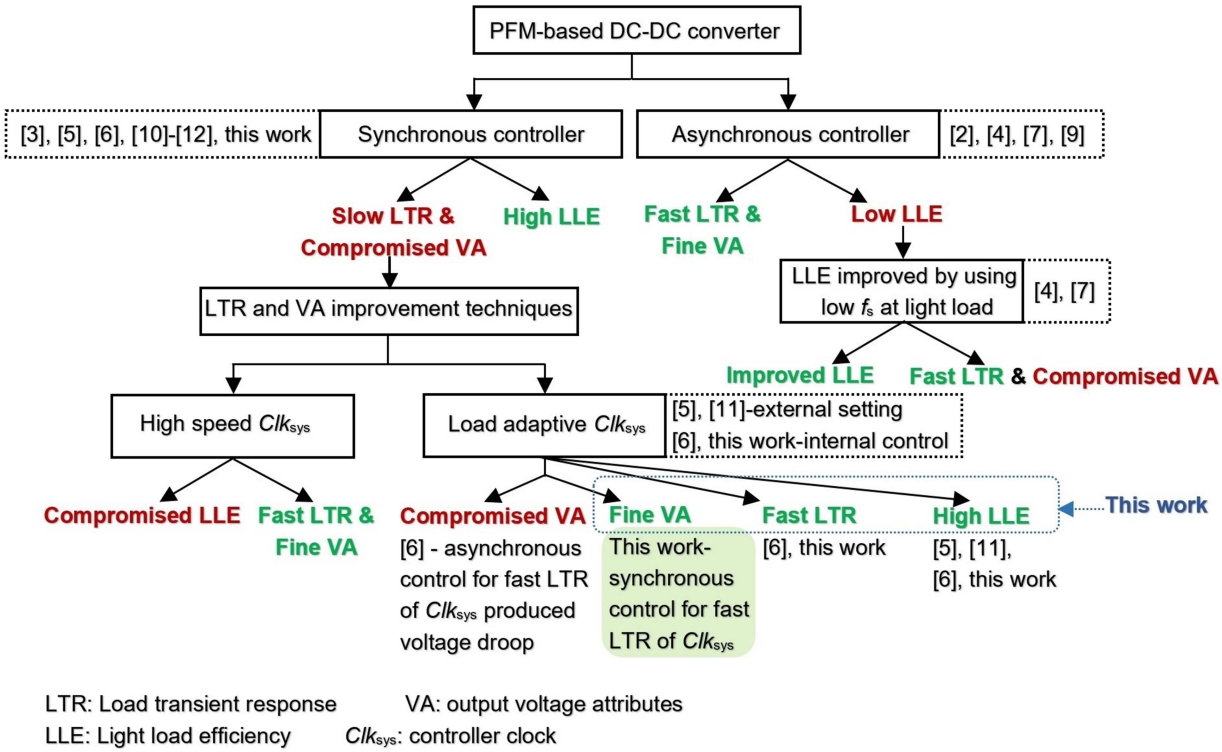


Fig. 1. Different implementations of PFM-based DC–DC converter with the associated performance.

power consumption by the controller. The controller clock is dynamically adapted to decrease or increase with load in prior works [5], [6], [11], [13], [14]. This adaptively reduces the controller power at lighter loads while also providing fine voltage characteristics across the range of load. Such works have dynamically changed the controller clock by external setting [5], [11] using the mode of the load [5] or even by internal control [6], [13], [14] as required for standalone systems. However, the load transient response rate of the converter would then be determined by the response speed of the dynamic clock to load transients. The limited load transient response rate in synchronous control was improved by an asynchronous control loop at the cost of a voltage droop caused by using a low-speed continuous time comparator in [6]. Gao et al. [13], [14] adapted the controller clock using the synchronous control loop itself for a fast load transient response. However, these pulse-skip modulation-based buck converters [13], [14] have maintained a high light load-η by using a range of low frequencies (1–15 kHz in [13], 1–120 kHz in [14]) and cause a dip in η (to $<$80%) at the maximum load.

ZCS in dc–dc converters needs to meet exact timing with minimum control power [15]. ZCS using digital delay tuning [6], [10], [11], [16], [17], [18], [19], [20] consume relatively lower control power. However, Chen et al. [10] Tsai et al. [20] suggested an effective improvement in the total η at light load, by disabling the digital ZCS-controller. This was in spite of the additional conduction loss due to the use of body diode conduction in [10] and [20]. Also, Liu et al. [21] projected the need for specifically employing analog ZCS instead of digital ZCS, to meet the requirement of instantaneously varying the ZCS time. Nevertheless, high-accuracy analog ZCS using comparator [4], [7], [15], [22], [23] are power-hungry [22] and these also need offset-compensation. The predetermined PFM in [12] calculates the OFF-time in advance and eliminates the power consumption by the otherwise used ZCS controller. However, in such predictive ZCS methods [3], [8], [12], [24], [25], the accuracy of reverse inductor current blocking is limited [4].

Fig. 1 summarises the different possible implementations of a PFM-based dc–dc converter. Asynchronous control [2], [4], [7], [9] provides fast load transient response and fine voltage attributes, at the cost of a relatively low light load-η. Any attempt to improve the light load-η by reducing the switching frequency f_s of the converter at light load [4], [7], compromises on the output voltage ripple and regulation characteristics. Also, while operation at a lower f_s to supply a given load reduces the switching related losses, the rms current $I_{\rm rms}$ and conduction losses are increased [24]. Thus, though a lower f_s can improve the light load-η, it does not give the best case-value for this η. A synchronous controller [3], [5], [6], [10], [11], [12] scores in terms of having an inherently lower controller power by using a clocked comparator. As the light load-η of PFM-based converters is largely dictated by the controller losses [4], [5], synchronous control innately provides a superior light load-η. Also, as most of the synchronous controller losses scale in proportion to the controller clock, the controller losses can be proportionally reduced with load by having a load adaptive controller clock [5], [6], [11]. This helps to maintain a high η even at very low loads. It is noted that though a fixed low speed controller clock improves η at light loads, it compromises on the load transient response rate and output voltage attributes. Similarly, the use of a high speed controller clock can improve the load transient

response and voltage attributes, at the cost of a lower η at light loads. Thus, in this work, we zero in on using a load adaptive controller clock for a synchronous controller. In such a case, load transient response rate can be improved by having a fast rate of adaptation of the controller clock with load. It is noted that works in [5] and [11] require external input for changing the controller clock. Liu et al. [6] demonstrated fast response for the internal adaptation of controller clock. However, converter in [6] shows a voltage droop due to the use of a low-speed continuous time comparator for enhancing the response rate to load transients. Our work addresses this challenge by improving the controller clock adaptation rate using the clocked comparator in synchronous control loop itself, which is expected to give a minimal voltage droop.

We propose a PFM-based buck converter that uses a synchronous controller. It internally scales its controller clock with load, by having the clock track twice the f_s, which is proportional to the load. The converter responds to 256x load rise transients within four switching periods using synchronous control for fine voltage attributes with no significant voltage droop, at 27 nF-C_o. The active diode (AD) implementation from our recent work [26], is used as the diode (that provides the discharge path for the L-current) of the buck converter. The deployment of the AD in this specific application circuit of a PFM-based buck converter presents the following advantages.

1) It provides ZCS in $\leq$10 ns with inherently no offset issue using an analog controller.
2) As the AD self-detects and turns ON only at the presence of a forward voltage across it, dead-time control [7], [27], [28], [29] for nonoverlap conduction of the switches in the buck converter, is automatically provided.
3) Controller of AD is bias-free and conducts only at the switching transitions, making the AD-controller losses proportional to f_s or load.
4) The analog AD makes the conduction phase-signal ($\emptyset_{dis}$) available instantaneously and it is employed to limit the in-rush current [9] at startup of the dc–dc converter.

As most of the losses of both the main synchronous controller and AD-controller, proportionally reduce with (f_s and, hence) load, the proposed converter promises a high light load-η. A survey of PFM-based dc–dc converters illustrated in Fig. 1, shows that our converter achieves the unique characteristic of simultaneously providing high light load-η, fast load transient response, and fine voltage attributes. This has been accomplished by having a load adaptive controller clock with fast response obtained using the clocked comparator itself. As the controller clock tracks $2\times f_s$ against $(3–4)\times f_s$ in prior work [6], our converter can work at a higher f_s for any given controller clock or controller loss. Furthermore, as the switching related and controller losses at any given f_s, are reduced by virtue of using the AD, a higher f_s can be used for a given allocation of these losses. A high f_s reduces conduction losses [24] and enables our converter to achieve a very high ($>$90%) η at higher loads including the maximum load. Also, the proposed converter limits the ripple voltage with a low value of C_o (27 nF), thanks to the higher values of f_s up to 1.25 MHz.

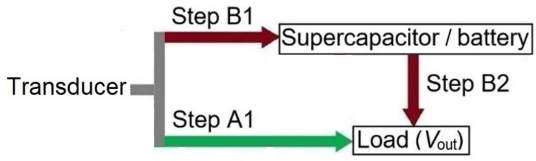


Fig. 2. Power conversion steps in energy harvesting systems [16], [19], [21], [22], [23], [30], [31], [32].

The rest of this article is organized as follows. Section II presents the application of the proposed buck converter in an energy harvesting system. Section III details the construction and working principle of our converter. Section IV describes the dynamic clock controller. Section V discusses the functions of the AD in the proposed converter. Section VI gives measurement results of the converter fabricated in 180 nm CMOS technology. Finally, Section VII concludes this article.

II. Application in Energy Harvesting System

The architecture of most energy harvesting systems [16], [19], [21], [22], [23], [30], [31], [32] can be depicted in terms of the involved power conversion steps, as shown in Fig. 2. Each power conversion step (step A1, step B1, or step B2) corresponds to a dc–dc converter. The converters for the conversion steps can share a common L.

The architecture of these energy harvesting systems allow both single-step (transducer→load) and two-step (transducer→battery→load) power conversions. Single-step conversion involves a single dc–dc converter, namely that for step A1, in the power transfer path from transducer to load. Two-step conversion (double-conversion [19]) engages two dc–dc converters, namely those for steps B1 and B2, in the power transfer path from transducer to load. The B1-B2 path also depends on a battery or supercapacitor for energy buffering.

With the architecture that supports both single-step and two-step conversions, techniques have been suggested in prior works [16], [19], [31] to have more single-step conversions and reduce two-step conversions. This has an objective of increasing the overall η of power transfer from transducer to load. As the technique for rejection of double-conversion in [19] can affect maximum power point tracking (MPPT) efficiency, we suggest buffering with a relaxed output voltage regulation range [16], [31] to encourage single-step conversions.

For delivering power from the transducer to two different loads, load-1 and load-2 at output voltages V_{out1} and V_{out2}, respectively, configuration-1 in Fig. 3(a) has been derived on the basis of the prior architectures (see illustrated in Fig. 2). In order to accommodate different specification requirements, we define a case where V_{out1} can afford to have relaxed regulation, whereas V_{out2} is desired to have fine voltage attributes across a wide dynamic range of load. Using configuration-1, generation of V_{out1} would typically involve a single step, namely, step A1. As buffering with a relaxed voltage regulation [16], [31], is not possible for V_{out2} which requires fine voltage characteristics, alternate buffering through battery or supercapacitor is required

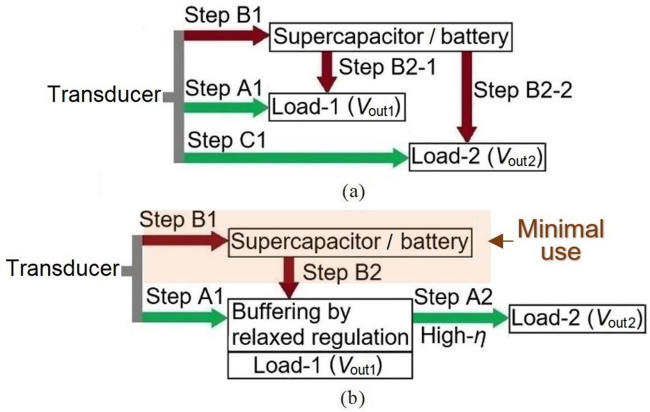


Fig. 3. Power conversion steps in power transfer from transducer to two loads, one at coarsely regulated voltage and the other at finely regulated voltage with wide load dynamics. (a) Configuration-1. (b) Configuration-2.

to absorb the load dynamics. Using configuration-1, power transfer from transducer to load-2 would typically require two steps, namely, steps B1 and B2-2. η of power transfer from transducer to load-1 is given by η_{L1} and that to load-2 is given by η_{L2}. These are specified in (1) and (2) for configuration-1

$$\eta_{\mathrm{L1}} = \eta_{\mathrm{A1}} \tag{1}$$

$$\eta_{\mathrm{L2}} = \eta_{\mathrm{B1}}\eta_{\mathrm{B2-2}} \tag{2}$$

where η_{A1}, η_{B1}, and $\eta_{\mathrm{B2\text{-}2}}$ are the η of power conversion steps A1, B1, and B2-2, respectively.

We propose to derive V_{out2} from V_{out1} as shown in the configuration-2 in Fig. 3(b). Power transfer from transducer to V_{out1} would typically involve a single step, namely, step A1, thanks to buffering at V_{out1} by its relaxed regulation. Accordingly, power is transferred from transducer to load-2 in two steps, namely, steps A1 and A2. While η_{L1} in configuration-2 is also given by (1), η_{L2} in configuration-2 is given by

$$\eta_{\mathrm{L2}} = \eta_{\mathrm{A1}}\eta_{\mathrm{A2}} \tag{3}$$

where η_{A2} is the η of power conversion step A2. As steps B1 and A1 use the same platform, similar η are expected for these steps. So η_{L2} for the proposed configuration-2 can be improved over that for the configuration-1 by having a higher η_{A2} than $\eta_{\mathrm{B2\text{-}2}}$.

For any current having a zero-offset triangular waveform in a dc–dc converter operating in discontinuous conduction mode, (4) holds.

$$I_{\mathrm{rms}}^2 = \frac{4\, I_{\mathrm{avg}}^2}{3\, d_{\mathrm{s}}} \tag{4}$$

As average current I_{avg} is fixed for given voltages and power transfer in a dc–dc converter, (4) shows that I_{rms} and hence conduction losses ($=I_{\mathrm{rms}}{}^2 \times$path resistance) reduce as duty cycle d_{s} (of the triangular pulse) increases. A shared-L system provides limited d_{s} for each converter due to time-sharing. Accordingly, it may be appreciated that in a shared-L system, η of each converter is relatively lower owing to higher conduction losses. Thus, we proposed an unshared-L for the converter performing step A2 to improve η_{A2}. It may be noted that as B2-2 is typically performed in prior systems (of configuration-1) using a converter with L-sharing, $\eta_{\mathrm{B2\text{-}2}}$ is expected to be less than η_{A2}.

As η_{A2} increases, the larger is the improvement of η_{L2} in the proposed configuration-2 with respect to η_{L2} in configuration-1. Configuration-2 also needs less battery usage as compared to configuration-1. As configuration-2 requires an additional L for the step-A2 converter that does not share the common L, it is desired to have a small L and/or C_{o} for the step-A2 converter.

As the proposed buck converter in this work provides a high η across the wide load range along with fast load transient response and fine voltage attributes at a low C_{o}, it can cater to providing the step-A2 conversion.

III. Proposed Buck Converter

The proposed PFM-based buck converter provides an output voltage V_{o} of 1.2 V from the line voltage V_{in}. V_{in} has a narrow range (see Section II) of 1.6–1.9 V and L is charged with constant ON-time [10] T_{on} (=200 ns) pulses. The converter uses a synchronous controller having a clocked comparator [16] for regulation of V_{o}.

The construction of the proposed buck converter is shown in Fig. 4(a). AD_{o} is used as the diode in the buck converter for discharging the L-current. AD_{o} is the AD implementation from our recent work [26]. The AD turns ON by sensing the forward voltage and it also provides ZCS. The active-low $\emptyset_{\mathrm{dis}}$-pulse corresponding to AD_{o}-conduction phase, is derived from AD_{o}. The detailed description of AD_{o} is covered in Section V.

Fig. 4(a) also shows the block level description of the controller of the buck converter. The operating waveforms of the controller are shown in Fig. 4(b). When (the fixed fraction of) V_{o} is less than the reference voltage, the output of the clocked comparator V_{cmp} goes high. This triggers the start of the switching cycle (SW_{on} = high). The rising-edge of SW_{on} triggers the start of the active-high $\emptyset_{\mathrm{on}}$-phase. L gets charged during the active $\emptyset_{\mathrm{on}}$-phase, which has a duration of T_{on}. Subsequent to this, AD_{o} conducts to discharge L. $\emptyset_{\mathrm{dis}}$-phase corresponds to the duration of discharge of L for time T_{dis}. The rising (stopping) edge of the active-low $\emptyset_{\mathrm{dis}}$ leads to the generation of end-of-cycle (EoC) pulse. This EoC pulse resets the high SW_{on}. Thus, it is ensured that in spite of a rising edge on V_{cmp}, the rising edge on SW_{on} occurs only after the full discharge of L. As $\emptyset_{\mathrm{on}}$ is triggered by the rising edge of SW_{on}, it is ensured that each charging of L happens only after the full discharge of L. This aids to prevent the ramping-up of inductor current [9].

A. Controller-Loss Scaling With Load

The losses of the synchronous controller are scaled in proportion to f_{s} by having the clock of the comparator (for V_{o}-regulation) track $2\times f_{\mathrm{s}}$. The comparator clock is internally adapted and given by the dynamic clock controller (DCC) as Clk_{DCC}. Rate of $Clk_{\mathrm{DCC}} = 2\times f_{\mathrm{s}}$. DCC frequency-divides ($\div$) a primary clock Clk_{prim} to obtain the required Clk_{DCC}. As the DCC itself works synchronously at Clk_{DCC}, the power consumed by DCC is proportional to f_{s}. The bias-free controller of AD_{o} conducts only at the switching transitions and AD_{o}-control power also scales with f_{s} [26]. It is later shown in this section

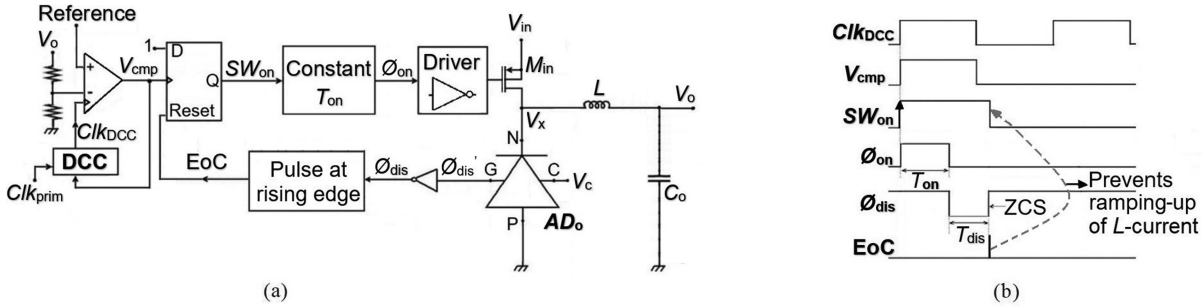


Fig. 4. Proposed buck converter. (a) Construction of converter and block diagram of controller. (b) Representative operating waveforms of controller.

that the average f_s is proportional to load at a given V_{in}. Thus, all controller losses except those from reference generator, Clk_{prim}, and leakage, are proportional to load. Note that the losses owing to Clk_{prim} are at its oscillator, driver, and frequency-divider.

B. Mathematical Relations

Load current I_o is given by the average L-current, as shown in

$$I_o = \frac{I_{L,peak}\ (T_{on} + T_{dis})\ f_s}{2}. \tag{5}$$

$I_{L,peak}$ is the peak L-current. It is expressed as given by

$$I_{L,peak} = \frac{(V_{in} - V_o)\ T_{on}}{L} = \frac{V_o\ T_{dis}}{L}. \tag{6}$$

From (6), T_{dis} is expressed in terms of T_{on} in

$$T_{dis} = \frac{(V_{in} - V_o)\ T_{on}}{V_o}. \tag{7}$$

From (5)–(7), I_o is defined by

$$I_o = \frac{(V_{in} - V_o)\ V_{in}\ T_{on}^2\ f_s}{2\ L\ V_o}. \tag{8}$$

From (8), it can be seen that at a given V_{in} and constant ON-time, $f_s \propto I_o$. Hence, all switching related power losses are proportional to load. The switching related losses correspond to all energy losses occurring at the switching transitions of a PFM-based buck converter. These include synchronization losses [33], [34] and driver losses of the MOSFET switches in the converter.

On the basis of the derivations of (5)–(8), at a given V_{in} and constant ON-time, $I_{avg} \propto f_s$ and $d_s \propto f_s$, in (4) for the currents in the buck converter. From (4) it is, thus, obtained that, ${I_{rms}}^2 \propto f_s$. As our converter has a constant ON-time and $f_s \propto I_o$, its conduction losses are proportional to load. Fig. 5 shows the expected scaling of conduction, switching related, and controller power losses with load.

In general, for any buck converter operated in discontinuous conduction mode, it can be inferred from (8) that heavier ($=b$ times, $b>1$) load current can be supplied by either scaling up T_{on} (by $b^{1/2}$) or by scaling up f_s (by b). It is also appreciated that with f_s–upscaling the associated d_s ($=T_{on}\ f_s$) would scale up by a higher value ($=b$) as compared to that ($=b^{1/2}$) with T_{on}–upscaling. For supplying a given maximum load current, increasing T_{on} without changing f_s will keep the switching

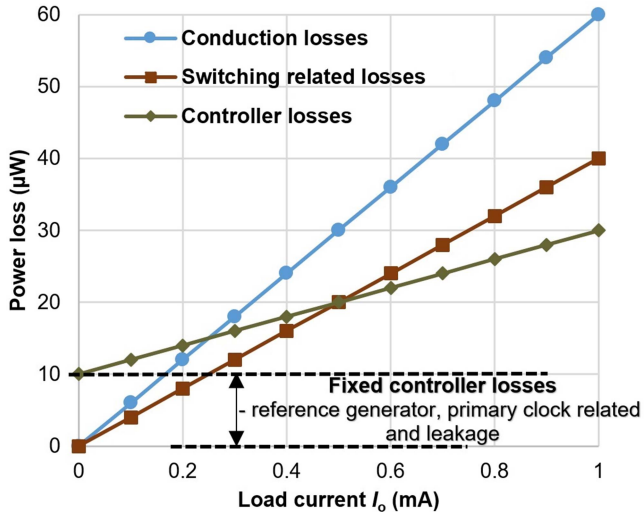


Fig. 5. Expected load adaptive losses in the proposed buck converter.

related and any f_s-proportional controller losses at bay. However, T_{on}–upscaling can lead to a higher conduction loss as compared to that with f_s–upscaling owing to the lower d_s with T_{on}–upscaling, as shown by (4). Thus, ideally, the optimum values of T_{on} and f_s need to be chosen such that the total losses are minimized and η is maximized, at any given load.

For our converter, the optimum (constant) T_{on} and f_s were first determined at the maximum load, in respect of minimizing the total losses. The losses at the maximum load are predominantly contributed by conduction, switching related, and f_s-proportional controller losses. As these losses scale with load for the proposed converter, η is expected to be maintained at the lower loads when neglecting the fixed controller losses (see Fig. 5). In consideration of these fixed losses, we have further made a choice of Clk_{prim} ($=f_s$ at the maximum load), as described in Section IV.

The ripple voltage V_{rpl} at V_o is given by

$$V_{rpl} = \frac{k_1\ I_{L,peak}\ (T_{on} + T_{dis})}{2\ C_o}. \tag{9}$$

Using (6)–(8) in (9), V_{rpl} can be expressed by

$$V_{rpl} = \frac{k_1\ I_o}{f_s\ C_o}. \tag{10}$$

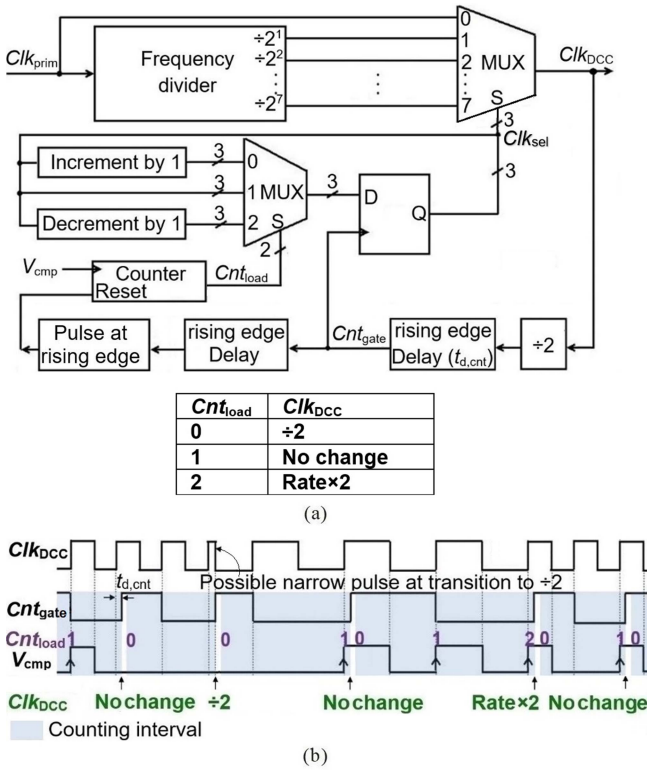


Fig. 6. Dynamic clock controller of buck converter. (a) Block diagram and logic table. (b) Operating waveforms.

The variable k_1 accounts for the possible dip in V_o due to discrete sampling by the clocked comparator at a finite rate given by Clk_{DCC}. The maximum value of V_{rpl} corresponds to the maximum value of the variable k_1. The maximum value of k_1 is 2 and it occurs when the average f_s is close to but less than either the rate of Clk_{prim} or half the rate of $Clk_{prim}\div 2^i$ (where integer i varies from 0 to 7). This can be inferred from the discussions in Section IV. Also, as seen from (10), the use of a high f_s can reduce the required size of C_o for limiting V_{rpl} to a specified value at a given I_o.

IV. Dynamic Clock Controller

DCC is used to provide the clock to the comparator of the synchronous controller. DCC gives Clk_{DCC} that continuously tracks $2\times f_s$. The block diagram of DCC is shown in Fig. 6(a). It chooses one of the clocks from $Clk_{prim}\div 2^i$ for Clk_{DCC}, based on the required f_s at any time. DCC works by determining the ratio of f_s to Clk_{DCC}-rate, at any time. While the control loop tries to maintain this ratio at 1:2, it switches to the next higher rate of Clk_{DCC} when the ratio is more than 1/2 and it switches to the next lower rate of Clk_{DCC} when the ratio is less than 1/2.

DCC counts the number of active-high V_{cmp}-pulses in each counting interval. A counting interval compromises of two periods of the current Clk_{DCC}. The count (Cnt_{load}) of V_{cmp}-pulses cannot be greater than 2 as each counting interval has only two active edges of Clk_{DCC} and there can be a maximum of only one V_{cmp}-pulse at each active edge of Clk_{DCC}. V_{cmp}-pulses are counted instead of $\emptyset_{on}$-pulses, as $\emptyset_{on}$-pulses are suppressed

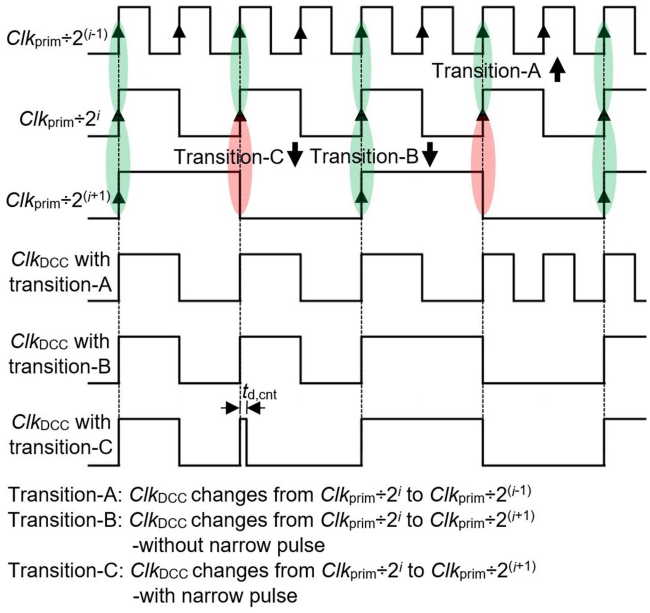


Fig. 7. Behaviour of the controller clock at its rate-transitions.

to prevent L-current ramping-up (at startup) and the actual f_s-requirement is captured by the V_{cmp}-pulses. When $Cnt_{load}=1$, it signifies the ratio of f_s to Clk_{DCC}-rate to be 1:2 and the current Clk_{DCC} is unchanged. When $Cnt_{load}=0$, DCC makes the Clk_{DCC}-rate half (as the said ratio is less than 1/2). When $Cnt_{load}=2$, DCC doubles the Clk_{DCC}–rate (as the said ratio is more than 1/2). Clk_{sel} is used to select one of the $Clk_{prim}\div 2^i$ clocks for Clk_{DCC} at any time. Clk_{DCC}-rate is made two times its current value by decrementing Clk_{sel} and Clk_{DCC}-rate is made half the current value by incrementing Clk_{sel}. At power on reset, Clk_{DCC} is at Clk_{prim}. Fig. 6(b) shows the operating waveforms of DCC. Cnt_{load} is reset at the start of each counting interval. Any change in Clk_{DCC} is effected instantaneously at the end of the counting interval (at Cnt_{gate}).

As the controller clock is at $2\times f_s$ against (3–4)$\times f_s$ in prior work [6], our converter can work at a higher f_s at any given controller frequency or controller loss. As shown in Section III, this helps to reduce conduction loss and also, to have a smaller C_o.

A. Behavior at Clock Rate-Transitions

Fig. 7 illustrates the possible patterns of Clk_{DCC} at its rate×2 and rate/2 transitions. The frequency-divider of Clk_{prim} consists of a cascaded set of frequency-divider units, with each unit performing a ÷2 operation. The output of (÷2) frequency-divider unit-i provides $Clk_{prim}\div 2^i$, for i in the range of 1 to 7. The rate transition of Clk_{DCC} corresponds to switching of Clk_{DCC} from the currently selected $Clk_{prim}\div 2^i$ to either $Clk_{prim}\div 2^{(i-1)}$ for rate×2 or $Clk_{prim}\div 2^{(i+1)}$ for rate/2. Clk_{DCC} rate-transition happens after (a small delay of $t_{d,cnt}$ from) a rising-edge on Clk_{DCC}. As each (÷2) frequency-divider unit is triggered at the rising edge, any rising edge on $Clk_{prim}\div 2^i$ coincides with the rising edge on $Clk_{prim}\div 2^{(i-1)}$. So, at rate×2-transition, there is no change in the logic (high) level of Clk_{DCC}, as shown in Fig. 7. The first rising-edge of Clk_{DCC} after the rate×2-transition

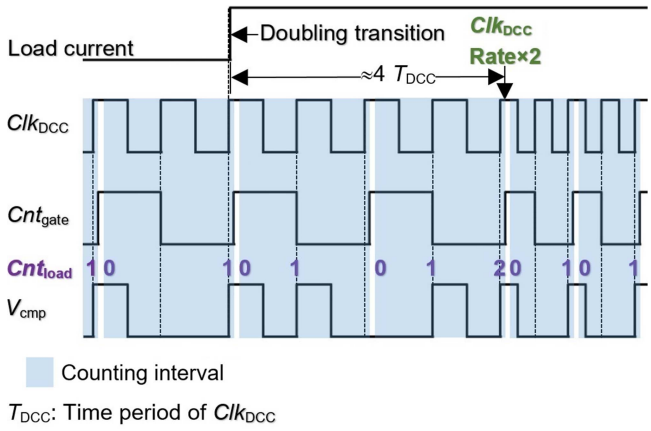


Fig. 8. Response time for controller clock adaptation to load doubling.

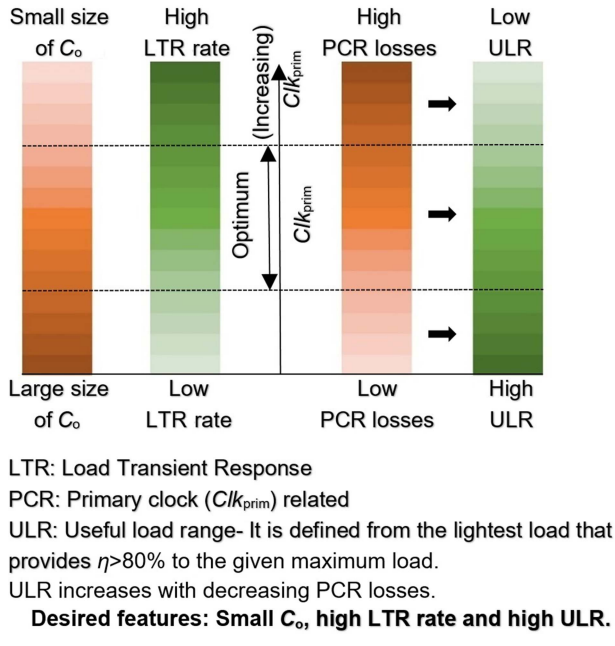


Fig. 9. Determination of the optimum primary clock based on the parameter dependencies, at a given maximum load rating and V_o-ripple.

comes after about one time period of the new Clk_{DCC}. However, a rising edge on $Clk_{prim}\div 2^i$ can coincide with either the rising or the falling edge on $Clk_{prim}\div 2^{(i+1)}$. So, at rate/2-transition, there can be either no change in the logic (high) level of Clk_{DCC} or a level change in Clk_{DCC} to logic-low resulting in a narrow pulse of width $t_{d,cnt}$ (in the case of a coinciding falling edge on $Clk_{prim}\div 2^{(i+1)}$). The first rising-edge of Clk_{DCC} after the rate/2-transition comes after about either one period of the new Clk_{DCC} or half period of the new Clk_{DCC} (in the case of narrow pulse). The possible narrow pulse at rate/2-transition does not affect system performance as Cnt_{load} is 0 for any rate/2-transition, which implies that there is no active switching cycle ($SW_{on} = 0$) at the transition.

B. Load Transient Response Time

As the counting interval scales with the time period of Clk_{DCC}, time taken for every doubling of load capacity (or rate×2-transition of Clk_{DCC}) progressively divides by 2. As shown in Fig. 8, assume the worst case of a load transition to double of its current value to occur immediately after the V_{cmp}-rising edge that coincides with the second Clk_{DCC} in a counting interval. It is also assumed that the current value of load is slightly less than the load corresponding to f_s equal to half-rate of the current Clk_{DCC}. As shown in Fig. 8, the subsequent counting interval could then only need one V_{cmp}-pulse resulting in no transition on Clk_{DCC}-rate. Only in the second counting interval, two V_{cmp}-pulses are expected, which results in the doubling of Clk_{DCC}-rate at the end of the counting interval. So, in this worst case, the time taken to double the Clk_{DCC}-rate for a load-doubling transition is ≈4 time periods of the original Clk_{DCC}. As Clk_{DCC} tracks $2\times f_s$, the capacity doubling time can also be expressed as 2 switching periods. Note that switching period is equal to $1/f_s$. With multiple such load doubling transitions starting from the lowest load corresponding to f_s equal to half-rate of $Clk_{prim}\div 2^7$ and with each such load doubling transition immediately following the Clk_{DCC}-rate×2-transition, the total time required for Clk_{DCC} to transition to Clk_{prim} from the time instant of application of the first load×2-transition, is given by

$$t_{load,rise,max} \approx \sum_{i=1}^{7} (2T_{s,i}). \tag{11}$$

$t_{load,rise,max}$ is the maximum response time of the converter to load rise transient. $T_{s,i}$ is the switching period for f_s at half-rate of $Clk_{prim}\div 2^i$. It may be noted that the converter can supply a maximum load corresponding to f_s equal to Clk_{prim}-rate. $t_{load,rise,max}$, thus, gives the maximum response time for 256x load rise transient. Deriving from (11), the response time of the converter to 256x load rise transient is expressed as $t_{load,rise}$ in

$$t_{load,rise} < 4\,T_{s,7}. \tag{12}$$

As the rate of Clk_{DCC} is greater than the required f_s at all times in a load fall transient, the system can work at the required f_s and there is no expected dip in V_o at the transient. By similar argument as discussed for the load rise transient, the transient response time for (1/256) load fall transient $t_{load,fall}$, is given by

$$t_{load,fall} < 2\,T_{s,7}. \tag{13}$$

As $t_{load,fall}$ is the time required for Clk_{DCC} to transition to $Clk_{prim}\div 2^7$, it does not include the additional time ($2T_{s,i}$) for $i = 7$.

C. Choice of Primary Clock

As $I_o \propto f_s$, the maximum load is delivered at the maximum f_s, which is the Clk_{prim}-rate. For a given maximum load, the choice of a high Clk_{prim} [by accordingly setting the constant T_{on} and L as per (8)] implies a high f_s at any load in the 256x range. As given by (10), this can help to reduce the size of C_o without affecting the V_o-attributes. Also, a high Clk_{prim} reduces $T_{s,7}$ in (12) and

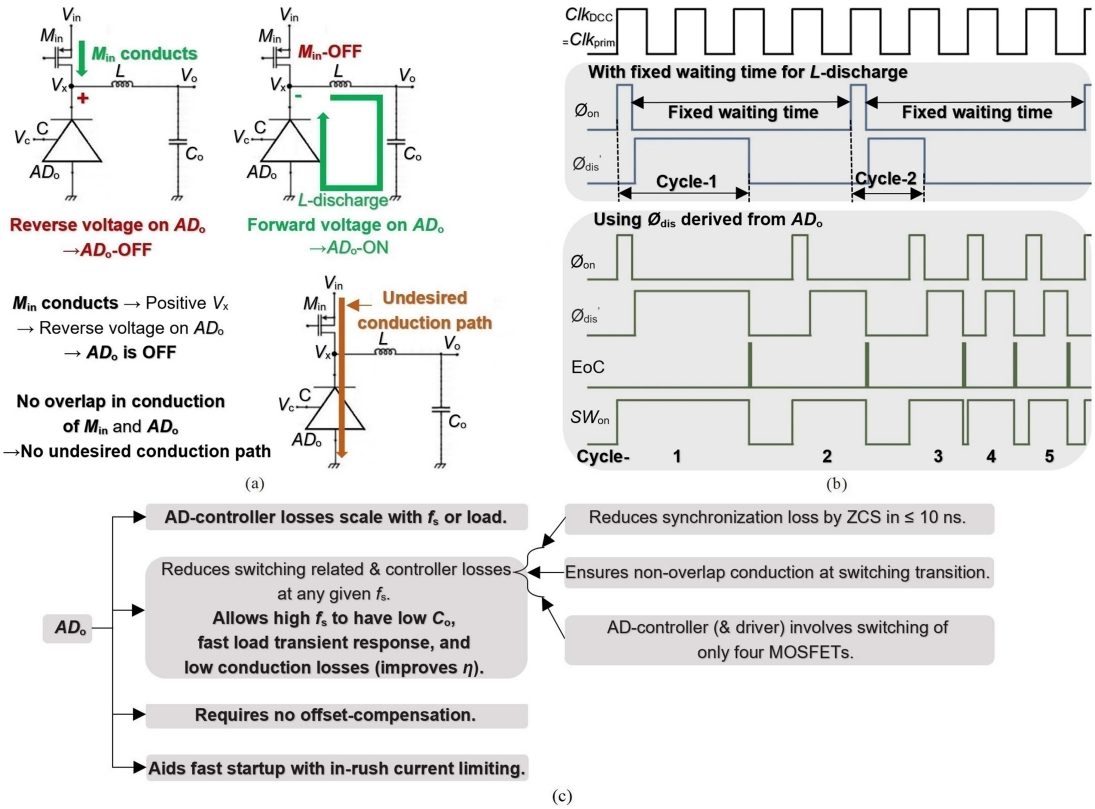


Fig. 10. Deployment of AD. (a) Illustration of non-overlap conduction of buck-converter switches. (b) Representative illustration of fast startup by using $\emptyset_{\rm dis}$ for in-rush current limiting. (c) Summary of merits of deployment of AD in PFM-based buck converter.

(13), which improves the load transient response rate. However, $Clk_{\rm prim}$ related losses resulting from the power consumption by its oscillator, driver and frequency-divider, proportionally increase with $Clk_{\rm prim}$. $Clk_{\rm prim}$ related losses do not scale with $Clk_{\rm DCC}$ or load. At light load, these losses become relatively significant and it degrades η. Thus, while a high $Clk_{\rm prim}$ increases the load transient response rate and requires a small $C_{\rm o}$, it limits the light load-η. An optimum value of $Clk_{\rm prim}$ is chosen so that all the related parameters are within the specified limits. Choice of the optimum $Clk_{\rm prim}$ based on the different dependent parameters, for a given maximum $I_{\rm o}$ and $V_{\rm rpl}$, is shown in Fig. 9.

V. Functions of AD

The AD implementation in our recent work [26] is employed as the L-current discharging diode ($AD_{\rm o}$) in the PFM-based buck converter. $AD_{\rm o}$ has NMOSFET as the AD-switch ($M1$ in [26]). It uses a low-threshold voltage device for the reverse voltage sensing MOSFET ($M2$ in [26]). The design chooses the appropriate width for $M2$ to limit the turn-OFF transition time $t_{\rm off,AD}$ of $AD_{\rm o}$ to 10 ns even at slow-slow simulation corner [26]. The additional "G" terminal of the AD shown in Fig. 4, is tapped from the gate terminal of $M1$ of the AD. The digital voltage at "G" provides the ON/OFF status of the AD. The voltage at "G" is logic-inverted to derive the active-low $\emptyset_{\rm dis}$.

Specific merits derived in the proposed buck converter by using the AD, are as follows. 1) Analog controller of AD is bias-free and conducts only at switching transitions, which makes the AD-controller losses to scale with $f_{\rm s}$ or load. 2) AD helps to reduce the following switching related and controller losses at any given $f_{\rm s}$.

1) As the AD provides fast ZCS in $\leq$10 ns, synchronization loss is reduced.
2) If the OFF-transition of the line-side switch $M_{\rm in}$ and ON-transition of $AD_{\rm o}$ coincide, there can be overlapped (or simultaneous) conduction by $M_{\rm in}$ and $AD_{\rm o}$ at the transition. This would result in additional current flow from $V_{\rm in}$ to ground, which is an undesired conduction path leading to power loss at the switching transition. However, as the AD self-detects and turns ON only at the presence of a forward voltage across it, nonoverlap conduction of the switches is ensured. As shown in Fig. 10(a), current flow in the undesired path is blocked. Furthermore, a low dead-time can be achieved due to the low turn-ON transition time $t_{\rm on,AD}$ of AD [26].
3) As the operation of AD-controller (including driver) involves the switching of only four MOSFETs [26] for achieving the dual functions of high-speed ZCS and dead-time control, the controller power consumption is kept low.

While keeping the switching related and controller losses at bay, the converter can be allowed to work at a high $f_{\rm s}$ that provides the benefits of small $C_{\rm o}$, fast load transient response, and low conduction losses (to improve η at any load). 3) AD has inherently no offset issue and does not need offset-compensation. 4) As the analog AD provides ZCS instantaneously right from startup, $\emptyset_{\rm dis}$ is accordingly available to prevent L-current from

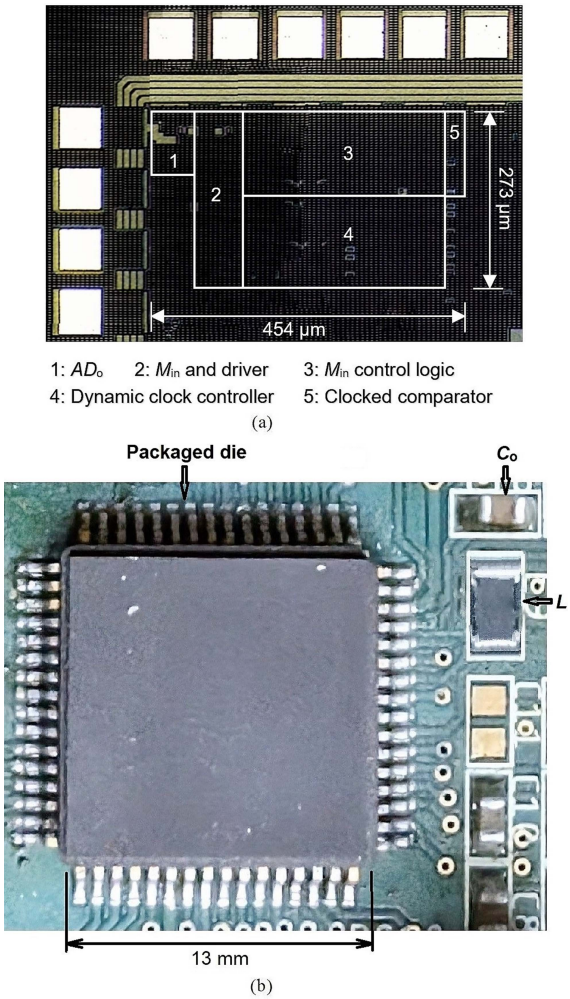


Fig. 11. Prototype of the PFM-based buck converter. (a) Die Microphotograph. (b) Photograph of packaged die, L, and C_o on the test board.

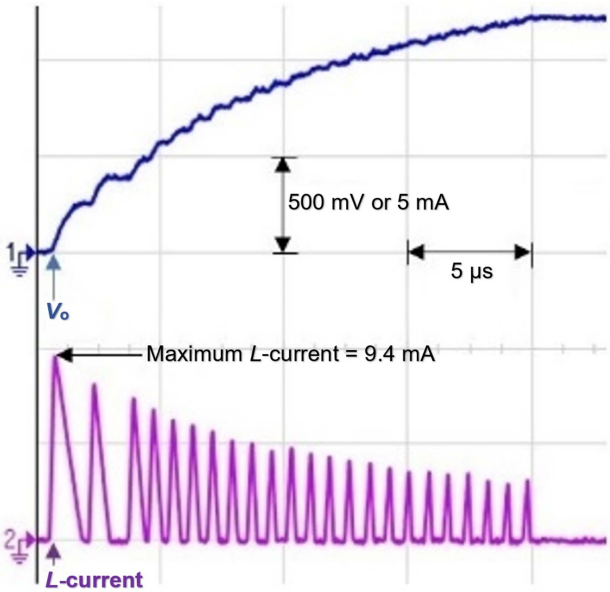


Fig. 12. Measured L-current at startup of buck converter with $V_{in} = 1.8$ V and at no load.

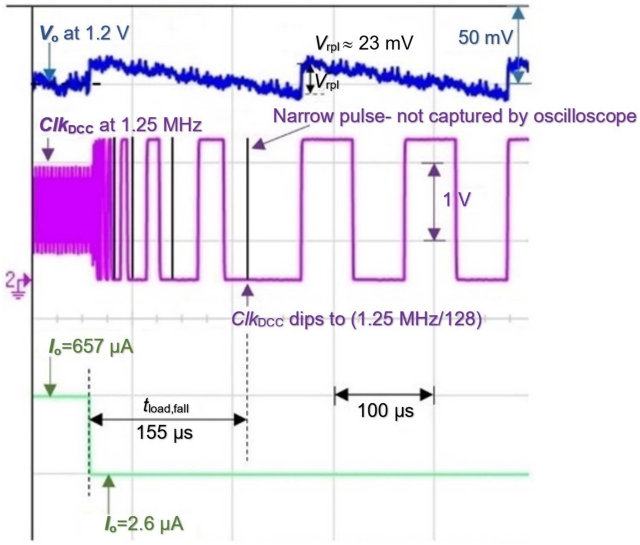


Fig. 13. Measured transient response of buck converter for load fall, at $V_{in} = 1.8$ V.

ramping-up. This eliminates the requirement of waiting for a fixed OFF-time at startup for ensuring the full discharge of L-current [9]. $\emptyset_{dis}$ at startup, allows L to be charged immediately after the completion of the current L-discharge at the following Clk_{DCC} ($=Clk_{prim}$). This helps to save time and provide a fast startup. Fig. 10(b) shows that the deployment of $\emptyset_{dis}$ for in-rush current limiting, can speed up the startup. It gives a representative illustration that depicts the completion of five switching cycles with the proposed scheme and the completion of only two switching cycles in the same time with the scheme using fixed waiting time. Fig. 10(c) summarizes the merits of deployment of the AD in the PFM-based buck converter.

VI. Measurement Results

The proposed system is fabricated and tested in 180 nm CMOS technology. Fig. 11(a) shows the die microphotograph of the PFM-based buck converter. The converter occupies an area of 108290 μm^2 on the chip. The die (which also houses other circuits not part of the proposed converter) has a size of 1520 μm$\times$1520 μm. Fig. 11(b) shows the packaged die and the externally connected components- L and C_o, on the test board. Reference generator and Clk_{prim}-oscillator are not part of the chip. The reference voltage and Clk_{prim} were externally provided for the testing. L, C_o, and Clk_{prim}-rate used were 33 μH, 27 nF, and 1.25 MHz, respectively. During the tests, the voltage at "C" V_c of AD_o, M_{in}-driver voltage $V_{drv,PMOS}$, main controller-voltage V_{cntrl}, and V_{in}, drawing currents I_c, $I_{drv,PMOS}$, I_{cntrl}, and I_{in}, respectively, were supplied by a single voltage source.

Fig. 12 shows the startup of the buck converter in $\approx$20 μs with $V_{in} = 1.8$ V and at no load. It shows that each charging of L happens only after its full discharge, resulting in no ramping-up of L-current.

The measured load transient response of the converter for a fall of load from the maximum I_o of 657 μA to (657/256) μA,

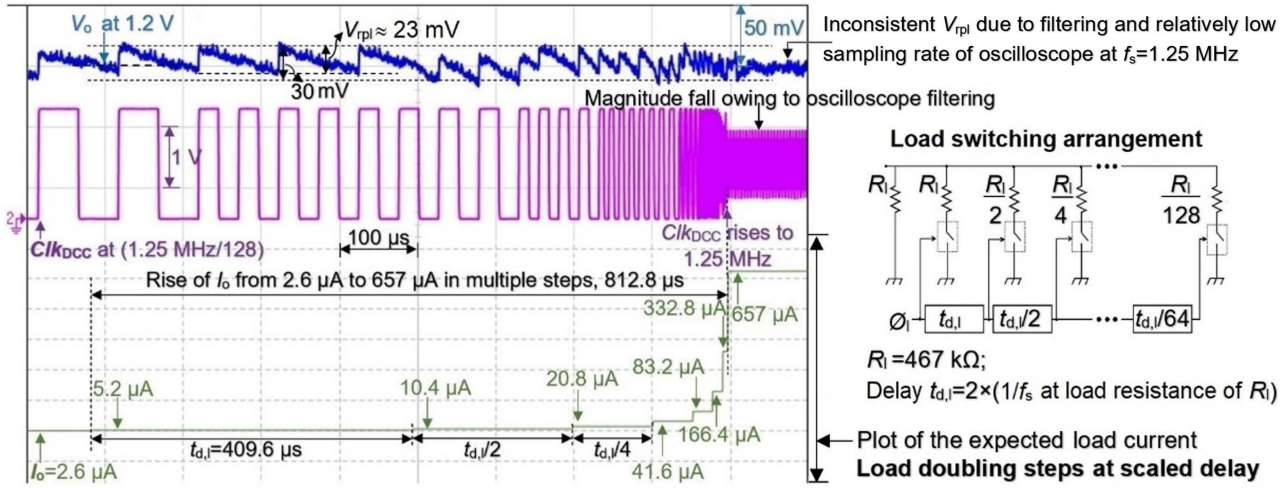


Fig. 14. Measured transient response of buck converter for load rise, at $V_{\rm in} = 1.8$ V.

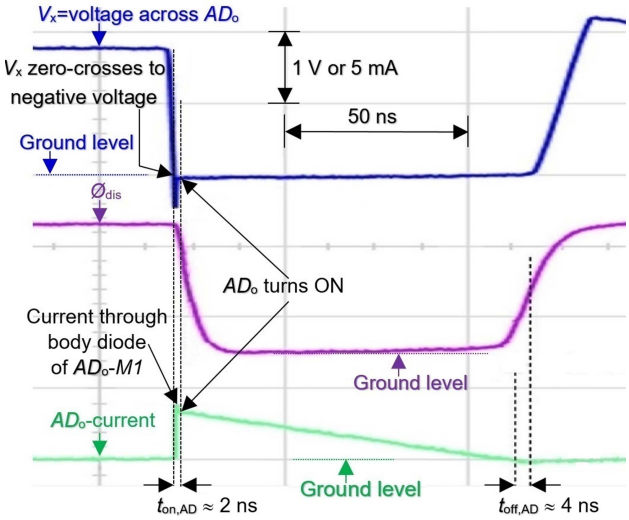


Fig. 15. Measured waveforms at $AD_{\rm o}$, with $V_{\rm in} = 1.8$ V and $I_{\rm o} = 328.5$ μA.

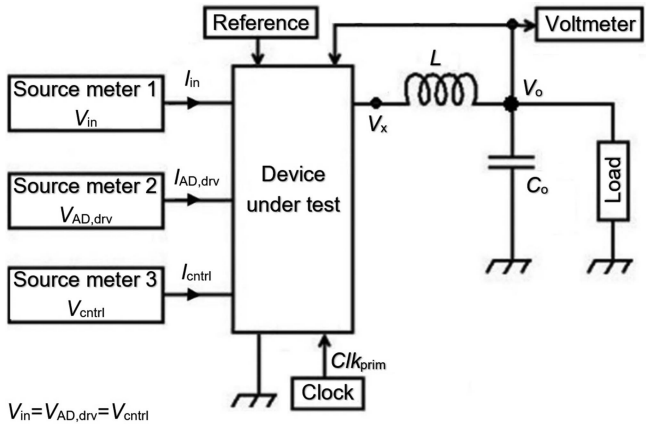


Fig. 16. Measurement setup of buck converter for demonstrating the scaling of different losses with load and for determining η.

is shown in Fig. 13. It shows the best case of $t_{\rm load,fall} = 155$ μs, which corresponds to the occurrence of narrow pulses at each $Clk_{\rm DCC}$-rate-transition and having the consecutive $Clk_{\rm DCC}$-rate-transitions separated by a duration of 1.5 times the time period of the existing $Clk_{\rm DCC}$ (before the rate-transition). The need of no significant voltage droop to respond to load-rise was confirmed by using the specified loading pattern, as shown in Fig. 14, at $C_{\rm o} = 27$ nF. Fig. 14 also shows the load switching arrangement used to obtain the required loading pattern. The measured waveform in Fig. 14 shows that the voltage droop was only 7 mV and the total minimum to maximum variation in $V_{\rm o}$ was 30 mV across 256x load range. Figs. 13 and 14 show the measured behavior of $Clk_{\rm DCC}$, which matches the expected. At $V_{\rm in} = 1.8$ V, the measured ripple voltage and load regulation were 23 mV and 0.7%, respectively, in the 256x load range.

Fig. 15 shows the waveforms related to $AD_{\rm o}$, at $V_{\rm in} = 1.8$ V and $I_{\rm o} = 328.5$ μA. It is seen that $AD_{\rm o}$ starts conducting only at the presence of a forward voltage (negative $V_{\rm x}$). Fig. 15 also shows the measured $t_{\rm on,AD}$ and $t_{\rm off,AD}$ of $AD_{\rm o}$.

The scaling of different losses in the buck converter with load was demonstrated by using the measurement setup in Fig. 16. It uses a different source meter for supplying and measuring each of $I_{\rm in}$, $I_{\rm AD,drv}$ (=($I_{\rm c} + I_{\rm drv,PMOS}$)), and $I_{\rm cntrl}$, at voltages of $V_{\rm in}$, $V_{\rm AD,drv}$, and $V_{\rm cntrl}$, respectively. Also, $V_{\rm in} = V_{\rm AD,drv} = V_{\rm cntrl}$. η of buck converter is calculated, as given by

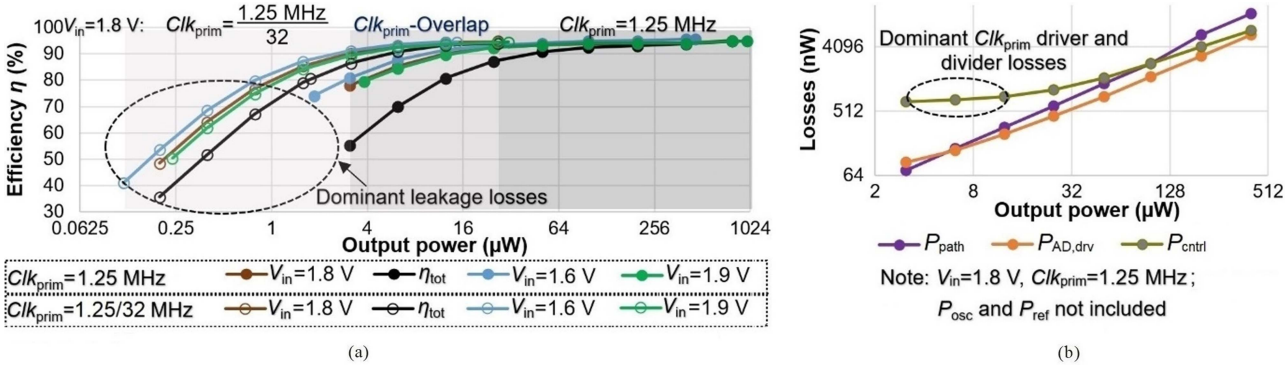
$$\eta = \frac{V_{\rm o} I_{\rm o}}{V_{\rm in}\ I_{\rm in,tot}}\ . \tag{14}$$

$I_{\rm in,tot}$ is the sum of $I_{\rm in}$, $I_{\rm AD,drv}$, and $I_{\rm cntrl}$. η was calculated by measuring $I_{\rm in,tot}$ at different values of $V_{\rm in}$ and output power $P_{\rm o}$ (=$V_{\rm o}I_{\rm o}$). As $Clk_{\rm prim}$-oscillator and reference generator are not part of the chip, the power consumption by these are not captured by η in (14). However, the power consumption by $Clk_{\rm prim}$-oscillator ($P_{\rm osc}$) and that by reference generator ($P_{\rm ref}$) can affect the overall η. Typical η at $V_{\rm in}$ of 1.8 V adjusted by including the possible $P_{\rm osc}$ and $P_{\rm ref}$, is denoted by $\eta_{\rm tot}$ and calculated, as shown in (15). $P_{\rm osc}$ of 1.5 μW was assumed at $Clk_{\rm prim}$ of 1.25 MHz based on prior works [5], [35] and $P_{\rm ref}$ of

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS ON BUCK CONVERTER

	[10] JSSC'16	[11] JSSC'17	[8] JSSC'18	[4] TCAS-I'22	[5] TPE'22	[6] JSSC'22	This work	
Technology	180 nm CMOS	65 nm CMOS	130 nm CMOS	180 nm BCD	350 nm CMOS	65 nm CMOS	180 nm CMOS	
V_{in}	0.55–1.0 V	1.2–3.3 V	1.8-3.3 V	2.7–4.7 V	2.7–4.2 V	1.5–2.3 V	1.6–1.9 V	
V_o	0.35–0.5 V	0.7–0.9 V	1.2 V	1.6 V	1.8 V	0.5–0.9 V	1.2 V	
Maximum I_o	20 mA	1 mA	2.65 mA	100 mA	50 mA	3 mA**	657 μA, V_{in}=1.8 V	
Minimum I_o (% of maximum I_o)	0.0005	0.00005	0.00377	0.001	0.2	0.000033**	0.02538	
P_o	50 nW–10 mW	400 pW–800 μW	120 nW–3.18 mW	1.6 μW–160 mW	180 μW–90 mW	0.5 nW–2.75 mW	0.2–788 μW, V_{in}=1.8 V	
Power density (P_o/die area)	14.7 mW/mm^2	2.5 mW/mm^2	22.7 mW/mm^2	290.9 mW/mm^2	201.3 mW/mm^2	11.6 mW/mm^2	9.0 mW/mm^2	
L, C_o	4.7 μH, 4.7 μF	47 μH, 350 nF	18 μH, 56 nF	4.7 μH, 4.7 μF	15 μH, 100 μF	22 μH, 4.7 µF	33 μH, 27 nF	
Control	Synchronous	Synchronous	Asynchronous	Asynchronous	Synchronous	Hybrid	Synchronous	
ZCS method	Digital tuning	Digital tuning	Predictive	duty-cycled comparator	N/R	Digital tuning	Bias-free analog AD [26]	
V_{rpl}	<10 mV	20 mV	29 mV	40 mV	3 mV	6.5 mV**	23 mV, V_{in}=1.8 V	
Load transient response: time to switch to high power mode or to high Clk_{sys}	N/R	Externally triggered	<200 ns (100 nA–2.65 mA)	Externally triggered	Externally triggered	**Synchronous control: 18 ms** (7-105 µA)** Asynchronous control with voltage droop of 56 mV: 173 μs (45 nA–1 mA)	**Synchronous control: 812.8 μs (2.6-657 μA)** Voltage droop=7 mV	
Minimum P_o with η^*>80%	22.5 μW**	0.9 nW	60 μW**	32 μW	Lowest P_o tested=180 μW, η=91.8%	4.3 nW	Power	Clk_{prim}
							12.4 μW	1.25 MHz
							1.75 μW	1.25/32 MHz
Peak η^*	92%	92%	92.15%	92.1%	94.8%	93%	94.8%	

N/R: Not explicitly reported. Clk_{sys}: Controller clock. * η_{tot} for this work. ** Estimated from results.



(a) (b)

Fig. 17. Measured performance of buck converter. (a) Efficiency at different $V_{\rm in}$ and $P_{\rm o}$. (b) Scaling of different power losses with $P_{\rm o}$, at $V_{\rm in} = 1.8$ V.

100 nW was used as per earlier work [4].

$$\eta_{\rm tot} = \frac{V_{\rm o} I_{\rm o}}{(V_{\rm in}\, I_{\rm in,tot} + P_{\rm osc} + P_{\rm ref})} \tag{15}$$

Fig. 17(a) shows the peak $\eta_{\rm tot}$ (considering $P_{\rm osc}$ and $P_{\rm ref}$ also,) to be 94.8% at the maximum $P_{\rm o}$ of 788 μW (with $f_{\rm s}$ = Rate of $Clk_{\rm DCC}$ = Rate of $Clk_{\rm prim}$ = 1.25 MHz). It also shows that a high $\eta_{\rm tot}$ (>80%) is attained even at $P_{\rm o}$, as low as 12.4 μW. Shift in $P_{\rm o}$-range with change in $V_{\rm in}$ is caused by the constant ON-time, as shown by (8). Fig. 17(b) shows the scaling of different losses (excluding $P_{\rm osc}$ and $P_{\rm ref}$) with $P_{\rm o}$ (or load), at $V_{\rm in} = 1.8$ V. The total power drawn by "C" of $AD_{\rm o}$ and that by driver of $M_{\rm in}$, is given by the power loss component $P_{\rm AD,drv}$. The power drawn by the controller (excluding $AD_{\rm o}$-controller) of converter is denoted by the loss component $P_{\rm cntrl}$. The power loss in the power flow path of the buck converter is given by $P_{\rm path}$. $P_{\rm AD,drv}$, $P_{\rm cntrl}$, and $P_{\rm path}$, are given by (16)–(18) and the measured values of these have been plotted in Fig. 17(b).

$$P_{\rm AD,drv} = V_{\rm AD,drv} I_{\rm AD,drv} \tag{16}$$

$$P_{\rm cntrl} = V_{\rm cntrl} I_{\rm cntrl} \tag{17}$$

$$P_{\rm path} = V_{\rm in} I_{\rm in} - P_{\rm o} \tag{18}$$

Fig. 17(b) shows that all losses at $M_{\rm in}$-driver and $AD_{\rm o}$–controller-and-driver, scale proportionally with load. Also, the losses in power flow path proportionally decrease with load, as expected. While the main-controller losses ($P_{\rm cntrl}$) also decrease with load, there is a load-independent loss component in $P_{\rm cntrl}$, which is primarily attributed to the losses in the $Clk_{\rm prim}$-driver and $Clk_{\rm prim}$-divider.

In a separate experiment, η was measured by changing a single parameter $Clk_{\rm prim}$ to 1.25/32 MHz. With no other parameter changed, the maximum $P_{\rm o}$ at $V_{\rm in}$ = 1.8 V is scaled down to 788/32 μW, as shown by (8). The range of load remains 256x and this extends the lower range of loads. The measured results have been shown in Fig. 17(a). $\eta_{\rm tot}$ was determined by allocating $P_{\rm osc}$ = 1.5/32 μW and $P_{\rm ref}$ = 100 nW. $\eta_{\rm tot}>80\%$ is obtained for $P_{\rm o}\geq$1.75 μW. It is seen that though the minimum $P_{\rm o}$ with $\eta_{\rm tot}>80\%$, has decreased by scaling down $Clk_{\rm prim}$ to 1.25/32 MHz, this minimum $P_{\rm o}$ has not proportionally scaled down. This is attributed to the fixed $P_{\rm ref}$ and leakage losses, which are independent of $Clk_{\rm prim}$. These losses become relatively significant at sub-μW-$P_{\rm o}$. Nevertheless, it may well be appreciated that the minimum $P_{\rm o}$ can be extended down to lighter loads, by dynamically changing the frequency of oscillator [5], [11] of $Clk_{\rm prim}$.

Table I shows that buck converters with synchronous control (including our converter) have better light load-η. To preserve voltage attributes, our converter enhances the state-of-the-art transient response rate of PFM-based converters in synchronous mode (to 2.6-657 μA in 812.8 μs). The proposed converter is seen to be unique in respect of simultaneously providing a fast load transient response, minimal voltage droop, very high peak efficiency ($\eta_{\rm tot}$) of $\approx$95% at the maximum load, high (>80%) light load-efficiency ($\eta_{\rm tot}$), and limited $V_{\rm rpl}$ with a low $C_{\rm o}$ of 27 nF.

The unique contribution has been made by the proposed converter by employing the DCC and the AD. Both DCC and AD are implemented on-chip. DCC is made up of standard digital circuits. AD [26] is an analog circuit consisting of only five MOSFETs (including the switch-*M1*). DCC and AD demand no tuning requirements. AD does not need offset-compensation. Thus, the proposed system can be implemented with relatively less complexity.

VII. Conclusion

A PFM-based buck converter is proposed that uses a synchronous controller to improve the light load-η. The controller losses are scaled with load by making the controller clock track $2\times f_{\rm s}$ using a DCC. The converter responds to 256x load rise transients within 4 switching periods using synchronous control for fine voltage attributes, at 27 nF-$C_{\rm o}$. Deployment of AD provides ZCS in $\leq$10 ns and nonoverlap conduction of switches in the buck converter. As the analog AD-controller is bias-free, it consumes minimal power, which also scales with $f_{\rm s}$ or load. Buck converter shows peak $\eta_{\rm tot}$ of 94.8% for the maximum $P_{\rm o}$ of 788 μW. $\eta_{\rm tot}>80\%$ is obtained for the minimum $P_{\rm o}$ of 12.4 μW and 1.75 μW at $Clk_{\rm prim}$ of 1.25 MHz and 1.25/32 MHz, respectively. Our converter enhances the state-of-the-art load transient response rate in synchronous mode (to 2.6–657 μA in 812.8 μs) for limiting the voltage droop to 7 mV. The proposed converter is unique in respect of simultaneously providing a fast load transient response, minimal voltage droop, very high (>90%) efficiency ($\eta_{\rm tot}$) at the maximum load, high (>80%) light load-efficiency ($\eta_{\rm tot}$), and limited $V_{\rm rpl}$ with a low $C_{\rm o}$ of 27 nF.

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