An Improved Nonlinear Droop Control Strategy in DC Microgrids

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***Abstract*—Droop control has drawn widespread attention and various nonlinear droop characteristics have been developed in dc microgrids. This article proposes an improved nonlinear droop control strategy, which uses the difference between the squared nominal voltage and the squared dc voltage as the droop input and generates the ac current reference directly from the droop characteristic. Compared with the traditional dual-loop droop control strategy, this method can provide faster transient response due to the elimination of the external dc voltage or current loop. And the bus voltage can be regulated very compactly, which is an optimization of steady-state performance. In this article, the stability assessment that violates the constraint conditions of the conventional impedance-based stability criterion is investigated, which considers the number of right-half-plane poles of the open-loop transfer function. The Nyquist criterion of generalized Bode plot is used to analyze the system stability. An adaptive current sharing strategy is proposed to improve the current sharing accuracy in multisource operation. This article also discusses the comprehensive design process for determining droop gain. Finally, experimental results validate the theoretical analysis.**

***Index Terms*—Bode plot, dc microgrid, droop control, impedance-based stability criterion, right-half-plane (RHP) poles.**

NOMENCLATURE

v_d, i_d	d-axis output voltage and current component of DG.
$v_{\rm dc}$, $i_{\rm dc}$	Output voltage, output current of DG.
k_i	Droop gain.
V_0	Nominal voltage.
R_i, L_i, C_i	Cable resistance, cable inductance, local capacitance.
e_d, e_q	PCC voltage in d-axis and q-axis.
R_s, L_s	AC source resistance, ac source inductance.
P_L	Power of CPL.
$V_{\rm bus}$	DC bus voltage in steady state.
ω_L	Control bandwidth of CPL.
ω_c	Inner control bandwidth.
C_b	Bus capacitance.
$R_{\rm CPL}$, $C_{\rm CPL}$, $L_{\rm CPL}$	CPL resistance, CPL capacitance, CPL inductance.

Manuscript received 6 July 2023; revised 6 October 2023 and 25 November 2023; accepted 27 December 2023. Date of publication 1 January 2024; date of current version 20 March 2024. This work was supported in part by the Science and Technology Project of China Southern Power Grid Company, Ltd., under Grant GDKJXM20222178, in part by the National Science Foundation Council of China under Grant 52377194, and in part by the Natural Science Foundation of Shanghai under Grant 22ZR1429800. Recommended for publication by Associate Editor Q. Shafiee. *(Corresponding author: Fei Gao.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3349027.

Digital Object Identifier 10.1109/TPEL.2023.3349027

I. INTRODUCTION

NOWADAYS, the issues of resource scarcity and environmental contamination have stimulated widespread attention on distributed generation (DG), including renewable energy, energy storage systems, and dc loads, such as electric vehicles [1], [2]. DC microgrids (dc MGs) could offer a simple control structure, higher reliability, efficient integration of renewable energy resources [3], and absence of reactive power compensation [4]. As such, they are commonly applied in electric vehicles [5], all-electric ships [6], buildings, and other fields.

When the load converters in dc microgrids are tightly regulated as constant power load (CPL), instability issues may arise due to the negative impedance characteristics. Therefore, system stability is a crucial concern, which depends on multiple factors such as CPL, the interactions among the interconnected converters, cable impedance, system damping, and control bandwidth. In this regard, conducting stability analysis around the operating point is essential. The small signal stability evaluation methods of power electronic systems mainly contain impedance-based analysis method and eigenvalue analysis method.

The eigenvalue analysis method requires comprehensive knowledge of the system's parameters and configuration to establish a detailed system model. However, in cases where the system is considered a "black box" with limited information, it is more advantageous to study the impedances of each subsystem. Analyzing the subsystem interactions and system stability through impedance analysis can provide valuable insights in such scenarios. A comprehensive review of impedance-based criteria, such as the Middlebrook Criterion [7], the Gain Margin and Phase Margin Criterion [8], the Opposing Argument Criterion [9], the Energy Source Analysis Consortium Criterion [10], and the Three Step Impedance Criterion [11], is presented in [12]. All these criteria define various forbidden regions of the polar plot of the minor loop gain and are sufficient but not necessary conditions for determining stability. Additionally, a

passivity-based stability criterion (PBSC) is proposed in [13], which does not require predetermination of source and load partition. While previous studies about PBSC only considered the perturbations of output current, Yu et al. [14] also take the influence of input voltage and reference voltage perturbations of the converter in addition to output current perturbations into account. The impedance sum criterion reported in [15] and [16] is quite simple but limited to a cascaded system consisting of two converters. Furthermore, the bus node impedance criterion, presented in [17], provides a sufficient and necessary condition for the stability of both centralized systems ignoring line impedance and distributed power systems considering line impedance.

The above criteria for assessing the stability of dc microgrids have a prerequisite that each subsystem impedance is individually stable. Liao and Wang [18] provided an alternative criterion that does not require open-loop right-half-plane (RHP) poles constraint and [19] extends it to multibus dc MG. The proposed droop-controlled system in this article may introduce RHP poles in the source subsystem, leading to undesired oscillations. To evaluate system stability, the Nyquist criterion based on the individual impedance Bode plot introduced in [18] and [19] is employed.

In practical dc MGs, the parallel multisource operation is prevalent, highlighting the importance of achieving appropriate power sharing among sources. To address this, decentralized droop control is typically utilized [20], [21] by introducing a virtual resistance at the output of converters [22]. As a passive load sharing approach [23], it does not require critical communication infrastructure, thereby enhancing the system's efficiency and reliability. Nevertheless, the conventional linear droop characteristic necessitates a tradeoff between voltage regulation and load sharing accuracy [24], [25]. While large droop gain exhibits good power sharing performance, the bus voltage deviation is substantial. Conversely, small droop gain optimizes voltage regulation but limits load sharing accuracy [26].

In response to the tradeoff between voltage regulation and load sharing accuracy in traditional linear droop control, several droop control strategies have been proposed. A piecewise linear droop control method is introduced in [27], which divides the droop curve into several segments with increasing droop coefficients to restrain the current sharing error, but its stability is threatened at the intersections of broken lines. Nonlinear droop functions have, thus, become widely used and continuously improved. In [28], a simple nonlinear droop strategy is proposed to identify the droop coefficient in specific heavy loads, incorporating a linear droop function with a negative droop coefficient for light loads to reduce bus voltage deviation. But the curve is nonmonotonic and on the boundary of the linear and nonlinear properties may result in a lower accuracy of the current sharing. Prabhakaran et al. [29] introduced three novel schemes: high-droop gain method, polynomial droop curve method, and polynomial droop curve with voltage compensation method, and extends the research by implementing high order polynomial droop expression and power bidirectional experiment. A generic polynomial expression for unifying different droop functions is proposed in [30], which verifies the superior steady-state performance of nonlinear droop strategies and their impact on system efficiency. Li et al. [31] introduced a V^2-P droop strategy that enables global smooth transition between various operation modes for bidirectional dc–dc converters, and the bus voltage regulation and power tracking control loop are combined through the droop controller. The current-limiting droop control strategy proposed in [32] is a nonlinear droop control essentially and changes the control structure. It offers the advantages of current limitation for converter protection and steady-state operation compared to traditional droop cascade PI control. However, it prioritizes current limitation when the input current reaches its maximum, potentially sacrificing power sharing. And the transient performance of the controller requires further improvement. In [33], different droop curves are proposed to enhance current sharing accuracy under the most probable load conditions for different time periods of a day. However, the delay generated in the transition process can impact current sharing accuracy and load voltage regulation in a brief time. In [34], a decentralized adaptive discrete piecewise droop control is introduced. This approach features a control structure that enables continuous command regulation. Additionally, it involves a comprehensive transient analysis and controller design process. In [35], a decentralized secondary droop control method is proposed, aiming to achieve accurate current sharing among all the converters. Notably, this method avoids the complexity of communication and is applicable in various configurations of dc MGs, including radial, ring, and mesh configurations.

Although the above-mentioned literatures improve the steady-state performance to some extent, they primarily fall under the traditional dual-loop droop control scheme. However, these approaches tend to become more complex with increasing droop function complexity and overlook dynamic performance considerations. To simplify the control structure, a novel ac–dc-coupled droop control strategy is proposed in [36], which generates the active component of ac current directly from the droop function, eliminating external dc voltage or current loop and achieving fast bus voltage dynamics during transients. Nonetheless, as concluded in [37], the voltage regulation performance of the ac–dc-coupled droop method is inferior to that of traditional nonlinear droop characteristics. The comprehensive literature review, which contains nonlinear droop methods is listed in Table I.

Inspired by V^2-P and ac–dc-coupled droop method, the proposed method in this article aims to overcome their limitation by incorporating the voltage squared difference and the elimination of outer current loop, thereby enhancing both the steady-state and dynamic performance of the system. The i_d-$v_{\mathrm{dc}}{}^2$ droop control strategy can be applied to various types of dc MGs, including converters that generate direct voltage output and are coupled to an ac link. This encompasses ac–dc converters, modular dc converters (such as the modular multilevel converter serving as an ac–dc converter [38], [39], and VSC-based transformer coupled dc–ac–dc systems [40], [41]). The main contribution of this article can be highlighted as follows.

TABLE I
LITERATURE REVIEW OF NONLINEAR DROOP METHOD

References	Methods	Number of cascaded loops	Steady-state performance enhancement	Dynamic performance enhancement	Stability analysis
[27]	Piece-wise linear method	2	√	×	×
[28]	Nonlinear and negative linear droop method	2	√	×	√
[29]	Polynomial droop curve with Voltage compensation (PDCVC) method	2	√	×	√
[30]	Generic polynomial expression-based method	2	√	×	√
[31]	V^2-P method	2	×	×	√
[32]	Current-limiting method	2	√	×	√
[33]	Load profile-based method	2	√	×	×
[34]	Decentralized adaptive discrete piecewise method	2	√	×	√
[35]	Decentralized secondary method	2	√	×	√
[36]	Ac/dc-coupled droop	1	×	√	√
This paper	Proposed method	1	√	√	√

1) A comparative analysis among four droop strategies is conducted to evaluate comprehensive system performances.
2) Open-loop RHP poles are identified and the Nyquist criterion based on the individual impedance Bode plot is considered for the stability analysis.
3) An adaptive current sharing strategy is proposed to improve the current sharing accuracy in the multisource operation. Also, the design process for determining droop gain is provided.

The rest of this article is organized as follows. Section II presents the proposed droop strategy and compares its steady-state performance with three alternative strategies. Section III covers the system architecture and small-signal modeling. Stability analysis of the single-source single-load system, including the impact of parameters, is discussed in Section IV. Section V focuses on multisource operation, while the experimental results are shown in Section VI to validate the proposed strategy. Finally, Section VII concludes this article.

II. PROPOSED NONLINEAR DROOP

Fig. 1 shows a typical dc MG consisting of multiple converters connected to a common dc bus through cable impedance. Fig. 2 presents a decoupled vector control strategy for voltage source converters (VSCs) where the active power is controlled in d-axis, and power sharing could be regulated by directly tuning i_d. It is worth-noting that our analysis is limited to systems incorporating VSCs controlled within the $dq0$ frame.

A. Overview of Three Droop Strategies

For the sake of steady-state comparison, this section first presents three other droop control strategies.

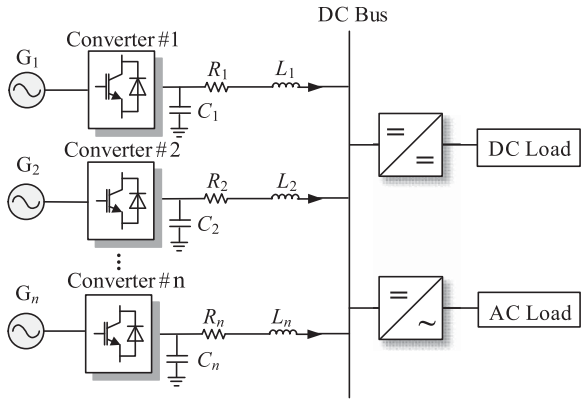

Fig. 1. Typical DC MG configuration.

The traditional current mode droop control scheme is depicted in Fig. 3(a) where the output corresponds to the dc current reference

$$i_{\mathrm{dc}}^{*} = \frac{V_0 - v_{\mathrm{dc}}}{k}. \tag{1}$$

In order to provide further contrast, a strategy is suggested that maintains the original current mode dual-loop control, while utilizing the voltage squared difference as droop input, as shown in Fig. 3(b). This approach can be expressed as

$$i_{\mathrm{dc}}^{*} = \frac{V_0^2 - v_{\mathrm{dc}}^2}{k}. \tag{2}$$

In addition, as shown in Fig. 3(c), the previously proposed ac–dc-coupled droop strategy presented in [34] is written as

$$i_{d}^{*} = \frac{V_0 - v_{\mathrm{dc}}}{k}. \tag{3}$$

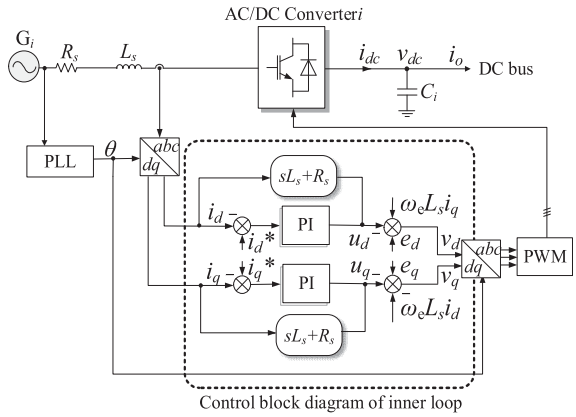

Fig. 2. Vector-controlled VSC.

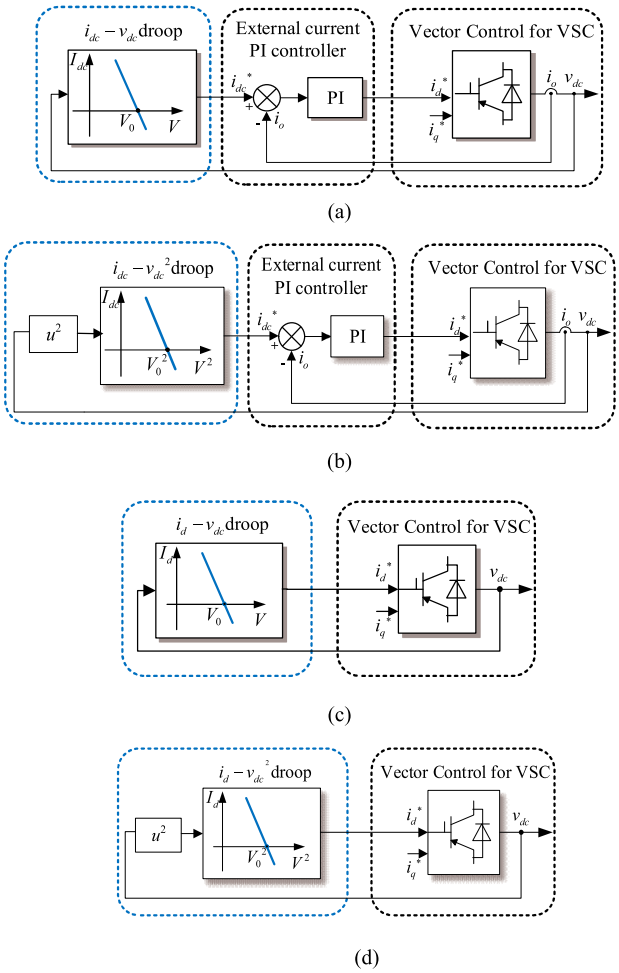

Fig. 3. Control scheme of droop strategy. (a) Traditional i_{dc}-v_{dc} strategy. (b) i_{dc}-$v_{\mathrm{dc}}{}^2$ strategy. (c) i_d-v_{dc} strategy. (d) Proposed i_d-$v_{\mathrm{dc}}{}^2$ strategy.

B. Proposed Droop Characteristic

To comprehensively enhance the performance of the system, an improved ac directly-controlled droop strategy is proposed. The i_d-$v_{\mathrm{dc}}{}^2$ droop characteristic can be formulated as follows:

$$i_d^* = \frac{V_0^2 - v_{dc}^2}{k} \tag{4}$$

where i_d* is the reference value of active component of ac current; V_0 represents the nominal voltage; k is the droop gain; v_{dc} is the sampled output dc voltage of VSC. The control scheme of proposed strategy is shown in Fig. 3(d).

On the one hand, compared with linear current-mode and i_{dc}-$v_{\mathrm{dc}}{}^2$ droop strategy, the d-axis current reference is directly generated from the droop characteristics, which ensures that the ac current is correlated with the load sharing performance. Consequently, this approach simplifies the control structure and optimizes the dynamic performance accordingly. On the other hand, compared with i_d-v_{dc} strategy, the proposed strategy reduces the bus voltage deviation. The voltage squared difference is introduced as the droop input, which is equivalent to the product of the voltage difference, as expressed in (3), and an additional term: $(v_{\mathrm{dc}} + V_0)$. This predicts that the proposed i_d-$v_{\mathrm{dc}}{}^2$ droop strategy exhibits a smaller voltage deviation for the same droop gain.

C. Steady-State Performance

1) Voltage Regulation: For the sake of simplicity, by assuming zero reactive power, the steady-state relationship between dc and ac voltage or current can be expressed as

$$\begin{cases} I_d = \frac{V_0^2 - V_{\mathrm{dc}}^2}{k} \\ V_d = e_d - I_d R_s \\ P_L = V_{\mathrm{dc}} I_{\mathrm{dc}} = \frac{3}{2} V_d I_d \end{cases} \tag{5}$$

where e_d is bus voltage at the point of common coupling (PCC); R_s is the ac side resistance; P_L is the load power. By combining (5), the *V-I* characteristic of the VSC under i_d-$v_{\mathrm{dc}}{}^2$ droop control can be derived, which reveals the nonlinear nature of the proposed strategy

$$I_{\mathrm{dc}} = \left(\frac{3e_d V_0^2}{2k} - \frac{3R_s V_0^4}{2k^2}\right)\frac{1}{V_{\mathrm{dc}}} + \left(\frac{3R_s V_0^2}{k^2} - \frac{3e_d}{2k}\right) V_{\mathrm{dc}} - \frac{3R_s}{2k^2} V_{\mathrm{dc}}^3. \tag{6}$$

When P_L is substituted, the dc voltage can be calculated by

$$V_{\mathrm{dc}} = \sqrt{\frac{2R_s V_0^2 - k e_d \pm k\sqrt{e_d^2 - \frac{8}{3} R_s P_L}}{2R_s}}. \tag{7}$$

Dc voltage associated with the ac–dc-coupled droop strategy can be derived as

$$V_{\mathrm{dc}} = \frac{6R_s V_0 - 3k e_d + k\sqrt{3(3e_d^2 - 8P_L R_s)}}{6R_s}. \tag{8}$$

Based on (7), (8) and the practical scenario illustrated in Table II, the voltage regulation comparison among the four strategies with same load and droop coefficient is shown in Fig. 4. The following three points require specific attention.

First, in Fig. 4(a), it can be observed that there might exist two intersection points between the load curve and the droop curve. The expression for the second intersection point $V_{\mathrm{dc}}{}^{(2)}$ is

$$V_{\mathrm{dc}}^{(2)} = \sqrt{\frac{2R_s V_0^2 - k e_d - k\sqrt{e_d^2 - \frac{8}{3} R_s P_L}}{2R_s}}. \tag{9}$$

TABLE II
SYSTEM PARAMETERS

Category	Parameter	Symbol	Value
Hardware parameters	Ac source resistance	R_s	0.05 Ω
	Ac source inductance	L_s	3 mH
	PCC voltage	e_d	100 V
	Local capacitance	C_i	1.6 mF
	Cable resistance	R_i	0.2 Ω
	Cable inductance	L_i	65 μH
	Bus capacitance	C_b	0.6 mF
	CPL resistance	R_{CPL}	9.2 Ω
	CPL capacitance	C_{CPL}	1 μF
	CPL inductance	L_{CPL}	1.3 mH
	Power of CPL	P_L	1000 W
Controller parameters	Inner control bandwidth	ω_c	800 Hz
	Nominal voltage	V_o	270 V
	CPL bandwidth	ω_L	10^3 rad/s

Then, the feasible droop gain to meet the above requirement can be obtained as

$$k < \frac{2R_sV_0^2}{e_d + \sqrt{e_d^2 - \frac{8}{3}R_sP_L}}. \tag{10}$$

Second, when the load curve and droop curve do not intersect, indicating the system has no operating point, e.g., $k = 1000$ in Fig. 4(c). However, with the $i_{\rm dc}$-$v_{\rm dc}$ strategy in Fig. 4(b), the operating point no longer exists when $k = 20$, limiting the feasible region of k. According to (7), the condition for the existence of operating points under i_d-$v_{\rm dc}{}^2$ strategy is

$$k < \frac{6R_sV_0^2}{3e_d - \sqrt{3}\sqrt{3e_d^2 - 8P_LR_s}}. \tag{11}$$

The right-hand side of inequality (11) of the i_d-$v_{\rm dc}$ strategy can be obtained by substituting $V_0{}^2$ with V_0, which indicates that the range of k under the proposed strategy is significantly larger.

Finally, it is worth noting that the voltage deviation reduction is achieved by the i_d-$v_{\rm dc}{}^2$ strategy, as shown in Fig. 4(a), can be mathematically explained by the voltage sum according to (3) and (4). Besides, Fig. 4(a) illustrates that when k is small, the droop curve behaves as an elliptic curve where operating point is located in the convex part. However, as k increases ($k = 1000$), the proposed droop curve takes a concave shape, which only intersects once with the CPL curve. Furthermore, Fig. 4(d) shows that the voltage regulation performance of $i_{\rm dc}$-$v_{\rm dc}{}^2$ strategy is nearly identical to that of i_d-$v_{\rm dc}{}^2$ strategy when k is small, but it remains a convex curve as increasing k, resulting in smaller voltage deviation than that of i_d-$v_{\rm dc}{}^2$ strategy. Given the similar characteristics of these two droop strategies, in scenarios where both dc–dc converters and VSCs coexist within a DC MG, employing i_d-$v_{\rm dc}{}^2$ strategy for the VSCs, while employing $i_{\rm dc}$-$v_{\rm dc}{}^2$ strategy for dc–dc converters can facilitate the droop gain design process.

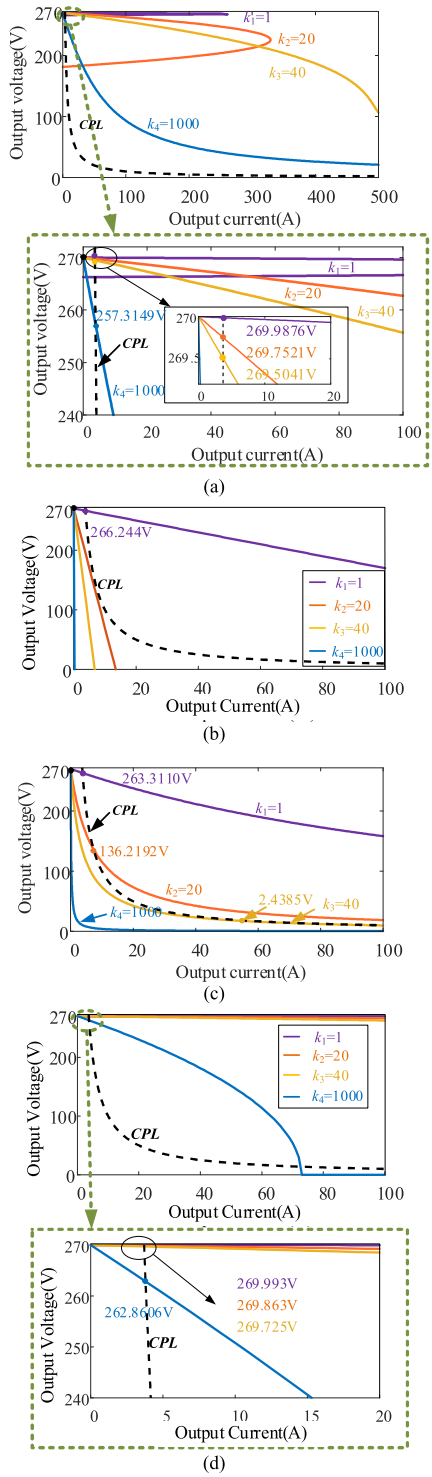

Fig. 4. Comparison of voltage regulation for different droop. (a) Proposed i_d-$v_{\rm dc}{}^2$strategy (better). (b) $i_{\rm dc}$-$v_{\rm dc}$ strategy (worse). (c) i_d-$v_{\rm dc}$ strategy (worst). (d) $i_{\rm dc}$-$v_{\rm dc}{}^2$strategy (best).

2) Load Sharing: Another aspect of system steady-state performance is load sharing performance. To facilitate comparison, a triple-source system with different cable resistances feeding a common CPL is considered. A function related to output voltage

TABLE III
CURRENT AND POWER SHARING COMPARISON

Category	i_d-v_{dc}^2	i_{dc}-v_{dc}	i_d-v_{dc}	i_{dc}-v_{dc}^2
k	745.986	2.451	1.406	1300.236
V_{dc1}	260.392 V	260.392 V	260.392 V	260.392 V
V_{dc2}	260.577 V	260.577 V	260.577 V	260.577 V
V_{dc3}	260.754 V	260.755 V	260.754 V	260.755 V
i_1: i_2: i_3	1.03988: 1.0195:1	1.0392: 1.0192:1	1.0404: 1.1092:1	1.0385: 1.0189:1
P_1: P_2: P_3	1.0383: 1.0188:1	1.0378: 1.0185:1	1.0390: 1.0185:1	1.0371: 1.0182:1
Result	worse	better	worst	best

and current, $d(v,i)$, obtained from (1) to (4) can be used to calculate the current sharing among the sources. The system is described by the following equation:

$$\begin{cases} V_{\text{bus}} = v_1 - R_1 i_1 = v_2 - R_2 i_2 = v_3 - R_3 i_3 \\ d(v_1, i_1) = d(v_2, i_2) = d(v_3, i_3) = 0 \\ V_{\text{bus}}(i_1 + i_2 + i_3) = P_L \end{cases} \tag{12}$$

where R_1 is 0.1 Ω, R_2 is 0.15 Ω, R_3 is 0.2 Ω, P_L is 3 kW, V_{bus} is 260 V.

Table III lists the current and power sharing ratio of the triple-source single-load system when V_{bus} is equal to 260 V. The results show that current and power sharing performance of the proposed strategy is slightly superior than i_d-v_{dc} strategy but a little bit worse than i_{dc}-v_{dc} and i_{dc}-v_{dc}^2 strategy. The droop method that incorporates voltage squared error demonstrates superior accuracy. Additionally, direct control of ac current compromises the accuracy.

In summary, for the i_d-v_{dc} strategy, the steady-state performance is even worse than the conventional linear droop due to its concave droop curve. However, by introducing voltage squared error as droop input, the feasible region of k can be increased. Meanwhile, voltage regulation performance and load sharing accuracy can be improved.

3) Influence of Resistance Mismatches: It can be inferred from 2) that the cable resistance mismatches between three modules will reduce the load sharing accuracy in the triple-source system. To further observe on the effect of varying cable resistance ratio, triple-source systems with same $V_{\text{bus}} = 260$ V are performed. In addition, it can be seen from (6) and (7) that the ac source resistance also have influence on the steady-state values of dc voltage and current. Figs. 5 and 6 illustrate the current sharing ratio versus the cable resistance mismatch ratio and ac source resistance, respectively. In conclusion, a lighter R_i or R_s mismatch leads to a higher accuracy of current sharing.

III. SYSTEM ARCHITECTURE AND MODELING

In this section, small signal modeling of overall closed-loop system is conducted and the impedance models of the source and load subsystem are established.

It is worth noting that there are two assumptions for modeling. On the one hand, the d-axis is manipulated to regulate active power, while assuming a fixed reactive power component of

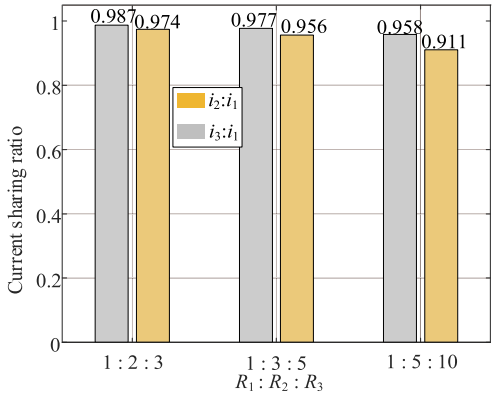

Fig. 5. Current sharing ratio versus the cable resistance mismatch ratio.

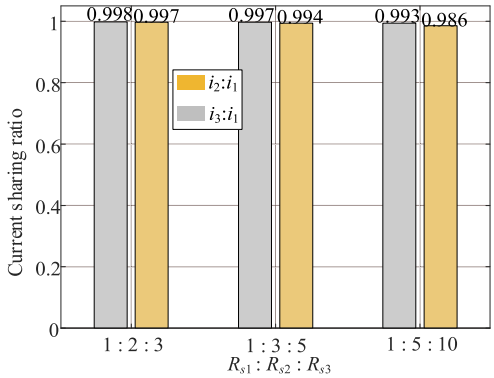

Fig. 6. Current sharing ratio versus the ac source resistance mismatch ratio.

zero. Furthermore, the amplitude of the phase voltage vector is represented by e_d. On the other hand, the internal current loop is approximated as a first-order lag system denoted as $T_{in}(s)$, featuring a corner frequency denoted as ω_{c}.

A. Dynamic Modeling

1) Inner Current Loop: Fig. 2 shows the control block diagram of the inner current loop when classical vector control is implemented. The output of the inner PI (u_d and u_q) can be expressed as

$$\begin{cases} u_d = -v_d + \omega_e L_s i_q + e_d \\ u_q = -v_q - \omega_e L_s i_d + e_q. \end{cases} \tag{13}$$

The output voltage of the dq-axis can be written as

$$\begin{cases} v_d = -(R_s + L_s s) i_d + \omega_e L_s i_q + e_d \\ v_q = -(R_s + L_s s) i_q - \omega_e L_s i_d + e_q \end{cases} \tag{14}$$

where R_s and L_s are the respective ac side resistance and inductance; ω_e is the electrical frequency of the ac source in rad/s; e_d and e_q are PCC voltage in d-axis and q-axis, respectively. In this article, the d-axis is used to regulate the active power. Thus, e_q is controlled to be zero and e_d is the magnitude of the phase voltage vector. And the reactive component is controlled to zero, i.e., $i_q = 0$. From (13) and (14), the expression of the decoupled

component can be derived

$$\frac{i_d(s)}{u_d(s)} = \frac{1}{L_s s + R_s}. \tag{15}$$

For the simplicity of controller design, the inner current loop can be approximated as a first-order lag system $T_{\text{in}}(s)$ with a corner frequency ω_c

$$T_{\text{in}}(s) = \frac{1}{1+\tau s} = \frac{1}{1+\frac{s}{\omega_c}}. \tag{16}$$

In Fig. 2, $T_{\text{in}}(s)$ can be rewritten as

$$T_{\text{in}}(s) = \frac{i_d(s)}{i_d^*(s)} = \frac{G_c(s)}{G_c(s) + L_s s + R_s} \tag{17}$$

where $G_c(s)$ is the PI transfer function of inner loop and $G_c(s) = k_{p,\text{in}} + k_{i,\text{in}}/s$. Given the control bandwidth of the inner current loop, ω_c, the proportional and integral gain of the PI can be derived, respectively, as follows:

$$k_{p,\text{in}} = \omega_c L_s, k_{i,\text{in}} = \omega_c R_s. \tag{18}$$

2) Outer Voltage Loop: According to (14), the linearized d-axis voltage Δv_d is expressed as

$$\Delta v_d \approx -(R_s + L_s s)\Delta i_d. \tag{19}$$

Based on the amplitude invariant transformation, the active power can be linearized at operating point (the voltage and current at the operating point are represented with subscript "0")

$$\begin{aligned} P &= \frac{3}{2}(v_d i_d + v_q i_q) = v_{\text{dc}} \cdot i_{\text{dc}} \\ \Rightarrow \Delta P &= \frac{3}{2}\left[(v_{d0} - R_s i_{d0}) - L_s i_{d0} s\right]\Delta i_d = v_{\text{dc0}} \cdot \Delta i_{\text{dc}}. \end{aligned} \tag{20}$$

By combing (17) and (20), the transfer function from d-axis current to converter output current in small signal can be derived

$$G_{vo}(s) = \frac{\Delta i_{\text{dc}}}{\Delta i_d^*} = \frac{3\left[(v_{d0} - R_s i_{d0}) - L_s i_{d0} s\right]}{2v_{\text{dc0}}(\tau s + 1)}. \tag{21}$$

At the output of the converter, the relationship between dc voltage and current

$$\begin{cases} \Delta i_o = -\frac{P_L}{v_{\text{dc0}}^2}\Delta v_{\text{dc}} \\ \Delta i_{dc} - \Delta i_o = Cs \cdot \Delta v_{\text{dc}} \end{cases} \Rightarrow \frac{\Delta v_{\text{dc}}}{\Delta i_{\text{dc}}} = \frac{1}{Cs - \frac{P_L}{v_{\text{dc0}}^2}}. \tag{22}$$

As for droop characteristic, the linearized model is

$$I_d^* = \frac{V_0^2 - \Delta v_{\text{dc}}^2}{k} \Rightarrow \Delta i_d^* = \frac{2(V_0 \Delta V_0 - v_{\text{dc0}}\Delta v_{\text{dc}})}{k}. \tag{23}$$

Fig. 7 shows the linearized control block diagram of the entire system. Taking the droop control into account, the corresponding voltage closed-loop transfer function is expressed as

$$T_{\text{closed}} = \frac{\Delta v_{\text{dc}}}{\Delta V_0} = \frac{2G_{vo}(s)}{2v_{\text{dc0}}G_{vo}(s) + k\left(Cs - \frac{P_L}{v_{\text{dc0}}^2}\right)} \cdot V_0. \tag{24}$$

Fig. 8 shows the closed-loop models of four droop strategies and Fig. 9 shows the corresponding dynamic performance analysis using Bode plots. The results indicate that the proposed

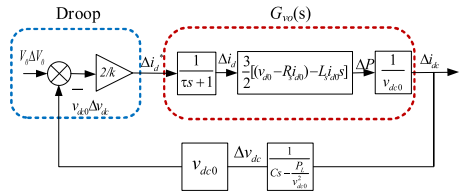

Fig. 7. Linearized control block diagram for the i_d–$v_{\text{dc}}{}^2$ droop-controlled system.

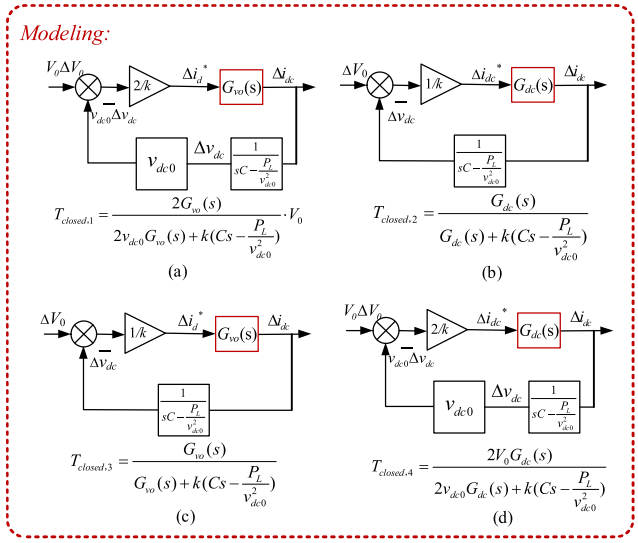

Fig. 8. Closed-loop model for four strategies. (a) i_d–$v_{dc}{}^2$ strategy. (b) i_{dc}–v_{dc} strategy. (c) i_d–v_{dc} strategy. (d) i_{dc}–$v$dc^2 strategy.

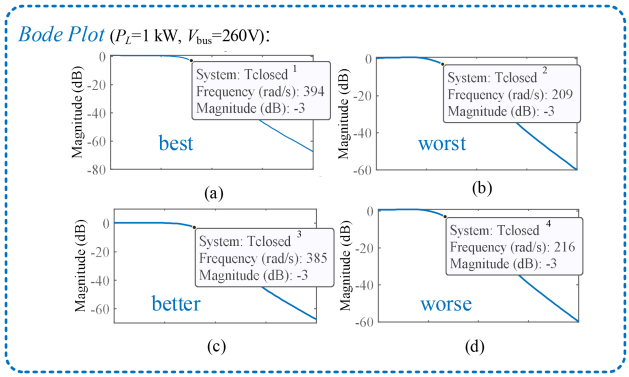

Fig. 9. Bode plot of closed-loop transfer function for four strategies based on the system parameter in Table II. (a) i_d–$v_{dc}{}^2$ strategy ($k = 730.3$). (b) i_{dc}–v_{dc} strategy ($k = 2.4$). (c) i_d–v_{dc} strategy ($k = 1.376$). (d) i_{dc}–$v_{dc}{}^2$ strategy ($k = 1273.85$).

strategy exhibits the fastest dynamic response, whereas the strategies that eliminate the external current loop (i_d–v_{dc} and i_d–$v_{\text{dc}}{}^2$ droop strategy) yield faster voltage dynamics.

B. Impedance Modeling of Subsystems

Impedance analysis has been widely used to address small signal stability issues, by dividing the system into subsystems and evaluating the minor loop gain using the Nyquist stability criterion.

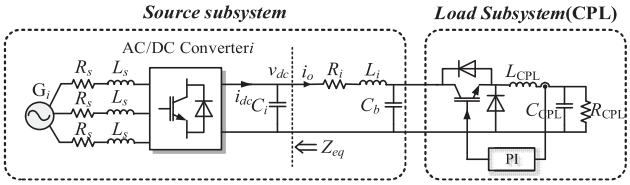

Fig. 10. Source and load subsystems of the single-source single-load system.

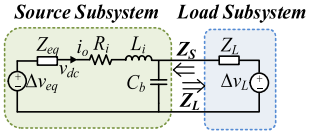

Fig. 11. Equivalent circuit of the single-source single-load system.

In the case of the single-source single-load system discussed in this article, the ac–dc converter, line impedance, and bus capacitance comprise the source subsystem, while CPL forms the load subsystem, as depicted in Fig. 10.

The following mathematical representations of the VSC can also be obtained from Fig. 7:

$$\Delta v_{\rm dc} = \frac{2V_0 G_{vo}(s)}{kCs + 2v_{\rm dc0}G_{vo}(s)}\Delta V_0 - \frac{k}{kCs + 2v_{\rm dc0}G_{vo}(s)} \triangleq \Delta V_{eq} - Z_{eq}\Delta i_o \tag{25}$$

where ΔV_{eq} is defined as equivalent voltage source and Z_{eq} is equivalent impedance. The source impedance can be derived on the basis of (25)

$$\begin{aligned} Z_S(s) &= \frac{1}{C_b s}//(R_i + L_i s + Z_{eq}) \\ &= [k(L_i C_i s^2 + R_i C_i s + 1) + 2v_{\rm dc0}G_{vo}(L_i s + R_i)]/ \\ &\quad [ks(L_i C_i C_b s^2 + R_i C_i C_b s + C_i + C_b) \\ &\quad + 2v_{\rm dc0}G_{vo}(L_i C_b s^2 + R_i C_b s + 1). \end{aligned} \tag{26}$$

Fig. 11 shows the equivalent circuit of the cascaded source and load subsystem. A tightly regulated buck converter is modeled as a CPL, and its input impedance model can be derived [42] as

$$\begin{cases} \Delta = L_{\rm CPL}C_{\rm CPL}s^2 + \frac{L_{\rm CPL}}{R_{\rm CPL}}s + 1 \\ Z_L(s) = \frac{V_{\rm bus}^2(s+\omega_L)\Delta}{P_L(R_{\rm CPL}C_{\rm CPL}s^2 + s - \omega_L\Delta)} \end{cases} \tag{27}$$

where $R_{\rm CPL}$, $C_{\rm CPL}$, and $L_{\rm CPL}$ are corresponding resistance, capacitance, and inductance, respectively; ω_L represents the control bandwidth of the CPL.

IV. Stability Analysis of Single-Source Single-Load System

Most impedance ratio-based criterion, such as Middlebrook et al., require that each subsystem is individually stable. Three steps of stability analysis are involved: the identification of open-loop RHP poles number; the identification of crossing number; effect of parameters. The Nyquist criterion of Bode plot of individual impedances is first introduced to establish a theoretical foundation for steps 1 and 2. The stability of an example is then evaluated according to the above criteria. In order to test the effectiveness of the proposed droop controller under a wider range of system conditions, a parametric analysis is performed in Section IV-B.

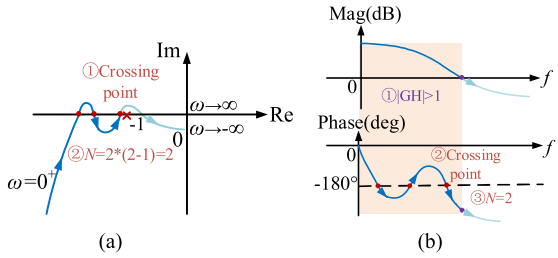

Fig. 12. Determination of N. (a) Nyquist curve of open-loop transfer function. (b) Bode plot of open-loop transfer function.

A. Stability Analysis With Open-Loop RHP Poles

1) Nyquist Criterion of Bode Plot: According to the well-known Cauchy's argument principle

$$Z = N + P \tag{28}$$

where Z is the number of RHP poles (RHPP) of the closed-loop system; N is the number of times that the Nyquist curve of open-loop transfer function clockwise encloses $(-1, j0)$; P is the number of open-loop RHPPs.

The Nyquist stability criterion states that the system is stable if $Z = 0$. The pole-zero map of impedance ratio can determine the value of P. Meanwhile, N can also be counted from the Bode plot, as shown in Fig. 12 [43], [44]. For the Nyquist curve, a positive crossing is defined as one bottom-up crossing through the left negative real axis of $(-1, j0)$, while the reverse is called a negative crossing. In the Bode plot, a positive crossing is the region where the magnitude is greater than 0 dB, and the phase crosses the $(2n + 1)180°$ (n is an integer) line once from above. A negative crossing occurs when it does not meet the above conditions. The formula for N is

$$N = 2(N_+ - N_-) \tag{29}$$

where N_+ represents the number of positive crossings; N_- represents the number of negative crossings. Noted that the above results only include the part of $\omega = 0 \to \infty$, while the Nyquist curve is symmetric about the real axis. Therefore, N is twice the number of crossings counted in the Bode plot.

2) Determination of P and N: For analytical convenience, the above criterion can be applied to the individual impedance Bode plot of subsystems. An example is implemented to demonstrate the detailed stability determination process, where inner loop bandwidth ω_c is 5 Hz, droop gain k is 500, and the other system parameters are referred to Table II. The process can be divided into four steps as follows.

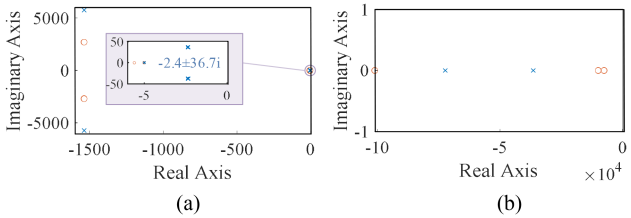

Fig. 13. Pole-zero maps of Z_S and Z_L. (a) Pole-zero map of Z_S. (b) Pole-zero map of Z_L.

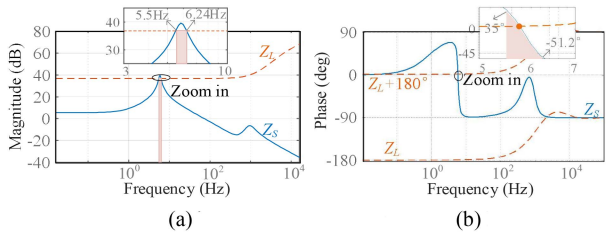

Fig. 14. Bode plot of Z_S and Z_L. (a) Magnitude-frequency response. (b) Phase-frequency response.

Step 1: Formulation of the minor loop gain.

Separate source and load subsystems as Fig. 8, and impedance modeling is conducted, respectively, as (26) and (27).

Step 2: Identification of open-loop RHPPs.

Draw the pole-zero map of Z_S and Z_L, and calculate the number of open-loop RHPPs by

$$P\left(\frac{Z_S}{Z_L}\right) = P(Z_S) + Z(Z_L) \tag{30}$$

where $P(Z_S)$ is the number of RHPPs of source impedance; $Z(Z_L)$ is the number of RHPZs of load impedance, which can be counted by the pole-zero map. It can be seen from Fig. 13 that $P = 0 + 0 = 0$.

Step 3: Identification of crossings.

First, the region where the magnitude of impedance ratio is greater than 1 can be reformulated as the magnitude of Z_S being greater than Z_L. Thus, only the part of Z_S higher than Z_L in magnitude-frequency response needs to be concerned, as shown in the pink shaded area of Fig. 14. Second, crossing boundary is defined by shifting the load impedance-phase curve of $(2n+1)180°$ (n is an integer) in order to help identify the number of crossings. When $\varphi(Z_S)$ crosses the $\varphi(Z_L) + (2n + 1)180°$ line once from above in the pink shaded area, which means that the phase difference of the two impedances crosses over $(2n + 1)180°$ once from the above where the magnitude-frequency response is greater than 0 dB, there will be a positive crossing, as denoted as the orange dot; otherwise, it is negative crossing once. Similarly, N is twice the number of crossings counted in the impedance Bode plots. It can be observed from Fig. 14 that $N = 2(1 - 0) = 2$.

Step 4: Stability prediction.

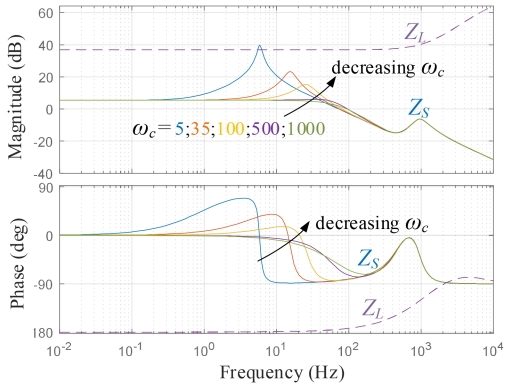

Fig. 15. Influence of inner current loop bandwidth on the source impedance.

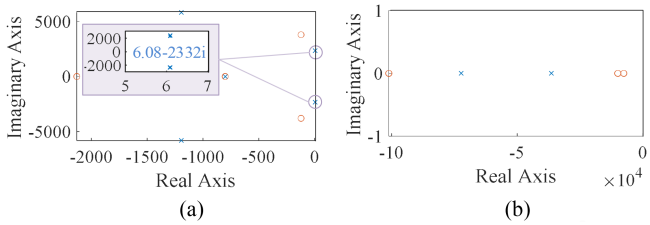

Fig. 16. Pole-zero maps when $k = 20$. (a) Pole-zero map of Z_S. (b) Pole-zero map of Z_L.

Z is determined according to (28) to assess the system stability. It can be seen from steps 1 and 2 that $Z = N + P = 2$, indicating that the system is unstable. The Nyquist stability criterion applied to impedances Bode plots reveals the interactions between source/load impedances graphically, and offers the insight of reshaping the impedances of subsystems to stabilize the system. In this case, there is no open-loop RHP pole. Make N = -P = 0, if Z_S remains, Z_L is reshaped that the impedance-phase curve after raising $+180°$ will not cross the impedance-phase curve of Z_S, or it will cross the impedance-phase curve of Z_S negatively once to compensate an existing positive crossing.

B. Sensitivity Analysis

1) Influence of Inner Loop Bandwidth: Following the above process in Section IV-A, the pole-zero maps when ω_c varies reveals that the individual stability remains intact with P always being 0. The influence of inner current loop bandwidth on the source impedance is investigated in Fig. 15. It can be found that the intersection of the magnitude-frequency responses occurs when slow ω_c (about 5 Hz) is applied, posing a challenge to the system stability. As a short summary here, increasing inner current bandwidth can diminish the peak magnitude and enlarge the stability margin, thereby rendering no upper limit for ω_c.

2) Influence of Droop Gain: In contrast to the case when varying ω_c, two RHPPs appear in Z_S when k is small (about less than or equal to 20), in other words, two open-loop RHPPs are introduced ($P = 2$). The pole-zero maps when $k = 20$ is shown in Fig. 16, while Fig. 17 displays the Bode plot of source and load impedance with different droop gains. No intersection

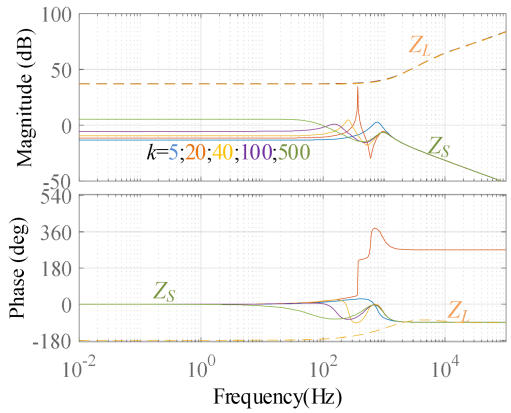

Fig. 17. Bode plot of source and load impedance with different droop gains.

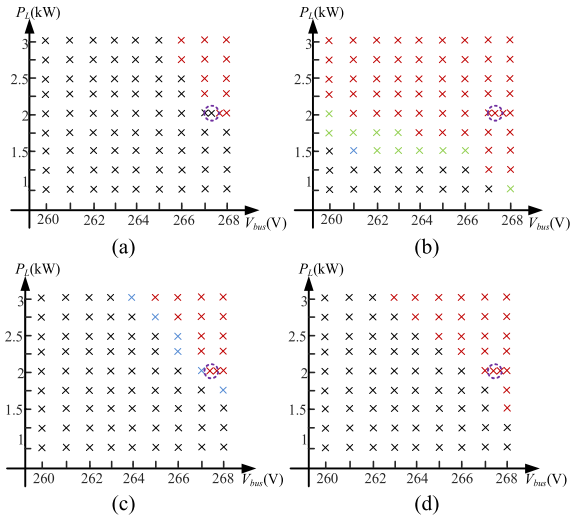

Fig. 18. Parameter map for stability of (a) proposed i_d-$v_{\rm dc}{}^2$strategy (best). (b) $i_{\rm dc}$-$v_{\rm dc}$ strategy (worst). (c) i_d-$v_{\rm dc}$ strategy (better). (d) $i_{\rm dc}$-$v_{\rm dc}{}^2$strategy (worse).

occurs when $k \leq 20$, leading to $N = 0$, and consequently, $Z = N + P = 2$. Hence, reducing the droop gain may cause individual instability of the source subsystem and consequent whole system instability. However, increasing droop gain can attenuate the peak magnitude and enlarge the stability margin.

Therefore, the stability margins under the four droop strategies are compared while maintaining the same load and bus voltage, as shown in Fig. 18. The black points indicate that the system is stable, blue points represent the oscillation of the waveform that eventually become stable (tend to be stable), green points indicate constant amplitude oscillations, and red points denote system instability. It can be inferred that removing the extra outer dc current loop not only improves dynamic performance but also enhances stability margin. Moreover, the proposed strategy reduces the likelihood of imminent system instability compared with i_d-$v_{\rm dc}$ strategy, as shown in the purple dashed circle.

3) Poles Placement: It is found that $Z = N + P = 2$ when $k \leq 20$, showing that two RHPPs exist in the source subsystem

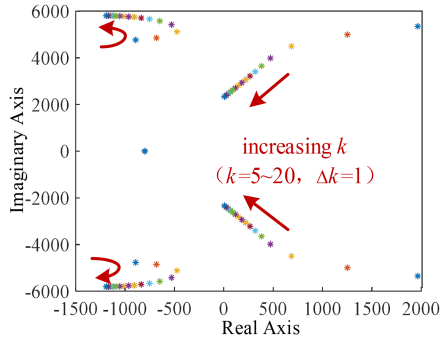

Fig. 19. Pole plot of source impedances by varying k.

TABLE IV
CURRENT SHARING RATIO

Category	Case 1	Case 2	Case 3	Case 4
k_1: k_2: k_3	1:2:1	1:3:1	1:4:1	1:5:1
V_{dc1} V_{dc2} V_{dc3}	260.194 V 260.381 V 260.194 V	260.157 V 260.456 V 260.157 V	260.132 V 260.506 V 260.132 V	260.114 V 260.542 V 260.114 V
i_1: i_2: i_3	1:0.508:1	1:0.344:1	1:0.261:1	1:0.210:1
$q_1 = q_3$ q_2	1.737 1.736	1.736 1.740	1.735 1.741	1.735 1.741
error	1.6 %	3.3 %	4.4 %	5 %

and system is unstable. Fig. 19 shows the pole plot of source impedances when k changes from 5 to 20, revealing that the same cluster of poles are initially in RHP and move to the left half plane as k increases. Therefore, it is necessary to place this same pair of complex poles to enhance the stability of the source subsystem.

V. ANALYSIS OF MULTISOURCE SYSTEM

In a multisource system, current sharing among sources is of importance. Initially, we simplify and approximate the current sharing ratio in a multisource system under i_d-$v_{\rm dc}{}^2$ droop control as the ratio of the inverse of the droop gain. This approximation is verified in a triple-source system. Subsequently, an adaptive current sharing strategy is proposed to improve the current sharing accuracy.

A. Current Sharing Accuracy

Let q_i be the ratio of the d-axis current to the dc output current of the ith source, which can be approximated as a constant (i.e., $I_{di} \approx q_i I_i \approx q I_i$). Meanwhile, $V_{{\rm dc}i} \approx V_{\rm bus}$ is assumed by neglecting the voltage drop on line resistance. The relationship between the current sharing ratio and droop gains is defined as

$$I_1 : I_2 : .. : I_n \approx I_{d1} : I_{d2} : \ldots : I_{dn} \approx \frac{1}{k_1} : \frac{1}{k_1} : \ldots : \frac{1}{k_n}. \tag{31}$$

Four cases (cases 1–4) with varying droop gain ratios are defined and Table IV presents the results of voltage, current sharing ratio q_i, and the current sharing error under the parallel operation of three sources with $P_L = 1$ kW and $V_{\rm bus} = 260$ V.

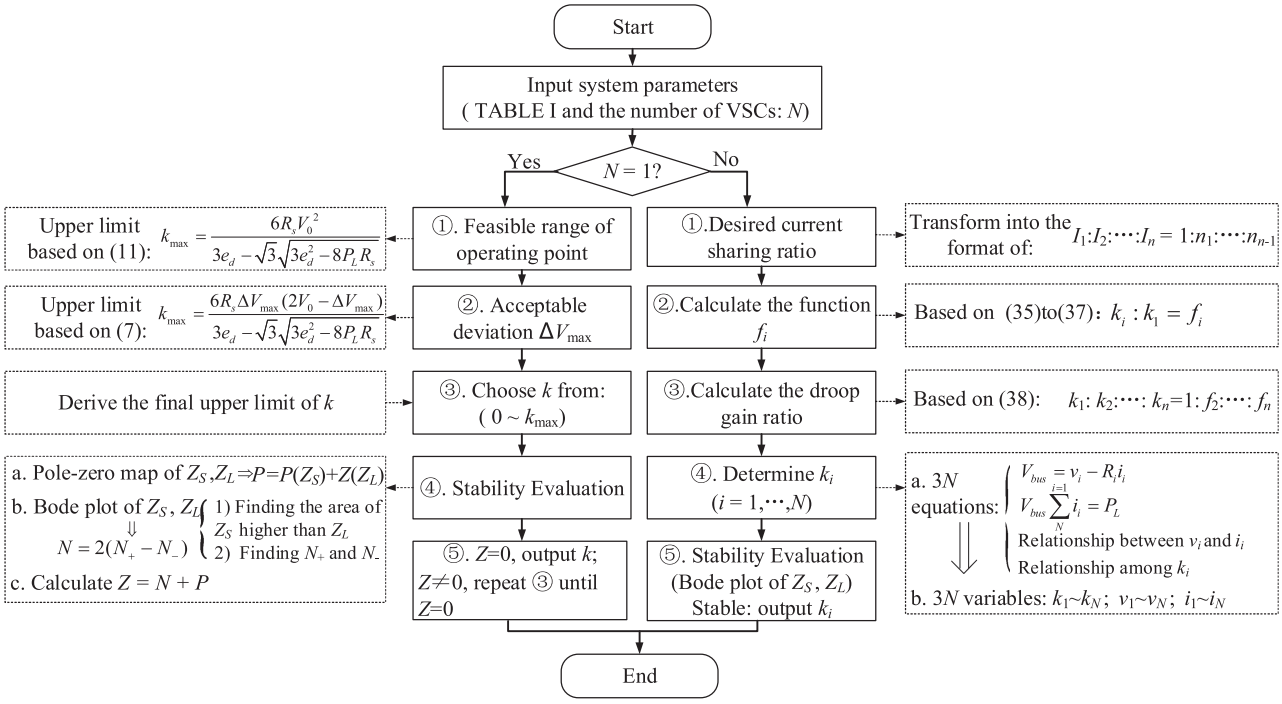

Fig. 20. Proposed current sharing strategy with the droop gain design.

TABLE V
ADAPTIVE CURRENT SHARING RATIO

Category	Case 1	Case 2	Case 3	Case 4
desired i_1: i_2: i_3	1:0.500:1	1:0.333:1	1:0.250:1	1:0.200:1
modified k_1: k_2: k_3	1:2.032:1	1:3.073:1	1:4.108:1	1:5.148:1

These results are consistent with the simplified analysis of (31), and it can be seen that as the droop gain k of second VSC increases, the current sharing error increases.

B. Adaptive Current Sharing

In order to improve the accuracy of current sharing, an adaptive current sharing strategy is proposed here. First, we assume that the desired current sharing ratio is

$$I_1 : I_2 : \ldots : I_i : \ldots : I_n = 1 : n_1 : \ldots : n_{i-1} : \ldots : n_{n-1}. \tag{32}$$

From (5) and (32), the output current of the 1st and ith VSC can be expressed as

$$\begin{cases} I_1 = \frac{P_L}{(1+n_1+\ldots+n_{i-1}+\ldots+n_{n-1})V_b} = \frac{P_L}{mV_b} \\ I_i = \frac{3}{2}\frac{(V_0^2-V_b^2)[k_i e_d - R_s(V_0^2-V_b^2)]}{kV_{\mathrm{dc}i}} = n_{i-1}I_1 = \frac{P_L n_{i-1}}{mV_b}. \end{cases} \tag{33}$$

Considering $V_{\mathrm{dc}i} = V_b + I_i R$, and neglecting the smaller term $I_i^2 R_i^2$, the relationship between k_i and I_i can be derived approximately as

$$k_i = \frac{3}{4}\frac{pe_d + q \cdot I_i + \sqrt{x}(2R_i V_b \cdot I_i - p)}{R_i I_i^2 + V_b I_i} \tag{34}$$

where p, q, x is defined as

$$p = V_0^2 - V_b^2, q = -2R_i V_b e_d, x = e_d^2 - 4R_s. \tag{35}$$

Consequently, the ratio between k_i and k_1 can be written as

$$k_i : k_1 = f_i = \frac{\left(wn_{i-1} + \frac{umV_b}{P_L}\right)\left(\frac{R_i P_L}{mV_b} + V_b\right)}{\left(w + \frac{umV_b}{P_L}\right)\left(\frac{R_i P_L n_{i-1}^2}{mV_b} + V_b n_{i-1}\right)} \tag{36}$$

where w, u is defined as

$$w = q + 2\sqrt{x}R_i V_b, u = pe_d - \sqrt{x}p. \tag{37}$$

Finally, the precise current sharing can be achieved through the adaptive droop gain ratio

$$k_1 : k_2 : \ldots : k_i : \ldots : k_n = 1 : f_2 : \ldots : f_i : \ldots : f_n \tag{38}$$

where f_i is a function related to the CPL power, the bus voltage, desired current sharing ratio, and the line resistance.

By applying this adaptive adjustment process, precise current sharing can be achieved. Table V presents the modified droop gain ratio, which can be determined according to (36) and (38).

Furthermore, Fig. 20 illustrates a comprehensive procedure of droop gain design. For single-source single-load operation, the droop gain is designed according to existing operating conditions and acceptable voltage deviation. The droop gain ratio of the multisource operation is determined by the desired current sharing ratio. And the final step involves conducting a stability assessment.

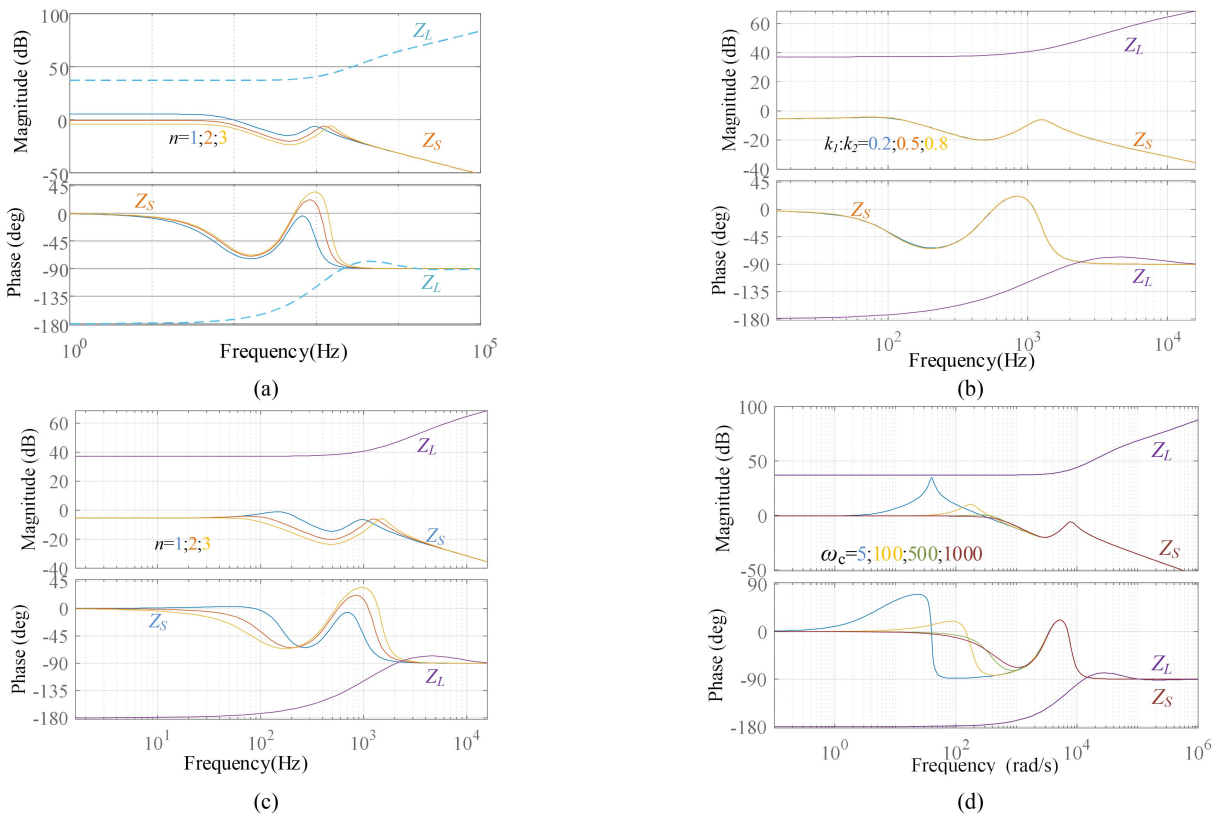

Fig. 21. Bode plot of source impedance in multisource operation. (a) Varying the number of VSCs keeping individual droop gain. (b) Varying load sharing ratio keeping steady-state performance. (c) Varying the number of VSCs keeping steady-state performance. (d) Varying inner loop bandwidth in dual-source system.

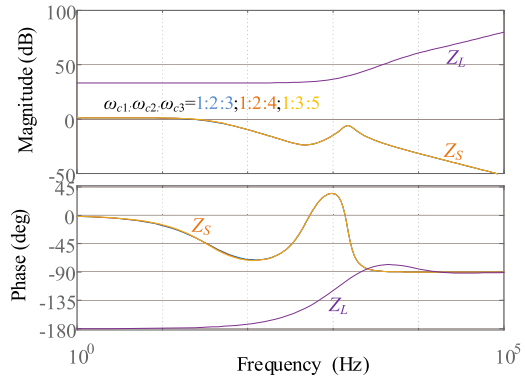

Fig. 22. Bode plot of source impedance in triple-source operation varying inner loop bandwidth ratio.

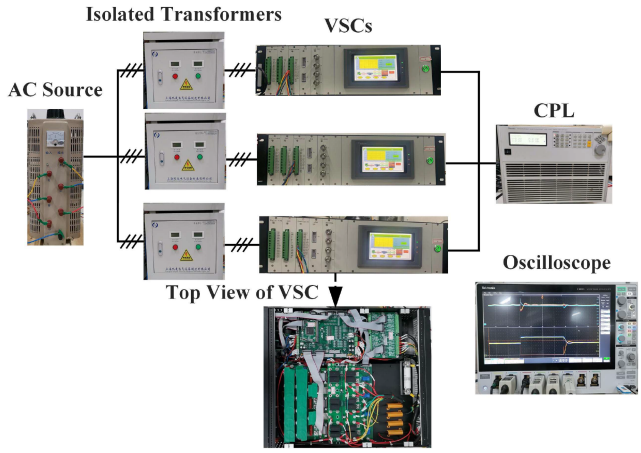

Fig. 23. Experimental platform.

C. Stability Analysis

1) Influence of k and ω_c: According to (26), the total impedance model of source side of n VSCs operating in parallel can be derived as follows:

$$Z_S(s) = \frac{1}{sC_b + \sum_{i=1}^{n} \frac{1}{R_i + sL_i + Z_{eq,i}}}. \tag{39}$$

Fig. 21 presents four cases set to comprehensively compare the effects of each parameter on the stability of the multisource system with i_d-$v_{dc}{}^2$ droop controller, and each case illustrates the stability performance when the parameter varies. Fig. 21(a) demonstrates the stability of single-source, dual-source, and triple-source systems, respectively, when the individual droop gain is the same ($k_i = 500$), and the load is equally shared. It is observed that with same k_i, the amplitude-frequency curve of Z_S moves down as the number of VSCs increases, and the stability margin increases. Fig. 21(b) examines the influence of load sharing ratio of dual-source system controlled by tuning droop gain ratio. Both of the CPL power and bus voltage are

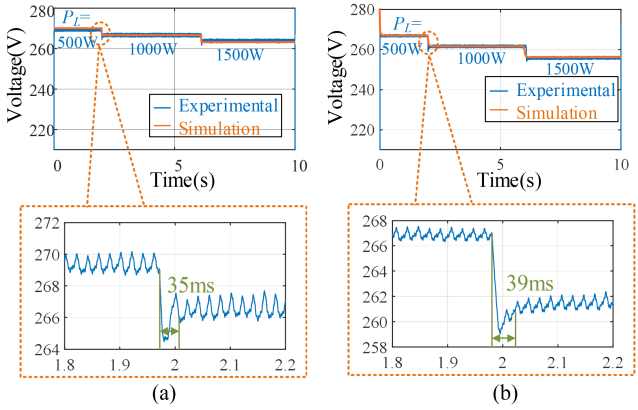

Fig. 24. Experimental and simulation results of bus voltage with different droop gains. (a) $k = 500$. (b) $k = 1000$.

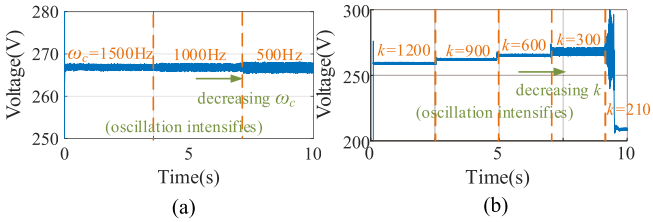

Fig. 25. Experimental results of bus voltage with different parameters. (a) Decreasing ω_c. (b) Decreasing k.

kept consistent, and k_1:k_2 is 0.2, 0.5, and 0.8, respectively. The amplitude-frequency curves of the three Z_S almost overlap, indicating that the load sharing ratio has no significant effect on the system stability. Fig. 21(c) explores the influence of the number of sources while maintaining bus voltage. It is found that the amplitude-frequency curve of Z_S moves down, and the stability margin increases with an increase in the number of VSCs. Furthermore, the influence of inner loop bandwidth on the dual-source system is shown in Fig. 21(d). Compared with Fig. 15, there is minimal difference in stability performance when the inner loop bandwidth is above 100 Hz, and the source and load impedance curve does not intersect at 5 Hz. Therefore, the dual-source system has a larger stability margin than a single-source system under the variation of the control bandwidth. In conclusion, as depicted in Fig. 21(a), (b), and (d), it can be inferred that a multisource system exhibits greater stability compared to a single-source system under i_d-v_{dc}^2 droop strategy.

2) Influence of Parameter Mismatches: Fig. 21(b) shows that the droop gain mismatch has no effect on dual-source system stability. Fig. 22 further illustrates the influence of the inner loop bandwidth mismatch for triple-source system when the individual droop gain is the same ($k_i = 500$). It is investigated that varying ω_c ratio will not sacrifice stability.

VI. Experimental Verification

This section presents the experimental results to verify the feasibility of the proposed droop strategy. An experimental prototype of dc MG is constructed, as depicted in Fig. 23. The experimental system parameters are listed in Table II.

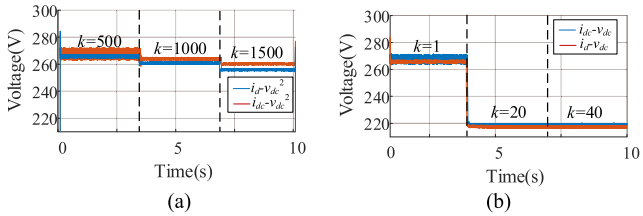

Fig. 26. Experimental results voltage regulation performance under four strategies. (a) i_d-v_{dc}^2 and i_{dc}-v_{dc}^2 droop. (b) i_d-v_{dc} and i_{dc}-v_{dc} droop.

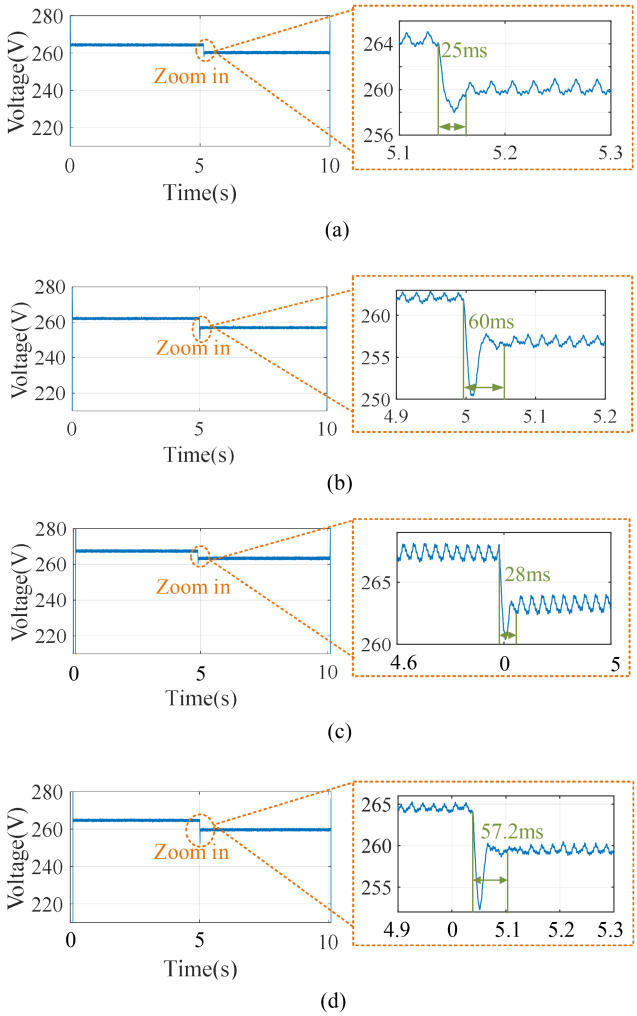

Fig. 27. Experimental results of bus voltage dynamics with different droop strategies. (a) i_d-v_{dc}^2 droop. (b) i_{dc}-v_{dc} droop. (c) i_d-v_{dc} droop. (d) i_{dc}-v_{dc}^2 droop.

A. Steady-State Performance

First, a single-source single-load MG is tested. With the proposed i_d-v_{dc}^2 droop characteristic, bus voltages with droop gains of 500 and 1000 are depicted in Fig. 24(a) and (b), respectively, while the load power is increased stepwise from 500 W to 1.5 kW.

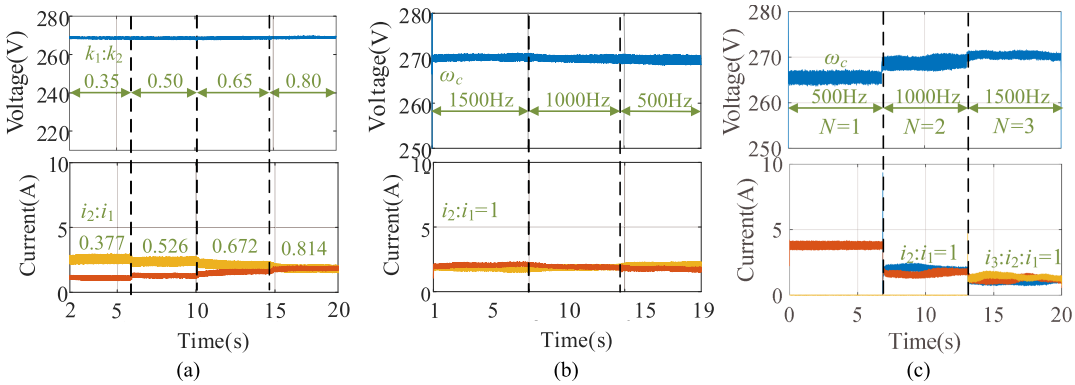

Fig. 28. Effect of load sharing ratio and inner loop bandwidth. (a) Effect of load sharing ratio with the same steady-state performance when $P_L = 1$ kW on the dual-source operation. (b) Effect of inner loop bandwidth with the same steady-state performance $P_L = 1$ kW and $k_1 = k_2 = 500$ on the dual-source operation. (c) Effect of cutting into sources with larger bandwidth and same droop gain $k_1 = k_2 = k_3 = 500$.

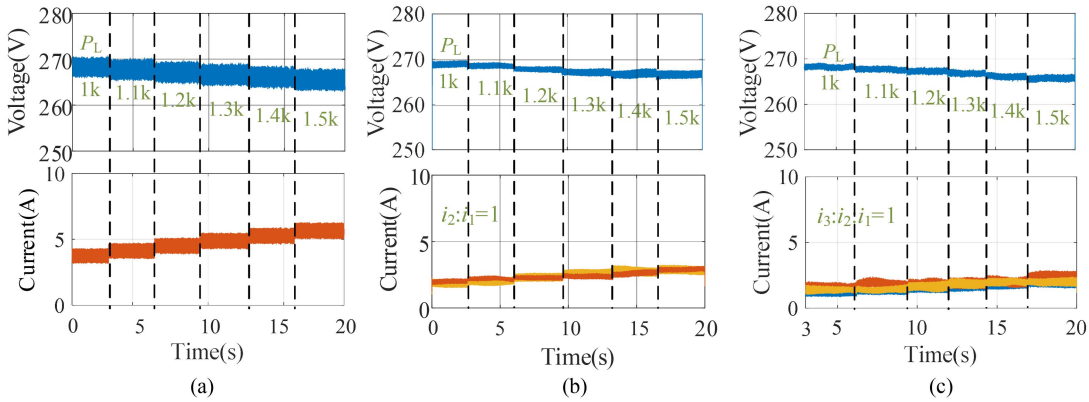

Fig. 29. Effect of the number of VSCs with the same steady-state performance when P_L is changed from 1 kW to 1.5 kW. (a) Single-source single-load operation with $k_1 = 339.05$. (b) Dual-source single-load operation with $k_1 = k_2 = 740.16$. (c) Triple-source single-load operation with $k_1 = k_2 = k_3 = 1141.36$.

The steady-state results are consistent with the simulation and theoretical analysis in Section II-B. It is seen that the voltage deviation is reduced with a smaller droop gain, and the voltage deviation is not significant with a larger droop gain, demonstrating the superior voltage regulation performance of the proposed strategy.

B. Influence of Inner Loop Bandwidth and Droop Gain

Fig. 25(a) illustrates the effect of the varying inner loop bandwidth on bus voltage with $k = 500$, $P_L = 1$ kW. A slower bandwidth ($\omega_c = 500$ Hz) intensifies the voltage ripples, which agrees with the theoretical analysis in Fig. 15. Fig. 25(b) demonstrates the impact of changing droop gain on bus voltage with $\omega_c = 800$, $P_L = 1$ kW. Decreasing the droop gain tends to jeopardize the system stability, which is in agreement with the theoretical analysis results in Fig. 17.

It is noteworthy that the experimental results have revealed the presence of voltage ripple, and Fig. 25(b) shows large voltage fluctuation at $k = 300$. The observed discordance between the theoretical expectations, suggesting system instability when $k \leq 20$, and the experimental findings demands explanation. There may be the following reasons for the inconsistency: simplification in small-signal modeling (e.g., neglecting the dynamic characteristic of CPL, PWM sampling, control signal delay, dead time of the switching transistor, the equivalent series resistance of the inductor, and so on); potential external interference in the experimental environment.

C. Comparison With Other Droop Strategies

1) Steady-State Performance: In order to verify the superiority of the proposed strategy in voltage regulation performance, the comparative experimental results are shown in Fig. 26 .

Fig. 26(a) shows the dc voltage values of i_{dc}-$v_{\mathrm{dc}}{}^2$ method and i_d-$v_{\mathrm{dc}}{}^2$ method under the same droop gain. It can be seen that the former is slightly larger than the latter, and they can both operate under large range of droop gain. The results are consistent with Fig. 4(a) and (d). Fig. 26(b) shows the dc voltage values of the i_{dc}-v_{dc} method and the i_d-v_{dc} method with the same droop gain. It can be observed that the dc voltage maintains the same value at $k = 20$ and 40. This is because the output voltage of the three-phase bridge rectifier has a minimum value, i.e., the average value of the dc voltage under three-phase uncontrolled rectification. This threshold is exceeded under these operating conditions.

2) Dynamic Performance: On the one hand, Fig. 24 displays the dynamic response of simultaneous loading under different droop gains. The response time is about 35 ms when $k = 500$, while it increases to 39 ms when $k = 1000$. Although the difference is small, the smaller droop gain corresponds to a faster dynamic process. On the other hand, to verify the superior dynamic performance of the proposed droop control strategy, the CPL is changed from 1 kW to 1.5 kW at $t = 5$ s. A bus voltage value of 260 V is chosen, and droop gains are set to 730.3 for the i_d-$v_{\rm dc}{}^2$ strategy, 2.4 for the $i_{\rm dc}$-$v_{\rm dc}$ strategy, 1.376 for the i_d-$v_{\rm dc}$ strategy, 1237.85 for the $i_{\rm dc}$-$v_{\rm dc}{}^2$ strategy, respectively. Fig. 27 shows the corresponding transient response times under different droop strategies, respectively, confirming that the system settling time is shortened due to the elimination of external current loop.

D. Multisource Operation

Fig. 28(a) and (b) illustrates the effects of load sharing ratio and inner loop bandwidth on the bus voltage and load currents of mutisource system. Fig. 28(a) demonstrates that the waveform of the bus voltage is relatively constant when the droop gain ratio of the dual source is 0.35, 0.5, 0.65, and 0.8 under the condition of $P_L = 1$ kW and $V_{\rm bus} = 265$ V, indicating that the load ratio has little impact on system stability, and the load current is shared approximately in inverse proportion to the droop gain. In Fig. 28(b), the bus voltage ripple approximately remains unchanged as the inner loop bandwidth changes from 1500 Hz to 1000 and 500 Hz. In contrast, Fig. 25(a) shows that the ripple of a single source is significantly increased with reduced inner loop bandwidth to 500 Hz. These results support the conclusion drawn in Fig. 21(d) that multisource systems have a larger stability margin than single-source systems. Fig. 28(c) further verifies that the system becomes stable when the source subsystem has a larger inner loop bandwidth.

Additionally, the voltage waveforms of single-source, dual-source, and triple-source operations under the same steady-state performance are shown in Fig. 29(a), (b), and (c), respectively. The ripple of multisource system decreases and the oscillation is reduced than single-source system, and the stability of the dual-source and triple-source systems is not much different, consistent with the findings of Fig. 21(c).

VII. Conclusion

This article presents an improved nonlinear droop control strategy, and the main findings of this article can be summarized as follows.

1) The proposed i_d–$v_{\rm dc}{}^2$ droop control strategy improves both steady-state and dynamic performance. It significantly reduces the bus voltage deviation and extends the feasible range of k by introducing the difference between squared nominal voltage and squared dc voltage as droop input. And the strategy simplifies the control structure by eliminating external dc voltage or current loop.
2) The stability assessment that considers the open-loop RHP poles is discussed by performing the extended Nyquist stability criterion. A small droop gain may introduce RHP poles of source impedance.
3) The sensitivity analysis of the influencing parameters is conducted in single-source and multisource system. Increasing the inner current loop bandwidth, droop gain, and the number of VSCs can enlarge the stability margin.
4) The adaptive current sharing strategy enhances current sharing accuracy in multisource systems by introducing a droop gain ratio function.
5) A comprehensive design process of droop gain is discussed by considering equilibrium points, acceptable voltage regulation, and desired current sharing ratio.

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