An FPGA-Based On-the-Fly Reconfigurable Low-Power SHEPWM Inverter With a Compact SiP Implementation

Nueraimaiti Aimaier, *Student Member, IEEE*, Yves Blaquière, *Member, IEEE*, Nicolas G. Constantin, *Senior Member, IEEE*, and Glenn E. R. Cowan, *Member, IEEE*

***Abstract*—This article presents a selective harmonic elimination pulsewidth modulation (PWM) (SHEPWM) full-bridge inverter featuring real-time on-the-fly reconfigurability of output waveform amplitude and frequency using a field-programmable gate array (FPGA). The inverter is integrated on a compact three-dimensional (3-D) system-in-package using low-temperature cofired ceramics as a substrate, reducing the printed circuit board (PCB) area. Validated through simulations and measurements at 0.12 W and 1.2 W peak output power, the inverter cancels harmonics up to the 34th order at switching nodes. With an *LC* filter having a 20 kHz cut-off frequency, total harmonic distortion at the load is below 5.1% for alternating current output signals, varying in modulation index from 0.2 to 0.9 and output frequencies from 5 to 10 kHz. The results also showed that for the same inverter conditions and output THD, the SHEPWM inverter with 0.12 W output power has an average of 17.3% and 4.2% better efficiency than a natural PWM (NPWM) inverter with an output frequency of 4 kHz and 10 kHz, respectively. For the inverter of 1.2 W output power, the SHEPWM inverter maintains better efficiency than the NPWM counterpart, by an average of 2.3% and 6.9%, respectively.**

***Index Terms*—Full bridge, gallium nitride (GaN), harmonic cancelation, inverter, low-power inverter, low-temperature cofired ceramics (LTCC), selective harmonic elimination pulsewidth modulation (SHEPWM), system-in-package (SiP).**

I. Introduction

RECENT advances in power transistors enable smaller and lighter power electronics boards. Among them, gallium nitride (GaN) devices are one of the best candidates for switch-mode operated converters thanks to their capability of fast switching and small size [1], [2], [3], [4], [5], [6]. However, the system volume and bulky power electronic parts need to be replaced by a reconfigurable power electronics unit to further reduce the overall size and distribute the power to different loads operating under different conditions. A heterogeneously integrated system-in-package (SiP) on a low-temperature cofired ceramics (LTCC) substrate is a promising candidate for this purpose since it has a good three-dimensional (3-D) integration density, thermal, and electrical performance [7], [8].

Low-power loads, such as electropneumatic servo valves, hall effect sensors, and low-power actuators, find common usage in a wide range of industries, including aerospace, automotive, industrial automation, and power systems. These applications necessitate precise control, sensing, and measurement of diverse parameters. In such scenarios, the switching losses of power devices in the inverter play a dominant role compared to conduction losses due to their operation at extremely low alternating current (ac) load currents. The operation frequency of these loads is usually in the range of several kHz to 10 kHz. A natural pulsewidth modulated (NPWM) inverter, where a reference sinewave is compared with a carrier signal to generate the pulsewidth modulated (PWM) signal, needs to operate with a high switching frequency to reduce the total harmonic distortion (THD) at the cost of high-switching losses [9]. This reduces the overall efficiency of the converter.

A selective harmonic elimination PWM (SHEPWM) technique can reduce switching losses. SHEPWM predetermines the switching angles of the PWM signal so that lower order harmonics are absent, enabling low THD without necessarily increasing the switching frequency of the power transistors. SHEPWM was first introduced in [10] and [11]. Since then numerous papers have been published on SHEPWM theory, especially on solving the nonlinear transcendental equations to get the optimal switching angles [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. Previous experimental works on the SHEPWM technique were mostly conducted in mid-to-high power and fixed low-frequency applications, and detailed hardware implementations were not given, or were described very briefly. For example, works in [19], [22], [23], [24], [25], [26], [27], [28] focused on 50 Hz fundamental output frequency (f_T) with direct current (dc) supply voltages ranging from 60 to 200 V, and the output frequency in [29] is 60 Hz with the dc supply voltage of 127 V. Cheng et al. [30] presented and analyzed the dynamic response of

Manuscript received 15 November 2023; revised 23 January 2024; accepted 30 January 2024. Date of publication 9 February 2024; date of current version 20 March 2024. This work was supported in part by the Natural Sciences and Engineering Research Council (NSERC) of Canada. Recommended for publication by Associate Editor L. Wang. *(Corresponding author: Nueraimaiti Aimaier.)*

Nueraimaiti Aimaier and Glenn E. R. Cowan are with the Department of Electrical and Computer Engineering, Concordia University, Montréal, QC H3G 1M8, Canada (e-mail: nueraimaiti.aimaier@mail.concordia.ca; gcowan@ece.concordia.ca).

Yves Blaquière and Nicolas G. Constantin are with the Department of Electrical Engineering, École de Technologie Supérieure (ÉTS), Montréal, QC H3C 1K3, Canada (e-mail: Yves.Blaquiere@etsmtl.ca; nicolas.constantin@etsmtl.ca).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3364534.

Digital Object Identifier 10.1109/TPEL.2024.3364534

the SHEPWM technique under a step in the output voltage from 0 to 200 V. Ahmed et al.[31] proposed a method for real-time calculation of switching angles, and presented a cascaded full H-bridge inverter with the step change of modulation index (MI). To the authors' best knowledge, no works have presented the SHEPWM inverter with a variable output frequency, which is required in some applications. The common hardware solution for the SHEPWM technique is using a field programmable gate array (FPGA) or digital signal processor to generate the PWM signals. The aforementioned works have a very limited description of hardware design, making it challenging for the reader to understand and/or replica the hardware implementation. In this study, an FPGA is selected to implement the SHEPWM technique owing to its advantages in mathematical operations optimization, increased interface capability, and higher clock frequency.

This article demonstrates a low-power full-bridge SHEPWM inverter with on-the-fly reconfigurable ac outputs in a compact 3-D SiP, with an emphasis on high-frequency applications to address the shortcomings of the aforementioned works. As no low-power SHEPWM inverter along with its output THD relationship with MI and the fundamental output frequency is reported in the literature, this article investigates these key aspects with a full range of MI and a wider range of output frequencies (several kHz to 10 kHz). Furthermore, a detailed FPGA hardware implementation in MATLAB SIMULINK is described in this article, which is simple and can be replicated easily. The method of FPGA hardware implementation is straightforward and does not require any knowledge of a hardware description language (HDL).

This work is a significant extension of [32], including on-the-fly configuration of both inverter output amplitude and frequency, in-depth treatment of the design and implementation, and experimental validation. The rest of this article is organized as follows. The review of the SHEPWM theory, architecture of SHEPWM hardware, and FPGA simulations are described in detail in Section II. In Section III, the inverter system implementation is described. The inverter simulations, experimental results, and discussions are provided in Section IV. Finally, Section V concludes this article.

II. SHEPWM Theory and Proposed FPGA Architecture

Unlike an NPWM inverter, the SHEPWM's switching angles are precalculated. Lower order harmonics at the switching node can be canceled without necessarily increasing the switching frequency of SHEPWM. A three-level differential SHEPWM signal can be generated at the differential switching nodes ($+V_{SW}-$ in Fig. 1) where PWM1 and PWM2 are driven by two gate drivers (GDs). Lower order harmonics at V_{SW} are canceled, while higher order harmonics are suppressed by an *LC* filter so that a single-tone ac output signal ($+V_{OUT}-$) is delivered to the load.

The architecture of the FPGA for SHEPWM is designed using Xilinx System Generator (SysGen) for digital signal processing, which is fully integrated into MATLAB Simulink. HDL codes are generated automatically using SysGen after validating

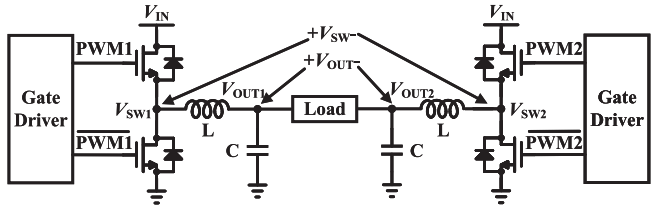


Fig. 1. Schematic of a full-bridge inverter output stage.

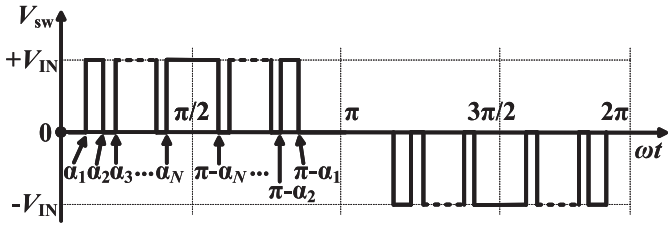


Fig. 2. Three-level odd-symmetrical SHEPWM waveform.

the SHEPWM block's function using Simulink. The proposed method is simple, cost-effective, and has the capability of on-the-fly configuration of both output amplitude and frequency. The detailed hardware implementation along with Simulink simulations are described in detail in this section.

A. Review of SHEPWM Theory

A three-level PWM is depicted in Fig. 2 with N switching angles per quarter cycle. V_{SW} can be represented by a Fourier Series as follows:

$$V_{SW}(\omega t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + \sum_{n=1}^{\infty} b_n \sin(n\omega t) \quad (1)$$

where a_0 is the dc component, n is the harmonic order, ω is the angular frequency in rad/second, t is time, a_n are the coefficients of the cosine terms, and b_n are the coefficients of sine terms. With odd quarter-wave symmetry, the dc component (a_0), cosine coefficients (a_n), and even order sine terms (b_2, b_4,..., b_{2n}) are inherently equal to zero. Thus, (1) can be simplified to

$$V_{SW}(\omega t) = \begin{cases} \sum_{n=1}^{\infty} b_n \sin(n\omega t) & \text{for odd } ns \\ 0 & \text{for even } ns \end{cases} \quad (2)$$

where

$$b_n = \frac{1}{\pi} \int_0^{2\pi} V_{SW}(\omega t) \sin(n\omega t) d(\omega t). \quad (3)$$

If the inverter input voltage is V_{IN}, then b_n can be expressed as

$$b_n = \frac{4V_{IN}}{n\pi} \sum_{k=1}^{N} (-1)^{k+1} \cos(n\alpha_k) \quad (4)$$

where k is an integer number ($1 < k < N$) and a_k is the kth switching angle in Fig. 2. Equation (4) can be expanded to the

TABLE I
INITIAL GUESSED AND CALCULATED OPTIMAL SWITCHING ANGLES IN DEGREES FOR DIFFERENT MIS

MI	$\alpha_1\uparrow^a$	$\alpha_2\downarrow^b$	$\alpha_3\uparrow$	$\alpha_4\downarrow$	$\alpha_5\uparrow$	$\alpha_6\downarrow$	$\alpha_7\uparrow$	$\alpha_8\downarrow$	$\alpha_9\uparrow$	$\alpha_{10}\downarrow$	$\alpha_{11}\uparrow$	$\alpha_{12}\downarrow$	$\alpha_{13}\uparrow$	$\alpha_{14}\downarrow$	$\alpha_{15}\uparrow$	$\alpha_{16}\downarrow$	$\alpha_{17}\uparrow$
	10.03^c	11.00^c	20.00^c	21.94^c	29.97^c	32.83^c	39.94^c	43.60^c	49.90^c	54.26^c	59.87^c	64.74^c	69.84^c	75.06^c	79.81^c	85.14^c	89.67^c
0.2	9.81	10.16	19.63	20.31	29.46	30.46	39.31	40.60	49.19	50.72	59.10	60.83	69.03	70.91	79.00	80.97	89.00
0.3	9.71	10.22	19.43	20.45	29.17	30.66	38.94	40.86	48.75	51.05	58.61	61.21	68.52	71.35	78.48	81.45	88.49
0.4	9.60	10.28	19.21	20.56	28.85	30.83	38.54	41.10	48.29	51.34	58.10	61.57	67.99	71.76	77.95	81.92	87.99
0.5	9.48	10.33	18.97	20.65	28.51	30.98	38.11	41.30	47.79	51.61	57.56	61.90	67.43	72.16	77.40	82.38	87.47
0.6	9.35	10.36	18.73	20.72	28.15	31.09	37.65	41.45	47.25	51.82	56.97	62.19	66.83	72.53	76.82	82.83	86.94
0.7	9.21	10.38	18.46	20.76	27.76	31.15	37.15	41.55	46.66	51.97	56.33	62.41	66.16	72.85	76.19	83.27	86.39
0.8	9.07	10.37	18.16	20.75	27.33	31.15	36.59	41.56	45.99	52.01	55.58	62.52	65.39	73.08	75.47	83.67	85.81
0.9	8.90	10.33	17.83	20.67	26.82	31.03	35.92	41.41	45.17	51.84	54.63	62.36	64.36	73.05	74.49	83.96	85.09

[a] ↑ indicates the rising edge of the switching angle, [b] ↓ indicates the falling edge of the switching angle, [c] Initial guessed switching angles.

following equations:

$$\begin{cases} \cos(\alpha_1) - \cos(\alpha_2) + \cdots \pm \cos(\alpha_N) & = \frac{\pi}{4V_{\text{IN}}} b_1 \\ \cos(3\alpha_1) - \cos(3\alpha_2) + \cdots \pm \cos(3\alpha_N) & = \frac{3\pi}{4V_{\text{IN}}} b_3 \\ \cos(5\alpha_1) - \cos(5\alpha_2) + \cdots \pm \cos(5\alpha_N) & = \frac{5\pi}{4V_{\text{IN}}} b_5 \\ \cdots & \\ \cos(n\alpha_1) - \cos(n\alpha_2) + \cdots \pm \cos(n\alpha_N) & = \frac{n\pi}{4V_{\text{IN}}} b_n \end{cases} \quad (5)$$

which must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \ldots < \alpha_N < \frac{\pi}{2}. \quad (6)$$

To cancel lower odd harmonics, b_3 to b_n in (5) are set to equal to zero. b_1 is the amplitude of the fundamental output signal and b_1/V_{IN} is defined as the MI. To solve for N unknown switching angles, N equations are needed, and $N-1$ odd harmonics can be canceled. More switching angles mean more harmonic cancelation, however, solving the nonlinear transcendental equations becomes more complicated and hardware resources for implementation increase as well. In addition, for small MI PWM signals, the pulses get narrow near 0° and 180°, therefore, a higher FPGA clock frequency (f_{CLK}) is needed for a better timing resolution for the switching angles, especially for an increased number of switching angles.

The example used in this article targets 17 switching angles per quarter-cycle, which eliminates 16 odd harmonics. That means third to 33rd odd harmonics are canceled and even harmonics do not exist in the odd symmetric SHEPWM signal. Therefore, the 35th harmonic is the first tone following the canceled harmonics. The equations are solved in MATLAB by guessing the initial switching angles. The resulting optimal switching angles in degrees for different MI are given in Table I and plotted in Fig. 3. In Table I, the odd index switching angles ($\alpha_1, \alpha_3, ..., \alpha_{17}$) are the rising edges and the even index switching angles (α_2, α_4, ..., α_{16}) are the falling edges of the SHEPWM signal. The second row is the set of initial (guessed) switching angles common for all the modulation indices (MIs). Subsequent rows show the solutions for optimal switching angles for each MI from 0.2 to 0.9. As seen in the table, the solved optimal switching angles for all MI are in the vicinity of initial switching angles.

B. Proposed SHEPWM FPGA Architecture

In this work, the precomputed optimal switching angles are stored in a look-up table (LUT), implemented using a block random access memory (BRAM) in the FPGA. To avoid reprogramming the FPGA when generating different ac output signals at the load, the switching angles (first half period) of different amplitude and frequency output signals can be stored in the LUT so that configuring outputs on-the-fly is achieved by simply sending a command signal to the FPGA.

A counter-based methodology is used to generate the pulses according to the computed switching angles, as shown in Fig. 4. In this work, 17 ($N = 17$) optimal switching angles per quarter-cycle are used. When the counter (ramp signal in Fig. 4) equals each switching angle (horizontal line), PWM signals change

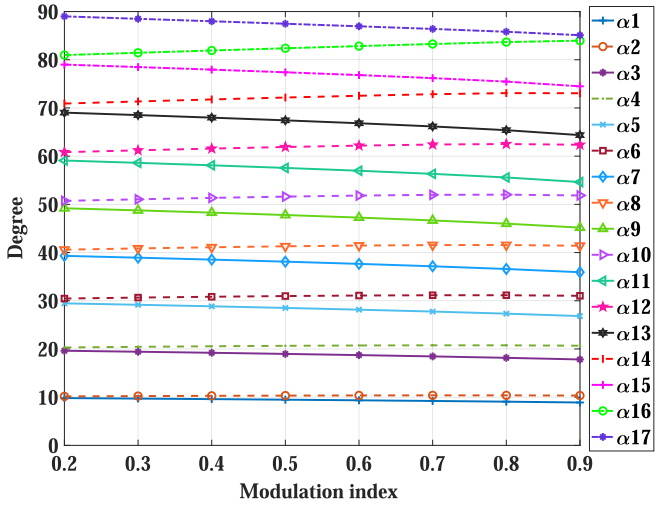


Fig. 3. 17 optimal switching angles per quarter-cycle for different MIs.

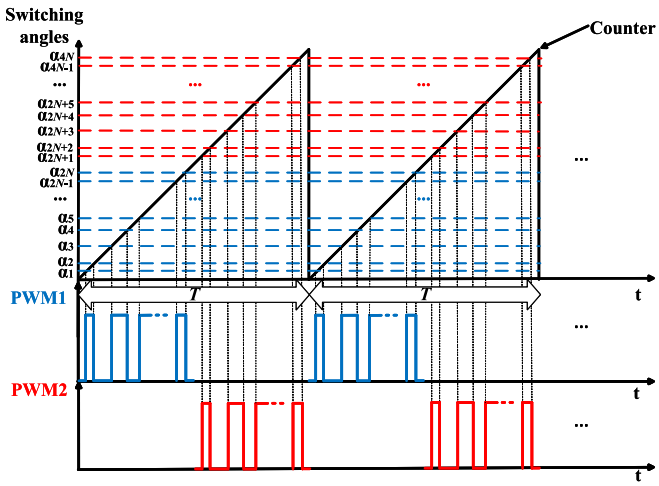


Fig. 4. Generating the SHEPWM pulses using a counter-based methodology.

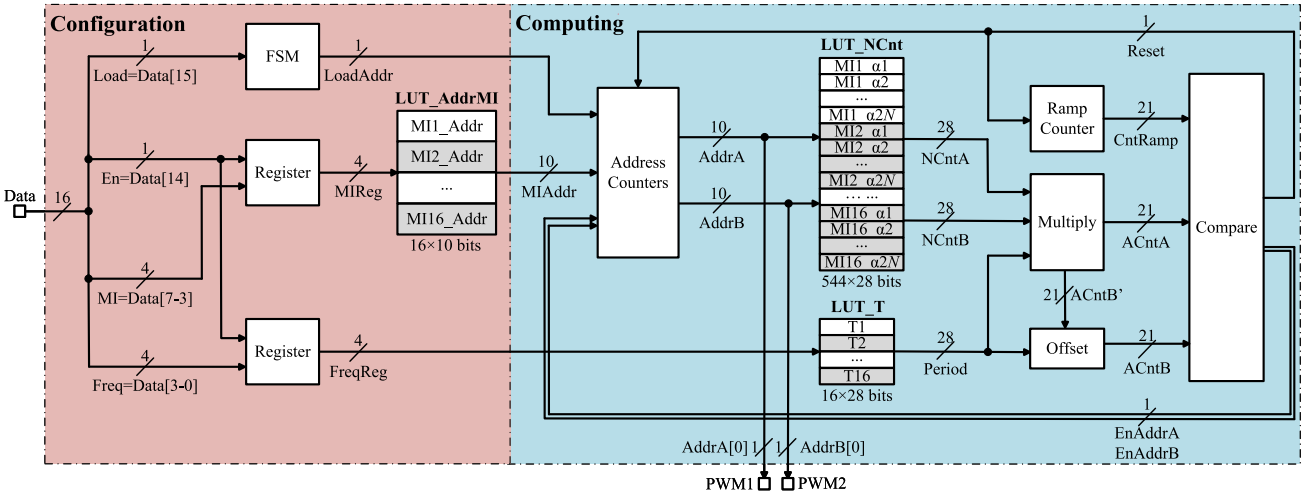


Fig. 5. SHEPWM architecture on the FPGA with $M = 16$ MIs and $N_{\mathrm{f}} = 16$ frequencies, employing $N = 17$ switching angles.

their logic levels. Switching angles in the first half-period (α_1 to α_{2N}) are used to generate the PWM1 signal and α_{2N+1} to α_{4N} are used to generate the PWM2 signal. PWM1 and PWM2 drive the full-bridge GaN devices from two sides and a three-level differential PWM signal is obtained at the switching nodes as shown in Fig. 1.

The architecture of the FPGA for the proposed SHEPWM algorithm is shown in Fig. 5. The architecture can be divided into two major blocks, namely the configuration block and the computing block. Each block is further divided into sub-blocks. The bit length of each signal is indicated in Fig. 5. The description of the two major blocks is as follows.

The configuration block: This block reads the input "data" that the user sends to the FPGA, setting a particular MI and inverter fundamental output frequency. The field Data [3:0] and [7:4] specify different output frequencies and MIs. The reserved Data [13:8] can be used if more output waveform is needed. Enable/disable function of PWMs generation is controlled by Data [14]. Data [15] loads the "Address Counters" through the finite state machine (FSM) so that the first switching angle of a specific MI is indexed in "LUT_NCnt." This mechanism allows real-time user-specific MI selection when a new "data" is sent to the FPGA.

The computing block: This block consists of logic for generating the switching signals PWM1 and PWM2. All calculations in the FPGA are based on fixed-point unsigned arithmetic. The calculated optimal switching angles (α_k) of the first half-cycle (α_1 to α_{2N}) for different MIs are normalized (NCntA/B$= f_{\mathrm{CLK}} \times \alpha_k/360^\circ$) to FPGA clock frequency (f_{CLK}) and prestored in a dual port LUT, "LUT_NCnt." Up to 16 periods ($T = 1/f_{\mathrm{T}}$) of different inverter ac output signals are stored in another LUT, "LUT_T." The counters AddrA and AddrB are initialized with the first switching angle of a specific MI when "LoadAddr" or "Reset" is asserted then count when their respective enable signals "EnAddrA" and "EnAddrB" are asserted. The "Period" of the inverter output signal from "LUT_T" is multiplied by normalized switching angles to generate the absolute switching angles: $\mathrm{ACntA} = T \times \mathrm{NCntA}$, $\mathrm{ACntB}' = T \times \mathrm{NCntB}$. As PWM2 is phase shifted by 180° with respect to PWM1, the final absolute switching angles for the second half-cycle (ACntB) are achieved by adding a period-dependent offset to ACntB', which is performed by the sub-block "Offset." This "Offset" block reduces the memory size of "LUT_NCnt" since switching angles from α_{2N+1} to α_{4N} are not stored in the LUT. As the switching angles are normalized to f_{CLK} (200 MHz in this work), the largest number in "LUT_NCnt" is $2{\cdot}10^8$. The outputs of this 2-port LUT require NCntA/B $= \mathrm{ceil}(\log_2(f_{\mathrm{CLK}}))$ bits, totaling 28 bits, to represent the normalized switching angles. As a result of the structure in Fig. 5, the size of LUT_AddrMI, the 2-port LUT_NCnt, and the LUT_T are $\mathrm{ceil}(\log_2(M{\cdot}2N))$, $M{\cdot}2N{\cdot}\mathrm{ceil}(\log_2(f_{\mathrm{CLK}}))$, and $N_{\mathrm{f}}{\cdot}\mathrm{ceil}(\log_2(f_{\mathrm{CLK}}))$ bits, respectively, where M is the number of MIs and N_{f} is the number of fundamental output frequencies. The total LUT size in Fig. 5 is 1.98 kB, while the implementation described in Section III for our experiments, with $M = 8$, $N_{\mathrm{f}} = 7$, and $N = 17$, is 0.985 kB.

In Table I, the switching angles have been precomputed using MATLAB and the floor method, with deliberate inclusion of an extensive number of decimal points to ensure the precision of the angles, followed by truncation. For simplicity, only two decimal points are shown in the table. The SHEPWM signal with the lower switching frequency gets more switching angle resolution than the higher switching frequency since f_{CLK} is fixed in the FPGA. The switching angle resolution in degrees can be calculated as

$$\Delta\alpha = \frac{360^\circ \times f_{\mathrm{T}}}{f_{\mathrm{CLK}}} \tag{7}$$

where f_{T} is the fundamental output frequency. With $f_{\mathrm{CLK}} = 200\,\mathrm{MHz}$, the switching angle resolution of the different fundamental output frequencies is given by Table II.

Simulink (SysGen) simulation results of important signals in the computing block are shown in Fig. 6. A periodic counter's ("Ramp Counter" sub-block) output signal "CntRamp" is compared with the final absolute switching angles "ACntA" and "ACntB" (first-row in Fig. 6). When they are equal, the comparator triggers "EnAddrA" and "EnAddrB," respectively (second-row

TABLE II
SWITCHING ANGLE RESOLUTION IN DEGREES FOR DIFFERENT FUNDAMENTAL OUTPUT FREQUENCY

f_T (kHz)	4	5	6	7	8	9	10
Resolution (10^{-3} degree)	7.2	9.0	10.8	12.6	14.4	16.2	18

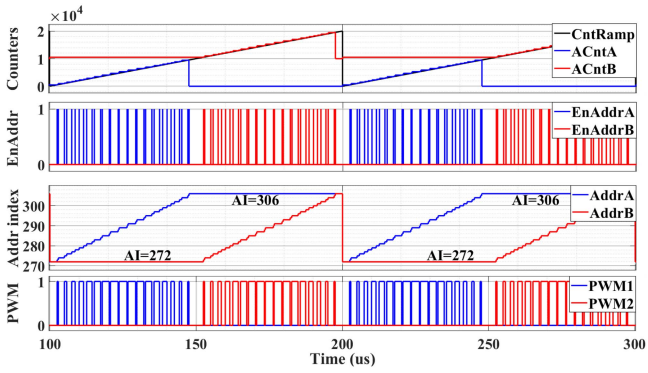


Fig. 6. SHEPWM simulation showing critical FPGA signals in Fig. 5.

in Fig. 6), so that address of the next switching angle is indexed in "LUT_NCnt" (third-row in Fig. 6). The signal CntRamp is then compared with the next absolute switching angle. This continues until all the switching angles within the same MI are compared with CntRamp. When the "Ramp Counter" counts to one full inverter output period, which is given by "LUT_T," the comparator output resets the "Ramp Counter" to zero, and loads the "Address Counters" so that the first switching angle of the same MI is indexed in "LUT_NCnt." For example, the first half-period of switching angles of MI = 0.1 occupies the first 34 addresses in "LUT_NCnt," and all the corresponding switching angles of MIs from 0.1 to 0.9 with a step of 0.1 are prestored in "LUT_NCnt." If the user sends a new input "Data" to the FPGA with an MI = 0.9, then "Address Counters" point to the address index (AI) of 272 $[(9-1)\times 34]$ in "LUT_NCnt." For MI = 0.9, the switching angles occupy the AI from 272 to 306 (see Fig. 6).

Finally, the two PWM signals are obtained from the least-significant bit of signals AddrA and AddrB (third to fourth-row in Fig. 6).

C. On-the-Fly Configuration of AC Output Signals

The proposed SHEPWM architecture can configure the PWM output signals on-the-fly, directly from the personal computer commands without reprogramming the FPGA. As a result, a variable output frequency and/or amplitude can be generated at the inverter output. Fig. 7 shows relevant FPGA signals during on-the-fly configuration. Fig. 8 shows V_{SW}, extracted from PWM1 and PWM2. An analog filter with a cut-off frequency of 20 kHz filters V_{SW} to give the differential output signal V_{OUT}.

From $t = 0.1$ ms to t = 0.87 ms, a waveform with MI = 0.9 and $f_T = 5$ kHz is generated. At t = 0.9ms, the waveform parameters are updated to MI = 0.5 and $f_T = 10$ kHz. Finally at t = 1.7 ms, a waveform with MI = 0.7 and $f_T = 7$ kHz is generated. It can

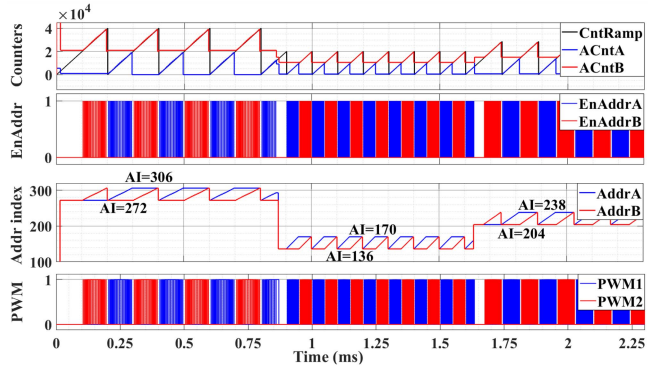


Fig. 7. FPGA signals during on-the-fly configuration.

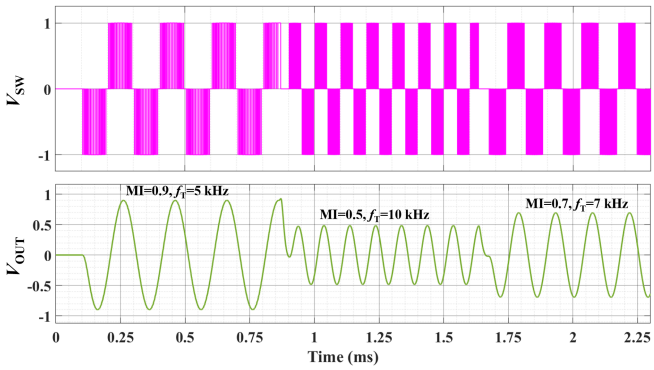


Fig. 8. Effect of on-the-fly configuration on the amplitude and frequency of the inverter output waveform.

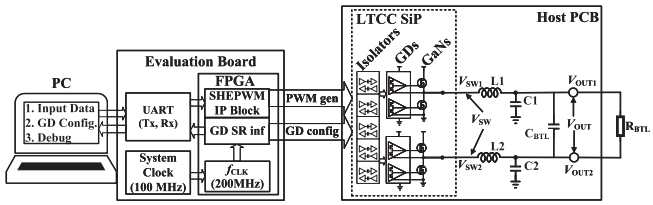


Fig. 9. Architecture of the SHEPWM inverter.

be seen in Fig. 7 (Top) that the higher frequency PWM signal's ramp counter peak is lower than in the case of a lower frequency PWM signal. The third row within Fig. 7 shows that smaller MI signals occupy lower AI. The discontinuity in the waveform between different MI and output frequency in Fig. 8 is due to uploading new "data" information from the MATLAB graphical user interface (GUI) and resetting the FSM in the SHEPWM block. Nevertheless, the results show that the on-the-fly configuration of different ac output signals in real time is achievable with this architecture.

III. INVERTER SYSTEM IMPLEMENTATION

The overall SHEPWM inverter system implementation is described in this section. Fig. 9 shows the architecture of the inverter. The system includes the MATLAB GUI, Nexys Video Artix-7 FPGA board, and a custom host printed circuit board

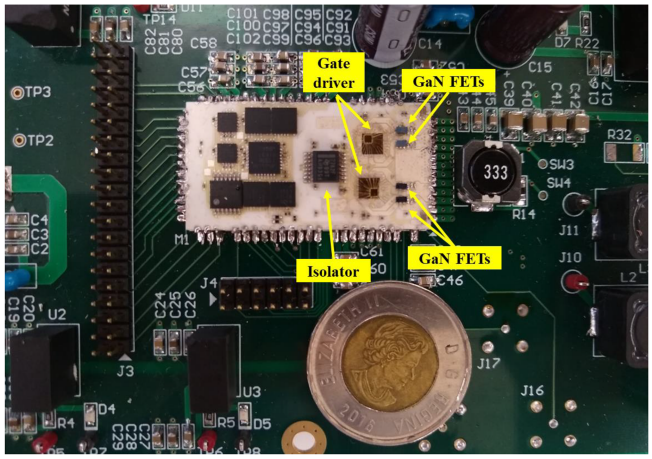


Fig. 10. LTCC SiP with a Canadian two-dollar coin (diameter = 28 mm) as a reference.

(PCB). The input "data" and GD configuration bits are sent from the MATLAB GUI through a universal asynchronous receiver/transmitter interface. The SHEPWM block generates two PWMs using a 200 MHz clock signal that gives 5 ns timing resolution of the switching angles. Faster clock frequency means better timing resolution of the switching angles but at the cost of more severe FPGA timing constraints and higher power dissipation. The host PCB includes the auxiliary power systems (not shown in Fig. 9), an LTCC SiP which consists of digital isolators, two custom-designed reconfigurable GDs [1] and GaN field effective transistors (FETs) (EPC2012C), and a hybrid second-order *LC* low-pass filter (LPF). The digital isolators protect the FPGA from any voltage/current spikes from the host PCB that circulates back to the FPGA. They also convert 3.3 V logic signals from the FPGA to 5 V logic for the GDs. Two GDs drive an H-bridge of GaN FETs and generate a three-level differential PWM signal at the switching nodes.

The highest fundamental output frequency achieved in this work is 10 kHz. Consequently, it is essential for the *LC* filter's cutoff frequency to exceed this value to prevent attenuation of the output voltage. To ensure robust performance, a cutoff frequency of approximately 20 kHz is selected. While higher order *LC* filters, such as a fourth order, are available, they come at the cost of doubling the size of the current second-order *LC* filter. Since one of the primary objectives of this work is to minimize the inverter's size, opting for higher order filters is not favourable. Lower order filters exhibit a gentler attenuation slope at high frequencies, which, in the context of SHEPWM modulation, exacerbates the issue of uncanceled harmonic power at high frequencies, resulting in increased THD at the output. Therefore, considering both filter size and THD performance, we choose a second-order *LC* filter with a cutoff frequency of approximately 20 kHz as the most suitable option.

Fig. 10 shows the LTCC SiP in which digital isolators, GDs, and GaN FETs are integrated with its size referenced to a Canadian two-dollar coin. The two GD ICs and some digital isolators on the bottom of the LTCC substrate are located in cavities

TABLE III
SHEPWM INVERTER TEST CONDITIONS

Parameters	Values
DC input voltage (V_{IN})	12 V
Supply voltage for GD IC	5 V
MI	0.2–0.9
Fundamental output frequency (f_T)	4–10 kHz
Bridge tied loads (R_{BTL})	50 Ω/500 Ω
Bridge tied capacitors (C_{BTL})	0.1 μF/0.01 μF
GD dead time	35 ns
Inductors L1, L2	270 μH/2.2 mH
DC resistance of L1, L2	0.248 Ω/3.1 Ω
Capacitors C1, C2	47 nF/2 nF

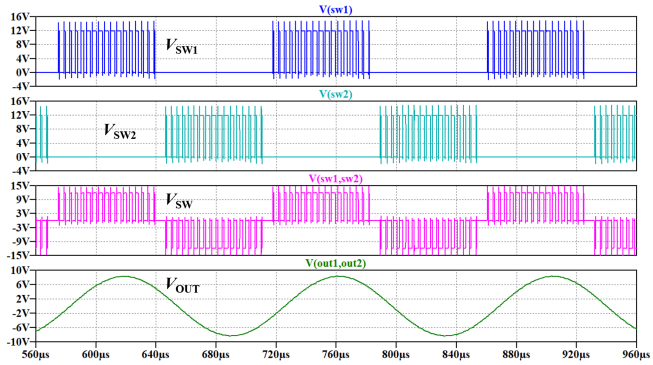


Fig. 11. Singled-ended switching node voltages (V_{SW1} and V_{SW2}), differential switching node (V_{SW}), and output voltage (V_{OUT}) waveforms from LTspice simulations.

to reduce the thickness of the SiP. More information about designing the LTCC SiP, its specifications and implementation can be found in [7] and [33].

IV. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the simulation and experimental results of the SHEPWM inverter system are presented. The generated SHEPWM waveform from MATLAB is imported into the LTspice environment in which real component values and models are used. The SHEPWM waveform drives the inputs of the GD and the amplified SHEPWM signal at the power stage is filtered out by the *LC* filter. The SHEPWM inverter was simulated using the conditions given in Table III with two different loads. The simulated singled-ended switching node voltages (V_{SW1} and V_{SW2}), differential switching node voltage (V_{SW}), and differential output voltage (V_{OUT}) for MI = 0.9, f_T = 10 kHz are shown in Fig. 11. It can be seen that a sinusoidal ac output signal with the correct MI and fundamental output frequency (f_T) is extracted from the three-level SHEPWM signal.

The experimental test setup of the SHEPWM inverter is shown in Fig. 12. Single probes are used to probe the single-ended switching node voltages (V_{SW1} and V_{SW2}) and output voltages (V_{OUT1} and V_{OUT2}). Differential probes are used to probe the differential switching node voltage (V_{SW}) and output voltage (V_{OUT}). Figs. 13 and 14 show the measured output waveforms for these signals. It can seen in Fig. 13 that there are 17 switching angles per quarter cycle in the measured differential switching node voltage (V_{SW}). In other words, 17 rectangle pulses are

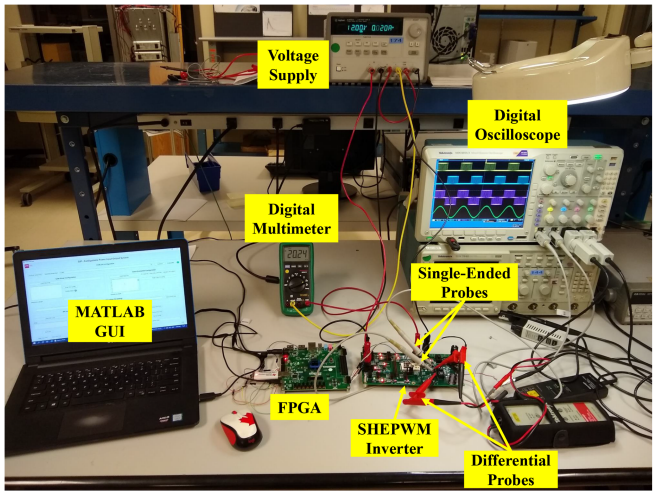


Fig. 12. SHEPWM inverter experimental test setup.

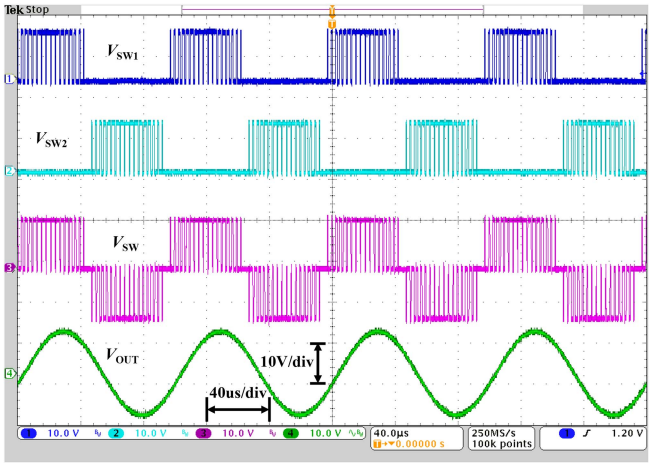


Fig. 13. Measured single-ended switching node voltages (V_{SW1} and V_{SW2}), differential switching node (V_{SW}), and output voltage (V_{OUT}) waveforms for MI = 0.9 and f_T = 10 kHz.

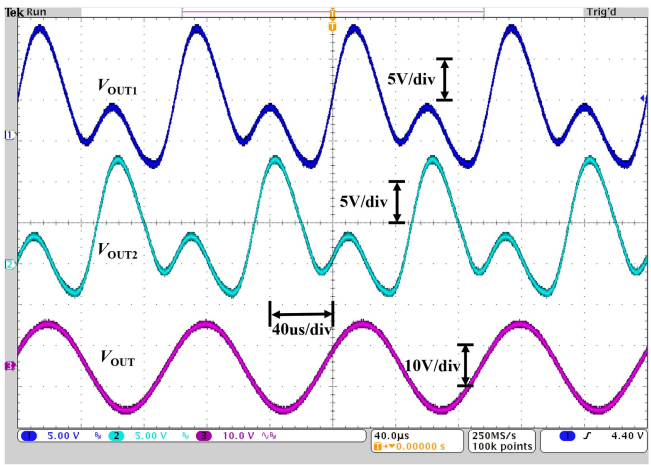


Fig. 14. Measured inverter single-ended (V_{OUT1} and V_{OUT2}) and differential (V_{OUT}) output signals for MI = 0.9 and f_T = 10 kHz.

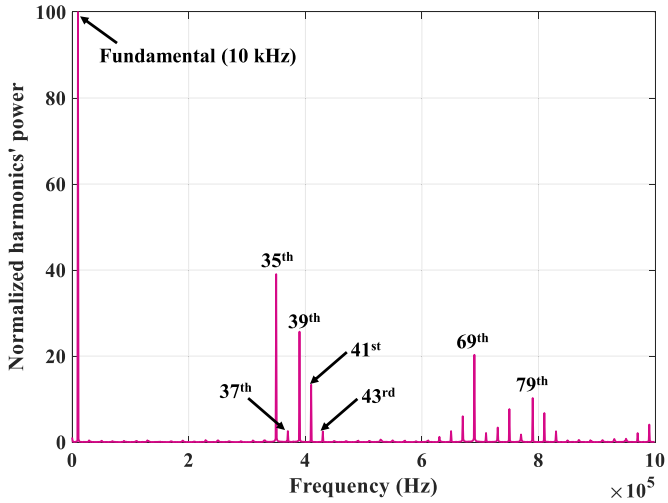


Fig. 15. Spectrum of the measured differential switching node voltage (V_{SW}).

generated in both positive and negative half-periods in V_{SW} with a peak-to-peak value of 24 V. The measured differential output voltage (V_{OUT}) has amplitude of approximately 21.3 V and frequency of 10 kHz, which matches the simulation results in Fig. 11.

The frequency spectrum of the measured switching node voltage (V_{SW}) is given in Fig. 15, where each harmonic's power is normalized to the fundamental harmonic's power. The fundamental output frequency (first harmonic) in this measurement is 10 kHz. It can be seen from the figure that lower order harmonics up to 34 are suppressed as expected. Some lower order harmonics are not fully eliminated due to timing errors introduced in the SHEPWM signal by the GD and power transistors, however, their power is very low compared to the fundamental's power as shown in Table IV, in which the first 50 harmonics' normalized power is given.

The SHEPWM inverter's output THD is measured according to the equation below:

$$\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots + V_i^2}}{V_1} \tag{8}$$

where V_i is the root mean squared (RMS) value of the ith harmonic voltage. The output THD and its relationship between MIs and fundamental output frequencies are shown in Fig. 16(a). The results show that the THD is low for high MI and output frequencies, and it increases gradually with decreasing MI and output frequency. This can be explained by the high power of the harmonic immediately after the canceled harmonics (35th harmonic in Fig. 15), which is suppressed by the LPF more for higher output frequencies since the filter's cut-off frequency is fixed at 20 kHz. For small MI SHEPWM, more power is concentrated in the harmonics after the canceled harmonics. With a faster FPGA clock frequency (7), the angle resolution gets better at smaller MI and THD at the output can be further reduced but at the cost of more hardware resources and accurate digital logic timing control. Overall, THD is equal or lower

TABLE IV
POWER OF THE HARMONICS OF THE DIFFERENTIAL SWITCHING NODE VOLTAGE (V_{SW})

Harmonic	Normalized power	Harmonic	Normalized power	Harmonic	Normalized power	Harmonic	Normalized power	Harmonic	Normalized power
1	100	11	0.25	21	0.09	31	0.39	41	13.32
2	0.07	12	0.01	22	0.03	32	0.05	42	0.03
3	0.32	13	0.26	23	0.22	33	0.41	43	2.49
4	0.02	14	0.01	24	0.01	34	0.08	44	0.04
5	0.24	15	0.07	25	0.42	35	39.06	45	0.23
6	0.05	16	0.05	26	0.04	36	0.08	46	0.04
7	0.12	17	0.15	27	0.16	37	2.57	47	0.03
8	0.01	18	0.03	28	0.01	38	0.13	48	0.01
9	0.16	19	0.36	29	0.08	39	25.67	49	0.14
10	0.02	20	0.02	30	0.03	40	0.03	50	0.05

*Fundamental frequency is 10 kHz; Each harmonic's power is normalized to the first harmonic. The dc harmonic's normalized power is 1.07.

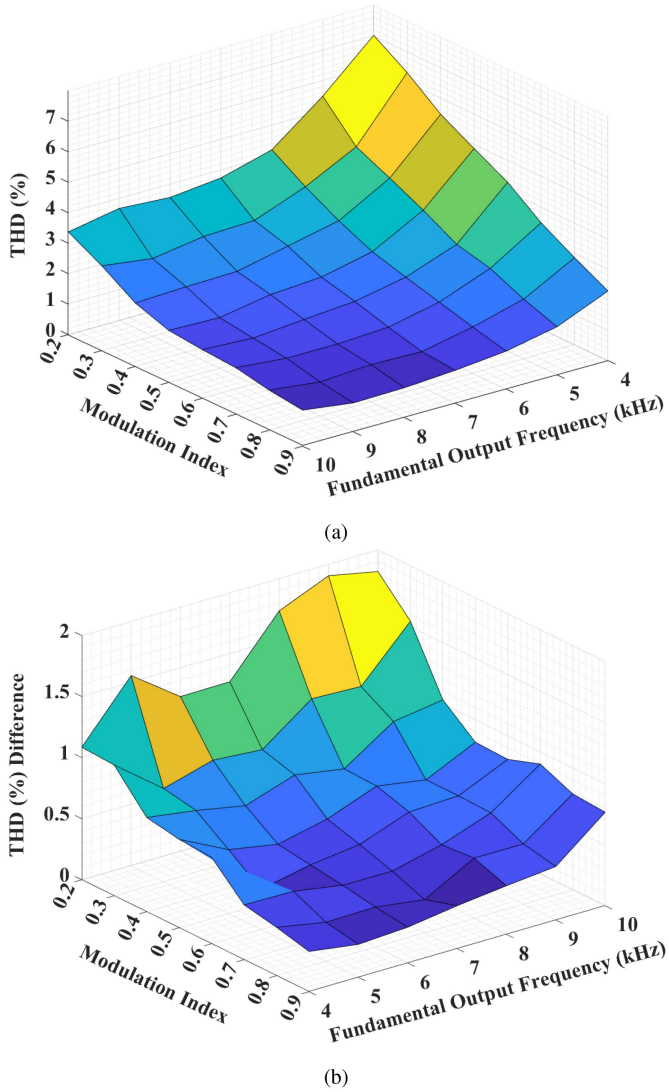


Fig. 16. (a) Measured THD versus different MIs and output frequencies. (b) THD difference between simulation and measurement.

than 5.1% for MI 0.2 to 0.9 and output frequency from 5 to 10 kHz (THD = 5.08% for MI = 0.2 and $f_T = 5$ kHz). The THD difference at the inverter output between simulation and measurement for different MI and the fundamental output frequency is given in Fig. 16(b) in which the simulated THD is lower than the measured one. The THD difference is larger in the regions of smaller MI and larger output frequencies. This is because short pulses with a fast-switching frequency at the switching node are more sensitive to timing errors. From the figure, it can be seen that the THD difference is less than 1% for most of the region, and MI degrades the measured THD more than the output frequency.

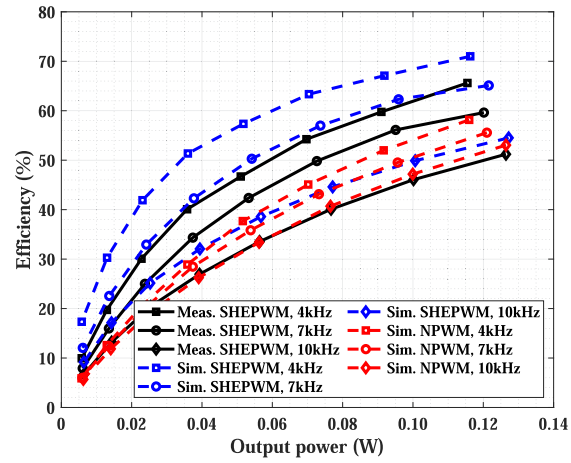
Although the higher switching frequency SHEPWM signal exhibits a lower switching angle resolution (see Table II), its output THD is lower compared to the lower switching frequency SHEPWM signals. Consequently, the degradation in THD for lower frequency output signals cannot be attributed primarily to the switching angle resolution. Even when adopting SHEPWM in a closed-loop control to achieve the ideal switching angles, the enhancement in THD output is almost insignificant. The THD degradation is primarily due to the fixed *LC* cutoff frequency, where higher switching frequency SHEPWM signals attenuate high-order harmonics more compared to lower switching frequency SHEPWM signals.

The power efficiency of the SHEPWM inverter is measured according to the equation as follows:

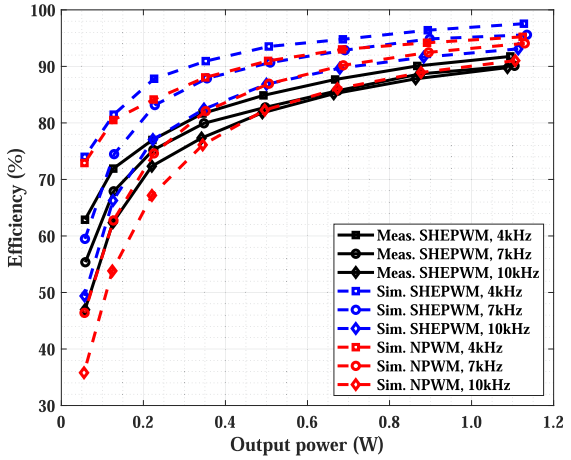
$$\eta = \frac{V_{\mathrm{OUT(RMS)}} \times I_{\mathrm{OUT(RMS)}}}{V_{\mathrm{IN}} \times I_{\mathrm{IN(AVE)}}} \tag{9}$$

where $V_{\mathrm{OUT(RMS)}}$ and $I_{\mathrm{OUT(RMS)}}$ are the rms values of the differential output voltage and current, V_{IN} is the inverter dc input voltage, and $I_{\mathrm{IN(AVE)}}$ is the average input current of the inverter. The inverter's efficiency is simulated and compared to an NPWM inverter.

Fig. 17 shows the power efficiency of the inverter for different output power, where dashed lines are for simulated efficiency and solid lines are for measured efficiency. For the same inverter conditions and output THD, the SHEPWM inverter has better efficiency than NPWM. The results showed that at fundamental output frequencies of 4 kHz, 7 kHz, and 10 kHz, the SHEPWM inverter, with an output power of 0.12 W, exhibited an average efficiency improvement of 17.3%, 11.7%, and 4.2% over the NPWM inverter, respectively. Conversely, when the output power was increased to 1.2 W, the efficiency advantage of SHEPWM, while slightly reduced, remained notable, with an average improvement of 2.3%, 6.2%, and 6.9%, respectively.



(a)



(b)

Fig. 17. Power efficiency comparisons of the SHEPWM and NPWM inverters for the same output THD. (a) P_{out}=0.12 W. (b) P_{out}=1.2 W.

For the SHEPWM inverter, the switching frequency at the switching node is scaled with the fundamental output frequency since there are fixed 34 rising/falling edges per one sine-wave cycle. However, there is no fixed switching period for the SHEPWM signal, and the switching frequency is instead a quasi-switching frequency. That is, for a 10 kHz fundamental output frequency, the switching node has a 340 kHz quasi switching frequency, and for the 7 kHz and 4 kHz fundamental output frequency, the quasi switching frequency is 238 kHz and 136 kHz, respectively. One thing is clear that the switching losses happen during the finite rising/falling time (where GaN FETs' drain–source voltage and current overlap), and the rising/falling edges count can be compared with NPWM. For the same inverter conditions and output THD, the NPWM inverter has a switching frequency of 370 kHz, 256 kHz, and 148 kHz for the fundamental output frequency of 10 kHz, 7 kHz, and 4 kHz, respectively. This implies that the SHEPWM exhibits lower switching activity compared to the NPWM, resulting in reduced switching losses dissipated in the SHEPWM.

For the same output power ($V_{\text{OUT(RMS)}} \times I_{\text{OUT(RMS)}}$), SHEPWM and NPWM have the same conduction loss ($P_{\text{con}} = I^2_{\text{OUT(RMS)}} \times R_{\text{PATH}}$), where R_{PATH} is the path resistance from input supply to output voltage, including the GaN FET's turn on resistor ($R_{\text{DS(ON)}}$), inductor series resistance, and any parasitic resistance in the path. The rest of the power losses come from the switching losses, which are proportional to the switching frequency of the inverter. These switching losses include but are not limited to switching loss due to the finite turning ON/OFF time of the power transistors, gate charge loss due to charging and discharging of the gate capacitance of the power transistors, dead-time loss due to the freewheeling conduction loss of the body diode of the power transistors, and some power loss due to the ripple current on the inductor. Therefore, to achieve lower THD than SHEPWM, NPWM would need to operate at an even higher switching frequency, incurring more switching losses that could degrade the overall inverter efficiency.

For the SHEPWM inverter, the efficiency is higher for the lower output frequency since the switching frequency at the switching node is scaled with the fundamental output frequency. The measured efficiency is less than the simulated efficiency, and the difference in efficiency is obvious for small output power but decreases for large output power. This can be attributed to the predominant switching losses at lower output power levels, and it is possible that the model accuracy of the GD and GaN FETs may not be optimal. Also, calculating the exact switching losses is almost impossible because the effect of the parasitic inductive components significantly alters the current and voltage waveform, as well as the switching times during the switching process. In addition, variables such as GaN FET capacitor values, gate threshold voltage, driver output impedance, and others introduce uncertainty in the calculation of switching losses in the GaN FET.

Another observation from Fig. 17 is the efficiency advantage of SHEPWM over NPWM is large for the low-power inverter but reduced for the high-power inverter. There are two reasons for this. One is as the power increases, the conduction loss increases. Hence, the switching losses from less switching activity from SHEPWM are insignificant. Second, SHEPWM consistently operates in hard-switching mode, whereas NPWM incorporates a partial soft-switching mechanism. Soft-switching is known for its higher efficiency compared to hard-switching. As the load current increases, the dominance of soft-switching becomes more pronounced in NPWM. In SHEPWM, the switching node has a switching activity when there is only a current going out of the switching node, and there is no switching activity when there is a current going into the switching node (see Fig. 13). On the other hand, in NPWM, there is continuous switching activity on both switching nodes. For half of the sine-wave cycle, the current flows out of the switching node, indicating hard-switching. During the other half-cycle, the current flows into the switching node, charging the output capacitance of the GaN FET. This contributes to the rising of the switching node during dead-time. After the dead-time concludes, the remaining rise of the switching node is attributed to the GD pulling up, which consumes power. With increasing load current, the output capacitor charges more rapidly, leading to reduced power consumption from the GD [34].

TABLE V
COMPARISON TO OTHER WORKS

	Power stage structure	Voltage levels	DC bus voltage	MI	Fundamental output frequency (f_T)	Transitions per quarter period	On-the-fly config of ac outputs
[17]	Cascaded H-Bridge	13	18×15 V	0−3.4 (discontinous)	50 Hz	9	No
[19]	H-Bridge	3	100 V	0−0.83 (continous)	50 Hz	8	No
[23]	Hybrid-clamped	4	150 V	0−1.15 (discontinous)	50 Hz	7	No
[24]	Module Multilevel	-	200 V	0.1−1 (continous)	50 Hz	17	No
[29]	Cascaded H-Bridge	7	3×50 V	1.65−2 (continous)	60 Hz	3	No
[31]	Cascaded H-Bridge	7	3×40 V	0.1−1.04 (continous)	50 Hz	3	Yes (MI only)
This work	H-Bridge	3	12 V	0.2−0.9 (continous)	4 − 10 kHz	17	Yes (MI and f_T)

This work is compared with other recent works based on the power stage structure, the number of switching node voltage levels, dc-bus voltage(s), MI range, fundamental output frequency, transitions per quarter period, and capability of configuring the ac outputs on-the-fly, as shown in Table V. For a multilevel cascaded H-Bridge topology, more than one isolated dc source is required. Depending on the topology, voltage level, and switching angle numbers, multilevel inverters' MIs may or may not be continuous in the full range of MI. For discontinuous MI, there is no solution for the optimal switching angles in some regions of MI, therefore, the inverter cannot generate an output voltage with the specific amplitude. Works in [17] and [23] have discontinuous MI ranges and only minimum and maximum MIs are given in Table V. In [31], an on-the-fly configuration of output amplitude is presented but at the cost of complex online computation of real-time switching angles. The proposed method in this article is simple, cost-effective, and has the capability of on-the-fly configuration of both inverter output amplitude and frequency. It is worth noting that the fundamental SHEPWM technique detailed in our work can be readily extended to high-power converters operating within the kilowatt range. This extension primarily involves increasing the input voltage for power transistors and adjusting the *LC* filter component values (ensuring that the power rating of the power transistors and *LC* filter components are suitable for the kilowatt range) to meet the specific requirements of higher power levels.

V. CONCLUSION

In this article, a low-power SHEPWM inverter is presented. The inverter is designed on a 3D-integrated compact LTCC SiP to save PCB area. The SHEPWM hardware design in MATLAB Simulink (SysGen) was described in detail and the proposed FPGA architecture has the capability of configuring the ac outputs on-the-fly with different MI and frequencies.

The theory of SHEPWM is validated experimentally in this article for low output power with MI ranges from 0.2 to 0.9, and output frequencies from 4 kHz to 10 kHz. Results show an example where lower order harmonics are canceled up to the 34th harmonic at the differential three-level PWM. The THD is very low for large MI and high output frequencies but degrades modestly for lower MI and output frequencies. The THD difference between simulation and measurement becomes more significant for smaller MI and larger output frequencies, and MI affects the THD more than the output frequency. For the same output THD, SHEPWM exhibits higher efficiency than NPWM due to its lower switching activity. This characteristic makes the SHEPWM inverter well-suited for driving low-power loads that require sinusoidal outputs.

ACKNOWLEDGMENT

The authors would like to thank Nam Ly, Gabriel Nobert, Abdul Hafiz Alameh, Van Ha Nguyen, and Tan Pham for helping with the prototype and test setup, LaCIME at ETS for providing experimental facility, and CMC Microsystems for providing the layout design tools and enabling device fabrication.

REFERENCES

[1] N. Ly, N. Aimaier, A. H. Alameh, Y. Blaquière, G. Cowan, and N. G. Constantin, "A high voltage multi-purpose on-the-fly reconfigurable half-bridge gate driver for GaN HEMTs in 0.18um HV SOI CMOS technology," in *Proc. 18th IEEE Int. New Circuits Syst. Conf.*, 2020, pp. 178–181.

[2] J. Sangid, G. Long, P. Mitchell, B. J. Blalock, D. J. Costinett, and L. M. Tolbert, "Comparison of 60V GaN and Si devices for class D audio applications," in *Proc. IEEE 6th Workshop Wide Bandgap Power Devices Appl.*, 2018, pp. 73–76.

[3] J. Chung, R. McKenzie, and W. T. Ng, "A comparison between GaN and silicon based class D audio power amplifiers with Pulse Density Modulation," in *Proc. 13th IEEE Int. Conf. Solid-State Integr. Circuit Technol.*, 2016, pp. 90–93.

[4] M. Mauerer and J. W. Kolar, "Distortion minimization for ultra-low THD class-D power amplifiers," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 4, pp. 324–338, Dec. 2018.

[5] O. Gedz, V. Lazebnyi, Y. Onikienko, and A. Vlasjuk, "EMI simulation of GaN power stage for audio class D amplifiers," in *Proc. 14th Int. Conf. Adv. Trends Radioelecrtronics Telecommun. Comput. Eng.*, 2018, pp. 204–207.

[6] A. Seidel and B. Wicht, "Integrated gate drivers based on high-voltage energy storing for GaN transistors," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3446–3454, Dec. 2018.

[7] G. Nobert, A.-H. Alameh, N. Ly, N. G. Constantin, and Y. Blaquière, "Towards an LTCC SiP for control system in safety-critical applications," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2021, pp. 1–5.

[8] B. Bayer et al., "LTCC embedding of SiC power devices for high temperature applications over 400 °C," in *Proc. IEEE 8th Electron. Syst.-Integration Technol. Conf.*, 2020, pp. 1–5.

[9] M. Jahmeerbacus and M. Sunassee, "Evaluation of selective harmonic elimination and sinusoidalPWM for single-phase DC to AC inverters under dead-time distortion," in *Proc. IEEE 23rd Int. Symp. Ind. Electron.*, Istanbul, Turkey, 2014, pp. 465–470. [Online]. Available: https://ieeexplore.ieee.org/document/6864658/

[10] H. S. Patel and R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I–harmonic elimination," *IEEE Trans. Ind. Appl.*, vol. IA-9, no. 3, pp. 310–317, May 1973. [Online]. Available: https://ieeexplore.ieee.org/document/4158397/

[11] H. S. Patel and R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part II – voltage control techniques," *IEEE Trans. Ind. Appl.*, vol. IA-10, no. 5, pp. 666–673, Sep. 1974.

[12] C. Wang, Q. Zhang, D. Chen, Z. Li, W. Yu, and K. Yang, "Application of newton identities in solving selective harmonic elimination problem with algebraic algorithms," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 5, pp. 5870–5881, Oct. 2022. [Online]. Available: https://ieeexplore.ieee.org/document/9807314/

[13] Y. Li, X.-P. Zhang, and N. Li, "An improved hybrid PSO-TS algorithm for solving nonlinear equations of SHEPWM in multilevel inverters," *IEEE Access*, vol. 10, pp. 48112–48125, 2022.

[14] S. Ahmad, A. Iqbal, M. Ali, K. Rahman, and A. S. Ahmed, "A fast convergent homotopy perturbation method for solving selective harmonics elimination PWM problem in multi level inverter," *IEEE Access*, vol. 9, pp. 113040–113051, 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9511423/

[15] M. Ahmed et al., "General mathematical solution for selective harmonic elimination," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4440–4456, Dec. 2020. [Online]. Available: https://ieeexplore.ieee.org/document/8786223/

[16] A. Janabi, B. Wang, and D. Czarkowski, "Generalized chudnovsky algorithm for real-time PWM selective harmonic elimination/modulation: Two-level VSI example," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5437–5446, May 2020. [Online]. Available: https://ieeexplore.ieee.org/document/8859270/

[17] K. Yang et al., "Unified selective harmonic elimination for multilevel converters," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1579–1590, Feb. 2017. [Online]. Available: https://ieeexplore.ieee.org/document/7442885/

[18] K. Yang, Q. Zhang, R. Yuan, W. Yu, J. Yuan, and J. Wang, "Selective harmonic elimination with groebner bases and symmetric polynomials," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2742–2752, Apr. 2016. [Online]. Available: https://ieeexplore.ieee.org/document/7128729/

[19] K. Yang, Z. Yuan, R. Yuan, W. Yu, J. Yuan, and J. Wang, "A groebner bases theory-based method for selective harmonic elimination," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6581–6592, Dec. 2015. [Online]. Available: https://ieeexplore.ieee.org/document/7000602/

[20] M. H. Etesami, N. Farokhnia, and S. H. Fathi, "Colonial competitive algorithm development toward harmonic minimization in multilevel inverters," *IEEE Trans. Ind. Informat.*, vol. 11, no. 2, pp. 459–466, Apr. 2015. [Online]. Available: https://ieeexplore.ieee.org/document/7038159/

[21] D. Czarkowski, D. Chudnovsky, and I. Selesnick, "Solving the optimal PWM problem for single-phase inverters," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 49, no. 4, pp. 465–475, Apr. 2002.

[22] M. D. Siddique, S. Mekhilef, S. Padmanaban, M. A. Memon, and C. Kumar, "Single-phase step-up switched-capacitor-based multilevel inverter topology with SHEPWM," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 3107–3119, May/Jun. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9115836/

[23] M. Wu, K. Wang, K. Yang, G. Konstantinou, Y. W. Li, and Y. Li, "Unified selective harmonic elimination control for four-level hybrid-clamped inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11488–11501, Nov. 2020. [Online]. Available: https://ieeexplore.ieee.org/document/9057441/

[24] A. Perez-Basante et al., "Circulating current control for modular multilevel converters with (N+1) selective harmonic elimination–PWM," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8712–8725, Aug. 2020. [Online]. Available: https://ieeexplore.ieee.org/document/8951241/

[25] A. Iqbal, M. Meraj, M. Tariq, K. A. Lodi, A. I. Maswood, and S. Rahman, "Experimental investigation and comparative evaluation of standard level shifted multi-carrier modulation schemes with a constraint GA based SHE techniques for a seven-level PUC inverter," *IEEE Access*, vol. 7, pp. 100605–100617, 2019. [Online]. Available: https://ieeexplore.ieee.org/document/8761853/

[26] K. Yang, X. Lan, Q. Zhang, and X. Tang, "Unified selective harmonic elimination for cascaded H-bridge asymmetric multilevel inverter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 2138–2146, Dec. 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8300507/

[27] M. Sharifzadeh, H. Vahedi, and K. Al-Haddad, "New constraint in SHE-PWM for single-phase inverter applications," *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4554–4562, Sep. 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8351939/

[28] L. Manai, F. Armi, and M. Besbes, "Flying capacitor multilevel inverter control considering lower order harmonics elimination based on Newton-Raphson algorithm," *Electric Power Compon. Syst.*, vol. 45, no. 17, pp. 1918–1928, Oct. 2017. [Online]. Available: https://www.tandfonline.com/doi/full/10.1080/15325008.2017.1401683

[29] H. Zhao, T. Jin, S. Wang, and L. Sun, "A real-time selective harmonic elimination based on a transient-free inner closed-loop control for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1000–1014, Feb. 2016.

[30] J. Cheng, T. Xu, D. Chen, and G. Chen, "Dynamic and steady state response analysis of selective harmonic elimination in high power inverters," *IEEE Access*, vol. 9, pp. 75588–75598, 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9438642/

[31] M. Ahmed, A. Sheir, and M. Orabi, "Real-time solution and implementation of selective harmonic elimination of seven-level multilevel inverter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1700–1709, Dec. 2017. [Online]. Available: https://ieeexplore.ieee.org/document/8019796/

[32] N. Aimaier, N. Ly, G. Nobert, Y. Blaquière, N. Constantin, and G. Cowan, "SHEPWM class-D amplifier with a reconfigurable gate driver integrated circuit," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2021, pp. 1–5.

[33] V. H. Nguyen et al., "A reconfigurable power system-in-package module using GaN HEMTs and IC bare dies on LTCC substrate: Design—implementation—experiment and future directions," in *Proc. 20th IEEE Int. NEWCAS Conf.*, 2022, pp. 188–192.

[34] H. Ma, R. van der Zee, and B. Nauta, "A high-voltage class-D power amplifier with switching frequency regulation for improved high-efficiency output power range," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1451–1462, Jun. 2015.

Nueraimaiti (Nurahmed) Aimaier (Student Member, IEEE) received the B.Eng. degree in electronic and information engineering from Soochow University, Suzhou, China, in 2011, and the M.Sc. degree in electronic engineering from Universiti Putra Malaysia, Selangor, Malaysia, in 2015. He is currently working toward the Ph.D. degree in low-power class-D amplifiers from Concordia University.

From 2015 to 2018, he was an Analog IC Design Engineer, focusing on power management ICs design, including LDOs and dc–dc buck converters. He joined Concordia University, Montreal, QC, Canada, in 2018. His research interests include analog/mixed-signal design, power management ICs and class-D amplifier design and their control methodology.

Yves Blaquière (Member, IEEE) received the B.Eng., M.Sc., and Ph.D. degrees in electrical engineering from the École Polytechnique de Montréal, Montreal, QC, Canada, in 1984, 1986, and 1992, respectively.

From 1987 to 2016, he was a Professor of Microelectronic Engineering with the University of Quebec in Montreal (UQAM), Montreal, QC, Canada. He has been a Professor with the École de Technologie Supérieure (ETS) Montréal, Montreal, QC, Canada, since 2016. He has done research and development projects in collaboration with several microelectronic companies. He is a member of the Regroupement Stratégique en Microélectronique du Québec and the Ordre des Ingénieurs du Québec (OIQ). At UQAM, he was the Director of the Laboratoire de Recherche de Conception en Microélectronique, from 1992 to 1999 and from 2004 to 2008, the Director of the Microelectronic Engineering Program from 2004 to 2010, and the Director of Engineering from 2011 to 2015. He currently works in the field of electrical/electronic/microelectronic engineering, specifically in ASIC/FPGA design, VLSI/WSI microsystems high-speed digital circuits, timing tools, architectures, defect tolerance, applications in signal processing, and embedded systems.

Nicolas G. Constantin (Senior Member, IEEE) received the B.Eng. degree from the École de technologie supérieure (ÉTS)—University of Quebec, Québec, QC, Canada, in 1989, the M.A.Sc. degree from the École Polytechnique de Montréal, Montréal, QC, Canada, in 1994, and the Ph.D. degree from McGill University, Montreal, QC, Canada, in 2009, all in electrical engineering.

He is currently an Associate Professor with the ÉTS, Montreal, QC, Canada. From 1989 to 1992, he worked in the design of microwave transceivers for point-to-point radio links. From 1996 to 1998, he worked as an RF Design Engineer with NEC, in the development of RF and microwave transceivers for mobile telephony. From 1998 to 2002, he was a Senior Design Engineer with Skyworks Solutions, Inc., Newbury Park, CA, USA, where he developed GaAs HBT RFIC PAs for wireless communications. At Skyworks, he was also actively involved in research on smart biasing and efficiency improvement techniques for RFIC PAs, and he is the author of several patents on the subject. His primary research interests are in the design and test of Analog, RF & Millimeter-wave ICs and Front-End modules for mobile wireless communications and satellite communications, as well as behavioral modeling of nonlinear analog and RF circuits and embedded test solutions for reliability improvement. He conducts research in these areas in collaboration with major companies in the wireless communication and aerospace industry.

Glenn E. R. Cowan (Member, IEEE) received the B.A.Sc. degree from the University of Waterloo, Waterloo, ON, Canada, in 1999, and the M.S. and Ph.D. degrees from Columbia University, New York, NY, USA, in 2001 and 2005, respectively, all in electrical engineering.

In 2007, he joined the Department of Electrical and Computer Engineering, Concordia University, Montreal, QC, Canada, where he is currently a Professor. His current research activities include low-power mixed-signal circuits for biomedical applications and wireline communication.

Dr. Cowan was a 2003 recipient of Analog Device's Outstanding Student Designer Award at Columbia, and the 2005 Eliahu I. Jury award for outstanding achievement by a graduate student.