An Accurate Predictive Method of Crosstalk Peaks Considering Dynamic Transfer Characteristics and Miller Ramp for SiC MOSFETs

Hao Yue, Jian Chen, *Member, IEEE*, Wensheng Song, *Senior Member, IEEE*, Haoyang Tan, and Pengcheng Xu, *Graduate Student Member, IEEE*

***Abstract*—Silicon carbide-based metal-oxide-semiconductor field effect transistors (SiC MOSFETs) have been widely applied due to their lower on-resistance and parasitic parameters compared with silicon devices. However, the unexpected crosstalk phenomenon occurs and could lead to false turn-ON or gate-oxide damage of the devices. In this article, an accurate predictive method of crosstalk peaks is proposed to provide theoretical guidance for crosstalk evaluation and suppression, which can improve the reliability of the systems. First, the generation of crosstalk and conventional predictive method are illustrated. Second, an improved crosstalk model considering dynamic transfer characteristics and Miller ramp is proposed. Furthermore, the dynamic transfer characteristics and Miller charge of SiC MOSFETs are obtained experimentally to realize the necessary supplement of the data provided by manufacturers. Finally, the crosstalk peaks predicted by the proposed method are compared experimentally with the actual measured values. The results have verified the proposed method can achieve accurate prediction of crosstalk peaks, and the relative errors of the predicted crosstalk peaks are below 10%.**

***Index Terms*—Crosstalk, dynamic transfer characteristics, miller ramp, silicon carbide (SiC) metal-oxide-semiconductor field effect transistors (MOSFETs).**

I. Introduction

DUE to low on-resistance and parasitic capacitance, silicon carbide-based metal-oxide-semiconductor field effect transistors (SiC MOSFETs) have lower losses and faster switching speeds compared to silicon-based insulated-gate bipolar transistors (Si IGBTs), which contributes to the replacement of Si-based IGBTs with SiC MOSFETs in many applications such as photovoltaic systems and electric vehicles [1], [2], [3]. However, the increase of switching speed may cause serious reliability issues including crosstalk [4], overvoltage during turn-OFF operation [5], and electromagnetic interference [6]. These issues have hindered the widespread application of SiC MOSFETs and received increasing attention in recent years.

For SiC MOSFETs, there are two package styles, namely, Kelvin package and non-Kelvin package. The SiC MOSFETs with Kelvin package have an independent Kelvin sense-source (ss) terminal, which means that they have better dynamic performance and have been widely applied in power converters [7]. Therefore, the SiC MOSFETs with Kelvin package are adopted to study the crosstalk phenomenon in this article. In the phase-leg configuration, the controlled device switching induces the high change rate (dv_{ds}/dt) of drain-source voltage, charging or discharging the Miller capacitor C_{gd} in the complementary device. Meanwhile, the charging and discharging currents flow through the gate loop, making the gate voltage induce positive and negative voltage spikes. The maximum amplitudes of positive and negative spikes are defined as positive and negative crosstalk peaks, respectively. The positive crosstalk spikes occur when the controlled device is turned ON. It is noteworthy that if the positive crosstalk peaks exceed the threshold voltage V_{th} of the complementary device, it will be falsely turned ON [8]. On the contrary, the negative crosstalk spikes occur when controlled device is turned OFF. For SiC MOSFETs, the negative crosstalk peaks are the critical parameter that influences the switching-induced V_{th} drift. Under the continuous negative crosstalk spikes, V_{th} could shift downward, which makes the devices easier to be falsely turned ON [9]. These problems seriously lower the reliability of the devices and threaten the safe operation of the systems. Setting negative turn-OFF gate voltage is widely suggested to address the false turn-ON caused by positive crosstalk spikes for SiC MOSFETs [10], [11], [12], [13], [14]. Nevertheless, the negative crosstalk spikes, generated on the basis of negative turn-OFF gate voltage, may potentially exceed recommended safe operating area (SOA). As described in [13], the continuous negative crosstalk spikes may shorten the lifetime of SiC devices. Moreover, if the negative crosstalk peaks are large enough, the gate-oxide layer of SiC MOSFETs will be damaged because of low negative gate voltage tolerance [15], [16]. Therefore, to ensure that the devices work within the recommended SOA,

Manuscript received 11 July 2023; revised 31 October 2023 and 18 December 2023; accepted 26 January 2024. Date of publication 6 February 2024; date of current version 20 March 2024. This work was supported in part by the National Natural Science Foundation of China under Grant U2368206 and Grant 52307224, and in part by the Sichuan Science and Technology Program under Grant 22CXTD0055 and Grant 2023YFH0050. Recommended for publication by Associate Editor M. Nawaz. *(Corresponding authors: Jian Chen; Wensheng Song.)*

The authors are with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu 610031, China (e-mail: yuehao6866@my.swjtu.edu.cn; chenjian@swjtu.edu.cn; songwsh@swjtu.edu.cn; thy@my.swjtu.edu.cn; pchxu1118@my.swjtu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3362367.

Digital Object Identifier 10.1109/TPEL.2024.3362367

both positive and negative crosstalk peaks should be accurately modeled and evaluated to select the optimal circuit parameters and negative turn-OFF gate voltage.

In previous works, the crosstalk phenomenon of SiC and gallium nitride (GaN) devices has been investigated in detail [17], [18], [19], [20], [21], [22], [23]. For SiC MOSFETs, the positive and negative crosstalk peaks are predicted by calculating dv_{ds}/dt and the duration time of each stage [22]. Meanwhile, a multilevel active gate drive circuit is developed to suppress the crosstalk spikes. The positive and negative crosstalk peaks are used as important selection basis of negative turn-OFF gate voltage to achieve better crosstalk suppression effect. Then, the nonlinearity of C_{gd} is mainly considered to improve the predictive accuracy in [23]. However, the parameters used in [22] and [23] are extracted from datasheets [24], [25] and determined under limited test conditions. The actual operating range of SiC MOSFETs is much wider than datasheets. In this case, the short-channel effect (SCE) will lead to the dynamic transfer characteristics under different blocking voltage of SiC MOSFETs [27], [28], [29]. And the C-V characteristics of SiC MOSFETs will also change in the high-speed switching operations [30]. Therefore, it is difficult to realize a wide range prediction of crosstalk peaks using the parameters in datasheets. Meanwhile, under the SCE, V_{th} of SiC MOSFETs is negatively correlated with drain bias, which means that the devices will more easily be falsely turned ON at higher drain bias. In previous studies, this phenomenon has been insufficiently concerned. Furthermore, the Miller plateau is considered as constant in [20], [22], and [23]. Nevertheless, the dynamic transfer characteristics of SiC MOSFETs will lead Miller ramp to replace Miller plateau [29], [36], which further increases the error of the predicted results. In [23], the maximum relative error of crosstalk peaks is about 30%, which has limited guiding significance for crosstalk evaluation and suppression. In addition, the packaging parameters are neglected in [20], [22], and [23]. Since V_{th} of SiC MOSFETs is determined in the presence of packaging parameters. The predictive method that ignores the packaging parameters may cause inaccurate crosstalk evaluation and suppression, so the actual gate voltage could still exceed the recommended SOA of SiC MOSFETs. For GaN devices, a crosstalk analytical model that considering all parasitic parameters, nonlinear C-V and I-V characteristics is first developed in [31]. The impacts of circuit parameters on positive crosstalk spikes are analyzed and the appropriate design guidelines are provided for crosstalk suppression. More or less, this model is relatively complex. In [32] and [33], the simplified analysis models of crosstalk spikes are established, and the complexity of crosstalk model is reduced by equating the controlled device to a slope power supply. Nevertheless, the dynamic transfer characteristics and V_{th} drift caused by SCE have not been fully concerned, which may cause inaccurate estimation of crosstalk peaks for SiC MOSFETs.

To solve these problems, an accurate predictive method of crosstalk peaks considering dynamic transfer characteristics and Miller ramp is proposed in this article. The main contributions are summarized as follows.

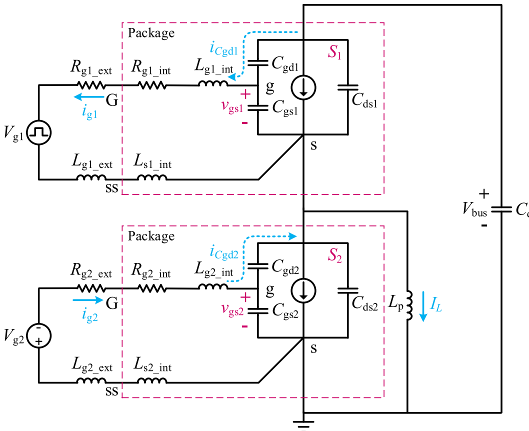


Fig. 1. Schematic diagram of DPT circuit with parasitic parameters.

1) The dynamic transfer characteristics are considered in the improved predictive method, which can achieve accurate prediction of positive and negative crosstalk peaks in a wide operating range.
2) For SiC MOSFETs, the impacts of V_{th} shift on crosstalk evaluation and suppression are analyzed, and the design suggestions for mitigating crosstalk are given.
3) An extracting method of Miller charge considering the load current is designed. In addition, the extracted Miller charge is used to compensate the error caused by Miller ramp, which further improves accuracy of the predictive results.

The rest of this article is organized as follows. Section II describes the crosstalk process and the conventional predictive method of crosstalk peaks. The limitations of conventional method are analyzed concretely. Then, an improved predictive method of crosstalk peaks is proposed in Section III. In Section IV, the experiment results are presented to verify the model and theoretical analysis. And the impacts of circuit parameters on positive and negative crosstalk peaks are discussed and the design suggestions are given. Finally, Section V concludes this article.

II. Conventional Predictive Method of Crosstalk Peak

In this article, the dual-pulse test (DPT) circuit with phase-leg configuration is adopted to analyze the crosstalk phenomenon, which includes the parasitic parameters, as shown in Fig. 1. Since the parasitic inductances of the drain and source are not concerned in this article, which is not illustrated in Fig. 1. The circuit parameters are shown as Table I, where the symbol $k =$ 1 or 2 represents different device. Internal parameters $L_{\mathrm{g}k_\mathrm{int}}$, $L_{\mathrm{s}k_\mathrm{int}}$, $R_{\mathrm{g}k_\mathrm{int}}$ represent the parameters of the device package, and external parameters $L_{\mathrm{g}k_\mathrm{ext}}$, $R_{\mathrm{g}k_\mathrm{ext}}$ are the parameters of print circuit board (PCB) component. In Fig. 1, the upper device S_1 is set in the ON/OFF state and the lower device S_2 keeps OFF, so that the crosstalk spikes of S_2 caused by the switching behavior of S_1 can be observed.

TABLE I
DEFINITIONS OF PARAMETERS IN DPT CIRCUIT

Parameters	Description
L_p	Load inductance
L_{gk_int}	Gate internal inductance
L_{sk_int}	Source internal inductance
L_{gk_ext}	Gate external inductance
R_{gk_int}	Gate internal resistance
R_{gk_ext}	Gate external resistance
C_{dsk}	Drain-source capacitance
C_{gsk}	Gate-source capacitance
C_{gdk}	Gate-drain capacitance
C_d	Decoupling capacitance
i_{gk}	Gate current of S_k
i_{Cgdk}	Miller current of S_k
v_{gsk}	Voltage of gate-source capacitors
v_{dsk}	Voltage of drain-source capacitors
V_{gdk}	Voltage of gate-drain capacitors
V_{gp}	Positive gate supply
V_{gn}	Negative gate supply
V_{bus}	DC-bus voltage

Remarks: "k" denotes different device (k = 1 for upper device S_1 and k = 2 for lower device S_2).

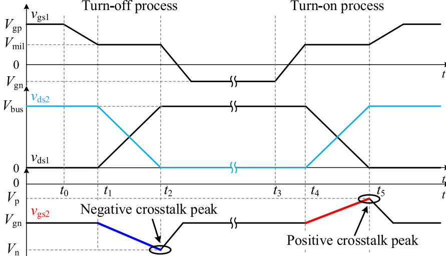


Fig. 2. Ideal switching trajectory of SiC MOSFETs.

A. Analysis of Crosstalk Process

In order to establish an accurate crosstalk model, it is important to analyze the crosstalk processes and critical parameters. As shown in Fig. 2, when the driver voltage V_{g1} changes from high to low at t_0, S_1 is turned OFF and its input capacitance C_{iss1} starts to discharge, which causes the gate-source voltage v_{gs1} to decrease rapidly. At t_1, v_{gs1} reaches the Miller voltage V_{mil} and the drain-source voltage v_{ds1} of S_1 will increase rapidly. Since the dc-bus voltage V_{bus} is fixed, the drain-source voltage v_{ds2} of S_2 decreases rapidly. At the same time, the Miller current i_{Cgd2} flows through the gate loop of S_2, which results in the gate-source voltage v_{gs2} to be pulled down. And the negative crosstalk spike is generated [see blue line in Fig. 2]. From Fig. 2, the crosstalk can be regarded as occurring when S_1 enters Miller stage and reaching a negative peak V_n at the end of Miller stage. As shown in Fig. 2, the turn-ON process of S_1 is similar to the above analysis. And the positive crosstalk spike is generated at t_4 and reaches the peak V_p at t_5 [see red line in Fig. 2]. Since the crosstalk occurs during the Miller stage of S_1 and is caused by the charging or discharging of C_{gd2}, the crosstalk peaks mainly depend on the duration time T_{mil} of Miller stage and the Miller charge Q_{gd2} of C_{gd2}.

Because of the low negative gate voltage tolerance for SiC MOSFETs, the sufficiently low negative crosstalk peak V_n may

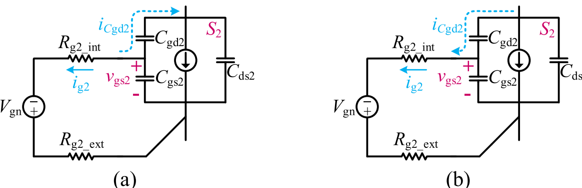


Fig. 3. Equivalent circuits of SiC MOSFETs when crosstalk occurs in [20] and [23]. (a) Negative crosstalk stage. (b) Positive crosstalk stage.

permanently damage the devices. Moreover, the threshold voltage of SiC MOSFETs is lower than that of Si devices, which indicates that a high enough V_p will falsely turn the devices ON. Therefore, the crosstalk spikes seriously reduce the reliability of the systems, and it is necessary to accurately predict the crosstalk peaks and provide theoretical guidance for crosstalk evaluation and suppression.

B. Conventional Predictive Method of Crosstalk Peaks

In the conventional method, the equivalent circuits that neglect packaging parameters of SiC MOSFETs are used to establish the crosstalk model, as shown in Fig. 3.

From Fig. 3(a) and (b), the equivalent circuits of positive and negative crosstalk are same, which means that the crosstalk peaks can be expressed by the identical differential equation. Thereby, the gate loop of S_2 satisfies (1) during the switching processes of S_1

$$V_{gn} = -R_{g2}\left(C_{gd2}\frac{dv_{gd2}}{dt} + C_{gs2}\frac{dv_{gs2}}{dt}\right) + v_{gs2} \quad (1)$$

where R_{g2} is the sum of R_{g2_ext} and R_{g2_int}. And according to Kirchhoff's law, the relationship between v_{gs2} and v_{ds2} is shown as

$$v_{gs2} = v_{gd2} + v_{ds2}. \quad (2)$$

The input capacitance of SiC MOSFETs composed of C_{gs} and C_{gd} is shown as

$$C_{iss} = C_{gd} + C_{gs}. \quad (3)$$

According to (2) and (3), (1) can be rewritten as

$$\frac{dv_{gs2}}{dt} = \frac{C_{gd2}}{C_{iss}}\frac{dv_{ds2}}{dt} + \frac{V_{gn} - v_{gs2}}{R_{g2}C_{iss}}. \quad (4)$$

In [23], Miller plateau is considered as constant. During the Miller stage, the average gate current of S_1 can be calculated as (5) by Kirchhoff's law

$$\begin{cases} I_{Mg1_on} = \frac{V_{gp}-V_{mil}}{R_{g1}} \\ I_{Mg1_off} = \frac{V_{gn}-V_{mil}}{R_{g1}}. \end{cases} \quad (5)$$

In the switching processes, the Miller voltage can be expressed as [23]

$$V_{mil} = V_{th} + \frac{I_L}{g_m} \quad (6)$$

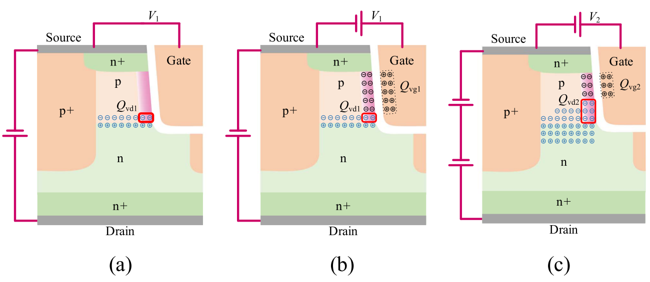


Fig. 4. Impacts of drain bias on SiC MOSFETs. (a) Low drain bias without gate bias. (b) Low drain bias with gate bias. (c) High drain bias with gate bias.

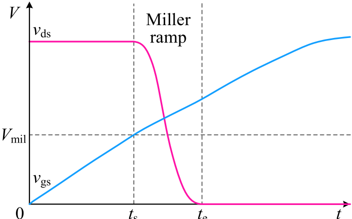


Fig. 5. Ideal turn-ON trajectory of SiC MOSFETs.

where I_{L} is the load current. And g_{m} is the transconductance of SiC MOSFETs, which is described as

$$g_{\mathrm{m}} = \sqrt[k_2]{\frac{k_1 I_{\mathrm{L}}^{k_2}}{I_{\mathrm{L}}}} \tag{7}$$

where k_1 and k_2 are coefficients, which can be acquired by the curve fitting from the datasheet [26]. Substituting (6) and (7) into (5), $I_{\mathrm{Mg1_ON}}$ and $I_{\mathrm{Mg1_OFF}}$ can be solved. Furthermore, the average slope of v_{ds2} is expressed as [23]

$$\frac{dv_{\mathrm{ds2}}}{dt} \approx -\frac{dv_{\mathrm{ds1}}}{dt} = \frac{I_{\mathrm{Mg1}}}{C_{\mathrm{gd1}}}. \tag{8}$$

According to Fig. 2, the T_{mil} is shown as [23]

$$\begin{cases} T_{\mathrm{mil_on}} = \frac{C_{\mathrm{gd1}} V_{\mathrm{bus}}}{I_{\mathrm{Mg1_on}}} \\ T_{\mathrm{mil_off}} = -\frac{C_{\mathrm{gd1}} V_{\mathrm{bus}}}{I_{\mathrm{Mg1_off}}}. \end{cases} \tag{9}$$

At this point, taking V_{gn} as the initial condition of the differential equation and T_{mil} as the duration time of crosstalk, the positive and negative crosstalk peaks in conventional method can be calculated as follows:

$$V_{\mathrm{gs2_peak}} = V_{\mathrm{gn}} + \frac{R_{\mathrm{g2}} C_{\mathrm{gd2}} I_{\mathrm{Mg1}}}{C_{\mathrm{gd1}}} \left(1 - e^{-\frac{T_{\mathrm{mil}}}{R_{\mathrm{g2}} C_{\mathrm{iss}}}}\right). \tag{10}$$

C. Influences of Dynamic Transfer Characteristics, Miller Ramp, and Packaging Parameters

In the conventional method, the crosstalk peaks can be obtained through Section II-B. However, due to neglecting the dynamic transfer characteristics, Miller ramp and packaging parameters, the error of conventional method is large, and the accuracy cannot satisfy the requirements. To develop an accurate predictive model of crosstalk peaks, the influences of dynamic transfer characteristics, Miller ramp, and packaging parameters are analyzed as follows.

1) Influence of Dynamic Transfer Characteristics: The trench SiC MOSFETs (IMZ120R060M1H) is used to study dynamic transfer characteristics caused by SCE in this article. The cell structure of this device is shown in Fig. 4. In Fig. 4(a), some negative charges Q_{vd1} are attracted to the reddish region by the drain stress. As shown in Fig. 4(b), once the gate bias V_1 is applied, the negative charges Q_{vg1} are attracted from the p region to the reddish region, and then the channel is formed in the reddish region by the charges Q_{vd1} and Q_{vg1}. In Fig. 4(c), if a higher drain bias is applied, more negative charges Q_{vd2} will be attracted to the reddish region by the drain stress. Once the gate bias V_2 is applied, the charges attracted by gate and drain stress will form a channel in reddish region, similarly. It is clear that Q_{vg2} are less than Q_{vg1} when a high drain bias is applied. Supposing V_1 and V_2 is the gate voltage that can just turn ON the device, i.e., threshold voltage, Q_{vg1} and Q_{vg2} can be represented by

$$Q_{\mathrm{vg}i(i=1,2)} = C_{\mathrm{iss}} V_i. \tag{11}$$

By (11), $V_1 > V_2$ can be deduced. Therefore, V_{th} will lower at higher drain bias for SiC MOSFETs. The similar phenomenon of threshold voltage shift has been demonstrated in [34] and [35]. In the initial Miller stage of the turn-ON process, V_{th} of SiC MOSFETs is low due to the high drain bias. During turn-ON process, the charges attracted by the drain bias are gradually released as v_{ds} decreases, which means that V_{th} will increase dynamically. Meanwhile, g_{m} will decrease dynamically [29]. The increase of V_{th} and the decrease of g_{m} will lead the transfer characteristics shift to the right. From (6), the SCE also causes the Miller voltage V_{mil} to raise gradually during turn-ON process, which is called Miller ramp, as shown in Fig. 5. In the Miller stage of the turn-OFF process, the decrease of V_{th} and the increase of g_{m} will lead the transfer characteristics dynamically shift to the left. The mechanism is similar to the turn-ON process and will not be repeated here.

In conventional method, V_{th} is obtained directly from the datasheet. And the coefficients k_1 and k_2 of g_{m} are also acquired by the curve fitting of transfer characteristics from the datasheet. However, the transfer characteristics and V_{th} in the datasheet are obtained under the drain-source voltage $v_{\mathrm{ds}} = 20$ V. When v_{ds} is much higher than 20 V, the transfer characteristics and V_{th} will change greatly. At this time, using the parameters obtained from the datasheet to solve (6) and (7) will cause significant error. Therefore, to accurately predict the crosstalk peaks of SiC MOSFETs, the dynamic transfer characteristics require to be considered.

2) Influence of Miller Ramp: In conventional model, (8) is used to solve T_{mil}, and its essence is to calculate the Miller charge Q_{gd1} of S_1. By integrating both sides of (8), Q_{gd1} can be expressed as (12) in conventional model

$$Q_{\mathrm{gd1}} = C_{\mathrm{gd1}} V_{\mathrm{bus}}. \tag{12}$$

In [23], C_{gd1} is established as a piecewise model to obtain Q_{gd1} accurately, and the piecewise model of C_{gd1} is obtained

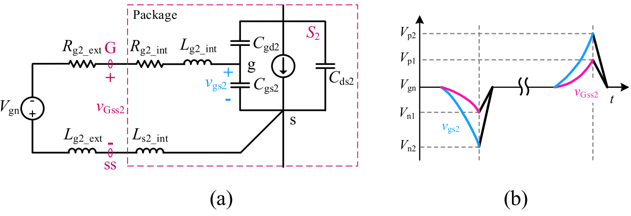


Fig. 6. (a) Equivalent circuit diagram of gate loop. (b) Comparison of v_{gs2} and v_{Gss2}.

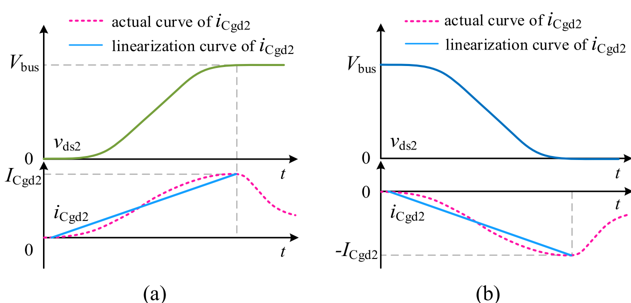


Fig. 7. Variation trends of Miller current with v_{ds2}. (a) When v_{ds2} increases. (b) When v_{ds2} decreases.

through the C-V curve in the datasheet. But the C-V characteristics of SiC MOSFETs will also change dynamically during the switching processes [30]. As a result, Q_{gd1} is inaccurate in conventional method. Furthermore, since the Miller plateau is considered to be constant, Q_{gd1} is the total gate charge at Miller stage. Based on this, substituting (12) into (9), the duration time of Miller stage can be rewritten as

$$\begin{cases} T_{mil_on} = \frac{Q_{gd1}}{I_{Mg1_on}} \\ T_{mil_off} = -\frac{Q_{gd1}}{I_{Mg1_off}}. \end{cases} \tag{13}$$

From the previous analysis, it can be seen that the dynamic transfer characteristics of SiC MOSFETs lead Miller ramp to replace Miller plateau. So, the change of v_{gs} results in the charging or discharging of C_{gs1}, and Q_{gs1} is generated in Miller stage. The total gate charge Q_{g1} in Miller stage can be expressed as

$$Q_{g1} = Q_{gs1} + Q_{gd1}. \tag{14}$$

For SiC MOSFETs, C_{gs} is much larger than C_{gd}, which means that the neglected Q_{gs1} in (13) will cause an inaccurate estimation of T_{mil}. Accordingly, the error of predictive results will be further amplified.

3) Influence of Packaging Parameters: In conventional model, the amplitudes of v_{gs2} are solved as crosstalk peaks by (10). However, depending on the high switching speeds of SiC MOSFETs, the voltage drop across the packaging parameters such as R_{g2_int}, L_{g2_int}, and L_{s2_int} cannot be ignored, which means that the amplitudes of v_{Gss2} and v_{gs2} are different, as shown in Fig. 6. According to Fig. 6(b), v_{Gss2} is smaller than v_{gs2}, and the relationship between them is nonlinear because of the parasitic inductance of the gate loop.

Moreover, since the threshold voltage for judging the switching behavior of SiC MOSFETs is determined in the presence of packaging parameters, it is illogical to calculate the amplitudes of v_{gs2} as crosstalk peaks in conventional model.

D. Limitations of Conventional Predictive Method

As described above, the several inherent limitations of conventional method are summarized and illustrated as follows.

1) The operating range of SiC MOSFETs is much wider than datasheets. However, the conventional method uses the transfer characteristics and C-V curve provided by datasheets in limited test conditions, which will lead to the wrong estimation of T_{mil}.
2) Because Miller ramp is considered as Miller plateau, the deviation of T_{mil} further increases and leads to unacceptable predictive results of crosstalk peaks.
3) Since the packaging parameters of SiC MOSFETs are neglected, the crosstalk peaks predicted by the conventional model are different from that considering the packaging parameters, which may cause the inaccurate crosstalk evaluation.

III. Proposed Predictive Method of Crosstalk Peaks

As mentioned above, the conventional predictive method has inherent limitations, which leads to an inaccurate predictive results. Aiming at the limitations of conventional method, an improved predictive method considering dynamic transfer characteristics and Miller ramp is proposed in this section. The principle of proposed method is sufficiently analyzed as follows.

A. Improved Predictive Model of Crosstalk Peaks

The Miller ramp is neglected in the conventional model, causing the incorrect estimation of T_{mil}. In the proposed model, the total gate charge is adopted to calculate T_{mil}, which can compensate the error caused by Miller ramp. Furthermore, the duration time T_{mil} of Miller stage can be expressed as follows:

$$\begin{cases} T_{mil_on} = \frac{Q_{g1}}{I_{Mg1_on}} \\ T_{mil_off} = -\frac{Q_{g1}}{I_{Mg1_off}} \end{cases} \tag{15}$$

where Q_{g1} is the total gate charge in Miller stage, which can be acquired in Section III-C. From (15), the average Miller current I_{Cgd2} of S_2 can be expressed as

$$\begin{cases} I_{Cgd2_on} = \frac{Q_{gd2}}{T_{mil_on}} \\ I_{Cgd2_off} = -\frac{Q_{gd2}}{T_{mil_off}} \end{cases} \tag{16}$$

where Q_{gd2} is the Miller charge of S_2, which can be obtained in Section III-C.

As shown in Fig. 7, the actual Miller current i_{Cgd2} is affected by parasitic parameters of gate loop and dv_{ds2}/dt, showing a ramp characteristic. To simplify the calculation, i_{Cgd2} is linearized to the ramp current in Fig. 7(a) and (b), and the slope of

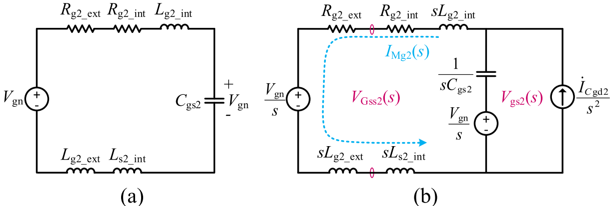


Fig. 8. Equivalent circuit diagram of the gate loop of S_2 at different stages. (a) Steady stage. (b) Crosstalk stage.

i_{Cgd2} can be expressed as

$$\begin{cases} \dot{I}_{\mathrm{Cgd2_on}} = \frac{2Q_{\mathrm{gd2}}}{T^2_{\mathrm{mil_on}}} \\ \dot{I}_{\mathrm{Cgd2_off}} = -\frac{2Q_{\mathrm{gd2}}}{T^2_{\mathrm{mil_off}}}. \end{cases} \tag{17}$$

According to the above analysis, the Miller capacitance C_{gd2} is equivalent to a ramp current source when crosstalk occurs. Furthermore, an improved model considering packaging parameters is built, and its equivalent circuit diagram is shown in Fig. 8(b). In Fig. 8(a), the gate loop of S_2 has reached steady state before crosstalk occurs. Once crosstalk occurs, the Miller capacitance C_{gd2} is equivalent to a ramp current source and excites the gate loop. Then, the crosstalk spikes can be considered as the response of the gate loop to the ramp current, which can be obtained by solving the complex frequency domain circuit in Fig. 8(b).

In Fig. 8(b), $V_{\mathrm{Gss2}}(s)$ and $V_{\mathrm{gs2}}(s)$ are different voltage due to the packaging parameters of SiC MOSFETs. It is unreasonable to use the predictive results of $V_{\mathrm{gs2}}(s)$ to evaluate the crosstalk level of the selected circuit parameters. To solve this problem, the voltage $V_{\mathrm{Gss2}}(s)$ is adopted as crosstalk voltage in this article, which can provide more accurate guidance for crosstalk suppression. Applying Kirchhoff's laws to the circuit in Fig. 8(b), the Miller current of S_2 can be derived as

$$I_{\mathrm{Mg2}}(s) = \frac{\dot{I}_{\mathrm{Cgd2}}}{(C_{\mathrm{gs2}}L_{\mathrm{g2}}s^2 + C_{\mathrm{gs2}}R_{\mathrm{g2}}s + 1)s^2} \tag{18}$$

where

$$L_{\mathrm{g2}} = L_{\mathrm{g2_ext}} + L_{\mathrm{g2_int}} + L_{\mathrm{s2_int}}. \tag{19}$$

Then, the crosstalk voltage $V_{\mathrm{Gss2}}(s)$ can be expressed as

$$V_{\mathrm{Gss2}}(s) = \frac{V_{\mathrm{gn}}}{s} + \frac{\dot{I}_{\mathrm{Cgd2}}(L_{\mathrm{g2_ext}}s + R_{\mathrm{g2_ext}})}{(C_{\mathrm{gs2}}L_{\mathrm{g2}}s^2 + C_{\mathrm{gs2}}R_{\mathrm{g2}}s + 1)s^2}. \tag{20}$$

The time-domain expression of $V_{\mathrm{Gss2}}(s)$ can be obtained by Laplace inverse transformation for (20) to investigate the crosstalk peaks, which is shown as (A1) in the Appendix. At this point, using V_{gn} as the initial condition, the crosstalk peaks can be solved by substituting (15) and (17) into (A1). The executing steps of the proposed method are shown in Fig. 9.

B. Measuring Method of Dynamic Transfer Characteristics

To achieve accurate prediction of crosstalk peaks, the dynamic transfer characteristics are considered in the proposed crosstalk model. As shown in Fig. 10(a), a simple method to obtain the actual transfer characteristics at different v_{ds} is proposed in [30]. In Fig. 10(a), a SiC MOSFET is connected in parallel with the dc supply and a coaxial shunt R_{shunt} is used to measure drain-source current i_{ds}. A narrow pulse about 1 μs is applied to the MOSFET to mitigate the harmful effect of self-heating, as shown in Fig. 10(b). Once v_{Gss} and i_{ds} reach steady state, the values of v_{Gss} and i_{ds} are recorded. Keeping the positive gate supply V_{gp} unchanged, the drain-source current I_{ds1} and I_{ds2} at different v_{ds} can be obtained.

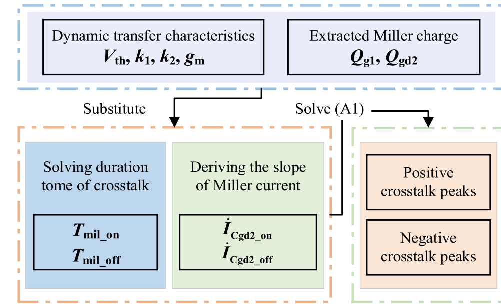


Fig. 9. Executing steps to predict the crosstalk peaks.

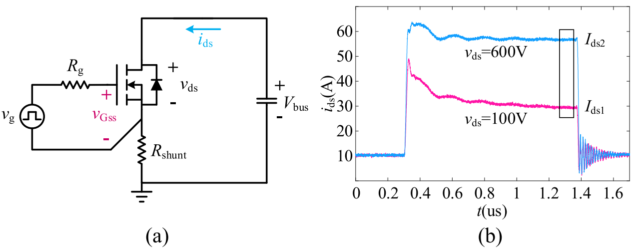


Fig. 10. (a) Extracting circuit of dynamic transfer characteristics. (b) Experimentally measured i_{ds} at $v_{\mathrm{Gss}} = 7.5$ V.

The channel current is usually expressed as

$$i_{\mathrm{ch}} = k_1(v_{\mathrm{Gss}} - V_{\mathrm{th}})^{k_2} \tag{21}$$

where k_1 and k_2 are same coefficients in (7). Then, configuring multiple V_{gp} and v_{ds}, k_1 and k_2 can be obtained by curve fitting of (21), accordingly. Besides, substituting the k_1 and k_2 into (6) and (7), V_{mil} and g_{m} at specific v_{ds} can be obtained.

C. Extracting Method of Miller Charge

In this subsection, an extracting method of Miller charge is designed to compensate the error caused by Miller ramp. A circuit prototype is proposed to extract Miller charge Q_{gd} in [30]. However, since the resistive load and single-pulse testing conditions, this method neglects the influence of load current on Q_{gd}, which could result in incorrect extracting results. Therefore, an improved method for Miller charge is designed considering the load current, as shown in Fig. 11. In Fig. 11, S_{b} is SiC MOSFET and D_{a} is freewheeling diode. To minimize the impact of parasitic parameters, $R_{\mathrm{g_ON}}$ is chosen as 620 Ω, which means that the turn-ON speed of SiC MOSFET is slow. And di_{g}/dt is so small that the induced voltage on the parasitic inductance is far less than v_{Gss} and can be ignored. Meanwhile, because $R_{\mathrm{g_on}}$ is

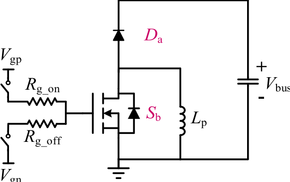


Fig. 11. Extracting circuit of Miller charge.

much larger than $R_{\mathrm{g_int}}$, the voltage drop across $R_{\mathrm{g_int}}$ can also be neglected. Furthermore, the measured v_{Gss} can be considered as the actual gate-source voltage. Besides, $R_{\mathrm{g_OFF}}$ is set as 15 Ω to get a high turn-OFF speed, thereby the load inductance L_{p} can provide initial current for next turn-ON process. The Miller charge can be obtained in the second turn-ON process.

In the Miller stage, Q_{gs} can be expressed as

$$Q_{\mathrm{gs}} = C_{\mathrm{gs}} \Delta V_{\mathrm{gs}} \tag{22}$$

where ΔV_{gs} is the variation of v_{gs} during the Miller stage. In the turn-ON process, the Miller current can be expressed as

$$i_{\mathrm{Mg}} = \frac{V_{\mathrm{gp}} - v_{\mathrm{Gss}}}{R_{\mathrm{g_on}}}. \tag{23}$$

In addition, the total charge in the Miller stage can be expressed as

$$Q_{\mathrm{g}} = \int i_{\mathrm{Mg}} dt. \tag{24}$$

Substituting (22) and (24) into (14), the gate charge Q_{g1} and Miller charge Q_{gd2} can be solved.

D. Comparison With Conventional Predictive Method of Crosstalk Peaks

The differences between the conventional method and the proposed method are summarized as follows.

1) In conventional method, the amplitude of v_{gs2} is solved as crosstalk peak, which is inaccurate for crosstalk evaluation. Instead, the amplitude of v_{Gss2} is solved as crosstalk peak in proposed model, considering the packaging parameters. Therefore, the proposed method is accurate and can guide crosstalk suppression much effectively.
2) The conventional model neglects the dynamic transfer characteristics of SiC MOSFETs. On the contrary, since considering the dynamic transfer characteristics, the proposed method can obtain accurate predictive results of crosstalk peaks in wide operating range.
3) The Miller ramp is considered in proposed method, and the total gate charge during the Miller stage is applied, thus, the error caused by Miller ramp can be compensated.

IV. Experimental Verification and Discussion

A. Measurement of Dynamic Transfer Characteristics

The transfer characteristics curves measured experimentally at various v_{ds} are shown in Fig. 12, and the corresponding parameters are obtained at $I_{\mathrm{L}} = 30$ A, as shown in Table II.

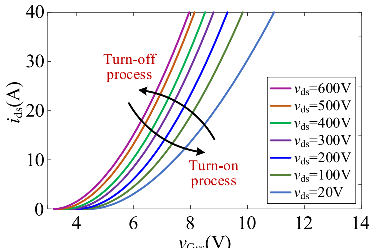


Fig. 12. Transfer characteristics curves measured experimentally at various v_{ds} (20–600 V).

TABLE II
PARAMETERS OF TRANSFER CHARACTERISTICS CURVES AT DIFFERENT DRAIN-SOURCE VOLTAGE

v_{ds}/V	100	200	300	400	500	600
k_1	1.5046	1.6214	1.9665	1.9985	2.3047	2.3029
k_2	1.9017	1.9273	1.8745	1.8874	1.8376	1.8354
g_{m}/S	6.2184	6.6009	7.0112	7.1420	7.3237	7.4081

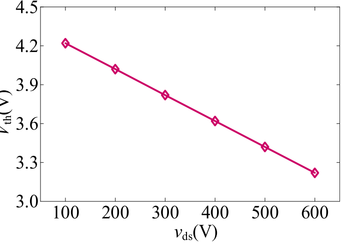


Fig. 13. Measured variation trend of V_{th} with v_{ds}.

In Fig. 12, the transfer characteristics curves gradually shift to the right as v_{ds} decreases, which closely aligns with the previous theoretical analysis.

Note that, there may still be a leakage current flowing through the source of SiC MOSFETs, even if a negative turn-OFF gate voltage is applied, which is called subthreshold current. At wide range of v_{ds}, obtaining V_{th} is challenging at $i_{\mathrm{ds}} = 0$ A. Therefore, a specific v_{Gss} at $i_{\mathrm{ds}} = 1$ A is chosen as the threshold voltage V_{th}. For example, using this method, $V_{\mathrm{th}} = 4.5$ V is obtained at $i_{\mathrm{ds}} = 1$ A and $v_{\mathrm{ds}} = 20$ V. In Fig. 13, it is illustrated that the measuring results of V_{th} vary with v_{ds}. With the increase of v_{ds}, V_{th} decreases almost linearly, which is similar to the mechanism of [34], [35].

B. Extraction of Miller Charge

In Fig. 14, the experimentally measured turn-ON trajectory is shown using the proposed method in Section III-C. It can be observed that v_{ds} starts to decrease rapidly at t_{s} and the slope of v_{Gss} slows down significantly at this point. This means that the device enters the Miller stage, and the specific v_{Gss} is considered as V_{mil} at this point. Compared to t_{s}, the ending time t_{e} of the Miller stage may hardly be observed because the slope of v_{Gss} is almost unchanged at this point. However, v_{ds} can be used as reference to determine the ending time of the Miller stage, i.e.,

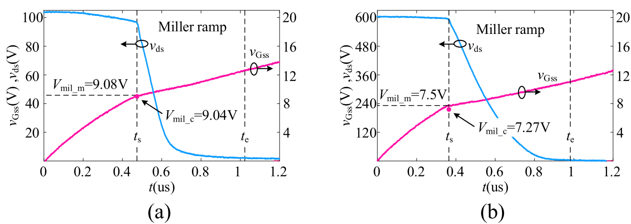


Fig. 14. Experimentally measured turn-ON trajectory of SiC MOSFETs at different v_{ds}. (a) When $v_{ds} = 100$ V. (b) When $v_{ds} = 600$ V.

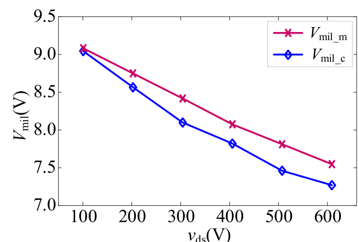
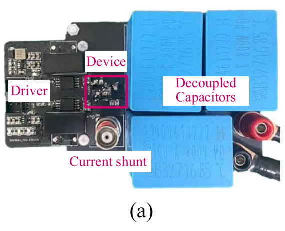
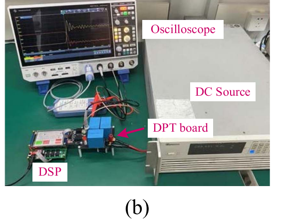


Fig. 15. Measured and calculated variation trends of V_{mil} with v_{ds}.

TABLE III
EXTRACTED RESULTS OF MILLER CHARGE AT $I_L = 30$ A

v_{ds}/V	100	200	300	400	500	600
Q_{g1}/nC	9.2190	9.7806	10.248	10.535	10.893	11.142
Q_{gd2}/nC	5.2131	5.8975	6.4076	6.8913	7.2065	7.5758





(a) (b)

Fig. 16. Experimental platform. (a) Details of DPT board. (b) Top view of the experimental platform.

TABLE IV
PARAMETERS OF EXPERIMENTAL PLATFORM

Parameter	Value	Parameter	Value
C_{gs1}/C_{gs2}	1060pF	R_{g1_ext}/R_{g2_ext}	15/20/25Ω
L_p	53uH	L_{g2_ext}	14.4nH
I_L	30A	L_{g1_int}/L_{g2_int}	12.5nH
V_{bus}	100-600V	L_{s1_int}/L_{s2_int}	5.8nH
V_{gp}/V_{gn}	20/-5.8V	R_{g1_int}/R_{g2_int}	6Ω

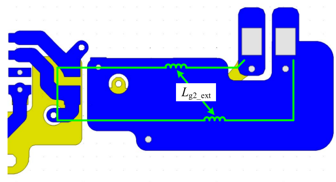
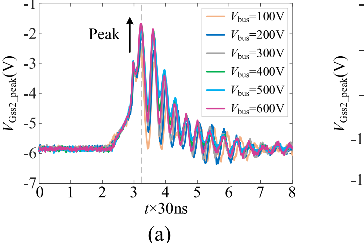


Fig. 17. Parasitic inductances extraction by Ansys Q3D.

TABLE V
INFORMATIONS OF MEASURING EQUIPMENT

Equipment	Name
SiC MOSFET	IMZ120R060M1H
Current shunt	SSDN-015 (1.2GHz)
Voltage probe	RT-ZP11 (700MHZ)
Isolated voltage probe	RT-ZHD15 (100MHz)
Oscilloscope	MXO44 (1GHz)



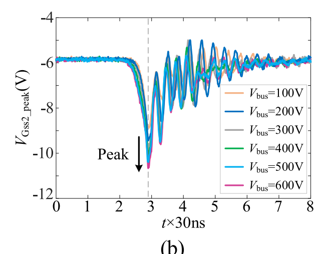


Fig. 18. Measured crosstalk spikes under various V_{bus} (100–600 V). (a) Positive crosstalk spikes at $R_{gk_ext} = 25\ \Omega$. (b) Negative crosstalk spikes at $R_{gk_ext} = 25\ \Omega$.

the Miller stage ends when v_{ds} reaches 0 V [36]. Then, ΔV_{gs} in (22) can be solved by using specific v_{Gss} at this point.

From Fig. 15, V_{mil_c} calculated by the parameters in Table II is closely to V_{mil_m} measured by experiments at different v_{ds}, which means that the measured results of dynamic transfer characteristics are accurate. Furthermore, the extracting results of Q_{g1} and Q_{gd2} using proposed method are shown in Table III.

C. Experimental Verification of Proposed Method

A DPT prototype is developed, as shown in Fig. 16. The parameters of DPT prototype are listed in Table IV, and the packaging parameters of the devices are obtained from the SPICE model [37] provided by the manufacturer. The PCB of the driver circuit is imported into the finite element simulation software, ANSYS. Parasitic inductance can be simulated by selecting appropriate current loop and excitation source. As shown in Fig. 17, the inductance L_{g2_ext} represents the sum of all parasitic inductances of the driver circuit. For SiC MOSFETs, the crosstalk processes are transient, and the crosstalk peaks may be only several volts. In this case, the actual crosstalk spikes may be attenuated or distorted due to the low bandwidth of the measuring equipment. The high bandwidth voltage probe and oscilloscope are essential to achieve accurate measurement of crosstalk spikes. Furthermore, to minimize the effect among different grounds of measuring probes, separate measurements should be performed for different signals whenever possible. In this article, to accurately measure the crosstalk peaks, the measuring equipment is shown in Table V.

The measured crosstalk spikes are shown in Fig. 18. It can be observed that the positive and negative crosstalk peaks increase along with V_{bus}, which is consistent with the changing trend of Q_{gd}. To verify the accuracy of the proposed method, the

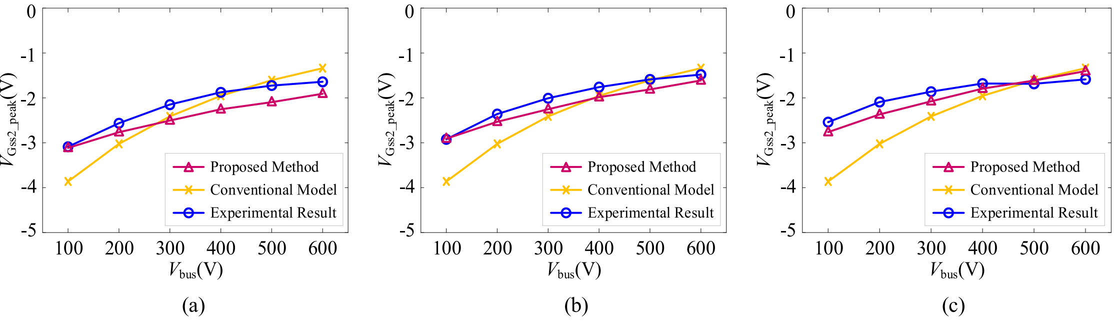


Fig. 19. Comparisons of the measured and predicted positive crosstalk peaks at different V_{bus} (100–600 V) and $R_{\text{g}k_\text{ext}}$ (15—25 Ω). (a) $R_{\text{g1_ext}} = R_{\text{g2_ext}} = 15$ Ω. (b) $R_{\text{g1_ext}} = R_{\text{g2_ext}} = 20$ Ω. (c) $R_{\text{g1_ext}} = R_{\text{g2_ext}} = 25$ Ω.

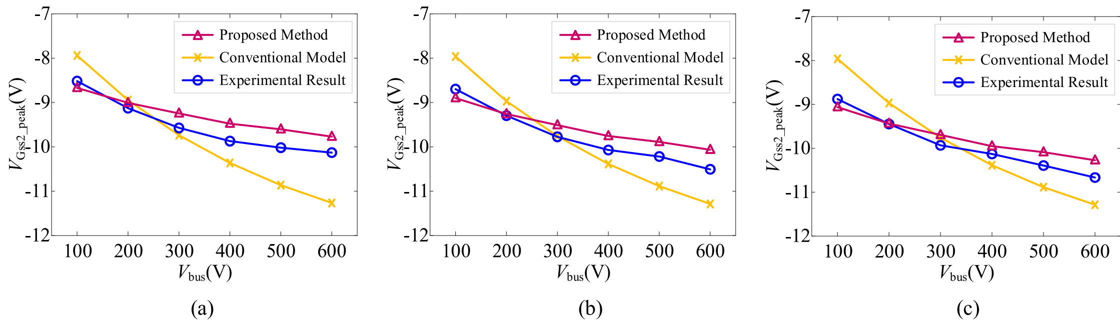


Fig. 20. Comparisons of the measured and predicted negative crosstalk peaks at different V_{bus} (100–600 V) and $R_{\text{g}k_\text{ext}}$ (15–25 Ω). (a) $R_{\text{g1_ext}} = R_{\text{g2_ext}} = 15$ Ω. (b) $R_{\text{g1_ext}} = R_{\text{g2_ext}} = 20$ Ω. (c) $R_{\text{g1_ext}} = R_{\text{g2_ext}} = 25$ Ω.

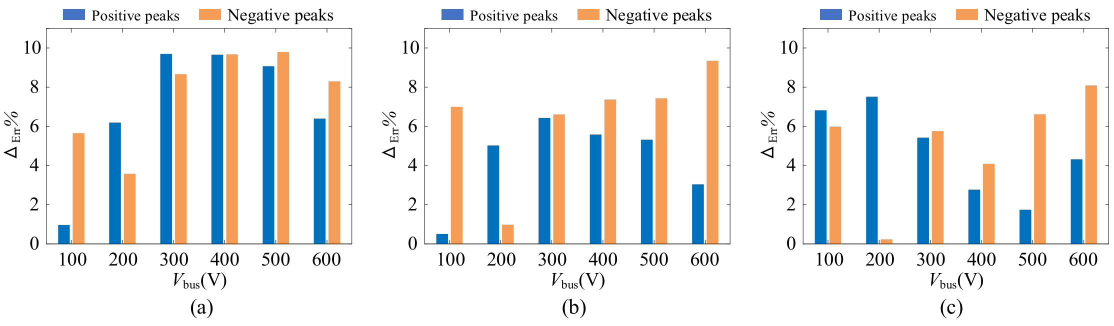


Fig. 21. Relative errors of the proposed method at different V_{bus} (100–600 V) and $R_{\text{g}k_\text{ext}}$ (15–25 Ω). (a) $R_{\text{g1_ext}} = R_{\text{g2_ext}} = 15$ Ω. (b) $R_{\text{g1_ext}} = R_{\text{g2_ext}} = 20$ Ω. (c) $R_{\text{g1_ext}} = R_{\text{g2_ext}} = 25$ Ω.

comprehensive comparisons among the conventional method, the proposed method and the experimental results are shown in Figs. 19 and 20. The results demonstrate that the predicted crosstalk peaks by the proposed method are more consistent with the experimentally measured results, compared with the conventional method.

The relative error is used to further evaluate the accuracy of proposed method, which is expressed as

$$\Delta_{\text{Err}}\% = 100\% \times \left| \frac{x_{\text{p}} - x_{\text{m}}}{x_{\text{m}} - V_{\text{gn}}} \right| \quad (25)$$

where x_{p} represents the predicted crosstalk peaks, and x_{m} represents the measured crosstalk peaks. It should be noted that the negative turn-OFF gate voltage V_{gn} is applied to prevent false turn-ON problem. Therefore, V_{gn} needs to be eliminated to ensure the fairness of (25).

The relative errors of the proposed method are illustrated in Fig. 21. It is obvious that the relative errors are satisfactory, and all are below 10%. Therefore, the proposed method can achieve accurate prediction of crosstalk peaks for SiC MOSFETs.

Predicting crosstalk peaks for other SiC MOSFETs with Kelvin package, the specific parameters should be updated to solve the (A1), and the dynamic transfer characteristics and Miller

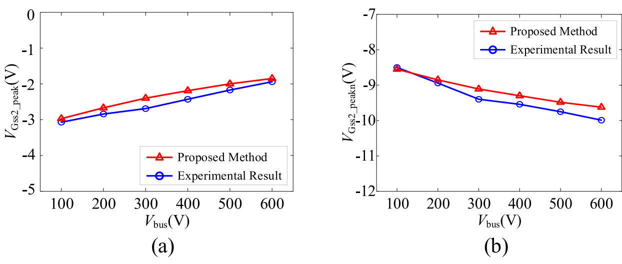


Fig. 22. Measured and predicted crosstalk peaks at $R_{gk_ext} = 20\ \Omega$ and different V_{bus} (100–600 V). (a) Positive crosstalk peaks of device B. (b) Negative crosstalk peaks of device B.

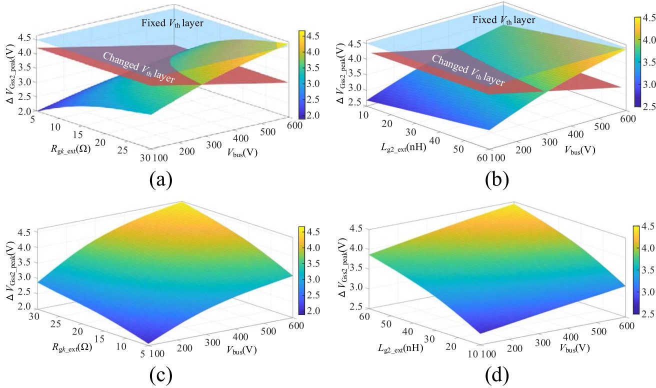


Fig. 23. Impacts of different circuit parameters on crosstalk peaks. (a) Impacts of R_{gk_ext} on positive crosstalk ($L_{g2_ext} = 14.4$ nH). (b) Impacts of L_{g2_ext} on positive crosstalk ($R_{gk_ext} = 15\ \Omega$). (c) Impacts of R_{gk_ext} on negative crosstalk ($L_{g2_ext} = 14.4$ nH). (d) Impacts of L_{g2_ext} on negative crosstalk ($R_{gk_ext} = 15\ \Omega$).

charge are necessary to be extracted, simultaneously. The executing steps in Fig. 9 are still appropriate. As a result, another 1.2 kV/40 mΩ SiC MOSFET with Kelvin package (device B, IMZA120R040M1H) is also tested with the same processes, which has different packaging parameters. The experimentally measured and predicted crosstalk peaks are shown in Fig. 22. It can be observed that the proposed method has also accurate predicted results for device B.

D. Impacts of Circuit Parameters on Crosstalk Peaks and Design Suggestions

The negative crosstalk peaks slightly exceeding the SOA will not cause devices damage, but continuous undershoots may potentially shorten the lifetime of the devices. Especially, negative crosstalk spikes and high drain bias may lead to the downward shift of V_{th}, which makes SiC MOSFETs more likely to be falsely turned ON. In this case, the threat of crosstalk spikes should be re-evaluated. In this section, the impacts of circuit parameters on positive and negative crosstalk peaks are discussed, which is meaningful for driving circuit design and crosstalk suppression.

Based on the proposed predictive model, the impacts of different circuit parameters on crosstalk peaks are shown in Fig. 23. And the impacts of the negative turn-OFF gate voltage on negative crosstalk peaks are shown in Fig. 24. In Figs. 23 and 24, V_{Gss2_peakn} refer to the negative crosstalk peaks, and ΔV_{Gss2_peak} are defined as $|V_{Gss2_peak}\text{-}V_{gn}|$. From Fig. 23, the larger R_{gk_ext} and L_{g2_ext} will lead to the higher crosstalk peaks, especially at higher V_{bus}. Therefore, the smaller R_{gk_ext} and L_{g2_ext} are effective to reduce the crosstalk peaks, but it still has limitations. As shown in Fig. 23(a) and (b), when a fixed $V_{th} = 4.5$ V [26] is employed, many circuit parameters are appropriate without considering the SCE. However, under the SCE, V_{th} will decrease as V_{bus} increases, thus the original appropriate circuit parameters may have potential risks. As shown in Fig. 23, the downward shift of V_{th} limits the selection margins of circuit parameters. Setting negative turn-OFF gate voltage not only accelerates the turn-OFF process speeds and reduces losses but also lowers the basis of positive crosstalk spikes. As a result, the selection margins of R_{gk_ext} and L_{g2_ext} can be effectively extended. Nevertheless, the basis of negative crosstalk spikes is also lowered. As shown in Fig. 24, the larger negative turn-OFF gate voltage will induce the higher negative crosstalk peaks and exceed the negative gate voltage limitation of SiC MOSFETs. According to Figs. 23 and 24, considering the SCE is beneficial to accurately select the optimal circuit parameters and negative turn-OFF gate voltage, making the devices operate in the recommended SOA.

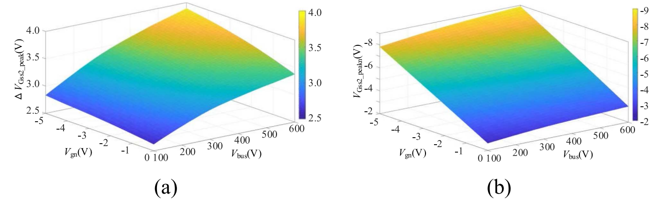


Fig. 24. Impacts of negative gate voltage bias on negative crosstalk at $R_{gk_ext} = 15\ \Omega$ and $L_{g2_ext} = 14.4$ nH. (a) Impacts of negative gate voltage bias on ΔV_{Gss2_peak}. (b) Impacts of negative gate voltage bias on V_{Gss2_peakn}.

Furthermore, when SiC MOSFETs work in synchronous rectification, the high negative turn-OFF gate voltage will result in the larger forward voltage of body diode. Then, the losses of the body diode will increase in the deadtime. Paralleling SiC Schottky barrier diode can improve this problem, but it will introduce extra component cost. Hence, the forward voltage of the body diode should be considered when selecting negative turn-OFF gate voltage for SiC MOSFETs, especially in high frequency applications. Finally, considering the SCE, predicting the positive and negative crosstalk peaks under the selected circuit parameters, and designing the optimal turn-OFF gate voltage bias, to ensure the excellent performance and reliable operation of SiC MOSFETs.

V. Conclusion

In this article, a predictive method of crosstalk peaks considering dynamic transfer characteristics and Miller ramp for SiC MOSFETs is proposed. First, to develop an accurate predictive model of crosstalk peaks, the limitations of conventional method are analyzed in detail. Then, both dynamic transfer characteristics and Miller ramp of devices are considered to

improve predictive accuracy in the proposed model. And the extracting methods of the dynamic transfer characteristics and Miller charge are discussed. Finally, the experimental results demonstrate that proposed predictive method is effective and accurate for crosstalk peaks of SiC MOSFETs with Kelvin package. Moreover, the impacts of SCE on crosstalk evaluation and suppression are analyzed, providing a reliable and practical reference for driving parameters design. The conclusions are summarized as follows.

1) The proposed method can get accurate predictive results of crosstalk peaks in a wide operating range, and the relative errors are less than 10%.
2) The analysis result indicates that the downward shift of V_{th} increases the risk of false turn-ON and reduces the selection ranges of driving parameters, and this issue will be more serious at high drain bias.
3) The SCE of SiC MOSFETs is considered in this article, so the design suggestions can accurately guide the selection of driving circuit parameters and negative turn-OFF gate voltage to mitigate the false turn-ON problem, without exceeding the negative gate voltage limit.

Furthermore, the proposed crosstalk model is mainly applicable to the SiC MOSFETs with Kelvin package, and the temperature is not considered. Hence, the crosstalk model with more parameters and wider applicability is the future work.

Appendix

By (20), the crosstalk peak of SiC MOSFETs is expressed as

$$\begin{aligned} V_{\mathrm{Gss2_peak}} = {} & V_{\mathrm{gn}} + \dot{I}_{\mathrm{Cgd2}}(-4L_{\mathrm{g2_ext}}^2 + C_{\mathrm{gs2}}R_{\mathrm{g2}}(R_{\mathrm{g2}}R_{\mathrm{g2_ext}}T_{\mathrm{mil}} \\ & + \mathrm{A}) + (\mathrm{A}_1\sqrt{\mathrm{B}_1}\sinh(\mathrm{C}T_{\mathrm{mil}}) + \mathrm{A}_2\sqrt{\mathrm{B}_2}\cosh \\ & (\mathrm{C}T_{\mathrm{mil}}))\exp(-R_{\mathrm{g2}}T_{\mathrm{mil}}/2L_{\mathrm{g2}}) - 4L_{\mathrm{g2_ext}} \\ & (R_{\mathrm{g2_ext}}T_{\mathrm{mil}} + L_{\mathrm{g2_int}} + L_{\mathrm{s2_int}}) - R_{\mathrm{g2_ext}}(C_{\mathrm{gs2}}^2 \\ & R_{\mathrm{g2}}^3 + 4(L_{\mathrm{g2_int}} + L_{\mathrm{s2_int}})T_{\mathrm{mil}}))/C_{\mathrm{gs2}}R_{\mathrm{g2_ext}}^2 \\ & + 2C_{\mathrm{gs2}}R_{\mathrm{g2_ext}}R_{\mathrm{g2_int}} + C_{\mathrm{gs2}}R_{\mathrm{g2_int}}^2 - 4L_{\mathrm{g2}} \end{aligned} \tag{A1}$$

where

$$\begin{aligned} \mathrm{A} = {} & 5L_{\mathrm{g2_ext}}R_{\mathrm{g2_ext}} + L_{\mathrm{g2_ext}}R_{\mathrm{g2_int}} + 4L_{\mathrm{g2_int}}R_{\mathrm{g2_ext}} \\ & + 4L_{\mathrm{s2_int}}R_{\mathrm{g2_ext}} \\ \mathrm{A}_1 = {} & C_{\mathrm{gs2}}R_{\mathrm{g2_ext}}^3 + 2C_{\mathrm{gs2}}R_{\mathrm{g2_ext}}^2R_{\mathrm{g2_int}} \\ & + C_{\mathrm{gs2}}R_{\mathrm{g2_ext}}R_{\mathrm{g2_int}}^2 \\ & - 3L_{\mathrm{g2_ext}}R_{\mathrm{g2_ext}} - L_{\mathrm{g2_ext}}R_{\mathrm{g2_int}} \\ & - 2L_{\mathrm{g2_int}}R_{\mathrm{g2_ext}} \\ & - 2L_{\mathrm{s2_int}}R_{\mathrm{g2_ext}} \\ \mathrm{A}_2 = {} & C_{\mathrm{gs2}}R_{\mathrm{g2_ext}}^2 + C_{\mathrm{gs2}}R_{\mathrm{g2_ext}}R_{\mathrm{g2_int}} - L_{\mathrm{g2_ext}} \\ \mathrm{B}_1 = {} & C_{\mathrm{gs2}}^2R_{\mathrm{g2_ext}}^2 + 2C_{\mathrm{gs2}}^2R_{\mathrm{g2_ext}}R_{\mathrm{g2_int}} + C_{\mathrm{gs2}}^2R_{\mathrm{g2_int}}^2 \\ & - 4C_{\mathrm{gs2}}L_{\mathrm{g2}} \\ \mathrm{B}_2 = {} & \mathrm{B}_1/C_{\mathrm{gs2}} \\ \mathrm{C} = {} & \mathrm{B}_1/2L_{\mathrm{g2}}C_{\mathrm{gs2}} \\ R_{\mathrm{g2}} = {} & R_{\mathrm{g2_ext}} + R_{\mathrm{g2_int}} \\ L_{\mathrm{g2}} = {} & L_{\mathrm{g2_ext}} + L_{\mathrm{g2_int}} + L_{\mathrm{s2_int}}. \end{aligned}$$

References

[1] J. W. Palmour, "Silicon carbide power device development for industrial markets," in *Proc. IEEE Int. Electron. Devices Meeting*, 2014, pp. 1.1.1–1.1.8.

[2] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[3] J. Millan, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[4] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.

[5] J. Noppakunkajorn, D. Han, and B. Sarlioglu, "Analysis of high-speed PCB with SiC devices by investigating turn-off overvoltage and interconnection inductance influence," *IEEE Trans. Transp. Electrific.*, vol. 1, no. 2, pp. 118–125, Aug. 2015.

[6] X. Chen, W. Chen, X. Yang, Y. Ren, and L. Qiao, "Common-mode EMI mathematical modeling based on inductive coupling theory in a power module with parallel-connected SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6644–6661, Jun. 2021.

[7] Y. Li, Y. Zhang, Y. Gao, S. Du, and J. Liu, "Switching characteristic analysis and application assessment of SiC MOSFET with common source inductance and kelvin source connection," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7941–7951, Jul. 2022.

[8] L. F. S. Alves, P. Lefranc, P.-O. Jeannin, and B. Sarrazin, "Review on SiC-MOSFET devices and associated gate drivers," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2018, pp. 824–829.

[9] J. O. Gonzalez and O. Alatise, "Impact of BTI-induced threshold voltage shifts in shoot-through currents from crosstalk in SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 3279–3291, Mar. 2021.

[10] B. Zhang, S. Xie, J. Xu, Q. Qian, Z. Zhang, and K. Xu, "A magnetic coupling based gate driver for crosstalk suppression of SiC MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9052–9063, Nov. 2017.

[11] Z. Zhang, J. Dix, F. F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent gate drive for fast switching and crosstalk suppression of SiC devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.

[12] J. Wang and H. S.-H. Chung, "A novel RCD level shifter for elimination of spurious turn-on in the bridge-leg configuration," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 976–984, Feb. 2015.

[13] Infineon Technol., "Guidelines for coolSiC™ MOSFET gate drive voltage window," 2018. [Online]. Available: https://www.infineon.com/

[14] Wolfspeed, "Design options for wolfspeed silicon carbide MOSFET gate bias power supplies," 2021. [Online]. Available: https://www.wolfspeed.com/

[15] F. Gao, Q. Zhou, P. Wang, and C. Zhang, "A gate driver of SiC MOSFET for suppressing the negative voltage spikes in a bridge circuit," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2339–2353, Mar. 2018.

[16] Q. Haihong, X. Kefeng, N. Xin, Z. Ziyue, Z. Zhiyuan, and F. Dafeng, "Characteristics of SiC MOSFET and its application in a phase-shift fullbridge converter," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 1639–1643.

[17] K. Murata and K. Harada, "A self turn-on mechanism of the synchronous rectifier in a DC-DC converter," in *Proc. 26th Annu. Int. Telecommun. Energy Conf.*, 2004, pp. 642–646.

[18] Z. Zhang, W. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Analysis of the switching speed limitation of wide band-gap devices in a Phase-leg configuration," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 3950–3955.

[19] S. Jahdi, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, "Temperature and switching rate dependence of crosstalk in Si-IGBT and SiC power modules," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 849–863, Feb. 2016.

[20] T. Wu, "Cdv/dt induced turn-on in synchronous buck regulators," in *Proc. Appl. Manual-Int. Rectifier*, 2012, pp. 1–6.

[21] M. R. Ahmed, R. Todd, and A. J. Forsyth, “Predicting SiC MOSFET behavior under hard-switching, soft-switching, and false turn-on conditions,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9001–9011, Nov. 2017.
[22] C. Li et al., “High off-state impedance gate driver of SiC MOSFETs for crosstalk voltage elimination considering common-source inductance,” *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2999–3011, Mar. 2020.
[23] H. Li, Y. Jiang, Z. Qiu, Y. Wang, and Y. Ding, “A predictive algorithm for crosstalk peaks of SiC MOSFET by considering the nonlinearity of gate-drain capacitance,” *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2823–2834, Mar. 2021.
[24] Wolfspeed, “C2M0025120D: Silicon carbide power MOSFET,” 2021. [Online]. Available: https://www.wolfspeed.com/
[25] Infineon Technologies, “IMZ120R045M1: CoolSiC$^{\mathrm{TM}}$ 1200V SiC Trench MOSFET,” 2019. [Online]. Available: https://www.infineon.com/
[26] Infineon Technologies, “IMZ120R060M1H: CoolSiC$^{\mathrm{TM}}$ 1200V SiC Trench MOSFET,” 2019. [Online]. Available: https://www.infineon.com/
[27] M. Noborio, Y. Kanzaki, J. Suda, and T. Kimoto, “Experimental and theoretical investigations on short-channel effects in 4H-SiC MOSFETs,” *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 1954–1962, Sep. 2005.
[28] K. Tachiki, T. Ono, T. Kobayashi, and T. Kimoto, “Short-channel effects in SiC MOSFETs based on analyses of saturation drain current,” *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1382–1384, Mar. 2021.
[29] N. Wang, J. Zhang, and F. Deng, “Improved SiC MOSFET model considering channel dynamics of transfer characteristics,” *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 460–471, Jan. 2023.
[30] Z. Dong, X. Wu, H. Xu, N. Ren, and K. Sheng, “Accurate analytical switching-on loss model of SiC MOSFET considering dynamic transfer characteristic and QGD,” *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12264–12273, Nov. 2020.
[31] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, “An analytical model for false turn-on evaluation of high-voltage enhancement-mode GaN transistor in bridge-leg configuration,” *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6416–6433, Aug. 2017.
[32] S. Ishiwaki, T. Iwaki, Y. Sugihara, K. Nanamori, and M. Yamamoto, “Analysis of false turn-on phenomenon of GaN HEMT with parasitic inductances for propose novel design method focusing on peak gate voltage,” in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 1395–1401.
[33] B. Li et al., “Modeling and analysis of bridge-leg crosstalk of GaN HEMT considering nonlinear junction capacitances,” *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4429–4439, Apr. 2021.
[34] R. Xie et al., “Switching transient analysis for normally-off GaN transistor with p-GaN gate in a phase-leg circuit,” *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3711–3728, Apr. 2019.
[35] J. Wei et al., “Charge storage mechanism of drain induced dynamic threshold voltage shift in p-GaN gate HEMTs,” *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 526–529, Apr. 2019.
[36] T. Basler, D. Heer, D. Peters, T. Aichinger, and R. Schoerner, “Practical aspects and body diode robustness of a 1200V SiC trench MOSFET,” in *Proc. Int. Exhib. Conf. Power Electron.*, 2018, pp. 1–7.
[37] Infineon Technologies, “Infineon coolSiC$^{\mathrm{TM}}$ silicon carbide MOSFET 1200V SPICE simulation models,” 2019. [Online]. Available: https://www.infineon.com/

Hao Yue received the B.S. and M.S. degrees in electrical engineering from the Henan Polytechnic University, Jiaozuo, China, in 2018 and 2021, respectively. He is currently working toward the Ph.D. degree in electrical engineering with Southwest Jiaotong University, Chengdu, China.

His current research interests include wide bandgap device characteristics and models and active gate drivers.

Jian Chen (Member, IEEE) received the B.S. degree from Qinghai University, Xining, China, in 2016, and the Ph.D. degree from Chongqing University, Chongqing, China, in 2021, both in electrical engineering.

He is currently an Assistant Professor with the School of Electrical Engineering, Southwest Jiaotong University, Chengdu, China. His current research interests include wide bandgap device characteristics and models, active gate drivers, and power electronic integration.

Wensheng Song (Senior Member, IEEE) received the B.S. degree in electronic and information engineering and the Ph.D. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2006 and 2011, respectively.

From 2009 to 2010, he was a Visiting Scholar with the Department of Electrical Engineering and Computer Science, University of California at Irvine, Irvine, CA, USA. From July 2015 to December 2015, he was a Visiting Scholar with the University of Alberta, Edmonton, AB, Canada. He is currently a Full Professor with the School of Electrical Engineering, Southwest Jiaotong University. His current research interests include power electronics, motor drives, health monitoring, and reliability of railway traction drive systems.

Haoyang Tan received the B.Eng. degree from Dalian Jiaotong University, Dalian, China, in 2022. He is currently working toward the master's degree with the Department of Electrical engineering, Southwest Jiaotong University, Chengdu, China, both in electrical engineering.

His current research interests include power semiconductor devices and the reliability of power electronics.

Pengcheng Xu (Graduate Student Member, IEEE) was born in Sichuan Province, China, in 2001. He received the B.Eng. degree in electrical engineering in 2022 from Southwest Jiaotong University, Chengdu, China, where he is currently working toward the M.S. degree in electrical engineering.

His current research interests include junction temperature evaluation and health condition monitoring of power semiconductor devices.