A Smart Silicon Carbide LED Driver IC With Integrated Dual-Level Condition-Monitoring Mechanism

Yuanqing Huang, *Member, IEEE*, and D. Brian Ma, *Senior Member, IEEE*

***Abstract*—To address ever-mounting reliability challenges faced by silicon carbide (SiC) power devices, this article develops an innovative dual-level condition-monitoring mechanism aimed at bolstering the robustness of power circuits. This monitoring mechanism is structured to scrutinize both chip and package levels. It also introduces an *in-situ* reliability-aware modulator to evaluate chip-level degradation precursor T_{ON}, package-level aging precursor dynamic on-resistance r_{DS_ON}, and the device's end-of-failure indicator I_{GSS} jointly. From a circuit design perspective, an integrated gate-driving module incorporates functions for T_{ON} and I_{GSS} extraction seamlessly, allowing for intelligent self-sensing with minimal design complexity. To validate the efficacy of these research endeavors, an SiC LED driver integrated circuit (IC) prototype was developed on a 180-nm HV bipolar-CMOS-DMOS process, with an active die area of 1.12 mm^2. The IC facilitates a power converter with up to 600 V input voltage, which efficiently regulates a nominal LED current of 300 mA at a maximum switching frequency of 500 kHz and delivers a maximum output power of 150 W. In comparison to its silicon-based counterpart, the SiC power converter operates at lower junction temperature, thereby enhancing thermal management capacity by around 16%. The integrated gate driver and the *in-situ* reliability-aware modulator occupy a mere 0.17 mm^2 of die area. The work successfully demonstrates consistent monitoring of both chip and package-related degradations, showcasing variations of 11.7% and 3.8%, respectively. It offers a highly cost-effective solution for mitigating the reliability challenges linked to SiC devices for high-performance power applications.**

***Index Terms*—Dual-level condition monitoring, gate oxide degradation, LED driver, package degradation, silicon carbide (SiC) power device.**

I. Introduction

SILICON carbide (SiC) power devices have rapidly gained prominence in the applications spanning aerospace, electric vehicles, and renewable energy regimes [1], [2], [3], [4]. Their ascension is attributed to SiCs remarkable properties, such as low on-resistance, high breakdown voltage, and exceptional thermal conductivity. However, because an SiC field-effect transistor (FET) generally presents lower transconductance than a silicon or GaN FET, it necessitates higher gate-to-source voltage to achieve low on-resistance. In addition, partially due to its high breakdown voltage and superior thermal performance, an SiC power device is often deployed in high-voltage and high-temperature environments. The combination of high voltage and elevated temperature, as major external factors, imposes substantial electrothermal stress, presenting a significant challenge to the SiC device reliability. On the other hand, an SiC power device also faces intrinsic device- and package-level reliability challenges internally. As illustrated in Fig. 1(a), the thin insulator layer renders an SiC device vulnerable to SiO_2 breakdown due to time-dependent dielectric breakdown mechanisms [5]. This vulnerability introduces more traps and defects at the SiC/SiO_2 interface [6]. Over the time, repetitive switching actions cause trapped charges accumulation in the insulator layer, leading to gradual threshold voltage shifts and consequent bias temperature instability (BTI). Furthermore, high V_{DS} stress during switch-on transients accelerates electron carriers with significant kinetic energy. These carriers inevitably inject into the insulator layer, causing hot carrier injection, further compromising gate-oxide reliability [7]. Meanwhile, on the package level, SiC FETs typically adopt TO-247 packages, which face considerable reliability challenges due to fundamental mismatches between thermal expansion coefficients. Operating SiC FETs at high ambient temperatures results in substantial thermomechanical stress across different packaging elements [8]. Further deteriorated with intrinsic bonding wire degradation by electromigration [9], SiC FETs encounter bond-wire fatigue issues, including bond-wire lift-off, heel cracks, and internal voids, which ultimately cause destructive device breakdown and system malfunction [5], [10].

In order to continuously acquire and update the health status of devices and, thereby, enhance the reliability of power systems, the monitoring of power device conditions has become a crucial endeavor. Notably, recent studies [11], [12] have successfully implemented online condition monitoring for GaN power devices, demonstrating promising accuracy in prognosis. These studies specifically track the aging progression of the devices using the dynamic on-resistance as an aging-dependent precursor. The monitoring of SiC device conditions has also been introduced, involving the measurement of aging precursors, such

Manuscript received 12 October 2023; revised 7 December 2023; accepted 12 January 2024. Date of publication 25 January 2024; date of current version 20 March 2024. This work was supported in part by Analog Devices Inc. and UT Dallas Distinguished Chair Professorship. Recommended for publication by Associate Editor F. J. Azcondo. *(Corresponding author: D. Brian Ma.)*

The authors are with the Department of Electrical and Computer Engineering, University of Texas at Dallas, Richardson, TX 75080 USA (e-mail: yuanqing.huang@utdallas.edu; brian.ma@utdallas.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3358634.

Digital Object Identifier 10.1109/TPEL.2024.3358634

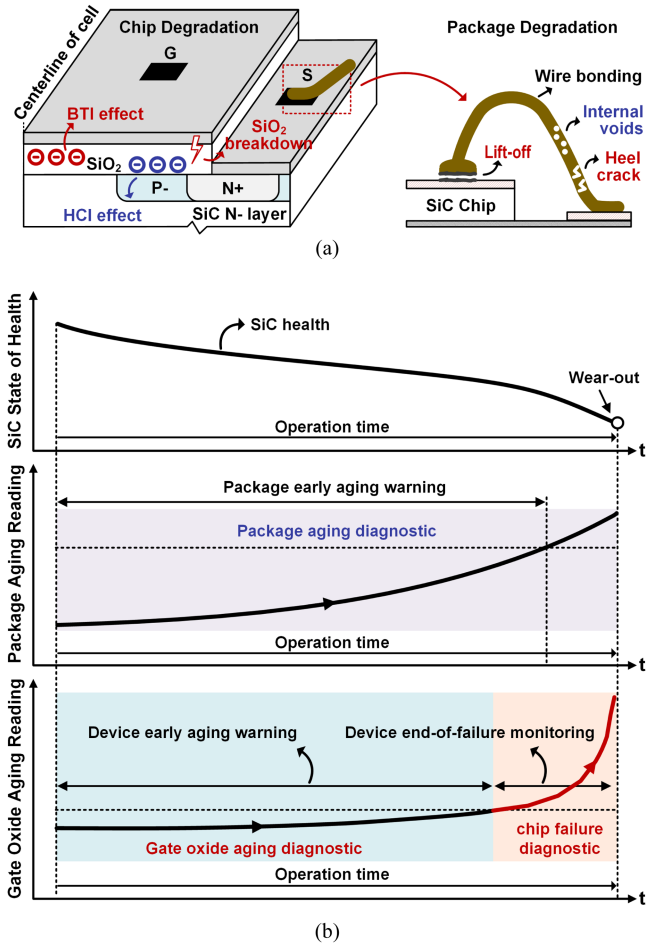

Fig. 1. Illustration of (a) SiC device die and bonding wire degradation and (b) its corresponding state of health.

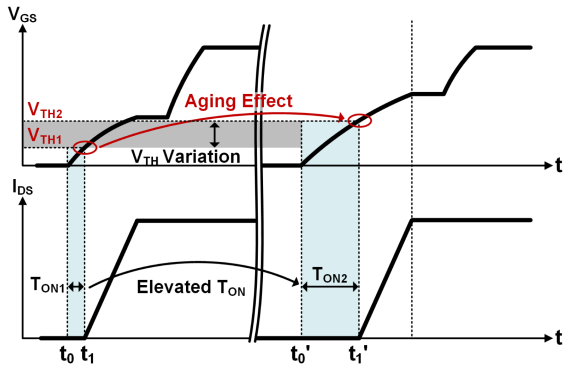

Fig. 2. Illustration of elongated T_{ON} along with gate-oxide degradation.

as on-resistance, junction capacitance, and body diode voltage drop [13], [14], [15]. However, these approaches are typically carried out offline, necessitating the complete shutdown of associated power circuits after specific switching intervals. This practice can be impractical and may introduce inevitable inaccuracies since the offline operations of a system can significantly differ from its real working conditions. Furthermore, all the reviewed approaches so far primarily focus on the detection and monitoring of the slow aging progress of power switches, allowing for early aging warnings. To effectively mitigate catastrophic system failures and maximize the utilization of power switches, characterizing the device at the end of its lifecycle is of paramount importance. In this sense, gate leakage current (I_{GSS}) is a widely recognized intrinsic electrical parameter indicating device gate structure deterioration. Recent findings have demonstrated that the I_{GSS} of an SiC FET experiences a sudden increase just before the final gate failure [16]. This phenomenon can be attributed to the direct formation of a tunneling path between the source and gate due to the accumulation of traps and defects in the insulator, resulting in a significant and immediate increase in I_{GSS}. When I_{GSS} reaches a critical level, the gate-oxide layer fails to provide insulation, leading to the ultimate device failure.

Overall, for SiC-based power systems, it would be highly advantageous to develop a dual-level condition-monitoring approach that encompasses both aging and failure characterization on both device and package levels. To accomplish such a goal, this article introduces two main design innovations. First, we develop an integrated gate-driving module that seamlessly reconfigures the gate driver stage to facilitate the measurement on T_{ON} and I_{GSS} with minimal design overhead. Second, to accurately assess the health condition of the device, we propose an *in-situ* reliability-aware modulator capable of diagnosing both device chip and package aging and failure simultaneously by evaluating the precursors T_{ON}, r_{DS_ON}, and I_{GSS}. We demonstrate the integration of these design innovations in an SiC-based LED driver, resulting in a dual-level condition-monitored power converter.

The rest of this article is organized as follows. Section II delves into the device physics of SiC aging and failure precursors, providing a detailed description of the proposed dual-level condition-monitoring scheme. Section III elaborates on the integrated gate driving with embedded online T_{ON} and I_{GSS} sensing. In Section IV, we detail the system architecture and key circuit implementations. The experimental results are presented in Section V to validate the design. Finally, Section VI concludes this article.

II. Dual-Level Condition-Monitoring Mechanism

To assess device aging and failure progression, researchers have identified several key parameters within power devices that serve as valuable aging precursors. It has been demonstrated through studies that the threshold voltage (V_{TH}) of power transistors increases as gate-oxide degradation advances [5], [17], primarily due to the near-interface charge trapping effect occurring at the SiC/SiO_2 interface. Fig. 2 illustrates how V_{TH} represents the initiation point of the *di/dt* period, playing a crucial role in the switching behavior. As a consequence of a positive shift in V_{TH}, a higher gate-to-source voltage V_{GS} is required to initiate the *di/dt* transition, thereby prolonging the device's turn-on delay from T_{ON1} to T_{ON2}. T_{ON}, which signifies the response time of the device turn-on, emerges as a promising indicator of gate-oxide aging. It possesses distinct advantages when compared with V_{TH}: it can be measured

without interrupting the normal operation of the device under test (DUT), rendering it a more practical parameter for monitoring aging effects. In addition, T_{ON} offers the potential for higher sensing resolution, as the switching transition can be actively controlled by modulating the gate-driving strength. Specifically, the turn-on delay can be described as follows [18]:

$$T_{ON} = R_G \times C_{ISS} \times \ln[(V_{CC} - V_{SS})/(V_{CC} - V_{TH})]. \quad (1)$$

In this context, R_G, C_{ISS}, and V_{TH} are defined as the equivalent gate resistance, total input capacitance, and threshold voltage of an SiC switch, respectively. In addition, V_{CC} and V_{SS} represent the voltage rail voltages of the associated gate driver. Equation (1) demonstrates that T_{ON} exhibits a positive correlation with the aging process. Furthermore, through the active manipulation of gate-driving capabilities and the adjustment of R_G, significant enhancements in T_{ON} sensing accuracy can be achieved.

On the other hand, as discussed in Section I, SiC switches packaged with bonding wires face significant challenges related to package degradation. Moreover, these switches often operate under the conditions of high voltage and extreme temperature, rendering them particularly vulnerable to electrical and thermomechanical stresses. These factors collectively expedite the deterioration of the SiC package's longevity, thereby underscoring the critical importance of monitoring package degradation. To address this issue, the dynamic on-resistance r_{DS_ON} has emerged as a widely adopted precursor closely associated with package degradation [19]. This choice is backed by the fundamental understanding of SiC device physics, where it is well established that the on-resistance of an SiC device decreases significantly when it operates within the ohmic region with a high V_{GS}. Consequently, the on-resistance attributed to the package becomes comparable to that of the device channel. Thus, any variation in drain-to-source resistance induced by package aging results in a substantial deviation in the r_{DS_ON} measurement, serving as a reliable indicator of the package's health condition. In contrast, as elucidated in Section I, concerning the end-of-failure behavior, the gate–source leakage current I_{GSS} maintains a minimal value during the device aging process but undergoes a remarkable increase once the gate ultimately fails. As such, I_{GSS} serves as a credible indicator of SiC end-of-failure characteristics, signifying the destructive deterioration of the gate oxide. I_{GSS} offers a clear representation of the final failure information while demonstrating remarkable immunity to the aging process, culminating in the assurance of reliable failure detection accuracy. Due to the unique and intrinsic link between I_{GSS} and device failure mechanisms, it has become a favored choice for estimating device lifetime before the occurrence of failure [20]. This preference is driven by I_{GSS}'s exceptional reliability and sensitivity to end-of-failure events.

To enable comprehensive SiC device health monitoring at both chip and package levels, we present the overarching block diagram of the proposed dual-level condition-monitoring scheme, as depicted in Fig. 3. This scheme is primarily composed of several key components: an r_{DS_ON}-based package-reliability evaluator, a T_{ON}-inspired chip-level aging precursor, and I_{GSS}-featured end-of-failure monitor and an *in-situ* reliability-aware modulator. The collection of vital parameters is

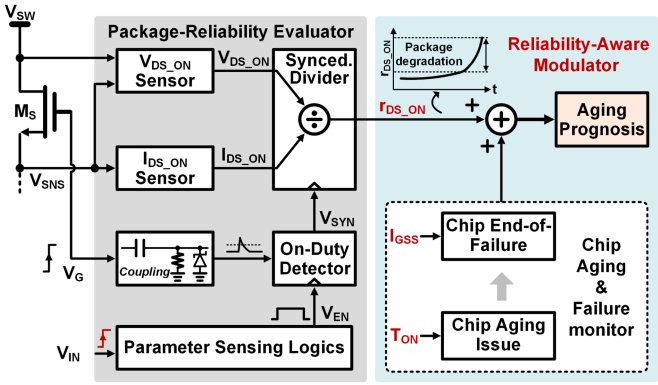

Fig. 3. Circuit block diagram of the proposed dual-level condition monitoring.

facilitated by the simultaneous measurement of r_{DS_ON}, V_{DS_ON}, and I_{DS_ON} of the DUT, M_S. These measurements, in conjunction with the on-duty time of M_S, are processed by a synchronized divider to compute r_{DS_ON}. Simultaneously, T_{ON} and I_{GSS}, vital indicators of gate-oxide aging and failure, are recorded using specialized sensing techniques, as elaborated in the subsequent sections. Correspondingly, the collected aging and failure parameters, T_{ON}, I_{GSS}, and r_{DS_ON}, undergo postprocessing and analysis by the *in-situ* reliability-aware modulator. When either T_{ON} or r_{DS_ON} surpasses predefined aging thresholds, an early warning signal is generated, signaling the overaging of the device's health condition. In response, M_S is replaced with a new power switch to ensure the continuity of high-performance power conversion. Alternatively, advanced techniques, such as active thermal control [11], [21], can be employed to mitigate thermomechanical stress on the DUT, thus extending device longevity. It is essential to note that these approaches may entail a compromise in power circuit performance, particularly in terms of proactive f_{SW} scaling [11]. On the other hand, if the sensed I_{GSS} exceeds the final failure threshold $I_{GSS,TH}$, it indicates that a critical end-of-failure event will soon occur to M_S. Consequently, an end-of-failure warning signal is generated, prompting the shutdown of the overall system to preempt any potential device breakdown issues and catastrophic system malfunction. This proactive approach to monitoring and responding to device health issues ensures the reliability and longevity of the SiC-based power system.

Fig. 4 provides an overview of the operation flowchart for the proposed dual-level condition-monitoring scheme. It is essential to note that the aging precursors, r_{DS_ON} and T_{ON} are sensitive to the junction temperature T_J [22]. Consequently, they tend to fluctuate in response to the variation of ambient temperature T_A and self-heating effect. These factors can potentially lead to overlooked failures and, in some cases, false triggering events, resulting in a high rate of false alarms [12]. To address this issue, the dual-level condition-monitoring scheme is activated during each power-on period, thereby mitigating the adverse effects of T_J variations and ensuring precise aging prognosis [23]. This approach enhances the scheme's accuracy and reliability in monitoring aging and failure conditions. By incorporating these design features and techniques on a single integrated circuit

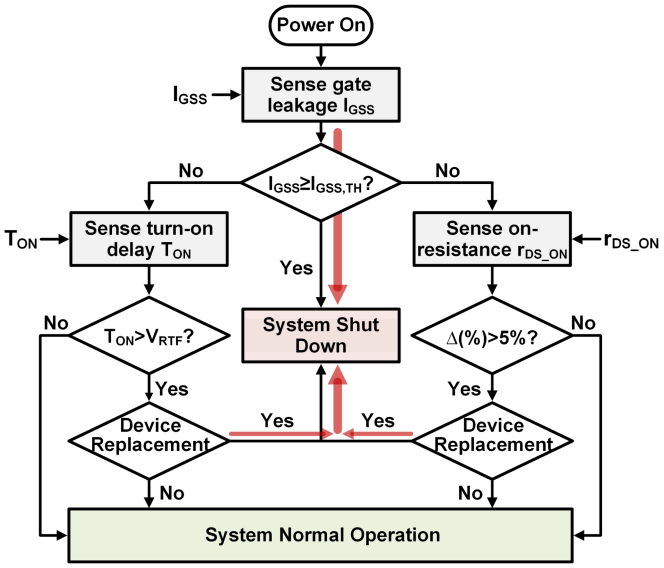

Fig. 4. Operation flowchart of the proposed dual-level condition-monitoring scheme.

(IC), a smart SiC LED driver IC with embedded dual-level aging and failure condition monitoring at both the chip and package levels is presented. Compared with previous methods that rely on offline solutions and off-chip implementations, this smart IC supports comprehensive dual-level device health monitoring with a high degree of accuracy while incurring minimal design overhead.

III. Integrated Gate Driving With Embedded Online T_{ON} and I_{GSS} Sensing

The block diagram of the proposed integrated gate-driving module, which serves as the core hardware of the smart SiC LED driver IC for self-sensing processing, is presented in Fig. 5(a). To address the challenge of self-turning-on induced by substantial V_{DS} spikes while minimizing switching losses, the gate driver stage incorporates an active deadtime t_{dead} controller with split pull-up/down channels. This design is tailored to facilitate the extraction of intelligent aging and failure precursors, T_{ON} and I_{GSS}, without interrupting the normal operation of the converter. To achieve this, adaptive strength gate driver stages and dedicated control modules have been developed.

This intelligent gate-driving stage operates in three distinct modes, as illustrated in Fig. 5(b). In the typical operational sequence, V_{EI} and V_{ET} are initialized at low states, allowing for the commencement of the power circuit's standard operation. Subsequently, as V_{PWMH} rises, V_L decreases following a cell-time-aligned delay. In the sequence that ensues, V_{DH} ascends, and its level is smoothly transitioned to the bootstrap (BST) rail once V_{DRL} descends, effectively mitigating any issues related to shoot-through current. Consequently, both $V_{DRH<0>}$ and $V_{DRH<1>}$ transition to a low state, activating driver output stages M_{HF} and M_{HS} in concert. This collaborative effort charges V_{GS} with the combined strength of $I_{fast} + I_{slow}$, facilitating the near-instantaneous activation of M_S.

Conversely, when V_{PWMH} drops low, a sufficient t_{dead} for the high-to-low transition is established within the complementary t_{dead} control logics. Upon the activation of M_L, V_G is promptly discharged to V_{SNS} via a low-impedance path through a substantial I_{DN}. This action effectively eradicates the self-turning-on issue triggered by a sudden surge in V_{DS}. The separation of the turn-on and turn-off driving channels offers the flexibility to adjust for a relatively gradual turn-on transition and a swift turn-off process. This duality enables robust SiC driving while simultaneously minimizing switching power loss induced by shoot-through current.

Furthermore, the in-cycle I_{GSS} extraction scheme is activated as V_{EI} rises. In this scheme, the high state of V_{PWMH} prompts the gate driver to activate M_S at full strength. After a predetermined time span, denoted as t_{SETTLE}, the driver outputs are proactively disconnected from V_G for a period represented as t_{SNSI}. This marks the initiation of I_{GSS} sensing. As discussed earlier, I_{GSS} experiences a sudden surge when catastrophic device failure occurs. This surge causes the discharge of the gate capacitor C_{ISS}, leading to a noticeable drop in gate voltage ΔV_{GS}, occurring at a rate of I_{GSS}/C_{ISS}. This voltage drop is then capacitively captured and transformed into a single-ended signal V_{GSS}. Upon the end of t_{SNSI}, V_{GSS} is recorded and assessed for further analysis of device failure.

Finally, the T_{ON} sensing scheme is set in motion at the leading edge of V_{PWMH} when V_{ET} transitions to a high state. To enhance T_{ON} sensing accuracy, $V_{DRH<0>}$ is raised high, deactivating M_{HF} and allowing M_{HS} to activate M_S gradually with a relatively low gate current, referred as I_{slow}. The measurement parameter of the turn-on delay V_{TON} is initiated at the leading edge of V_{PWMH} and is brought to a close when V_{SNS} hits V_{RT}. Despite the implementation of slow-switching turn-on transitions, practical sensing delays may introduce sensing inaccuracies, thus challenging the precision of aging prognosis. To rectify this issue, an adaptive T_{ON} correction technique has been devised. This inherent negative feedback loop adaptively fine tunes the end point of V_{TON} until V_{SNS} aligns precisely with V_{RT}, thereby ensuring a high degree of accuracy in T_{ON} sensing.

IV. System Design and Circuit Implementation

A. System Architecture

In order to facilitate the aging and failure characterization of SiC power devices at both the chip and package levels, the overall system architecture of a smart SiC LED driver with embedded dual-level condition monitoring is proposed in Fig. 6. This system primarily comprises an SiC-based offline buck converter power stage, a closed-loop controller with peak current regulation, a smart gate-driving module, and an *in-situ* reliability-aware modulator.

In the power stage, we utilize an SiC MOSFET and an SiC Schottky diode as power switches to achieve superior switching performance. To enable peak current control, a small resistor R_{SNS} actively functions as a peak current sensor. The introduction of the smart gate-driving module, featuring embedded online T_{ON} and I_{GSS} sensing, allows for intelligent and

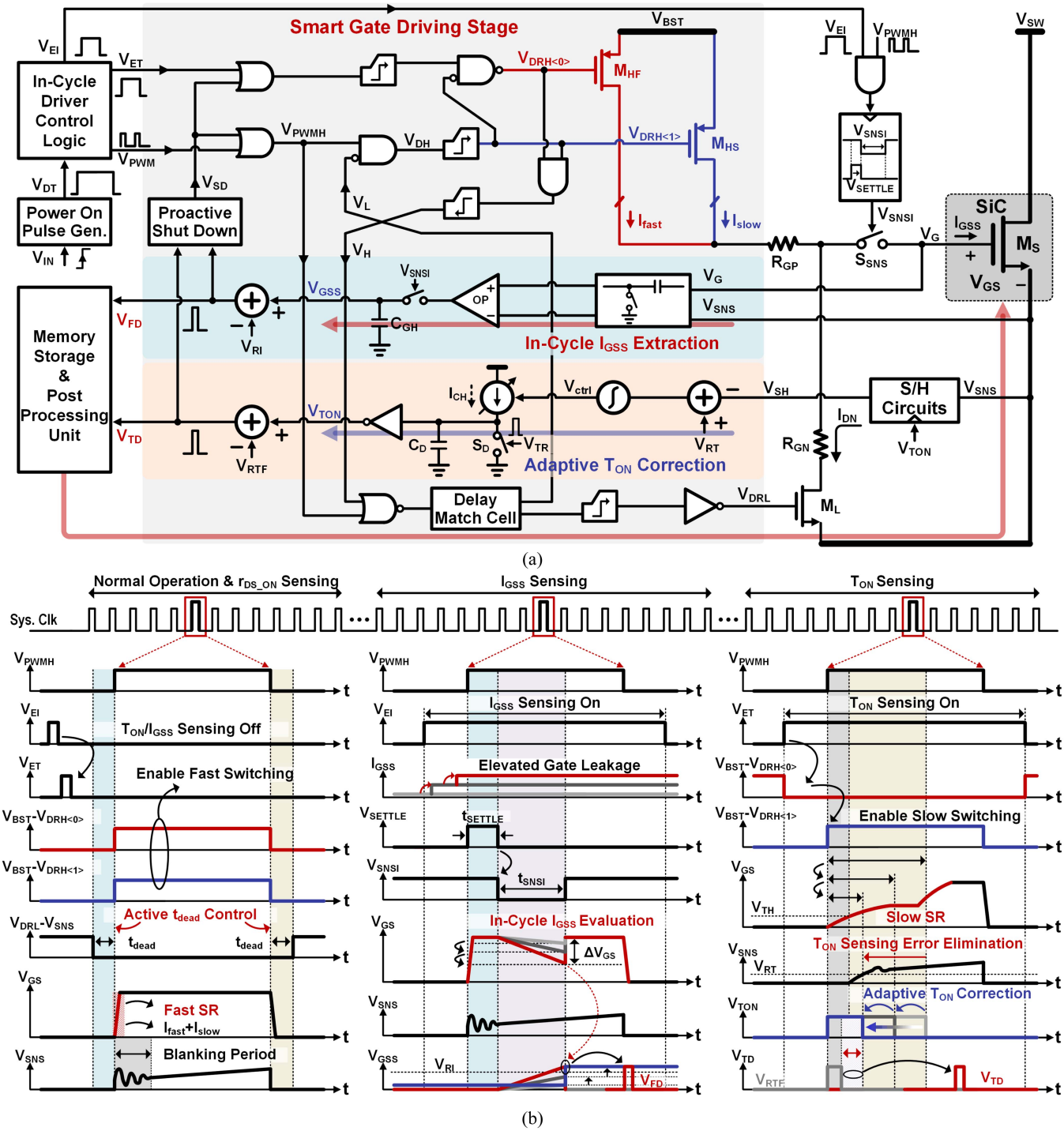

Fig. 5. (a) Circuit schematic and (b) key operation waveforms of the proposed integrated gate driving with embedded online T_{ON} and I_{GSS} sensing.

reliable precursor extraction. The use of an adaptive strength gate driver, capacitively coupled in-cycle I_{GSS} extraction, and adaptive T_{ON} correction techniques ensures feasible and highly accurate precursor measurements with minimal design overhead. On the other hand, the *in-situ* reliability-aware modulator assesses the aging and failure information of the chip obtained in the initial phase. It records the dynamic on-resistance using the classic r_{DS_ON} sensor [11], ultimately establishing a dual-level condition-monitoring system.

B. Adaptive T_{ON} Correction

As a key hardware of device health monitoring, Fig. 7(a) depicts the circuit schematic of the adaptive T_{ON} sensing and correction module. It mainly consists of a modulated gate-driving stage and an adaptive T_{ON} correction loop. T_{ON} sensing-enable logic reconfigures the operation mode of the gate diver stage and actively adjusts the gate charge current I_G to achieve enhanced T_{ON} sensing resolution. To realize an

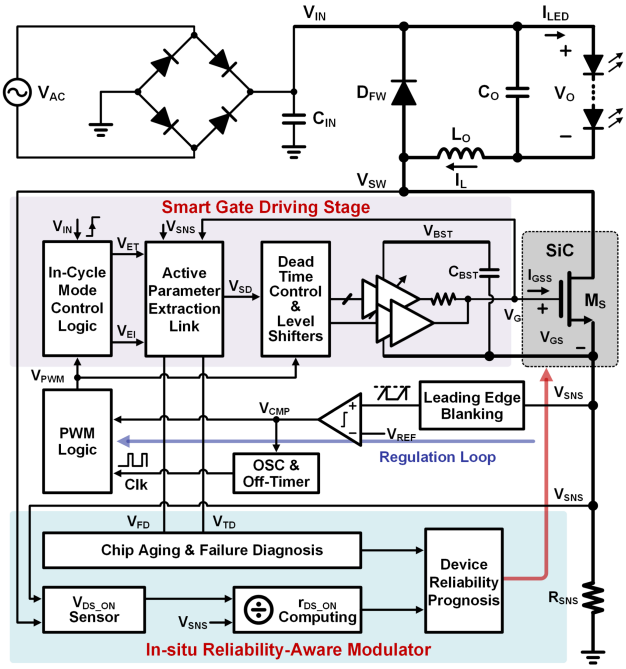

Fig. 6. Block diagram of the proposed smart SiC LED driver with embedded dual-level condition monitoring.

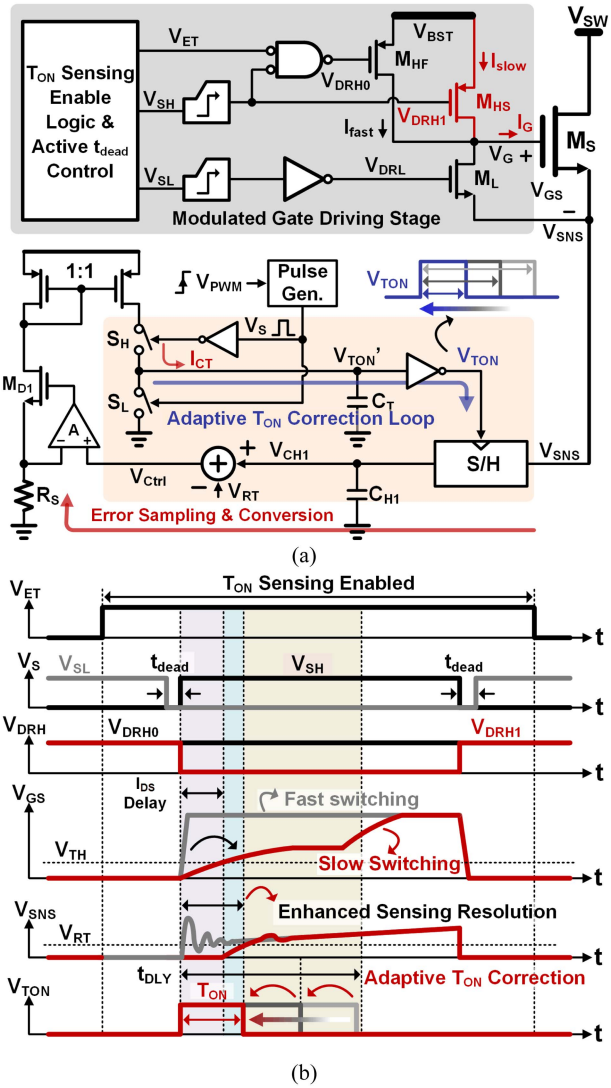

Fig. 7. (a) Circuit schematic and (b) key operation timing diagram of the adaptive T_{ON} correction.

adjustable gate-driving stage, the pull-up network is implemented with two switches M_{HF} and M_{HS}. By supplying high charge current I_{fast}, M_{HF} forms a fast charging path. In contrast, M_{HS} is a slow charging path supporting low I_{slow}. Due to the device property, the gate charge required to enable/disable an SiC switch is substantially high. Accordingly, to maintain power switch fast turn-on/off, the gate driver output stages M_{HF}, M_{HS}, and M_L are deliberately designed with large transistors. To prevent large shoot-through current for high power efficiency as well as improve the design robustness, active t_{dead} control [24] is employed. Meanwhile, at the trailing edge of the sensed turn-on delay V_{TON}, a sample and hold (S/H) block captures the V_{SNS} voltage information as V_{CH1}. The G_m-cell, formed by M_{D1}, R_S, and amplifier A, is dedicated to transfer the sampling error V_{Ctrl} to a charge current I_{CT}. The adaptive T_{ON} correction loop adaptively regulates the trailing edge of V_{TON} at a reference voltage V_{RT}, calibrating T_{ON} sensing errors precisely through the negative feedback.

The key operation timing diagram of the adaptive T_{ON} correction scheme is illustrated in Fig. 7(b). Once V_{ET} is high, T_{ON} sensing is enabled. Accordingly, V_{DRH0} is set to high immediately to disable M_{HF}. When V_{SL} becomes low, M_L is activated to switch off M_S shortly. After a fixed deadtime t_{dead}, V_{SH} ramps up momentarily to manipulate V_{DRH1} to low, enabling slow charging slew rate path M_{HS} accordingly. Afterward, V_G is charged slowly with a tiny gate charge current I_{slow}. Therefore, the start point of the *di/dt* transition is actively postponed, extending the T_{ON} effectively for improved sampling resolution. At the trailing edge of V_{TON}, the drain-to-source current information V_{SNS} is captured as V_{CH1}. It is then compared to a reference voltage V_{RT}, generating an error voltage V_{Ctrl}. Through the G_m-cell, V_{Ctrl} is converted into a charge current I_{CT} for the charge pump stage. If V_{CH1} is higher than V_{RT}, a larger I_{CT} is generated. Therefore, it is transferred into a smaller delay time t_{DLY}, which is calculated as follows:

$$t_{DLY} = C_T \times V_{TH1} \times R_S / V_{Ctrl}. \tag{2}$$

Here, V_{TH1} and R_S are the threshold voltage of the subsequent inverter and the resistor in the G_m-cell, respectively. Such a t_{DLY} will reduce the duration of V_{TON} in the next switching cycle. Such a process repeats until the trailing edge of V_{TON} hits the time instant when V_{SNS} exactly reaches V_{RT}, accomplishing precise T_{ON} detection. In a similar fashion, V_{TON} is adaptively modulated when V_{CH1} is lower than V_{RT}, achieving well-regulated V_{TON} with respect to V_{RT}. As the adaptive T_{ON} correction loop is dedicated to regulating the trailing edge of V_{TON} to ensure that the sampled V_{SNS} equals V_{RT}, the T_{ON} detection error is significantly canceled out. Thanks to the proposed adaptive T_{ON} correction scheme, high-resolution T_{ON} measurement is realized with low design overhead.

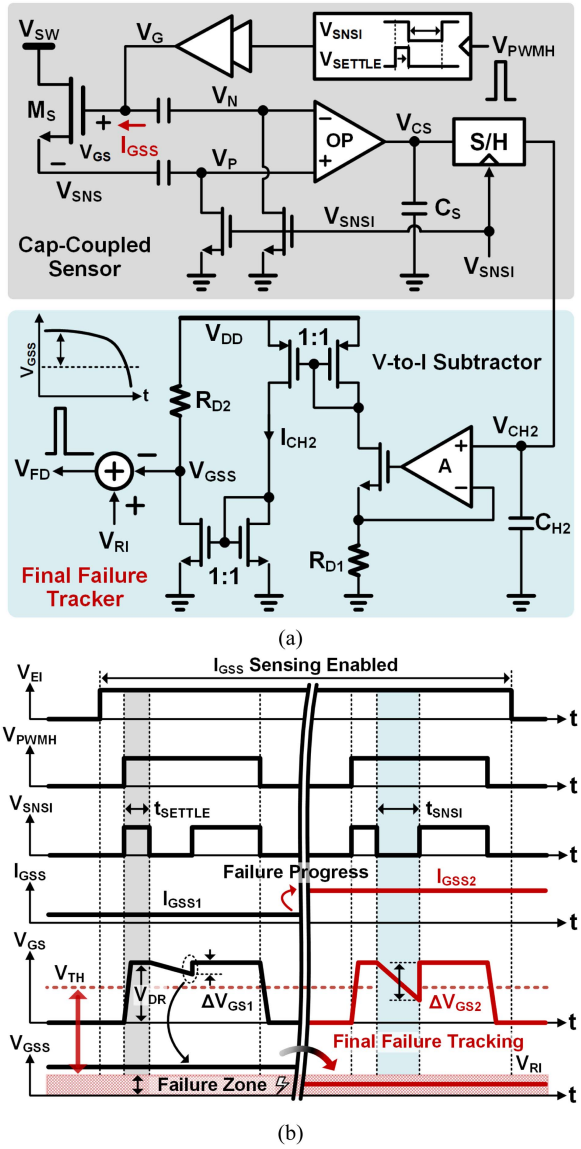

Fig. 8. (a) Circuit schematic and (b) key operation timing diagram of the in-cycle I_{GSS} extraction.

C. In-Cycle I_{GSS} Extraction

As discussed in Section II-A, measuring I_{GSS} is crucial to predict SiC device's final failure on the package level. Conventionally, I_{GSS} information is often obtained using a large gate resistor for reasonable sensing resolution [25]. However, this could lead to unexpected gate-driving delays and substantial switching power loss, limiting high switching frequency operation and degrading efficiency.

To mitigate such, capacitive coupling in-cycle I_{GSS} extraction is adopted [11] and the circuit implementation is shown in Fig. 8(a), which includes a capacitively coupled I_{GSS} sensor to determine I_{GSS} credibly and a final failure tracker as a postprocessing stage for device end-of-failure monitoring. Fig. 8(b) depicts the operation timing diagram of the in-cycle I_{GSS} extraction. Once V_{EI} goes high, I_{GSS} sensing is enabled. Accordingly, at the very beginning of each on-state, high pulsewidth modulation (PWM) control signal V_{PWMH} enables the gate driver to charge V_{GS} with full driving strength to initialize the turn-on process of M_S. After a settling time of t_{SETTLE}, V_{GS} reaches the full driving rail voltage V_{DR}, fully turning on M_S. Afterward, the gate driver is actively disabled for a short period of time, disconnecting the driver from the gate temporarily to enable I_{GSS} sensing. Accordingly, I_{GSS} starts to discharge the input capacitance C_{ISS}, causing a gate-to-source voltage drop ΔV_{GS}. With a sensing period of t_{SNSI}, ΔV_{GS} can be expressed as

$$\Delta V_{GS} = I_{GSS} \times t_{SNSI}/C_{ISS}. \tag{3}$$

It should be noted that, in order to ensure the operation reliability, t_{SNSI} should be designed much shorter than the on-time of the power switch so that ΔV_{GS} stays much smaller than the gate-drive voltage. Accordingly, ΔV_{GS} is coupled capacitively and converted into a single-ended voltage V_{CS}. To record the device's final failure status, V_{CS} is then evaluated and stored as V_{CH2} using an S/H circuit at the trailing edge of V_{SNSI}. Furthermore, V_{CH2} is then converted into I_{CH2} after passing through a V-to-I circuit block, which can be computed as

$$I_{CH2} = V_{CH2}/R_{D1}. \tag{4}$$

Afterward, a stable failure reference V_{GSS} is generated as

$$V_{GSS} = V_{DD} - I_{CH2} \times R_{D2}. \tag{5}$$

Substituting (4) into (5), we have

$$V_{GSS} = V_{DD} - V_{CH2} \times R_{D2}/R_{D1}. \tag{6}$$

Once t_{SNSI} expires, the gate driver stage is reconnected to V_G for the remaining on-time of the converter, resuming the normal operation. Equation (6) reveals that V_{GSS} decreases abruptly once the device's final failure occurs. Eventually, once V_{GSS} drops below a failure threshold voltage V_{RI}, a failure indicator signal V_{FD} is created, shutting down the whole system to avoid potential system malfunction.

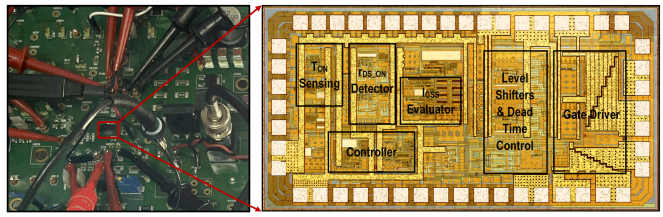

Fig. 9. Photos of test printed circuit board (PCB) and IC die.

V. Experimental Verification

To validate the proposed research work, an IC prototype is fabricated using a 180-nm HV bipolar-CMOS-DMOS process with an active die area of 1.12 mm^2. The testing board and the chip micrograph are shown in Fig. 9. A 1200 V enhancement-mode SiC MOSFET in TO247-package is employed as the power switch M_S. Meanwhile, a 600 V SiC Schottky diode is used as the freewheeling power switch D_{FW}. Furthermore, a 220 μH high voltage inductor L and a 4.7 μF output capacitor C_O are

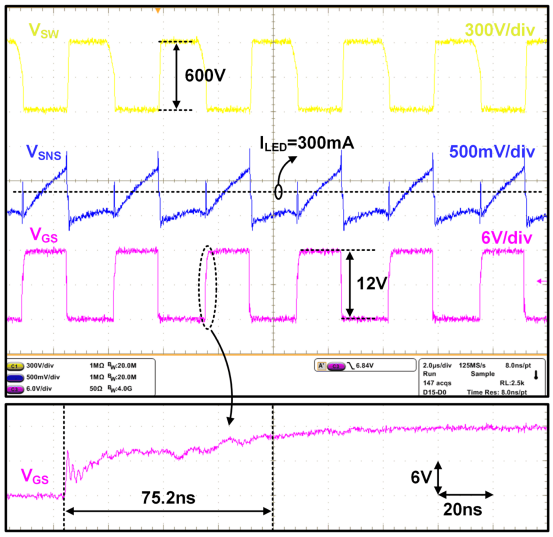

Fig. 10. Measured steady-state operation.

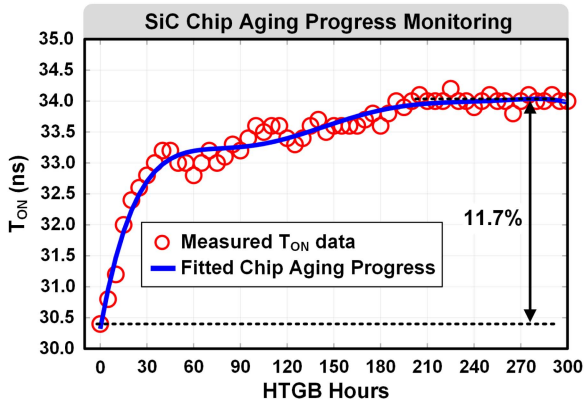

Fig. 11. Measured T_{ON} under HTGB-based aging test.

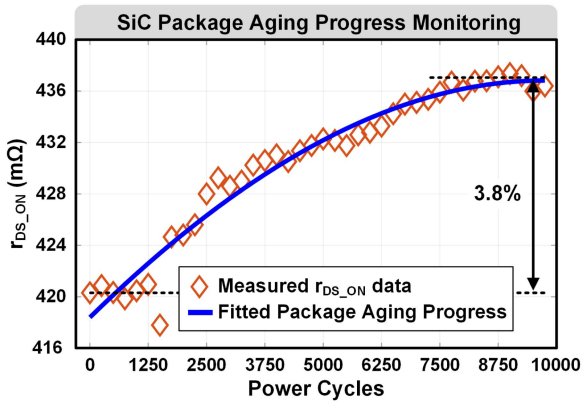

Fig. 12. Measured r_{DS_ON} under power cycling-based aging test.

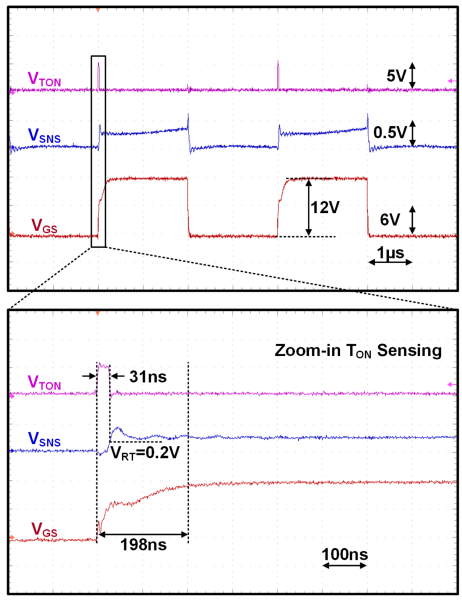

Fig. 13. Measured turn-on delay signal V_{TON} with slow slew rate switching and adaptive T_{ON} correction.

used in the power stage, whereas Cree XQ-E high-density white LEDs are driven as the load of the LED driver IC. Operating at a switching frequency up to 500 kHz, the converter supports a 600 V V_{IN} supply and regulates 300 mA LED current, with a maximum output power of 150 W.

To verify the robust operation of the integrated SiC gate driver, we present the measured key switching voltages, namely V_{SW}, V_{SNS}, and V_{GS}, in the steady state, while supplying a 300-mA LED current. As shown in Fig. 10, during the driver on-state, the SiC power switch demonstrates a commendable performance with a V_{GS} of 12 V, resulting in a switch turn-on delay of 75.2 ns. Conversely, it achieves a complete off-state with a V_{GS} of 0 V. These waveforms serve as concrete evidence of the effective and successful switching behaviors of both the IC driver and the power stage.

To substantiate the efficacy of T_{ON}-based gate-oxide health monitoring, we conducted a high-temperature gate bias (HTGB) test, specifically designed to expedite the gate-oxide degradation process. Based on the discussion in Section I, high V_{GS} voltage would generate a high electric field on the oxide, causing BTI issues and, thus, accelerating the gate-oxide degradation. Accordingly, the SiC switch threshold voltage V_{TH} increases gradually, which then elongates T_{ON} correspondingly. In this experiment, the SiC switch is biased at positive 29 V V_{GS} and repetitively switches at 150 °C ambient temperature. After each 5 h HTGB test, T_{ON} is measured and recorded. Fig. 11 shows the measured T_{ON} data. With a total 300 h HTGB aging test, T_{ON} increases consistently as the gate-oxide aging process proceeds and finally shows an overall increment of 11.7% with respect to its original value, proving the effective monitoring of device chip-level health condition.

On the other hand, to verify the r_{DS_ON}-based package aging prognosis, dc power cycling test [26] is used to accelerate the package aging. In this test, the SiC switch is thermally stressed between 40 and 150 °C for 10 000 power cycles. The package aging-related r_{DS_ON} is evaluated using the on-chip sensing network every 250 cycles. Fig. 12 demonstrates the measured r_{DS_ON} along with the power cycles, which increases gradually as the power cycles goes up and eventually introduces a 3.8%

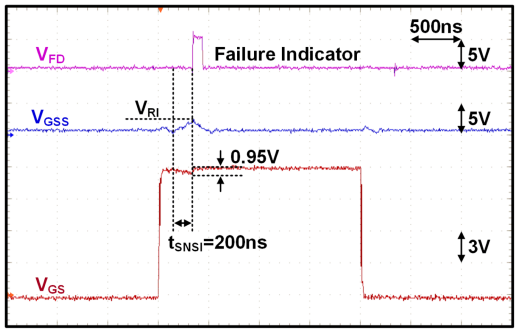

Fig. 14. Measured gate-driving voltage with I_{GSS}-based SiC end-of-failure monitoring.

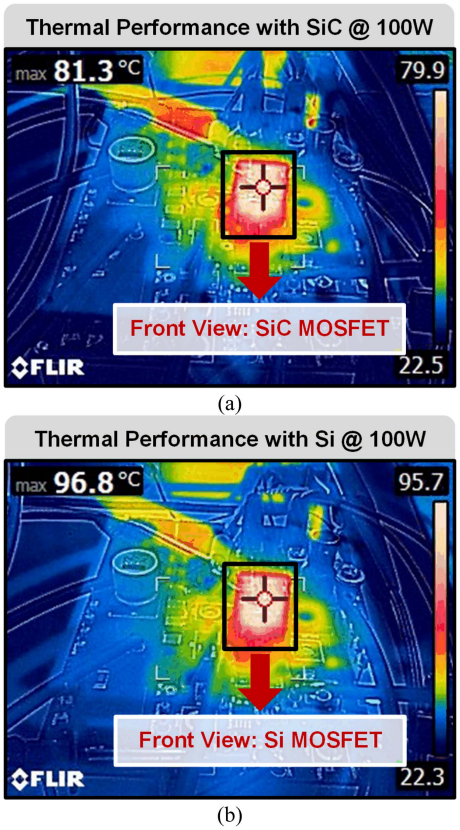

Fig. 15. Performance comparison of thermal capacity between (a) SiC MOSFET and (b) Si counterpart.

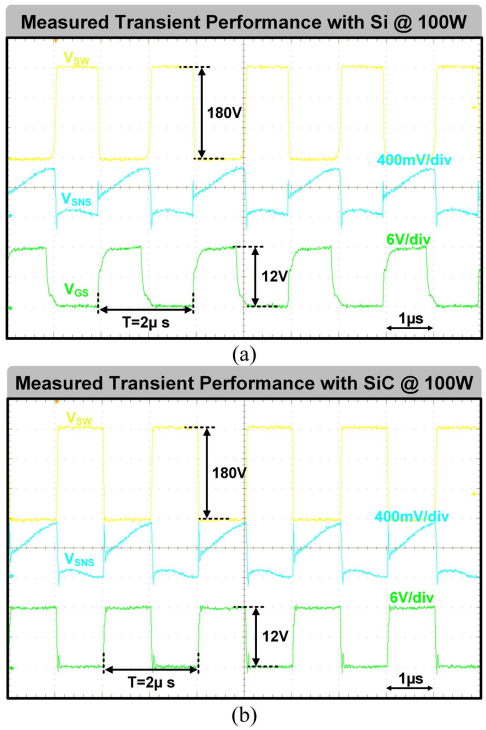

Fig. 16. Performance comparison of switching actions between (a) Si MOSFET and (b) SiC counterpart.

increase by the end of the 10 000 aging cycles, indicating the effectiveness of the integrated package-level aging detection.

To validate the operation principle of T_{ON} sensing, Fig. 13 provides the transient measurement results of the turn-on delay at V_{TON}. The slow slew rate switching mode is actively enabled with a 198 ns delay at the leading edge. Thanks to the adaptive T_{ON} correction technique, the trailing edge of V_{TON} is precisely regulated at the instant that V_{SNS} hits the reference voltage, capturing the T_{ON} as 31 ns.

Fig. 14 shows the measured gate-driving voltage when the SiC switch final failure occurs. With a 200 ns t_{SNSI}, ΔV_{GS} is measured as 0.95 V. It triggers the failure indicator V_{FD} successfully, validating the effectiveness of the proposed circuits.

To assess the thermal performance, Fig. 15(a) displays a thermal map of the SiC-based power converter at 100 W output. Notably, the highest temperature recorded is 81.3 °C, localized within the power switch. In contrast, Fig. 15(b) presents the corresponding thermal image obtained after replacing the SiC power switch with a silicon counterpart, while retaining the converter operation under identical test condition, which reveals a maximum device junction temperature of 96.8 °C. Thanks to the wide bandgap characteristics of SiC material, the thermal capacity of the SiC power converter outperforms its silicon counterpart, which relaxes the cooling system design. Finally, Fig. 16 provides the associated transient measurements of the thermal image samples.

VI. Conclusion

This article introduces a smart SiC LED driver IC with embedded dual-level condition monitoring. The integrated gate-driving module proactively adapts the gate driver stage to seamlessly enable self-sensing processing by monitoring chip-level aging and failure precursors, such as T_{ON} and I_{GSS}, all achieved with minimal design complexity. Furthermore, an *in-situ* reliability-aware modulator has been incorporated to support dual-level condition monitoring, significantly enhancing system robustness and offering promising prognosis accuracy. Through the integration of these innovative schemes and techniques, the converter facilitates simultaneous aging and end-of-failure condition monitoring at both chip and package levels of SiC switches. Experimental results successfully validate the efficacy of these proposed techniques and circuits.

REFERENCES

[1] F. Iacopi, M. van Hove, M. Charles, and K. Endo, "Power electronics with wide bandgap materials: Toward greener, more efficient technologies," *MRS Bull.*, vol. 40, no. 5, pp. 390–395, May 2015.

[2] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[3] J. W. Palmour, "Silicon carbide power device development for industrial markets," in *Proc. IEEE Int. Electron Devices Meeting*, San Francisco, CA, USA, 2014, pp. 1.1.1–1.1.8.

[4] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017.

[5] S. Pu, F. Yang, B. T. Vankayalapati, and B. Akin, "Aging mechanisms and accelerated lifetime tests for SiC MOSFETs: An overview," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 1232–1254, Feb. 2022.

[6] C. X. Zhang et al., "Origins of low-frequency noise and interface traps in 4H-SiC MOSFETs," *IEEE Electron Device Lett.*, vol. 34, no. 1, pp. 117–119, Jan. 2013.

[7] L. C. Yu et al., "Channel hot-carrier effect of 4H-SiC MOSFET," *Mater. Sci. Forum*, vol. 615–617, pp. 813–816, Mar. 2009.

[8] H. Luo, F. Iannuzzo, F. Blaabjerg, M. Turnaturi, and E. Mattiuzzo, "Aging precursors and degradation effects of SiC-MOSFET modules under highly accelerated power cycling conditions," in *Proc. IEEE Energy Convers. Congr. Expo.*, Cincinnati, OH, USA, 2017, pp. 2506–2511.

[9] C. S. Hau-Riege, "An introduction to Cu electromigration," *Microelectron. Rel.*, vol. 44, pp. 195–205, Feb. 2004.

[10] Z. Qiu, J. Zhang, P. Ning, and X. Wen, "Reliability modeling and analysis of SiC MOSFET power modules," in *Proc. IEEE 43rd Annu. Conf. Ind. Electron. Soc.*, Beijing, China, 2017, pp. 1459–1463.

[11] Y. Chen and D. B. Ma, "Self-aging-prognostic GaN-based switching power converter using T_J-independent online condition monitoring and proactive temperature frequency scaling," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5022–5031, May 2021.

[12] Y. Huang, Y. Chen, and D. B. Ma, "A self-health-learning GaN power converter using on-die logarithm-based analog SGD supervised learning and online T_J-independent precursor measurement," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, USA, 2020, pp. 286–288.

[13] E. Ugur and B. Akin, "Aging assessment of discrete SiC MOSFETs under high temperature cycling tests," in *Proc. IEEE Energy Convers. Congr. Expo.*, Cincinnati, OH, USA, 2017, pp. 3496–3501.

[14] M. Farhadi, F. Yang, S. Pu, B. T. Vankayalapati, and B. Akin, "Temperature-independent gate-oxide degradation monitoring of SiC MOSFETs based on junction capacitances," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8308–8324, Jul. 2021.

[15] E. Ugur, C. Xu, F. Yang, S. Pu, and B. Akin, "A new complete condition monitoring method for SiC power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1654–1664, Feb. 2021.

[16] R. Ouaida et al., "Gate oxide degradation of SiC MOSFET in switching conditions," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1284–1286, Dec. 2014.

[17] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015.

[18] Z. Wang, F. Yang, S. L. Campbell, and M. Chinthavali, "Characterization of SiC trench MOSFETs in a low-inductance power module package," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 4157–4166, Aug. 2019.

[19] S. Pu, F. Yang, B. T. Vankayalapati, E. Ugur, C. Xu, and B. Akin, "A practical on-board SiC MOSFET condition monitoring technique for aging detection," *IEEE Trans. Ind. Appl.*, vol. 56, no. 3, pp. 2828–2839, Jun. 2020.

[20] F. Erturk, E. Ugur, J. Olson, and B. Akin, "Real-time aging detection of SiC MOSFETs," *IEEE Trans. Ind. Appl.*, vol. 55, no. 1, pp. 600–609, Feb. 2019.

[21] C. H. van der Broeck, L. A. Ruppert, R. D. Lorenz, and R. W. De Doncker, "Methodology for active thermal cycle reduction of power electronic modules," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 8213–8229, Aug. 2019.

[22] F. Yang, E. Ugur, and B. Akin, "Evaluation of aging's effect on temperature-sensitive electrical parameters in SiC mosfets," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6315–6331, Jun. 2020.

[23] J. Liu, G. Zhang, Q. Chen, L. Qi, Y. Geng, and J. Wang, "In situ condition monitoring of IGBTs based on the miller plateau duration," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 769–782, Jan. 2019.

[24] M. K. Song, L. Chen, J. Sankman, and D. B. Ma, "On-chip HV bootstrap gate driving for GaN compatible power circuits operating above 10 MHz," *IEEE J. Solid-State Circuits*, vol. 57, no. 3, pp. 942–952, Mar. 2022.

[25] P. Wang, J. Zatarski, A. Banerjee, and J. S. Donnal, "Condition monitoring of SiC MOSFETs based on gate-leakage current estimation," *IEEE Trans. Instrum. Meas.*, vol. 71, 2022, Art. no. 2000710.

[26] B. T. Vankayalapati, F. Yang, S. Pu, M. Farhadi, and B. Akin, "A highly scalable, modular test bench architecture for large-scale DC power cycling of SiC MOSFETs: Towards data enabled reliability," *IEEE Power Electron. Mag.*, vol. 8, no. 1, pp. 39–48, Mar. 2021.

Yuanqing Huang (Member, IEEE) received the B.E. degree in electronic science and technology from Xidian University, Xi'an, China, and the M.S. degree in electrical and computer engineering from the University of Macau, Macau, China, in 2014 and 2018, respectively. He is currently working toward the Ph.D. degree in electrical engineering with The University of Texas at Dallas, Richardson, TX, USA.

His research interests include high step-down dc–dc conversion, wide bandgap power device/circuit reliability and condition monitoring, and artificial intelligence driven smart power converters.

Mr. Huang was a recipient of the UT Dallas GSA Student Travel Grant Award in 2022 and the SRC and Texas Analog Center of Excellence Annual Symposium Best Poster Award in 2023.

D. Brian Ma (Senior Member, IEEE) received the B.S. and M.S. degrees in electronic science from Nankai University, Tianjin, China, in 1995 and 1998, respectively, and the Ph.D. degree in electrical and electronic engineering from the Hong Kong University of Science and Technology, Hong Kong, in 2003.

He is currently a Full Professor of electrical and computer engineering and the Distinguished Chair in Microelectronics of The University of Texas at Dallas, Richardson, TX, USA. He is also the Director of Integrated Power Electronics System Laboratory with The University of Texas at Dallas. He has served on the Executive Committee of Semiconductor Research Corporation (SRC) Texas Analog Center of Excellence (TxACE) since 2010 and was the Lead of the Energy Efficiency thrust between 2010 and 2018. He was also the Director of Texas Instruments Foundational Technology Research Center on Power Density from 2018 to 2021. His research focuses on integrated power electronics, with primary interests in power circuit control and operation, wide bandgap power electronics, power device and circuit reliability, aging and security, and artificial intelligence driven smart power systems. He has authored or coauthored over 200 peer-reviewed journal and conference papers and five book and book chapters on these subjects. He also delivered over 130 invited talks, education tutorials, and presentations in prominent conference and industry venues. His research works have been sponsored by the U.S. federal agencies, including the National Science Foundation, SRC, DARPA, and leading international semiconductor companies.

Dr. Ma is investitured as *Analog Devices Professor* (2004–2008), *TxACE Distinguished Chair* (2010–2012), *Erik Jonsson Distinguished Chair* (2012–2017) and *Distinguished Chair in Microelectronics* (2017-present). He is the recipient of the AAFSAA *Outstanding Faculty Award* from the University of Arizona in 2006, and *Fusion Innovation Award* from The University of Texas at Dallas in 2012. He received the *United States National Science Foundation CAREER Award* in 2009. He was also the recipient of 12 technical paper awards from international journals and conferences.