A Practical Automatic Resonant Frequency Tracking Method Based on Instant Transformer Voltage in Unregulated *LLC* Converters

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***Abstract*—An unregulated *LLC* circuit is often used in two-stage converters for electrical isolation and fixed-ratio voltage transformation. When the resonance parameters deviate from the design, the preset switching frequency deviates from the actual resonant frequency, decreasing the efficiency. By analyzing the time-based waveforms of different *LLC* circuit operation modes, we found that above a certain power load, the instant transformer voltage at the edge of the primary bridge voltage is unity above the resonant frequency and is distinctly smaller than unity below the resonant frequency. Accordingly, a new automatic resonant frequency tracking method based on the instant transformer voltage is proposed. When the instant transformer secondary voltage sampled at a specific time is smaller than the output voltage, the switching frequency increases by a minor step. Otherwise, the switching frequency decreases by a minor step. The switching frequency gradually converges to the resonant frequency. Meanwhile, the applicable load power and inductor ratio ranges of the method are discussed in detail. The method is digitally implemented using the DSP with practical issues, including parasitic capacitors and parameter deviations of the control circuit considered. The proposed method is verified on a 1.5 kW 48 V prototype.**

***Index Terms*—DC transformer, frequency tracking, *LLC* converters, operation modes.**

I. Introduction

THE *LLC* topology is highly efficient due to its primary zero-voltage switching (ZVS) and secondary zero-current switching (ZCS). The *LLC* circuit is commonly used as the front or rear stage of a two-stage converter; it operates in an open-loop manner to provide electrical isolation and fixed ratio voltage transformation, while the other stage circuit provides voltage regulation [1], [2], [3], [4], [5], [6], [7].

To achieve high efficiency, the switching frequency of the unregulated *LLC* is always set to the resonant frequency [1], [2], [3], [4], [5], [6], [7]. However, manufacturing errors and the influences of temperature, humidity, and aging cause the resonant capacitor and resonant inductor to deviate from their designed values. As a result, the switching frequency deviates from the actual resonant frequency.

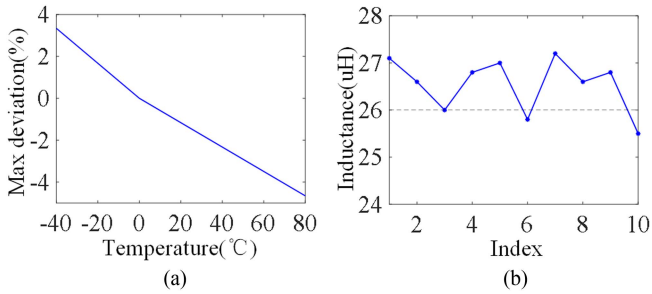

Fig. 1. Deviation of capacitance and inductance. (a) Capacitance as a function of the ambient temperature (max). (b) Inductances of ten mass-produced inductors from Shinenergy.

For instance, the metallized polypropylene film capacitor MKP385 has a factory tolerance of ±5%. Fig. 1(a) shows the maximum variation of its capacitance in relation to temperature [8]. A tolerance of ±7% may exist for resonant inductors, as Fig. 1(b) shows the inductances of ten resonant inductors rated 26 μH from a mass-produced product. Additionally, the inductance may vary during operation due to dc bias.

If the actual capacitance and inductance are 10% lower than their designed values, the actual resonant frequency would be 11% greater than the preset switching frequency. The frequency deviation decreases the efficiency and may cause the circuit operation to exceed the normal range; for example, the *LLC* circuit may lose ZVS, and the *LLC* stage or the other stage may experience overvoltage or overcurrent due to the variation in the gain of the *LLC* circuit. In addition, in applications adopting an open-loop synchronous rectifier driver [9], [10], to avoid energy transfer backward and overcurrent, the on-time of the synchronous rectifier driver should reserve enough margin. Keeping the switching frequency at the resonant frequency is helpful for expanding the on-time of the synchronous rectifier driver, thereby significantly reducing the losses of the synchronous rectifier.

Therefore, an automatic frequency tracking method is required for unregulated *LLC* topologies. A series of frequency

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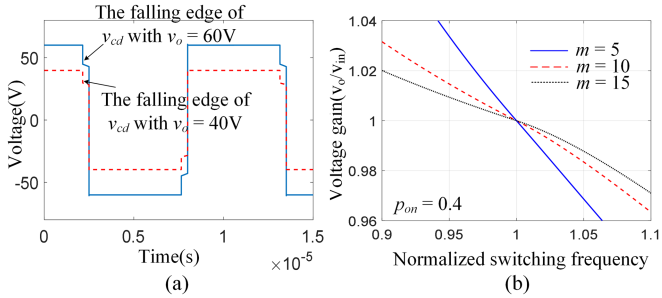

Fig. 2. Limitations of methods based on optocouplers [11] and voltage ratios [23]. (a) Secondary bridge voltage v_{cd} with output voltages of 60 and 40 V. (b) Voltage gain of the output voltage to the input voltage for *LLC* circuits with various inductor ratios m.

tracking methods have been proposed [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22].

In [11], a unified bidirectional resonant frequency tracking algorithm is proposed for unregulated bidirectional *CLLC* resonant converters. The optimal switching frequency is obtained by keeping the voltages of both sides of the resonant tank in phase. Two high-speed optocouplers and two eCAP modules in DSP are used to capture the voltage edges and detect the phase difference. This method provides a simple, digital, and low-cost solution. However, in applications with a broad voltage range and light loads, the falling edges of the secondary bridge voltage at a higher output voltage and low output voltage may not overlap, as shown in Fig. 2(a); thus, the optocoupler cannot detect these two edges simultaneously. As a result, this method may be incapable of tracking resonant frequency at light loads in broad output voltage range applications.

A pulsewidth locked loop (PWLL) for automatic resonant frequency tracking is proposed in [12]. First, the synchronous rectifier (SR) gate-driving signals are tuned by eliminating body diode conduction. Then, the PWLL is presented. By minimizing the pulsewidth difference between the main switch and the well-tuned SR gate driving signals, the *LLC*-DC-DC transformer (DCX) always runs at the f_0 point to achieve the highest efficiency. This method can be digitally implemented; however, its accuracy depends on the SR driving signals, which are sensitive to noise.

The technique in [13] is developed by detecting the zero-crossing point and peak point of the resonant current using the eCAP module in the DSP. The time between the ZCP and PCP is 1/4 of the resonant period. ZCP and PCP detection are easily impacted by noise, in turn impacting the frequency tracking performance.

Theoretically, the time of the zero diode current in the secondary rectifier is zero when the working frequency is equal to or greater than the resonance frequency, and it varies with the frequency when the working frequency is less than the resonance frequency. The method proposed in [14] tracks resonance frequency based on the time measurement of the zero diode current. A closed-loop digital controller is designed for the proposed tracking approach. This method avoids the influence of noise by sampling the average value of the voltage pulses representing the diode conduction. However, the current sensor can be very bulky or energy consuming in low-voltage high-current applications. In [15], the secondary diode zero current duration characteristic is also utilized, as in [14].

The method in [16] is based on tracking the minimum value of the total resonant current harmonic for resonant frequency tracking. A closed-loop digital controller is presented to calculate the total resonant current harmonic and estimate the waveform shape. However, very high sampling and calculating rates are required to calculate the harmonics of the resonant current; therefore, this method is inconvenient and costly to implement.

In [17] and [18], Kundu et al. propose an automatic resonant frequency tracking scheme for parallel and series *LLC* converters. The proposed strategy detects frequency drift by monitoring either the phase or gain relationship of an exclusive variable pair in an *LLC* tank. The most suitable variable pair is chosen based on the sensitivity criteria. For series *LLC*, the phase relation between the primary bridge voltage and the L_m voltage is chosen. The scheme comprehensively analyzes the variable pairs. However, analog implementation of this strategy is inconvenient for digital converters.

When the *LLC* converter operates below the resonant frequency region, the ratio of the average transformer secondary voltage to the output voltage is less than unity, while the ratio is unity at the resonant frequency. By adopting this characteristic, the resonant frequency is tracked by comparing the calculated voltage ratio and unity, and the switching frequency is subsequently adjusted to track the resonant frequency [19]. This method is simple and effective. While when the resonant capacitance is very large, which occurs in high current applications, the decrease in the average transformer secondary voltage when the switching frequency decreases from f_r may not be significant, making the tracking method sensitive to noise.

In [20] and [21], a novel automatic resonant frequency tracking scheme based on an adaptive extended state observer for an unregulated *LLC* converter is proposed. A second-order *LLC* converter small-signal model using an extended describing function method with a simplified resonant circuit is presented. In addition, a new adaptive scheme that automatically updates the inner model of the extended state observer is proposed. This method requires acquiring the second derivative of the voltage, and the algorithm is complex, making implementing this method in products difficult.

In [22] and [23], the converter voltage conversion ratio is computed online by sensing the output voltage and input voltage. Based on comparisons of the calculated gain and unity, the switching frequency is adjusted accordingly, achieving resonant frequency tracking. This method is insensitive to noise and easy to implement. However, when a voltage sensor error exists or when the transformer ratio deviates from the design value, which tends to occur in high current applications where the number of coil turns of the transformer is small and the coils are not tightly wound, the resulting voltage ratio deviates from unity, and the tracking accuracy decreases, especially under a high output load and high inductance ratio, where the gain curve has a smaller slope in relation to frequency [24]. As Fig. 2(b) shows, if the resulting voltage ratio of v_o to v_{in} after tracking is 1.02, then the switching frequency deviates from f_r by –3%, –7%, and –10% under inductor ratios of $m = 5$, 10, and 15, respectively.

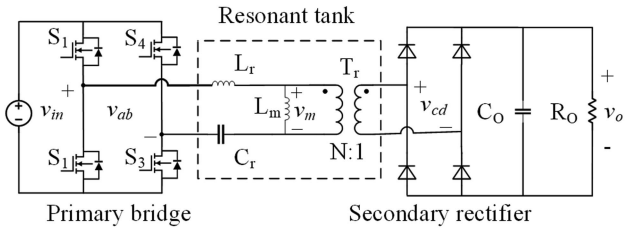

Fig. 3. Full-bridge *LLC* circuit.

There have been many advances in the literature, but there are also shortcomings as follows: 1) The scope of application of methods that are crucial to application has not been analyzed; the impact of other practical factors has also been less discussed. Min and Ordonez [11] mentioned that the method is still applicable when the load decreases to 30% of the rated load according to simulations and experiments; however, no generalized derivation was provided. 2) The accuracy and load range of the existing methods are limited in applications with broad output voltage range and high output current. The method [11] based on optocouplers is ineffective at light loads in broad output voltage range applications. The method in [22] and [23] based on the voltage ratio may introduce large errors when the transformer turn ratio deviates. The method [14] based on the zero-current duration time of a secondary diode would be bulky and energy-consuming in high output current situations.

In this study, a new comprehensive digital frequency tracking method using the DSP is proposed, and its applicable range, which is a crucial aspect for application, is analyzed in detail. Notably, the applicable range analysis is also adapted to other methods. Practical factors such as parasitic capacitors and parameter deviations of control circuits are discussed in detail. Unlike methods based on optocouplers and voltage ratios, the performance of the proposed method will not decrease in applications with broad output voltage range and high output current. In Section II, we review the operation modes of the *LLC* using the time-based method. In Section III, we find that above a specified output load, the instant value of the transformer second voltage at the falling edge of the primary bridge voltage is distinctly smaller than the output voltage when the switching frequency is below the resonant frequency. If the switching frequency is above the resonant frequency, the instant voltage is equal to the output voltage. Based on this, a frequency tracking method is developed, and its applicable range is discussed. In Section IV, the implementation of the proposed method is described using the DSP, and practical issues are investigated. A 1.5 kW 48 V prototype is built in Section V, and the method and applicable load range are verified on this prototype.

II. Operation Mode Analysis

The *LLC* topology is illustrated in Fig. 3, where N is the transformer turn ratio, v_o is the output voltage, L_r is the resonant inductance, L_m is the magnetic inductance, C_r is the resonant capacitance, R_o is the output load resistance, $v_{\rm in}$ is the input voltage, v_{ab} is the primary side bridge voltage, and v_{cd} is the transformer secondary voltage. These expressions are also used in the remainder of the text.

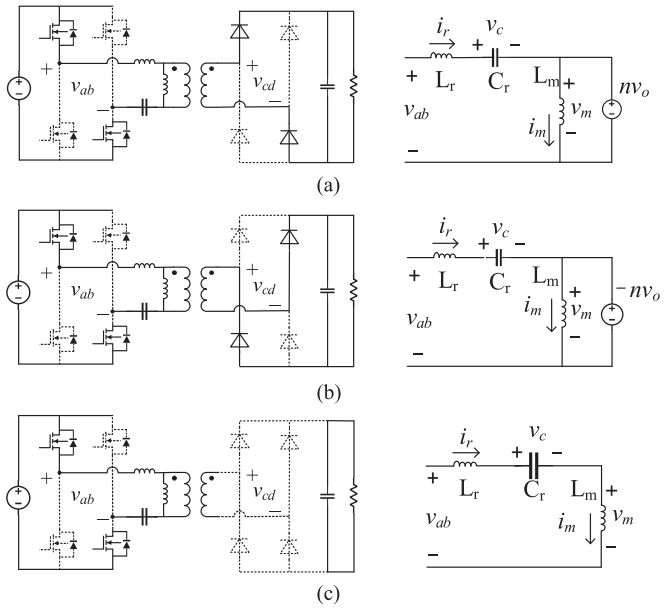

Fig. 4. Equivalent circuits for different stages. (a) P-stage. (b) N-stage. (c) O-stage.

To derive the proposed frequency tracking method, the time-based operation mode analysis proposed in [25] and [26] is briefly reviewed in this section.

For convenience, the following normalized expressions are used:

normalized switching frequency: $f_{sn} = f_s/f_r$

normalized voltage variable: $v_n = v/(Nv_o)$

normalized current variable: $i_n = i/\left(Nv_o/\sqrt{L_r/C_r}\right)$

normalized load power:

$$p_{\rm on} = v_o i_o/\left(N^2 {v_o}^2/\sqrt{L_r/C_r}\right) = \sqrt{L_r/C_r}/(N^2 R_o)$$

inductor ratio: $m = (L_m + L_r)/L_r$

voltage gain: $M = Nv_o/v_{in}$

where f_s is the switching frequency and f_r is the resonant frequency calculated by $1/(2\pi\sqrt{L_r C_r})$.

To simplify the analysis, the parasitic parameters, dead time, and switching time of MOSFETS are not considered in this section.

A. Operation Modes

Due to symmetry, in the text, we analyze only the *LLC* circuit in Fig. 3 in the half switching period when the primary switches S1 and S3 are conducting. Thus, the normalized v_{ab} is positive and equals 1/M.

Due to the unidirectional secondary rectifier, the *LLC* circuit has three different operational stages, P, N, and O, as shown in Fig. 4. As shown, in the P-stage and N-stage, the rectifier

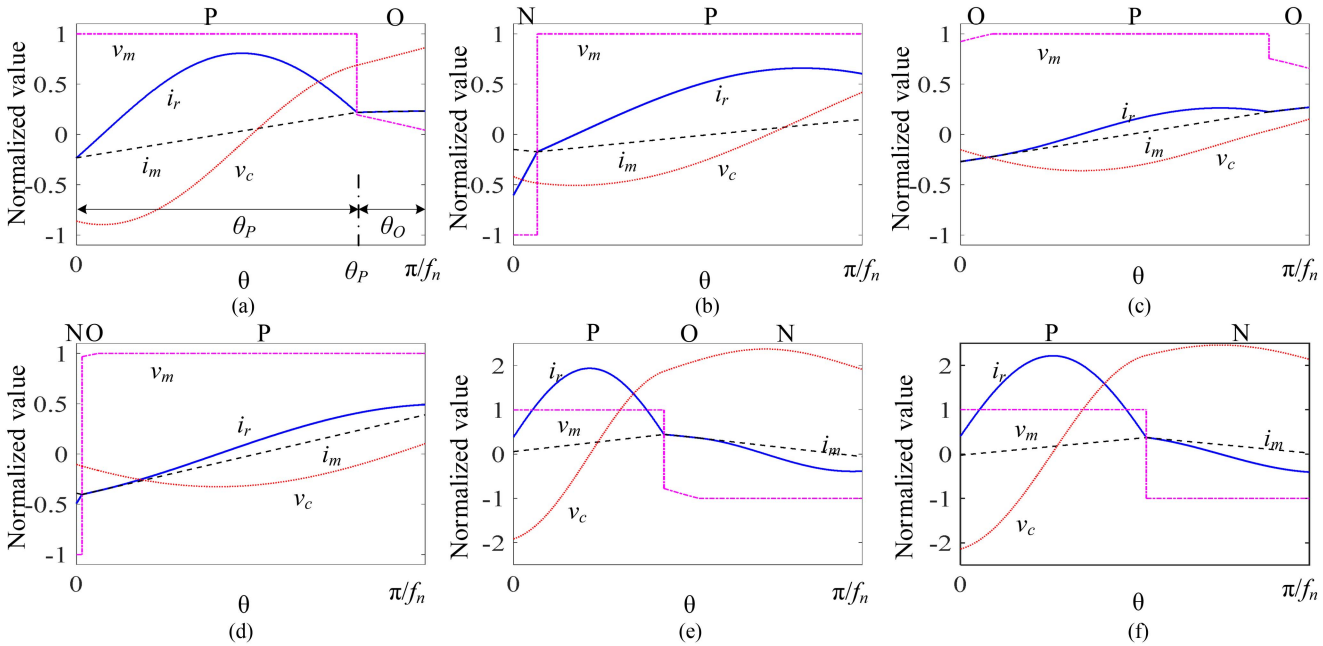

Fig. 5. Waveforms of different *LLC* operation modes in the half period where $v_{ab} = 1$. (a) PO mode with $m = 8$, $p_{\rm on} = 0.4$, and $f_{sn} = 0.8$. (b) NP mode with $m = 8$, $p_{\rm on} = 0.4$, and $f_{sn} = 1.3$. (c) OPO mode with $m = 8$, $p_{\rm on} = 0.07$, and $f_{sn} = 0.8$. (d) NOP mode with $m = 4$, $p_{\rm on} = 0.1$, and $f_{sn} = 1.3$. (e) PON mode with $m = 8$, $p_{\rm on} = 0.6$, and $f_{sn} = 0.5$. (f) PN mode with $m = 8$, $p_{\rm on} = 0.85$, and $f_{sn} = 0.6$.

is conducting, and L_m is clamped to positive and negative output voltages, respectively, while in the O-stage, the rectifier is blocked, and L_m participates in resonance with L_r and C_r. The equivalent circuits of the resonant tank are also shown in Fig. 4. With different switching frequencies f_{sn} and load powers $p_{\rm on}$, different combinations of the stages, which are called operation modes, occur during operation. Named by the sequence of stages occurring during the half switching period, six common operation modes exist: PO, NP, NOP, OPO, PON, and PN. Typical waveforms are shown in Fig. 5, and the calculation method is provided in Section II-B uses mode PO as an example.

B. Time-Based Analysis

When the inductor and capacitor are in resonance, the waveform of the inductor current i_r is sinusoidal, and when the inductor L_m is exposed to a constant voltage in the P-stage and N-stage, its current changes linearly. Accordingly, the inductor current and capacitor voltage in stages P, N, and O can be expressed in normalized form by (1)– (3), where θ is the angle representing time by $\theta = 2\pi f_r t$, I_{rn} is the normalized magnitude of the L_r current i_r, θ_0 is the initial phase angle of i_r, and I_m is the normalized initial L_m current i_m

$$\begin{cases} i_{rPn}(\theta) = I_{rPn}\sin(\theta+\theta_0) \\ i_{mPn}(\theta) = I_{mPn} + \theta/(m-1) \\ v_{cPn}(\theta) = -I_{rPn}\cos(\theta+\theta_0) - 1 + 1/M \end{cases} \tag{1}$$

$$\begin{cases} i_{rNn}(\theta) = I_{rNn}\sin(\theta+\theta_0) \\ i_{mNn}(\theta) = I_{mNn} - \theta/(m-1) \\ v_{cNn}(\theta) = -I_{rNn}\cos(\theta+\theta_0) + 1 + 1/M \end{cases} \tag{2}$$

$$\begin{cases} i_{rOn}(\theta) = i_{mOn}(\theta) = I_{rOn}\sin(\theta/\sqrt{m}+\theta_0) \\ v_{cOn}(\theta) = -\sqrt{m}I_{rOn}\cos(\theta/\sqrt{m}+\theta_0) + 1/M. \end{cases} \tag{3}$$

Since the capacitor voltage and inductor current are state variables and remain continuous during operation, their values at the end of the previous stage are equal to those at the beginning of the latter stage. Therefore, for the PO mode, (4) holds, where θ_P is the duration of stage P

$$\begin{cases} i_{rPn}(\theta_P) = i_{rOn}(0) \\ v_{cPn}(\theta_P) = v_{cOn}(0) \\ i_{mPn}(\theta_P) = i_{mOn}(0). \end{cases} \tag{4}$$

Since waveforms are periodic and symmetrical when the circuit is at steady state in one cycle, (5) holds for the PO mode, where θ_O is the duration of the O-stage

$$\begin{cases} i_{rPn}(0) = -i_{rOn}(\theta_O) \\ v_{cPn}(0) = -v_{cOn}(\theta_O) \\ i_{mPn}(0) = -i_{mOn}(\theta_O). \end{cases} \tag{5}$$

Additionally, the duration of the PO mode satisfies the following:

$$\theta_P + \theta_O = \pi/f_{sn}. \tag{6}$$

Because the output power is transmitted only in the P-stage and N-stage, $p_{\rm on}$ can be expressed as follows:

$$p_{\rm on} = \frac{f_{sn}}{\pi}\left[\int_0^{\theta_P}(i_{rPn} - i_{mPn})d\theta + \int_0^{\theta_N}(i_{rNn} - i_{mNn})d\theta\right]. \tag{7}$$

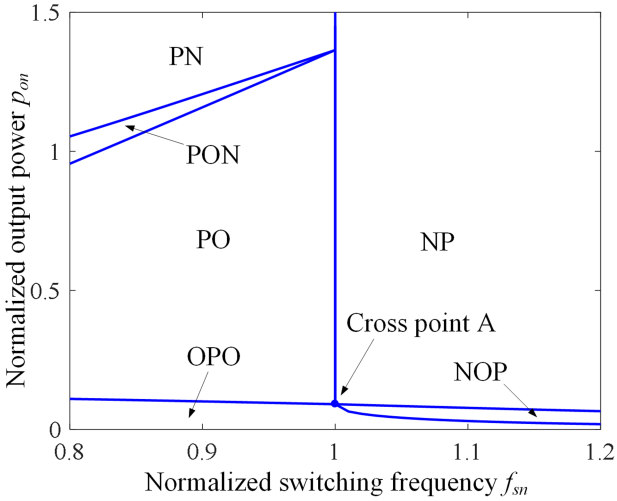

Fig. 6. Operation mode distribution and boundary lines with $m = 8$.

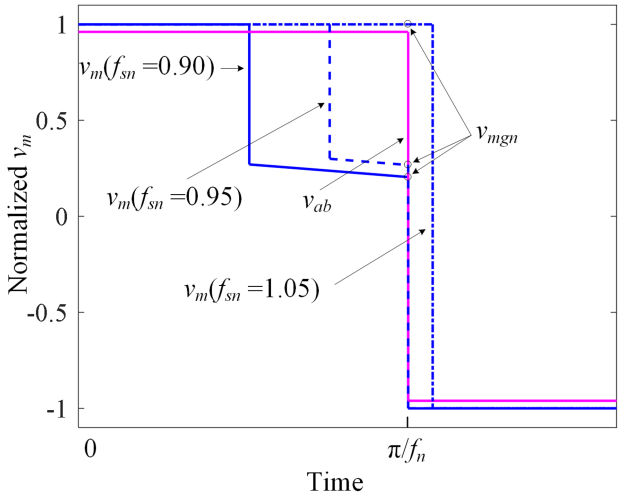

Fig. 7. Variation process of the v_m waveform with increasing f_{sn}.

By combining (1) and (3)–(7), given the inductor ratio m, the switching frequency f_{sn}, and load power $p_{\rm on}$, variables for the PO mode can be solved numerically, and a calculation result with $m = 8$, $p_{\rm on} = 0.4$, and $f_{sn} = 0.8$ is illustrated in Fig. 5(a). The variables in other operation modes can be solved similarly. Fig. 5 shows the numerically calculated typical waveforms of different operation modes in the half period of the positive v_{ab}. The waveforms in the other half period of the negative v_{ab} can be obtained through symmetry.

C. Mode Boundaries and Distribution

With different switching frequencies and load powers, the circuit may work in different operation modes. The mode distribution in the region of f_{sn} and $p_{\rm on}$ can be obtained based on the mode calculation method above. In addition, accurate numerical boundary lines between different operation modes can also be calculated. We continue to take the PO mode as an example.

When the L_m voltage v_m in the O-stage reaches nv_o, as expressed in (8), stage O transitions to stage P. When the P-stage follows the O-stage in operation, due to the continuity of v_c, according to (8), the L_m voltage v_m at the initial moment of the P-stage satisfies (9). Therefore, by combining (9) with constraints (1), (3), and (7) of the PO mode, the boundary line between the PO mode and the OPO mode can be obtained

$$v_{mn} = \frac{L_m}{L_m + L_r}(v_{abn} - v_{cOn}) = \frac{m-1}{m}\left[\frac{1}{M} - v_{cOn}\right] = 1 \tag{8}$$

$$\frac{m-1}{m}\left[\frac{1}{M} - v_{cPn}(0)\right] = 1. \tag{9}$$

The other boundaries can be calculated similarly. Fig. 6 shows the boundaries between different modes and the mode distribution with an inductor ratio of $m = 8$.

As shown in Fig. 6, the PO mode and NP mode intersect at $f_{sn} = 1$, and this boundary line intersects with the OPO mode and NOP mode at point A. At the boundary line of the PO mode and NP mode, there is only the P-stage. At point A, boundary condition (9) between mode PO and mode OPO still holds. Thus, by combining (1), (5), (6), (7), (9) and $f_{sn} = 1$, the normalized power at point A can be obtained as follows:

$$P_{{\rm on}A} = \frac{2}{\pi(m-1)}. \tag{10}$$

III. Proposed Resonant Frequency Tracking Method

A. Instant L_m Voltage at the Falling Edge of the V_{ab}

As shown in Fig. 6, modes PN, PON, and PO are distributed on the left side of the resonant frequency f_r ($f_{sn} = 1$), while modes NP and NOP are distributed on the right side of f_r. Mode OPO is in the low output load region and distributed on both sides of f_r. On the right side of f_r, mode OPO is distributed below point A, that is, in the area of $p_{\rm on} < P_{{\rm on}A}$.

As shown in Fig. 5, for modes PO, OPO, PN, and PON, the v_m voltage drops quickly from unity before the half cycle ends. This is because at the end of the P-stage, L_m is no longer clamped and participates in resonance, bringing a sudden decrease in the rate of i_m, which subsequently leads to a sudden drop in v_m. Moreover, for the NP and NOP modes, v_m remains at unity until the end of the half cycle, and according to symmetry, v_m decreases in the following adjacent half cycle. Because the end of the half cycle is also the falling edge of v_{ab}, the relation of the v_m voltage dropping before or after the end of the half cycle can be regarded as the occurring sequence of the falling edges of v_m and v_{ab}.

Returning to Fig. 6, on the right side of f_r, the OPO mode exists only below point A. As a result, we can conclude that in the region above point A, that is, when $p_{\rm on} > P_{{\rm on}A}$, for the modes on the left side of f_r, the falling edge of v_m leads to the falling edge of v_{ab}, while for the modes on the right side of f_r, the falling edge of v_m lags behind the falling edge of v_{ab}.

The above occurring sequence of the falling edges of v_m and v_{ab} can be depicted by the phase relationship between v_m and v_{ab}, as in [11] and [18], and can also be characterized by

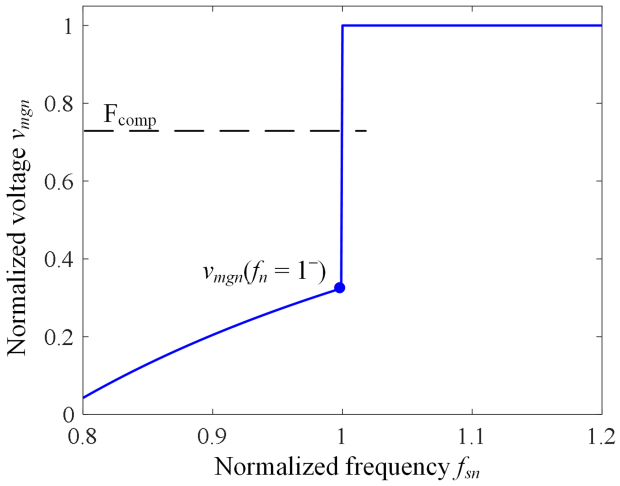

Fig. 8. Variation in the L_m voltage at the falling edge of v_{ab} with the switching frequency f_{sn}.

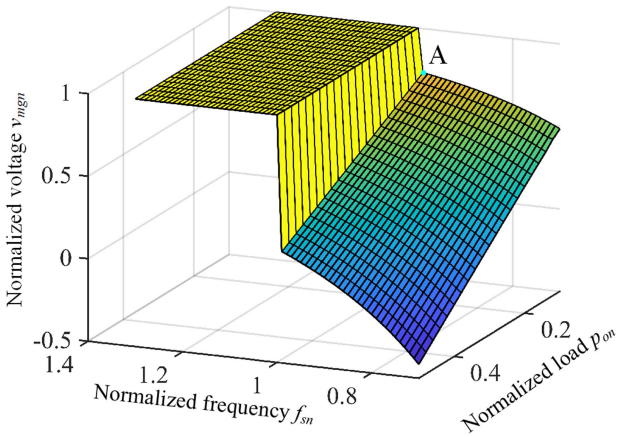

Fig. 9. Instant L_m voltage at the falling edge of v_{ab} with $m = 8$.

the quantitative relationship between unity and the instant v_m voltage at the falling edge of v_{ab}, which is the basis of this study.

Fig. 7 shows the v_m waveforms as the switching frequency f_{sn} increases from 0.90 to 1.05 and $m = 8$. As shown, when $f_s < f_r$, the falling edge of v_m leads to the falling edge of v_{ab}, and the instant v_m value at the falling edge of v_{ab}, which can be termed v_{mg}, is distinctly smaller than unity. When $f_s > f_r$, the falling edge of v_m lags behind the falling edge of v_m, and v_{mg} equals unity. The waveforms of mode PO and mode NP are illustrated, but these relationships can also be adapted to the other modes above point A.

Fig. 8 illustrates the relationship between v_{mg} and f_s more clearly. As shown, a distinct gap exists in v_{mg} between $f_s < f_r$ and $f_s > f_r$, and v_{mgn} jumps to unity from v_{mgn} $(f_{sn} = 1^-)$ at f_r. Fig. 9 more comprehensively depicts v_{mgn} in the region of $0.5 > p_{\text{on}} > P_{\text{on}A}$ and $1.3 > f_{sn} > 0.7$. As shown, the relationship in v_{mg} between $f_s < f_r$ and $f_s > f_r$ exists in the entire region plotted. In the region of $f_s < f_r$, v_{mgn} decreases from point A as f_{sn} decreases and p_{on} increases.

B. Proposed Method

As discussed above, because $v_{mgn} = 1$ above f_r when $p_{\text{on}} > P_{\text{on}A}$ and $v_{mgn} < 1$ below f_r, v_{mg} is a characteristic variable for identifying whether the switching frequency is below or above f_r. Moreover, the distinct gap between v_{mg} above and v_{mg} below f_r can tolerate acquisition errors, noise, and high-frequency oscillations, making v_{mg} insensitive to interference as the characteristic variable.

F_{comp} is defined as the comparison factor, as shown in Fig. 8. The proposed resonant frequency tracking method is as follows. When v_{mgn} is larger than F_{comp}, the switching frequency is larger than the resonant frequency f_r, and the current switching frequency f_s decreases by a minor step. When v_{mgn} is smaller than F_{comp}, the switching frequency f_s is smaller than f_r, and the current switching frequency f_s increases by a minor step. Through this method, f_s will eventually converge to f_r and then fluctuate around it with a minor step.

The resonant frequency can be tracked only in the region $p_{\text{on}} > P_{\text{on}A}$. When $p_{\text{on}} < P_{\text{on}A}$, the OPO mode extends to the region of $f_{sn} > 1$, and v_{mgn} of the OPO mode is still smaller than unity when $f_{sn} > 1$. When $p_{\text{on}} < P_{\text{on}A}$, this method tracks the boundary line of the OPO and NOP modes, as depicted in Fig. 6; this boundary line is larger than f_r.

As in Fig. 8, since v_{mgn} is equal to unity at $f_{sn} > 1$ and lower than v_{mgn} $(f_{sn} = 1^-)$ at $f_{sn} < 1$, to track $f_{sn} = 1$, the comparison factor F_{comp} should be selected in the range between v_{mgn} $(f_{sn} = 1^-)$ and unity. Suppose that in practice, the method is set to work when $p_{\text{on}} > P_{\text{on}m}$, where $P_{\text{on}m}$ is larger than $P_{\text{on}A}$. Since v_{mgn} is greater with a smaller p_{on}, as shown in Fig. 9, to make the method compatible with the entire workable load range, the comparison factor F_{comp} should be selected between unity and v_{mgn} $(f_{sn} = 1^-, p_{\text{on}} = P_{\text{on}m})$.

By combining (1) and (4)–(7), v_{mg} $(f_n = 1^-)$ can be solved analytically as (11). By substituting p_{on} with $P_{\text{on}m}$ as in (11), v_{mgn} $(f_{sn} = 1^-, p_{\text{on}} = P_{\text{on}m})$ can be obtained

$$v_{mgn}\left(f_n = 1^-\right) = \frac{L_m}{L_m + L_r}\left[v_{abn} - v_{cPn}\left(\theta_P\right)\right] = \frac{m-1}{m}\left(1 - \frac{\pi \cdot p_{\text{on}}}{2}\right). \tag{11}$$

An example of an F_{comp} selection follows. Given $m = 8$ and $P_{\text{on}m} = 0.15$, v_{mg} $(f_n = 1^-, p_{on} = 0.15)$ is calculated by (11) as 0.67. Then, F_{comp} should be selected between 0.67 and 1, such as 0.85.

To implement this method, v_{mgn} can be obtained by $v_{mg}/(\text{N}v_o)$, where v_{mg} is obtained by sampling the transformer primary or secondary voltage at the specific instant of the falling edge of the bridge voltage v_{ab}, and the output voltage v_o as the normalization base is sensed by a voltage sensor. In some cases, the resonant inductors are integrated into the transformer primary coils; thus, only the transformer secondary voltage can be used to obtain v_{mg}. The normalized load p_{on} is calculated by $v_o i_o/(N^2 {v_o}^2/\sqrt{L_r/C_r})$, where L_r, C_r, and N are the design parameters and i_o is the output current sampled by a current sensor.

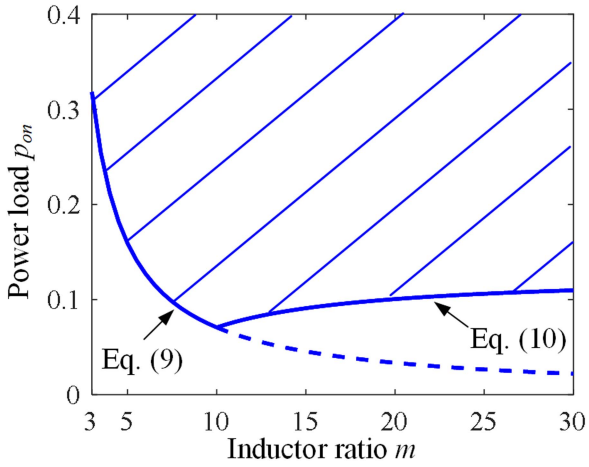

Fig. 10. Applicable ranges were $p_{\mathrm{on}} > P_{\mathrm{on}A}$ and v_{mne} ($f_n = 1^-$) > 0.8.

The output voltage and output current are often already sensed for control purposes; therefore, only the transformer voltage sensor is newly added for the proposed tracking method. The proposed method tends to be robust. First, the variables used are large signals insensitive to noise. Second, despite the presence of noise, as long as the number of correct values collected exceeds the number of incorrect values with noise, the resonance frequency will eventually be tracked. In addition, compared to the optocoupler-based method, which is not adaptable to applications with broad output voltages range and low loads, this method has a wider load range. This is because the output voltage is sampled and the normalized voltage value utilized is adjusted with respect to the output voltage. Thus, the performance of this method is not affected by the output voltage. Additionally, the method is not affected by the transformer ratio error.

C. Applicable Range

As mentioned previously, the proposed method is valid when the load range is $p_{\mathrm{on}} > P_{\mathrm{on}A}$, and the method loses efficacy when the load range is below this range. Thus, $P_{\mathrm{on}A}$ is the theoretical limit of power loads for this method.

Moreover, as shown by (11), when the p_{on} is very low, v_{mgn} may be very close to unity. For example, when $m = 30$ and $p_{\mathrm{on}} = 0.03$, v_{mgn} is calculated by (11) as 0.92. Distinguishing them with the sensor error, noise and high-frequency oscillation would then be difficult, leading to an incorrect frequency tracking result. If $v_{mgn} < 0.8$ is required for robust identification of f_r, the applicable range of p_{on} can be calculated with v_{mgn} ($f_{sn} = 1^-$) $= 0.8$ by (11). The calculated results for various m values are plotted in Fig. 10, where the shaded area represents the applicable area. As shown, for m greater than 10, the applicable range is limited by $v_{mgn}(f_{sn} = 1^-) \leq 0.8$, instead of $P_{\mathrm{on}A}$. Note that 0.8 is an estimated value to illustrate the load range of this method, and the actual value may vary in practice according to the noise level.

One basis of the proposed method is that in the mode distribution, modes OPO, PO, PON, and PN are in the area below f_r and above point A, and mode NP is in the area above f_r and point A, which is extracted from the mode distribution plot with $m = 8$. Proving this analytically is infeasible due to nonlinearity, but situations with m ranging from 2 to 50, which cover the inductor ratios in [1], [2], [3], [4], [5], [6], and [7], verify that the mode distribution feature always exists. Fig. 11 shows two mode distributions with $m = 2$ and $m = 50$. In addition, other analysis bases also have no limitations on the inductor ratio m. Therefore, the proposed method has no special limitations on the inductor ratio m.

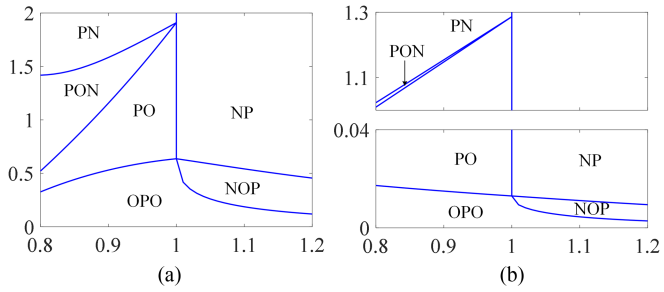

Fig. 11. Mode distribution. (a) $m = 2$. (b) $m = 50$.

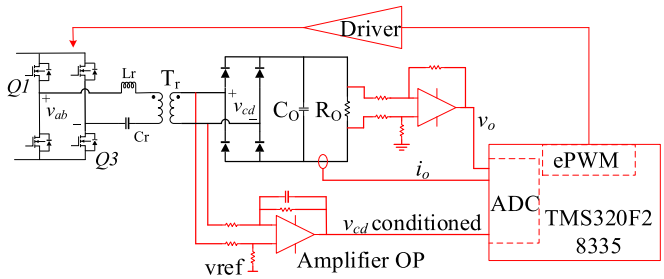

Fig. 12. Implementation circuit.

Because the output efficiency at a higher load power has a greater impact on the energy loss and temperature rise of the equipment than does the output efficiency at a lower load power, the applicable load range of this method, which is effective at higher loads, is feasible.

Notably, the applicable load range analysis above can also be adapted to other existing methods. For example, the methods based on the phase relationship in [11], [17], and [18] have the same applicable load range as the proposed method in this article. The methods based on SR gate-driving signals [12], zero-current duration time of secondary diode [14], and average transformer voltage [19] cannot be used at very high p_{on} because the duration time of the secondary diode is zero both in PN mode below f_r and in NP mode above f_r and because the average transformer voltage is equal to the output voltage both in PN mode and in NP mode.

IV. Implementation and Considerations

A digital circuit using the digital microcontroller TMS320F28335 is utilized to implement the proposed method. As shown in Fig. 12, the signals of the output voltage, output current, and transformer secondary side voltage are sensed by the internal ADC module of the DSP. The driving pulsewidth

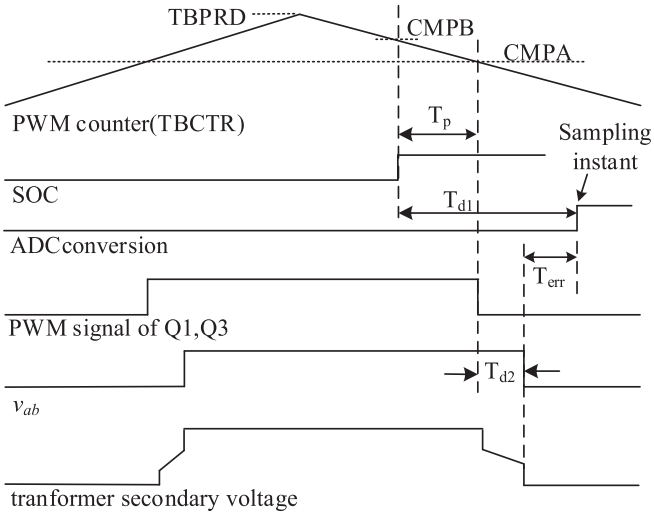

Fig. 13. Timing sequence in implementation.

modulation (PWM) signals generated by the ePWM module are applied to the primary MOSFETs after being enhanced by the driver chip.

A. Hardware

The approach for acquiring the output voltage and output current is typical. The key idea of this approach is to acquire the instant value of the transformer secondary voltage v_{cd} at the right moment of the falling edge of the primary bridge voltage v_{ab}.

According to the TMS320F28335 user manual [27], the ADC sampling is triggered by the start of conversion (SOC) signal, which can be generated by the event of the ePWM module. After the SOC is generated, an interval of 6.5 ADC clock cycles passes before the ADC module performs the sampling, given the length of the sampling window being four. The actual sampling takes place 260 ns after the SOC signal is generated, given that the ADC clock frequency is 25 MHz.

A delay also exists between the falling edge of the original PWM signals of Q1 and Q3 generated by the ePWM module and the falling edge of the primary bridge voltage v_{ab}. The delay consists of two parts: the propagation delay of the driver chip and the MOSFET turn-OFF delay. For example, the isolated coreless transformer driver chip 1ED3124MU12AH has a typical propagation delay of 90 ns [28], and the 650 V SiC MOSFET IMZA65R048 has a typical propagation delay of 17 ns [29].

To acquire v_{cd} at the falling edge of v_{ab}, the configuration in the timing diagram in Fig. 13 is adapted. As shown, the PWM time-base counter increases from 0 and decreases after reaching the TBPRD. When the counter equals the CMPA, which is fixed to half of the peak value of the TBPRD, the PWM signal toggles up and down. When the counter decreases and equals CMPB, the ADC start-of-conversion (SOC) event is generated. To simplify the analysis, T_{d1} is defined as the delay between the SOC and the actual sampling event, T_{d2} is the delay between the falling edge of the original PWM signal of Q1 and Q3 and the bridge voltage v_{ab}, $T_{\rm err}$ is the time deviation between the actual sampling and the v_{ab} falling edge (a positive sign indicates that the sampling lags to the v_{ab} falling edge, a negative sign indicates that the sampling leads to the v_{ab} falling edge), and T_p is the time interval from the CMPB to the CMPA). Then, the following holds:

$$T_{\rm err} = T_{d1} - (T_p + T_{d2}). \tag{12}$$

Given T_{d1} and T_{d2} by the chip manual or by testing, the actual sampling time deviation $T_{\rm err}$ can be controlled by T_p. In other words, with the CMPA fixed to half of the TBPRD, the actual sampling time in relation to the falling edge of the v_{ab} can be controlled by setting the CMPB.

In addition, because v_{cd} is a rapidly changing signal, an amplifier with a bandwidth of at least tens of MHz is needed. Otherwise, the processed v_{cd} signal will be distorted, degrading the frequency tracking accuracy.

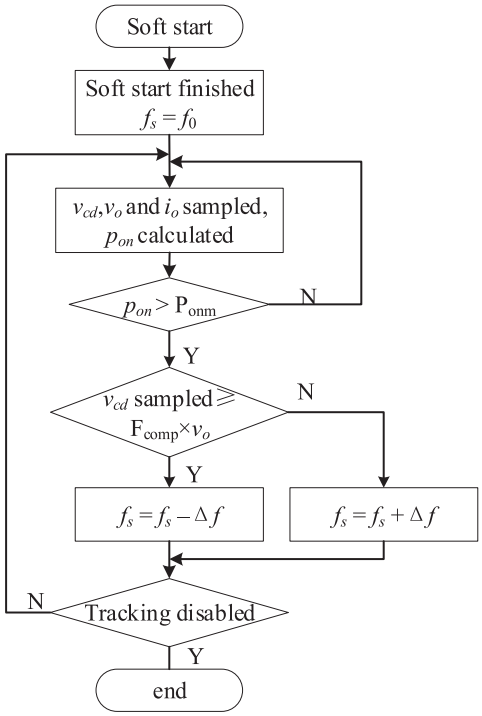

Fig. 14. Tracking logic in the software.

B. Software Workflow

As in Fig. 14, at startup, the *LLC* circuit generally performs a soft start, with the switching frequency decreasing from several times the preset frequency to the preset frequency. After the soft start process is finished and the circuit status becomes stable, the tracking program begins working.

In the tracking program, first, the secondary bridge voltage v_{cd} is sampled at the edge of the primary bridge voltage v_{ab}, the load current i_o and the output voltage v_o are sensed, and the normalized power load $p_{\rm on}$ is calculated. If $p_{\rm on}$ is larger than the preset constant limit $P_{{\rm on}m}$, then the method is in the applicable load range. Then, the sampled v_{cd} is compared with $v_o \times F_{\rm comp}$. If the sampled $v_{cd} \geq v_o \times F_{\rm comp}$, the current switching frequency

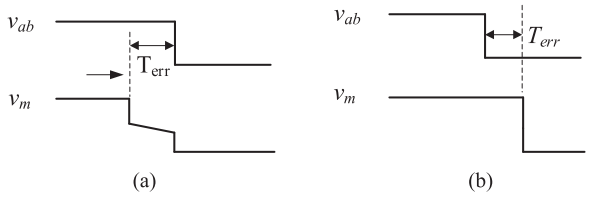

Fig. 15. Resulting operation modes with (a) $T_{\rm err} < 0$ and (b) $T_{\rm err} > 0$.

f_s decreases by a small step Δf. Otherwise, f_s increases by a small step Δf. The tracking logic runs cycle by cycle. Gradually, the switching frequency will converge to the resonant frequency. Note that the constants $P_{{\rm on}\,m}$ and $F_{\rm comp}$ can be evaluated using the ideal (10) and (11) in the article or obtained by experiments.

C. Influence of the Sampling Time Drift

Because the clock frequency of the ADC module is lower than the clock frequency of the ePWM module in the DSP, after the SOC event of the ePWM module is generated, the event may not be detected by the ADC module for up to one ADC clock cycle. Therefore, the delay from the SOC event to ADC sampling varies between 6.5 and 7.5 ADC clock cycles; that is, $T_{d1} = 260$–300 ns. Moreover, due to the individual differences in the driver chips and the MOSFETs and the influences of the environment and aging, the delay T_{d2} between the original PWM signals generated by the DSP and v_{ab} also varies. For example, according to the user manual, the propagation delay of the driver chip 1ED3124MU12AH varies between 80 and 100 ns [28].

This causes the sampling deviation time $T_{\rm err}$ to vary and not remain at the ideal value of zero. After the frequency tracking process, the falling edge of v_{cd} coincides with the ADC sampling instant, so the resulting operation modes for $T_{\rm err} < 0$ and $T_{\rm err} > 0$ are PO and NP, respectively, as illustrated in Fig. 15. For $T_{\rm err} < 0$, the duration of stage O equals $T_{\rm err}$, which can be expressed by the following, where T_s is the switching period:

$$T_{\rm err} = \frac{\theta_O}{\pi}\frac{T_s}{2}. \tag{13}$$

The tracking error is defined as follows:

$$e_t = f_{sn} - 1 \tag{14}$$

By combining (1), (2), (4)–(7), (13) and (14), the tracking error for $T_{\rm err} < 0$ can be obtained. The tracking error for $T_{\rm err} > 0$ can also be obtained similarly by solving the NP mode. Fig. 16 shows the impact of $T_{\rm err}$ on the tracking error. As shown in Fig. 16(a), the tracking error increases as $T_{\rm err}$ increases, the tracking error is much greater at $T_{\rm err} > 0$ than at $T_{\rm err} < 0$, and the inductor ratio has a small impact on the tracking error. Fig. 16(b) demonstrates that the impact of the power load on the tracking error is relatively low when $T_{\rm err} < 0$, while the impact is relatively high when $T_{\rm err} > 0$. Fig. 16(c) illustrates that the tracking error increases as the resonant frequency increases. This is because the proportion of the sampling time drift to the switching cycle increases as the switching frequency increases. When $T_{\rm err}$ is -100 ns, the tracking errors at 100, 200, and 500 kHz are 2%, 4%, and 9%, respectively. To achieve a tracking error less than 5% at 500 kHz, $T_{\rm err}$ should be less than 50 ns, which is not easy to implement. Thus, this method is not recommended for very high switching frequencies, such as 500 kHz and MHz. In fact, hardware deviations of the control circuit also limit the application of other tracking methods at very high frequencies. For example, a deviation in the propagation delay time of tens of nanoseconds of optocouplers and current sensor errors reduce the accuracy of optocoupler-based and secondary diode conduction time-based methods, respectively, at high frequencies.

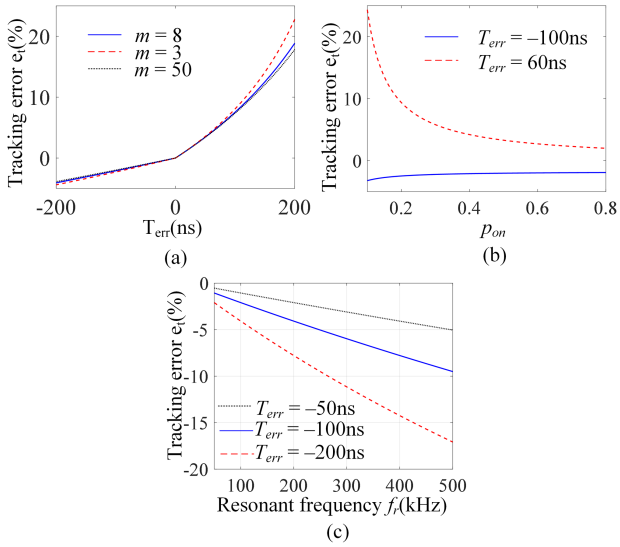

Fig. 16. Tracking errors with (a) various $T_{\rm err}$ and m values at $f_r = 100$ kHz, (b) various loads at $f_r = 100$ kHz, and (c) various switching frequencies.

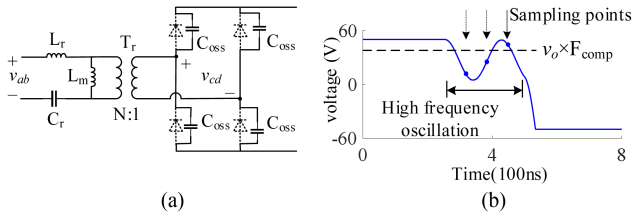

Fig. 17. Influence of the parasitic capacitor $C_{\rm oss}$. (a) $C_{\rm oss}$ in the circuit. (b) Waveforms of v_{cd} and the sampling points.

D. Considering Parasitic Capacitors

The diode or MOSFET in the secondary rectifier of the *LLC* circuit has a parasitic output capacitor of hundreds to thousands of pF. This capacitor is labeled as $C_{\rm oss}$ in the datasheet. In the P-stage, $C_{\rm oss}$ is bypassed by the diode or MOSFET. When the circuit transitions from the P-stage to the O-stage, $C_{\rm oss}$ participates in resonance with the resonant tank, as shown in Fig. 17(a), bringing high-frequency oscillations to the transformer voltage [30], [31], as shown in Fig. 17(b).

As the frequency gradually increases during the frequency tracking process, the peak of the high-frequency oscillation is eventually sensed. If the peak is higher than the comparison value $F_{\rm comp} \times v_o$, according to the tracking logic, the time of

TABLE I
PARAMETERS OF THE *LLC* CONVERTER PROTOTYPE

Parameters	Values
Output voltage range	40–60 V
Turn ratio	4:1
Input voltage range	160–240 V
Resonant inductor (measured, leakage inductance included)	17.8 μH
Resonant capacitor (measured)	142 nF
Magnetic inductor	122.5 μH
Dead time	120 ns
ADC Clock	25 MHz

the peak will be identified as the falling edge of $v_{cd,}$ and the current switching frequency will be incorrectly treated as the resonant frequency, introducing a large error to the resulting frequency.

To overcome this problem, we sample the v_{cd} signal multiple times successively, as shown in Fig. 17(b). This can be achieved by selecting the v_{cd} channel multiple times in the ADC channel select sequencing control registers (ADCCHSELSEQn). The lower value before the oscillation peak in the high-frequency oscillations can then be detected, and the fake falling edge can be identified.

The tracking program is then revised such that when all the sampled points of v_{cd} are larger than $v_o \times F_{\mathrm{comp}}$, the current switching frequency f_s decreases by a small step Δf. Otherwise, f_s increases by a small step Δf. In addition, the SOC signal for the ADC conversion should be advanced by $M \times K$ ADC clocks, where M is the acquisition window length and N is the number of sampling points.

By this method, the interference of the high-frequency oscillation peak is eliminated without impacting the tracking function.

In summary, the implementation of this method mainly relies on two functions of the DSP TMS320F28335. The first is that the ADC sampling can be triggered by the PWM counter. The second is the oversampling function, in which one channel can be sampled multiple times successively with an interval of tens or hundreds of ns. The second function is utilized to eliminate the impact of transformer voltage oscillations due to parasitic capacitors. These two functions are common in industrial MCUs, such as the C2000 series from TI, the STM32 series from ST, and the dsPIC33 series from MICROCHIP. Thus, the method can also be implemented with other common MCUs.

V. EXPERIMENTAL RESULTS

To verify the performance of the proposed method, a 1.5 kW 100 kHz experimental setup composed of several discrete boards and magnetic components is built in a laboratory, as shown in Fig. 18. The rated output voltage is 48 V, and the output voltage range is 40–60 V. The hardware configurations of the circuit are listed in Tables I and II. The inductor ratio m is 8, and the rated p_{on} is 0.5. The hardware parameters conform to the design principles in [32]. To reduce the effect of the dc bias on the resonant inductance, large E70 magnetic cores with large air gaps are used for the resonant inductor. The transformer secondary voltage is sensed for tracking purposes.

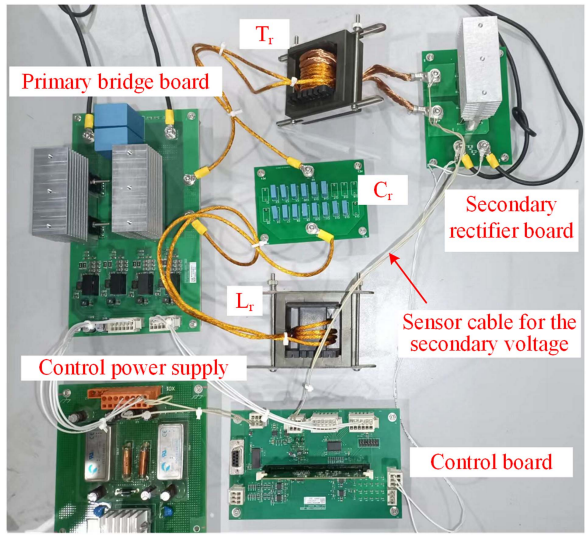

Fig. 18. Experimental setup.

TABLE II
MAIN CHIPS AND MODELS

Chips	Models
Primary bridge MOSFET	IMZA65R048M1H
Secondary bridge MOSFET	Two IPP051N15N5 paralleled
Operational amplifier	LTC6228
Primary driver chip	1ED3124MU12H

A. Test Preparation

1) Software Configuration: The comparison factor F_{comp} is set to 0.85. The frequency adjustment step Δf is 0.1 kHz. ADC sampling and frequency tracking are both executed every switching cycle. The tracking program is located in the interrupt function generated at the end of the sampling sequence. An RS232 upper monitor is used to manually initiate the tracking process.

2) Waveform of $\mathrm{v_{cd}}$*:* To be sensed by the ADC module in the DSP, v_{cd} is attenuated by the conditioning circuit with the high-frequency operational amplifier LTC6228. The output of the conditioning circuit is tested at $p_o = 900$ W ($p_{\mathrm{on}} = 0.3$) and $f_s = 80$ kHz, as depicted in Fig. 19(a). The attenuated v_{cd} signal has good fidelity. Note that in Fig. 19(a), the vertical scale of the attenuated v_{cd} signal is adjusted to have the same scale as v_{cd} for clarity.

Additionally, Fig. 19(a) demonstrates that the period of high-frequency oscillation in the O-stage caused by the parasitic capacitors is approximately 600 ns. To eliminate the interference of high-frequency oscillation on tracking accuracy, the v_{cd} signal is sampled twice successively at 300 ns intervals, as described in Section IV-D.

3) Test of $\mathrm{T_{d\,2}}$ *and Selection of* $\mathrm{T_p}$*:* The T_{d2} delay between the falling edge of the PWM signal generated by the DSP and the primary bridge voltage v_{ab} is found to be 145 ns through testing. This delay includes a driver chip propagation delay of 95 ns and a MOSFET turn-OFF delay of 50 ns. The waveforms are shown in Fig. 19(b).

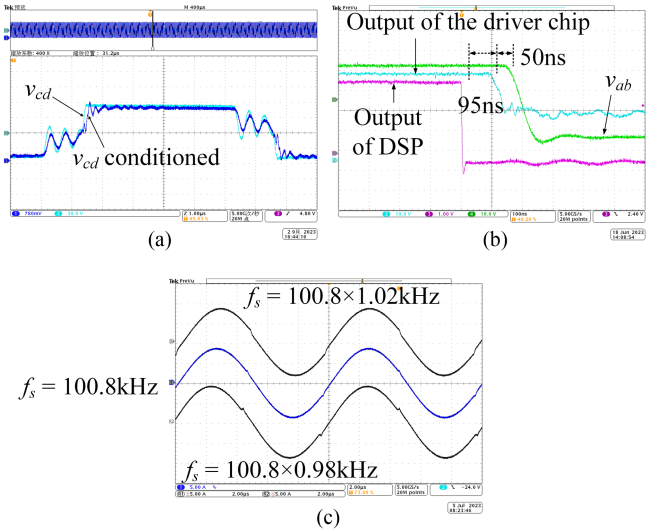

Fig. 19. Test preparation. (a) Conditioned v_{cd}. (b) T_{d2} delay test. (c) Resonant current.

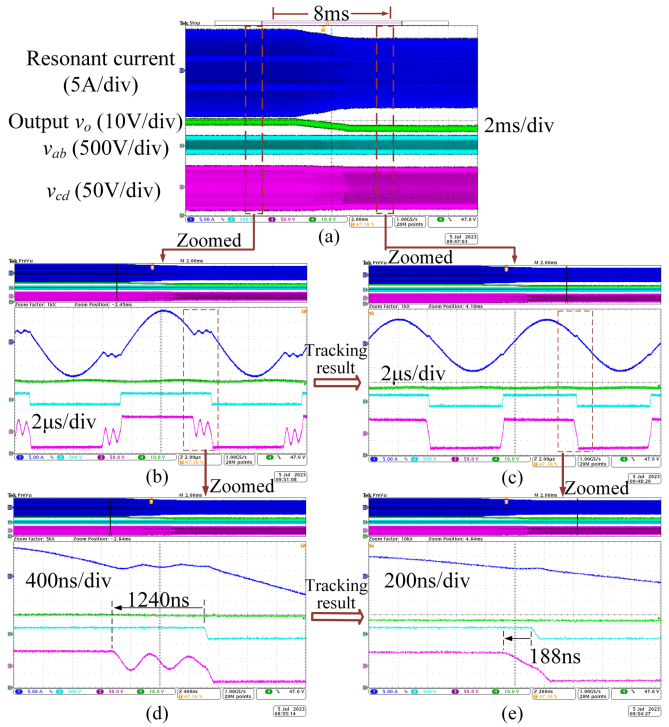

Fig. 20. Tracking process with an initial frequency of 80 kHz, which is 20% smaller than the resonant frequency. (a) Tracking process. (b) Initial waveforms. (c) Resulting waveforms. (d) Enlarged initial waveforms. (e) Enlarged resulting waveforms.

In practice, T_{d2} may vary given individual differences, the environment, and aging. The impacts of the environment and aging are small because the driving resistors and MOSFET parasitic capacitors are quite stable to the environment and aging [33], [34]; the variation occurs mainly due to individual differences, which can be obtained from manufacturer data. For this setup, we assume that the possible variation range of T_{d2} is 145 ± 50 ns.

As described in Section IV, the tracking error with $T_{\rm err} < 0$ is much smaller than that with $T_{\rm err} > 0$, and the resulting PO mode with $T_{\rm err} < 0$ is beneficial for ZVS. Therefore, by setting a large CMPB, $T_{\rm err} < 0$ in the entire variation range of T_{d1} and T_{d2}. Thus, from (12), the following is obtained:

$$T_{\rm err\_max} = T_{d1\_max} - (T_p + T_{d2\_min}) < 0 \qquad (15)$$

With $T_{\rm d1\_max} = 300$ ns and $T_{\rm d2\_min} = 95$ ns, T_p is obtained as $T_p > 205$ ns. In the software, T_p is set to 300 ns; thus, $T_{\rm err}$ generally ranges from –235—-95 ns.

4) Identification of the Actual Resonant Frequency: We assume that at the ideal frequency, the waveform of the resonant current is completely sinusoidal. Considering the measurement error and the effect of the parasitic parameters, we use the ideal frequency instead of the theoretically calculated resonant frequency as the base for evaluating the tracking accuracy. Fig. 19(c) shows the resonant currents at three different frequencies for $p_{\rm on} = 0.3$. As shown, the resonant current at 100.8 kHz is very close to the sinusoidal waveform, whereas the waveform visibly deviates from the sinusoidal wave when the switching frequency is increased or decreased by 2%. Therefore, the ideal frequency at $p_{\rm on} = 0.3$ is selected as 100.8 kHz.

B. Tracking Processes

The tests are conducted with $v_{\rm in} = 190$ V, $p_{\rm on} = 0.3$ ($p_o \approx 800$ W), and $v_o \approx 48$ V, which changes with the working frequency during the tracking process. Two cases are tested: in the first case, the initial switching frequency is 80 kHz, which is 20% lower than the resonant frequency; in the second case, the initial switching frequency is 120 kHz, which is 20% higher than the resonant frequency. The two cases simulate situations where the actual resonant frequency is higher or lower than the preset working frequency due to the deviation of the resonant parameters.

After the circuit begins working and achieves stability, the tracking program is initiated. The waveforms of the tracking processes of the two cases, which are captured by the variation edge of the output voltage, are shown in Figs. 19 and 20. Subfigures (b)–(e) are temporal enlargements of subfigure (a).

Fig. 20(d) and (e) illustrate that before tracking, the falling edge of v_{cd} occurs prior to the falling edge of v_{ab} by –1240 ns, and after the tracking process is completed, the time difference is reduced to -188 ns. Fig. 21(d) and (e) demonstrate that the time difference between the falling edge of v_{ab} and v_{cd} turns from 120 to –188 ns after tracking, which is equal to the previous test case. In addition, the two test cases are tested more than 50 times, and the resulting frequencies converge to the same value. These results indicate that the tracking performance of this method is stable.

The two test cases are also conducted under output voltages of 40 and 60 V, respectively. In the tests, the switching frequencies track the resonant frequency well, which verifies that the proposed method can be used for applications with a wide output voltage range. Because the tracking waveforms of these experiments are identical to those above, for brevity, they are not displayed here.

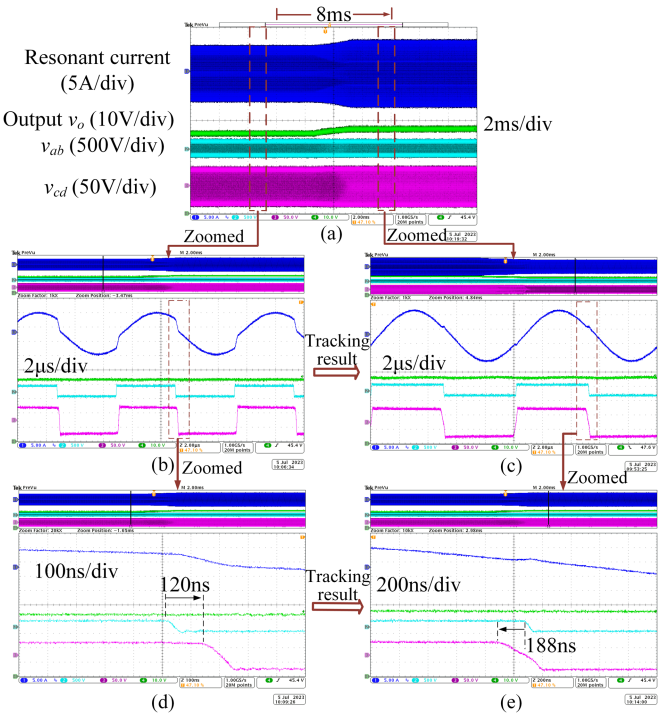

Fig. 21. Tracking process with an initial frequency of 120 kHz, which is 20% greater than the resonant frequency. (a) Tracking process. (b) Initial waveforms. (c) Resulting waveforms. (d) Enlarged initial waveforms. (e) Enlarged resulting waveforms.

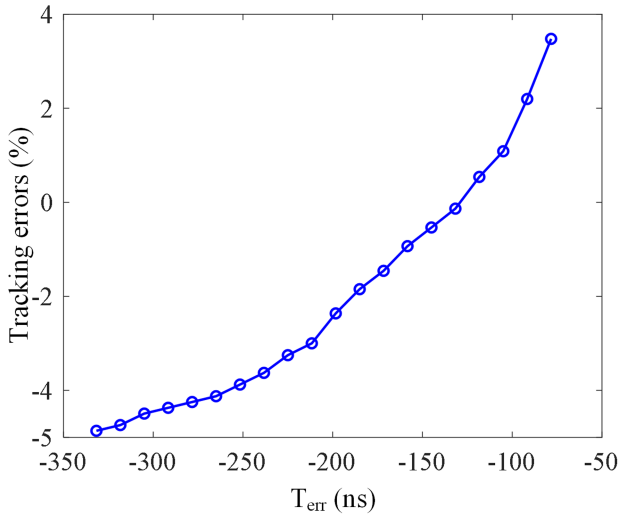

Fig. 22. Variation in the tracking error with $T_{\rm err}$.

C. Influence of the Variation in T_{err}

As T_{d1} and T_{d2} vary, the sampling time deviation $T_{\rm err}$ and the tracking accuracy also vary. Fig. 22 shows the impact of $T_{\rm err}$ on the tracking error by testing. The trend of the curve is the same as that depicted in Fig. 16(a). When the error is above zero, it increases faster. The tracking error is less than 5% within the possible $T_{\rm err}$ range of −235–95 ns.

The $T_{\rm err}$ corresponding to the zero tracking error is –130 ns, not zero, because the falling edge of v_{cd} has a fall time due to the parasitic capacitors, and the equivalent edge is later than the ideal edge, as shown in Fig. 20(e).

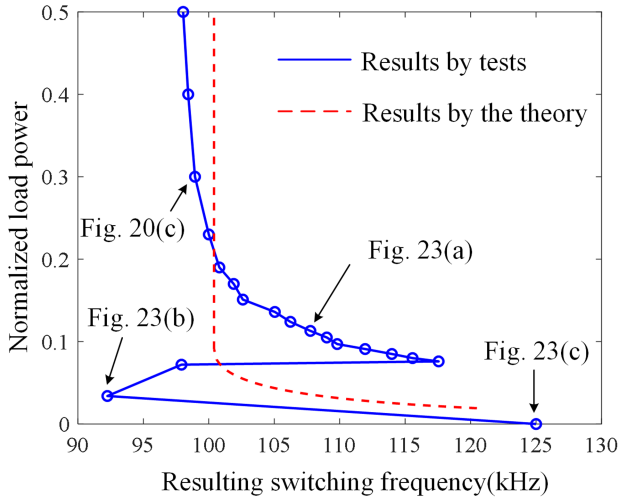

Fig. 23. Resulting switching frequencies at different loads.

D. Performance Under Various Load Powers

The tracking method performance over the entire load range from no load to full load is tested. The resulting switching frequencies are shown in Fig. 23, and the typical electrical waveforms are shown in Fig. 24.

Fig. 23 illustrates that the tracking performance can be divided into four categories. In the range of $0.15 < p_{\rm on} < 0.5$, that is, 510 W $< p_o <$ 1.5 kW, the resulting frequencies are close to the resonant frequency, and the resulting resonant currents are close to sine, as shown in Fig. 20(c). In the range of $0.08 < p_{\rm on} < 0.15$, that is, 270 W $< p_o <$ 510 W, the resulting frequencies quickly diverge from the resonant frequency as the load decreases. However, the resonant currents are still quite sinusoidal, as shown in Fig. 24(a). In the range of $0 < p_{\rm on} < 0.08$, that is, 0 W $< p_o <$ 270 W, the resulting frequencies are smaller than the resonant frequency. The multiple sampling approach described in Section IV-D can extend the applicable range in light loads, but when the load is too small and v_{cd} in the O-stage is too close to the output voltage, as shown in Fig. 24(b), the method loses efficacy. At $p_{\rm on} = 0$, that is, at an empty load, the resulting frequency is 125 kHz, which is the preset upper limit in the software. Fig. 24(c) shows that at an empty load, the transformer secondary voltage oscillates, and the output voltage equals the oscillating peak due to the unidirectional rectifier. This means that the secondary voltage at the falling edge of v_{ab} is always smaller than the output voltage and that the resulting frequency always increases during the tracking process.

In practice, the applicable range of the tracking method for this setup can be set to $p_{\rm on} > 0.15$. In this range, a sinusoidal resonant current can be obtained, the steep transition at $p_{\rm on} = 0.08$ can be avoided, and the switching frequencies are not significantly greater than the resonant frequency, which can lower the switching loss. Thus, 70% of the rated load power can be within this range.

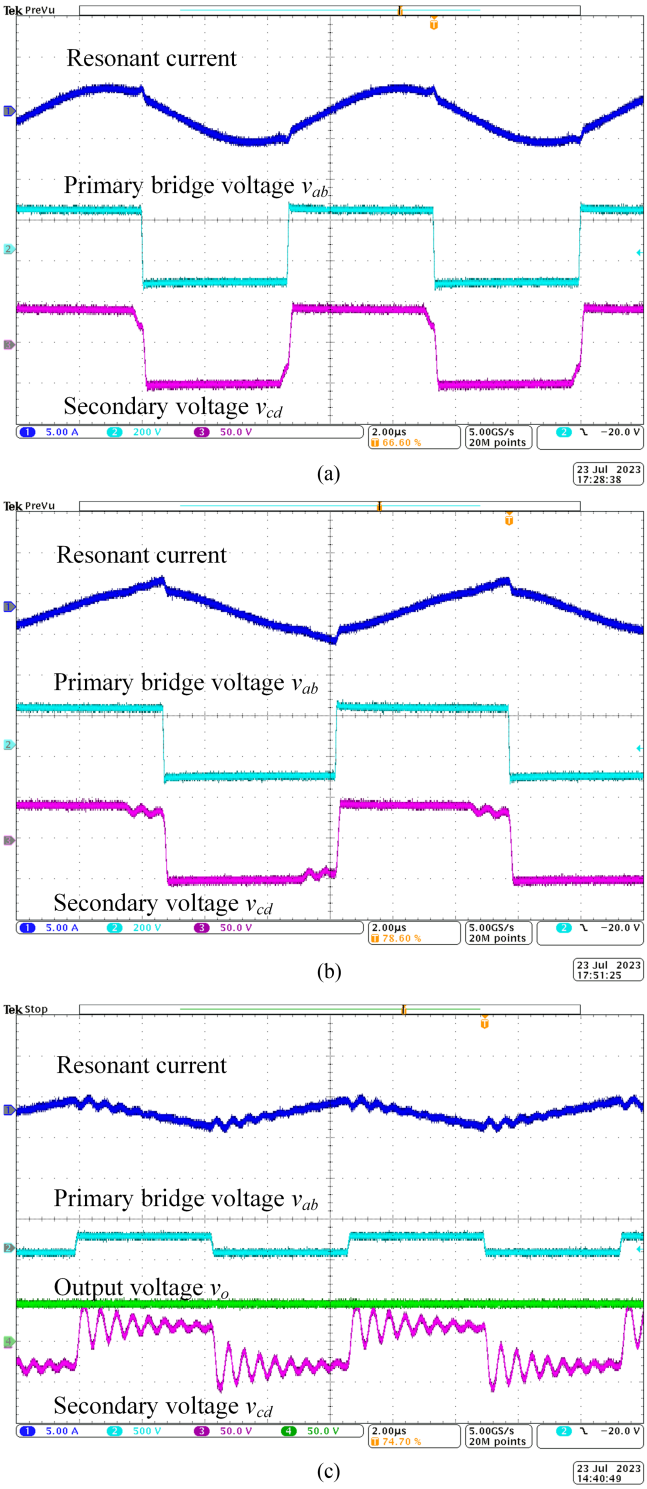

Fig. 24. Typical waveforms at different loads. (a) $p_{\rm on} = 0.11$. (b) $p_{\rm on} = 0.03$. (c) $p_{\rm on} = 0$.

In Fig. 23, the theoretical tracking curves are also presented. The trend of the actual tracking result curve is consistent with the theoretical curve, but there are also differences. In the range of high loads, the two curves are very close, tracking the resonant frequency. In the lower load range, both curves rapidly shift to the right, tracking the boundary line of the OPO and NOP modes. This indicates that the theoretical analysis of the load range in Section III is reliable. However, due to the influence of parasitic parameters, especially parasitic capacitance, the turning point of the actual curve is greater than that of the theoretical curve.

VI. Conclusion

In this study, an automatic frequency tracking method based on the instant transformer voltage at the falling edge of the primary bridge voltage is proposed. The method is digitally implemented with a DSP TMS320F28335 and verified on a 1.5 kW experimental setup with various output voltages. The method is comprehensive, with the applicable range, impact of parasitic capacitors and parameter deviation of the control circuit clearly discussed. The analysis of the applicable load range is also adapted to other existing methods.

The advantages of this method include that it can handle circuits well in applications with broad output voltage ranges and high output current, such as high-power battery chargers. For this situation, this method has a wider load range and a higher accuracy than existing methods based on optocouplers and voltage ratios. Additionally, the method is fast, simple, and insensitive to noise. However, this method is not suitable for situations with very high switching frequencies, such as 500 kHz or MHz, because the tracking accuracy relative to the switching frequency decreases due to the ADC sampling time deviation.

The proposed method is a practical candidate for products using unregulated *LLC* circuits.

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