A New Insight on Four-Level Neutral Point Clamped Converters: Four-Level = Two-Level + Three-Level

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***Abstract*—This article proposes a new insight on the four-level neutral point clamped converters: Four-level = two-level + three-level. With the proposed idea, every four-level neutral point clamped converter topology can be regarded as a hybrid combination of a two-level converter and a three-level converter. Thus, the common and complex capacitor voltage imbalance issue of four-level neutral point clamped converters can be simplified into closed loop control of the two-level converter unit and simple voltage balancing control of the three-level converter unit. Specifically, the middle capacitor voltage balancing control is realized based on the two-level converter unit using a variable-reference modulation scheme, while the upper and lower capacitor voltages are balanced based on the three-level converter unit using zero sequence voltage injection methods. Simulation and experimental results have been conducted on a four-level active neutral point clamped converter as an example to verify the proposed idea and the proposed voltage balancing control methods.**

***Index Terms*—Four-level converter, voltage balancing control, zero sequence voltage injection.**

I. Introduction

FOUR-LEVEL neutral point clamped (NPC) converters can be used in low and medium-voltage industrial applications, including motor drive, wind power generation, solar generation, and uninterruptible power supply (UPS). For example, Schneider Electric built a UPS product with 1.25 MW power rating based on a four-level active NPC (4L-ANPC) converter in 2016. It is claimed that the four-level product achieve 2.1% efficiency improvement compared to the three-level counterpart [1]. Wang et al. [2] reported a 100 kW/1.2 kV electric vehicle powertrain system based on 4L-ANPC converter and SiC power modules.

In general, the four-level NPC converters include the conventional four-level NPC converter [3], 4L-ANPC converter [4], [5], four-level nested converter [6], [7], four-level dual T-type converter [8], the four-level five-switch converter [9], four-level hybrid NPC converter [10], and four-level hybrid clamped converter [11], [12]. However, the four-level NPC converters are less commercialized than three-level NPC converters due to the complex voltage balancing control of the three series-connected capacitor voltages at the dc-link side. In the commercialized product [1], the capacitor voltage imbalance issue is overcome using additional switched-capacitor resonant circuits [13], which inevitably leads to increased power loss, size, and weight. In contrast, voltage balancing methods are more appealing.

As there are no redundant switching states, the three capacitor voltages are prone to imbalance if using the conventional level-shifted carrier modulation or the space vector pulsewidth modulation (PWM) method [3], [4], [14], [15]. Besides, the limits of voltage balancing control for four-level NPC converters have been highlighted in [16] that the dc-link capacitor voltages are difficult to be balanced at high modulation indices and high power factors. To address this issue, some new modulation methods have been proposed, including a virtual vector PWM [17], [18] along with its corresponding carrier-based implementation method [19], carrier-overlapped PWM method [20], variable-carrier method [8], [9], [21], variable-reference method [22], [23], variable-angle method [24], and other closed-loop methods [25], [26], [27], [28]. Comparatively, the variable-reference method is easier to implement in a digital chip.

The variable-reference method is essentially the same as the variable-carrier method, which aims to control the middle capacitor voltage at 1/3 of the dc-link voltage while the upper and lower capacitor voltages are automatically balanced under ideal condition. However, considering practical applications, there is voltage drift between the upper capacitor voltage and the lower capacitor voltage. Besides, there are triple-fundamental-frequency voltage fluctuations on the upper and lower capacitors when the four-level NPC converters operate at low fundamental frequency conditions. The voltage drift and low-frequency voltage fluctuations will make blocking voltages across power switches easily go beyond their safety margins. Moreover, the output phase-to-phase voltages will contain low-frequency harmonics [29], [30].

To overcome the problems above, this article proposes to treat every four-level NPC converter as a hybrid topology configuration consisting of a two-level converter unit and a three-level converter unit. Based on this idea, a joint approach consisting of the variable-reference voltage balancing control for the middle

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TABLE I
SWITCHING STATES OF FOUR-LEVEL NPC CONVERTERS

Voltage Level	S_{x1}	S_{x2}	S_{x3}
$U_{dc}/2$	1	1	1
$U_{dc}/6$	0	1	1
$-U_{dc}/6$	0	0	1
$-U_{dc}/2$	0	0	0

capacitor voltage and the zero sequency voltage (ZSV) injection control for the upper and lower capacitor voltages, is proposed in this article.

The rest of this article is organized as follows. Section II analyzes the capacitor voltage imbalance mechanism of four-level NPC converters with the conventional level-shifted carrier modulation. Section III presents the proposed "variable-reference + ZSV injection" methods, Section IV presents simulation results and comparative analysis of the existing method and the proposed methods. Experimental verifications of the proposed methods are carried out in Section V. Finally, Section VI concludes this article.

II. NEW INSIGHT ON FOUR-LEVEL CONVERTERS

A. New Idea "Four-Level = Two-Level + Three-Level"

A concept of four-level (4L) = two-level (2L) + three-level (3L) is proposed. Every four-level NPC converter can be divided into one two-level converter unit and one three-level converter unit.

1) The 4L-NPC-I converter in Fig. 1(a) can be viewed as a combination of a two-level converter (C_2, S_{x2}, S_{x2}') and a 3L-NPC converter (C_1, C_3, S_{x2}, S_{x3}, S_{x1}', S_{x2}', D_{x3}, D_{x4}).
2) The 4L-NPC-II converter in Fig. 1(b) can be viewed as a combination of a two-level converter (C_2, S_{x2}, S_{x2}') and a 3L-NPC converter (C_1, C_3, S_{x1}, S_{x3}, S_{x1}', S_{x3}').
3) The 4L-ANPC converter in Fig. 1(c) can be viewed as a combination of a two-level converter (C_2, S_{x2}, S_{x2}') and a 3L-ANPC converter (C_1, C_3, S_{x1}, S_{x1}', S_{x3}, S_{x3}').
4) The 4L-Nested converter in Fig. 1(d) is a transformation of the 4L-ANPC converter.
5) The 4L-DT converter in Fig. 1(e) can be viewed as a combination of a two-level converter (C_2, S_{x2}, S_{x2}') and a 3L-T converter (C_1, C_3, S_{x1}, S_{x1}', S_{x3}, S_{x3}').
6) The 4L-5S converter in in Fig. 1(f) can be regarded as a transformation of the 4L-DT converter.
7) The 4L-HNPC converter in Fig. 1(g) can be viewed as a combination of a two-level converter (C_2, S_{x2}, S_{x2}') and a 3L-NPC converter (C_1, C_3, S_{x1}, S_{x1}', S_{x3}, S_{x3}', D_{x1}, D_{x2}).
8) The 4L-HANPC converter in Fig. 1(h) can be viewed as a combination of a two-level converter (C_2, S_{x2}, S_{x2}') and a 3L-ANPC converter (C_1, C_3, S_{x1}, S_{x1}', S_{x3}, S_{x3}', S_{x4}, S_{x5}).

For any four-level NPC converter, its output voltage level depends on the switching state combination (S_{x1}, S_{x2}, S_{x3}), as shown in Table I. Each voltage level corresponds to one switching state: $U_{dc}/2$ corresponds to (1, 1, 1); $U_{dc}/6$ corresponds to (0, 1, 1); $-U_{dc}/6$ corresponds to (0, 0, 1); $-U_{dc}/2$ corresponds to (0, 0, 0). The above correspondences are easily satisfied for the four-level NPC converters in Fig. 1(c)–(e) and (g). As for the 4L-5S topology in Fig. 1(f), one IGBT (S_{x0}) and two diodes replace the two switches S_{x1}' and S_{x3} in Figs. 1(a)–(e), and S_{x0} is denoted as $S'_{x1} \cap S_{x3}$. As for the 4L-HANPC converter in Fig. 1(h), the switching signals of S_{x4} and S_{x5} are the same as those of S'_{x1} and S_{x3}, respectively.

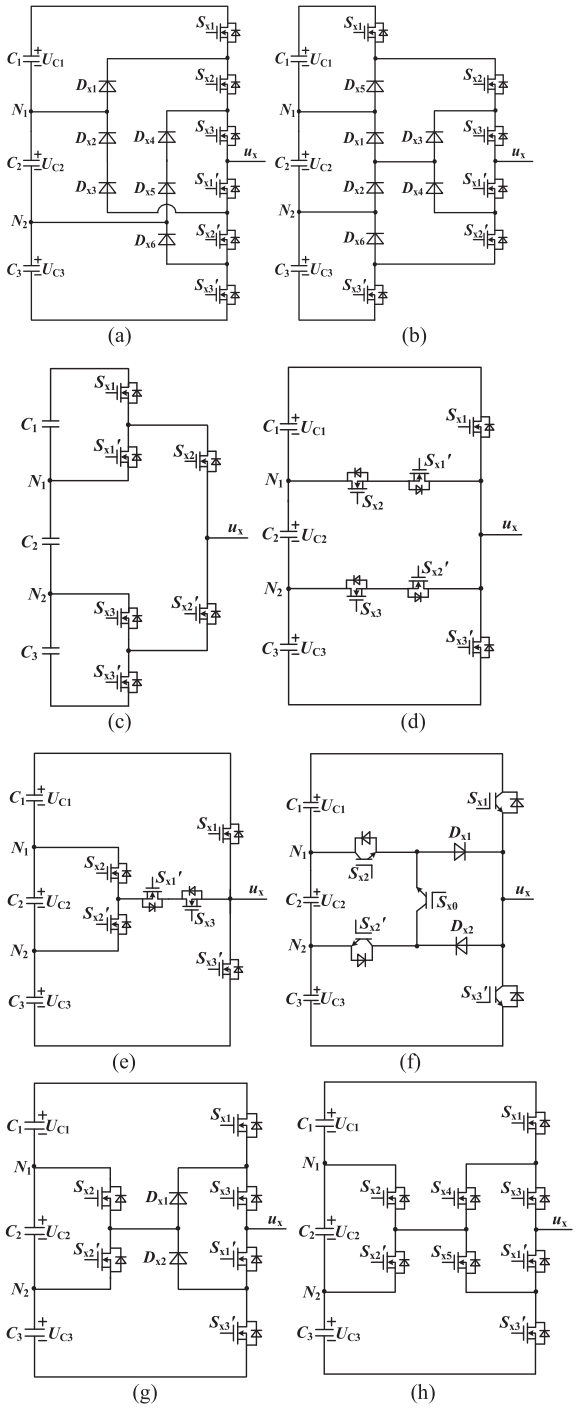

Fig. 1. Existing four-level NPC converter topologies. (a) 4L-NPC-I. (b) 4L-NPC-II. (c) 4L-ANPC. (d) 4L-Nested. (e) 4L-DT. (f) 4L-5S. (g) 4L-HNPC. (h) 4L-HANPC.

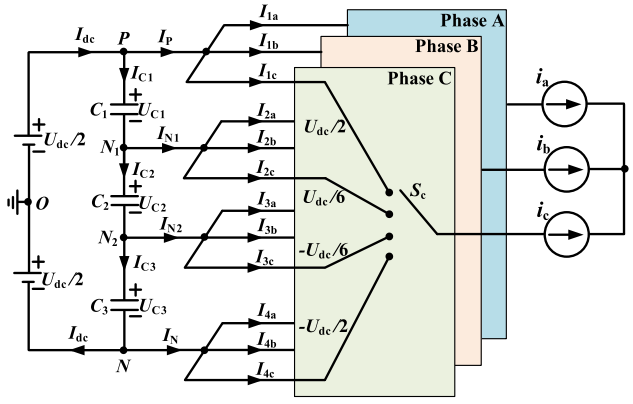

Fig. 2. Simplified model of four-level NPC converters.

From the modulation view of point, the two 4L-NPC converters in Fig. 1(a) and (b) can be viewed as a combination of a two-level converter and a 3L-NPC converter. On the one hand, S_{x1} and S_{x3} are both turned ON to obtain the voltage level $U_{dc}/2$, and both OFF to obtain the voltage level -$U_{dc}/2$. Besides, when S_{x1} is turned OFF and S_{x3} is turned ON, the voltage levels $\pm U_{dc}/6$ can be achieved. C_1, C_3, S_{x1}, S_{x3}, S_{x1}', S_{x3}' develop a 3L-NPC converter. On the other hand, S_{x2} is turned ON to achieve the positive voltage levels and OFF to obtain the negative voltage levels. Therefore, C_2, S_{x2}, and S_{x2}' develop a two-level converter. Furthermore, when $U_{C2} = 0$ and $U_{C1} = U_{C3} = U_{dc}/2$, the neutral points N_1 and N_2 have the same potential, which is equated to the neutral point of the 3L-NPC converter. In this case, the output voltage is degraded to three levels: (1, 1, 1) corresponds to $U_{dc}/2$; both (0, 1, 1) and (0, 0, 1) correspond to 0; (0, 0, 0) corresponds to -$U_{dc}/2$. The output voltage level changing between $U_{dc}/2$ and 0 depends on S_{x1}, while changing between -$U_{dc}/2$ and 0 depends on S_{x3}. The 4L-NPC converter, is viewed as a superposition of a pair of $\pm U_{dc}/6$ determined by S_{x2} and S_{x2}' only at the voltage level 0 of the 3L-NPC converter.

As a summary, structurally not all four-level NPC converter topologies can be intuitively decomposed into combinations of 2L and 3L converter structures. But from the modulation point of view, the modulation of any four-level NPC converter topology can be simplified to a combination of 2L modulation and 3L modulation, which generate the switching signals S_{x2} and (S_{x1}, S_{x3}), respectively. This is the root cause of the proposed idea "4L = 2L + 3L" in this article.

B. Capacitor Voltage Imbalance Mechanism Analysis

To reveal the capacitor voltage imbalance mechanism of four-level NPC converters, a general simplified mathematic model is built in [31]. It is presented in Fig. 2 where two split dc sources are provided to develop a virtual ground. I_{dc} is the average input current, and I_{C1}, I_{C2}, I_{C3} are the average currents flowing through C_1, C_2, C_3, respectively. I_{1x}, I_{2x}, I_{3x}, I_{4x} (x = a, b, c) are the average branch currents flowing through the terminals P, N_1, N_2, and N into each phase leg. I_P, I_{N1}, I_{N2}, I_N are the average currents flowing out of the terminals P, N_1, N_2, and N. It should be noted that all the average currents mentioned above are defined during one fundamental period.

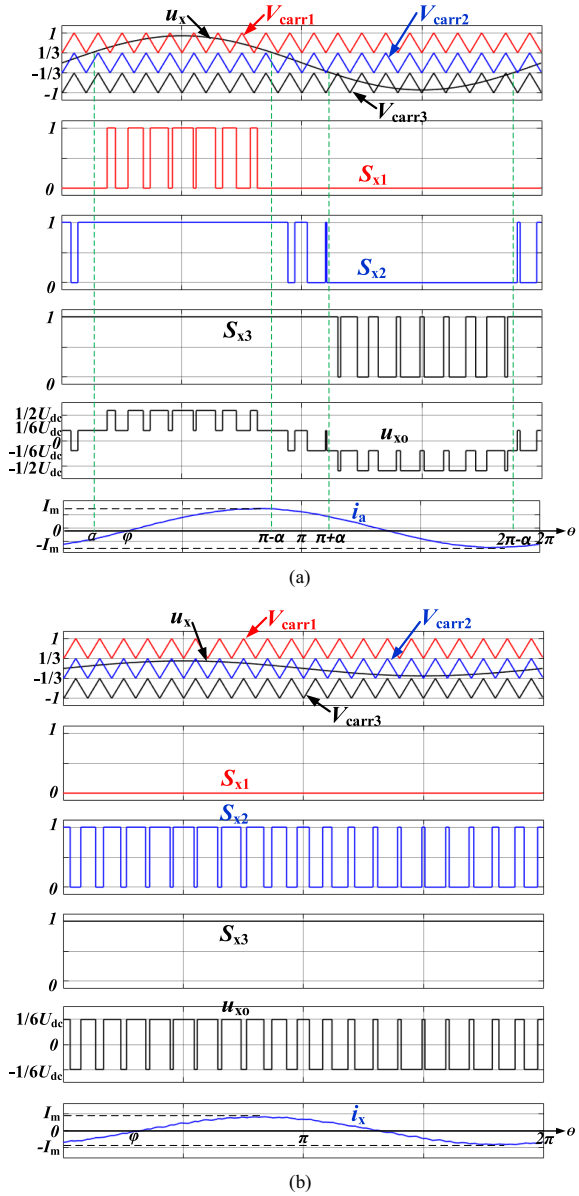

Fig. 3. PWM patterns of power switches S_{x1}, S_{x2}, S_{x3} and the phase voltage and current. (a) when $1/3 < m \leq 1$. (b) when $0 < m \leq 1/3$.

According to the conventional level-shifted carrier modulation scheme in Fig. 3(a) [4], three triangular carriers V_{carr1}, V_{carr2}, and V_{carr3} with the same carrier frequency f_s and amplitude $2/3V_m$ are compared with the reference signal u_x (x = a, b, c) to generate the gate signals of S_{x1}/S_{x1}', S_{x2}/S_{x2}', and S_{x3}/S_{x3}'. The reference signal u_{refx} is given in (1) where m is the modulation index, f_m is the fundamental frequency, and ϕ_x (x = a, b, c) is equal to 0 for Phase A, -2π/3 for Phase B, and 2π/3 for Phase C, respectively, as follows:

$$u_{refx} = m \sin(\theta + \phi_x); \ \theta = 2\pi f_m t. \tag{1}$$

The output phase currents i_a, i_b, and i_c in Fig. 3 can be unified by i_x (x = a, b, c), as shown in (2). Besides, I_m is the peak phase current and φ is the power factor angle

$$ix = I_m \sin(\theta + \phi_x - \varphi). \tag{2}$$

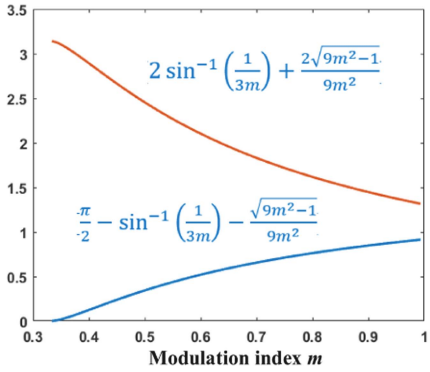

Fig. 4. Mathematical value comparison.

Taking one phase leg as an example, the switching angle α in Fig. 3(a) meets for

$$m \sin \alpha = \frac{1}{3}. \tag{3}$$

As presented in [31], when the modulation index m is over 1/3, the average capacitor currents are obtained by

$$\begin{cases} I_{\mathrm{C}}1 = I_{\mathrm{C}}3 = I_{\mathrm{dc}} - \frac{9mI_m \cos\varphi}{4\pi}\left[\frac{\pi}{2} - \sin^{-1}\left(\frac{1}{3m}\right) - \frac{\sqrt{9m^2-1}}{9m^2}\right] \\ I_{\mathrm{C}}2 = I_{\mathrm{dc}} - - \frac{9mI_m \cos\varphi}{4\pi}\left[2\sin^{-1}\left(\frac{1}{3m}\right) + \frac{2\sqrt{9m^2-1}}{9m^2}\right]. \end{cases} \tag{4}$$

According to the value comparison in Fig. 4, $I_{\mathrm{C}1}$ is equal to $I_{\mathrm{C}3}$, but they are both higher than $I_{\mathrm{C}2}$ when m is over 1/3.

Similarly, when m is less than 1/3, there is

$$\begin{cases} I_{\mathrm{C}}1 = I_{\mathrm{C}}3 = I_{\mathrm{dc}} \\ I_{\mathrm{C}}2 = I_{\mathrm{dc}} - - \frac{9mI_m}{4} cos\varphi. \end{cases} \tag{5}$$

Overall, $I_{\mathrm{C}1}$ is equal to $I_{\mathrm{C}3}$, but they are both higher than $I_{\mathrm{C}2}$ when the modulation index m is among (0, 1]. It means the middle capacitor C_2 is charged less than C_1 and C_3 without any voltage balancing circuit or voltage balancing control method. Eventually, the middle capacitor voltage $U_{\mathrm{C}2}$ will be discharged to zero while C_1 and C_3 share the dc-link voltage U_{dc} equally. This is the root cause of the capacitor voltage imbalance of the four-level NPC converters.

III. Proposed "Variable-Reference + ZSV Injection" Voltage Balancing Control Methods

According to the idea "4L = 2L + 3L", new voltage balancing methods are proposed to solve the capacitor voltage imbalance issue of the four-level NPC converters, including two parts: 1) the middle capacitor voltage balancing control and 2) the upper and lower capacitor voltage balancing control.

A. Middle Capacitor Voltage Balancing Control Based on Variable-reference Modulation

The authors have proposed variable-carrier modulation and variable-reference modulation schemes to realize capacitor voltage balancing control of the four-level NPC converters [8], [22]. Essentially, the two voltage balancing methods are equivalent and they aim to control the middle capacitor voltage $U_{\mathrm{C}2}$ at

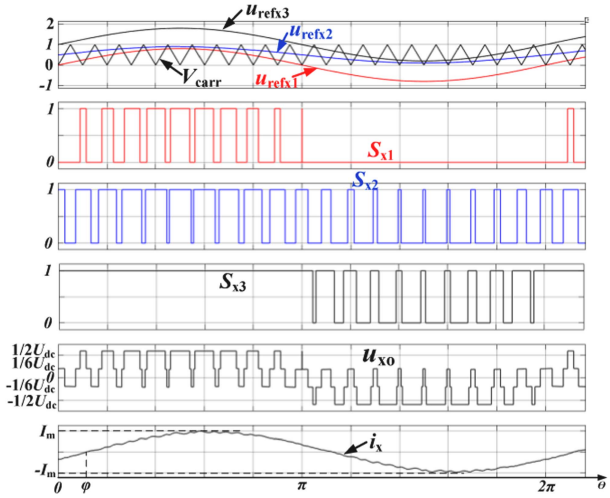

Fig. 5. Key waveforms when using the variable-reference scheme.

$1/3U_{\mathrm{dc}}$ with a proportional-integral (PI) regulator. The voltage control error of $U_{\mathrm{C}2}$ is defined by

$$\Delta U_{\mathrm{C}2} = \frac{1}{3}(U_{\mathrm{C}1} + U_{\mathrm{C}2} + U_{\mathrm{C}3}) - U_{\mathrm{C}2}. \tag{6}$$

Taking the variable-reference voltage balancing method in [22] as an example, the reference signal $u_{\mathrm{ref}x}$ is reshaped into three new reference signals $u_{\mathrm{ref}x1}$, $u_{\mathrm{ref}x2}$, and $u_{\mathrm{ref}x3}$ in

$$\begin{cases} u_{\mathrm{ref}}x1 = u_{\mathrm{ref}}x \\ u_{\mathrm{ref}}x2 = \frac{u_{\mathrm{ref}}x + 1}{k} \\ u_{\mathrm{ref}}x3 = u_{\mathrm{ref}}x + 1. \end{cases} \tag{7}$$

The PI regulator outputs a parameter k that can be used to reshape a new reference signal $u_{\mathrm{ref}x2}$. Besides, the other two reshaped reference signals $u_{\mathrm{ref}x1}$ and $u_{\mathrm{ref}x3}$ are level-shifted with the value of 1 that is the amplitude of the triangular carrier V_{carr}. Finally, $u_{\mathrm{ref}x1}$, $u_{\mathrm{ref}x2}$, and $u_{\mathrm{ref}x3}$ are compared with V_{carr} to output the PWM signals of the switches S_{x1}/S_{x1}', S_{x2}/S_{x2}', S_{x3}/S_{x3}'. Though the variable-reference voltage balancing method has been proposed in [22] by the author of this article, the capacitor voltage balancing mechanism of it was missing before. In this article, this work is added to make the variable-reference scheme comprehensively understood.

The PWM patterns of $S_{\mathrm{x}1}$, $S_{\mathrm{x}2}$, $S_{\mathrm{x}3}$, the phase voltage waveform u_{xo} and the phase current waveform i_{x} are presented in Fig. 5. Generally, the switching frequency is much higher than the fundamental frequency and, thus, the reference signal can be regarded as constant in one switching period. Therefore, according to the reference signals in (7), the duty cycles of $S_{\mathrm{x}1}$, $S_{\mathrm{x}2}$, and $S_{\mathrm{x}3}$ are easy to obtain by

$$d_{Sx1} = \begin{cases} m\sin(\theta + \phi_x) & 0 < \theta + \phi_x \le \pi \\ 0 & \pi < \theta + \phi_x \le 2\pi \end{cases} \tag{8}$$

$$d_{Sx2} = \frac{m}{k}\sin(\theta + \phi_x) + \frac{1}{k} \quad 0 < \theta + \phi_x \le 2\pi \tag{9}$$

$$d_{Sx3} = \begin{cases} 1 & 0 < \theta + \phi_x \le \pi \\ 1 + m\sin(\theta + \phi_x) & \pi < \theta + \phi_x \le 2\pi \end{cases}. \tag{10}$$

The average current I_{1x} is related to the voltage level $U_{dc}/2$, which can be achieved when S_{x1} is turned ON during $[0, 2\pi]$ of Fig. 5. Thus, it is expressed by

$$I_{1x} = \frac{1}{2\pi} \int_0^{2\pi} d_{Sx1} i_x d\theta = \frac{m I_m \cos\varphi}{4}. \tag{11}$$

The average current I_{2x} is related to the voltage level $U_{dc}/6$, which can be achieved when S_{x2} is turned ON and S_{x1} is turned OFF during $[0, \pi]$, and achieved when S_{x2} is turned ON during $[\pi, 2\pi]$, as shown in Fig. 5. Thus, I_{2x} can be expressed by

$$\begin{aligned} I_{2x} &= \frac{1}{2\pi} \int_0^{\pi} (d_{Sx2} - d_{Sx1}) i_x d\theta + \frac{1}{2\pi} \int_{\pi}^{2\pi} d_{Sx2} i_x d\theta \\ &= \frac{(2-k)\, m I_m}{4k} \cos\varphi. \end{aligned} \tag{12}$$

The average current I_{3x} is related to the voltage level $-U_{dc}/6$, which can be achieved when S_{x2} is turned OFF during $[0, \pi]$, and achieved when switch S_{x3} is turned ON and S_{x2} is turned OFF during $[\pi, 2\pi]$, as shown in Fig. 5. Thus, I_{2x} can be expressed by

$$\begin{aligned} I_{3x} &= \frac{1}{2\pi} \int_0^{\pi} (1 - d_{Sx2})\, i_x d\theta + \frac{1}{2\pi} \int_{\pi}^{2\pi} (d_{Sx3} - d_{Sx2})\, i_x d\theta \\ &= -\frac{(2-k)\, m I_m}{4k} \cos\varphi. \end{aligned} \tag{13}$$

The average current I_{4x} is related to the voltage level $-U_{dc}/2$, which can be achieved when S_{x3} is turned OFF during $[\pi, 2\pi]$ of Fig. 5. Thus, it can be expressed by

$$I_{4x} = \frac{1}{2\pi} \int_{\pi}^{2\pi} (1 - d_{Sx3})\, i_x d\theta = -\frac{m I_m \cos\varphi}{4}. \tag{14}$$

According to (8)–(14), there are

$$\begin{cases} I_{C}1 = I_{C}3 = I_{dc} - - \frac{3 m I_m \cos\varphi}{4} \\ I_{C}2 = I_{dc} - - \frac{3 m I_m \cos\varphi}{2k}. \end{cases} \tag{15}$$

According to (15), all the three average capacitor currents I_{C1}, I_{C2}, and I_{C3} are equal under ideal conditions when k is equal to 2 theoretically. However, considering practical parameter inconsistency and dynamic conditions, a PI regulator is required in the variable-reference scheme to regulate and stabilize k at 2 to balance U_{C2}. Furthermore, the PI regulator operates at the switching period to guarantee the middle capacitor voltage U_{C2} is charged and discharged during every switching period. Therefore, there is not any low-frequency voltage fluctuations on U_{C2}.

B. Voltage Balancing Control of the Upper and Lower Capacitors Based on ZSV Injection

According to (15), the upper and lower capacitor voltages should be automatically balanced during one fundamental period. However, there are large triple-fundamental-frequency voltage fluctuations on C_1 and C_3 in practical applications. This can be found from the experimental results in [22] even though a third harmonic is injected. In fact, low-frequency voltage fluctuation on the dc-link capacitors is a common issue of three-level NPC converters [32].

According to the proposed idea "4L = 2L + 3L", the upper and lower capacitors serve as the dc-link capacitors of the 3L inverter unit. Therefore, theoretically any ZSV injection method for 3L converters can be applied to balance the upper and lower capacitor voltages of the four-level NPC converters. In this section, two different ZSV injection methods are utilized and discussed.

1) ZSV Injection Method I: Referring to the ZSV injection method for three-level converters [32], [33], the reference signal u_{refx} in (1) is reshaped into two reference signals u_{refx1} and u_{refx3} with a ZSV signal u_{zx} injected per phase leg

$$\begin{aligned} u_{zx} = k_{zp} * |U_{c1} - U_{c3}| * \text{sign}\left[i_x * (U_{c1} - U_{c3})\right] * \\ \text{sign}\left[0.5 \max(u_a,\ u_b, u_c) - 0.5 \min(u_a,\ u_b, u_c) - 1\right]. \end{aligned} \tag{16}$$

As presented in (16), the term $k_{zp}*|U_{C1}–U_{C3}|$ defines the absolute value of the ZSV signal u_{zx}, and the term sign(i_x*(U_{C1} – U_{C3}))*sign(0.5 max(u_a, u_b, u_c) - 0.5 min(u_a, u_b, u_c) - 1) defines a sign of u_{zx}. The reshaped reference signals u_{refx1} and u_{refx3} are compared with the triangular carrier signal V_{carr} to output the PWM signals of S_{x1}, S_{x1}', S_{x3}, and S_{x3}'.

Finally, with the variable-reference modulation scheme and the ZSV injection method I, three reference signals u_{refx1}, u_{refx2}, and u_{refx3} for each phase leg are summarized in (17). Thus, the proposed voltage balancing method I is presented in Fig. 6(a)

$$\begin{cases} u_{ref}x1 = 0.5 u_{ref}x - 0.5 \min(u_{refa}, u_{refb}, u_{refc}) + u_{zx} \\ u_{ref}x2 \\ = \frac{u_{ref}x - 0.5\min(u_{refa},u_{refb},u_{refc}) - 0.5\max(u_{refa},u_{refb},u_{refc}) + 1}{k} \\ u_{ref}x3 = 0.5 u_{ref}x - 0.5 \max(u_{refa}, u_{refb}, u_{refc}) + 1 + u_{zx}. \end{cases} \tag{17}$$

2) ZSV Injection Method II: In the ZSV injection method I, there are three ZSV signals u_{za}, u_{zb}, and u_{zc} in total and they are related to the phase currents. In this section, a second ZSV injection method called ZSV injection method II is introduced. In the ZSV injection method II, there is only one common ZSV signal u_{com}, which is obtained via a second PI regulator with the input definition

$$\Delta U_{C13} = U_{C1} - U_{C3}. \tag{18}$$

Finally, the three reshaped reference signals u_{refx1}, u_{refx2}, and u_{refx3} for each phase leg are summarized in (19) and the proposed voltage balancing method II is presented in Fig. 6(b)

$$\begin{cases} u_{ref}x1 = 0.5 u_{ref}x - 0.5 \min(u_{refa}, u_{refb}, u_{refc}) + u_{com} \\ u_{ref}x2 \\ = \frac{u_{ref}x - 0.5\min(u_{refa},u_{refb},u_{refc}) - 0.5\max(u_{refa},u_{refb},u_{refc}) + 1}{k} \\ u_{ref}x3 = 0.5 u_{ref}x - 0.5 \max(u_{refa}, u_{refb}, u_{refc}) + u_{com} + 1 \end{cases} . \tag{19}$$

In the two ZSV injection methods above, the ZSV signals are injected into the two reference signals u_{refx1} and u_{refx3}. The dual-reference-signal modulation is helpful to suppress the low-frequency voltage fluctuations as it increases switching transitions to enable the upper and lower capacitors to be charged and discharged during one switching period. Meanwhile, the ZSV injection can eliminate the voltage drift between the upper

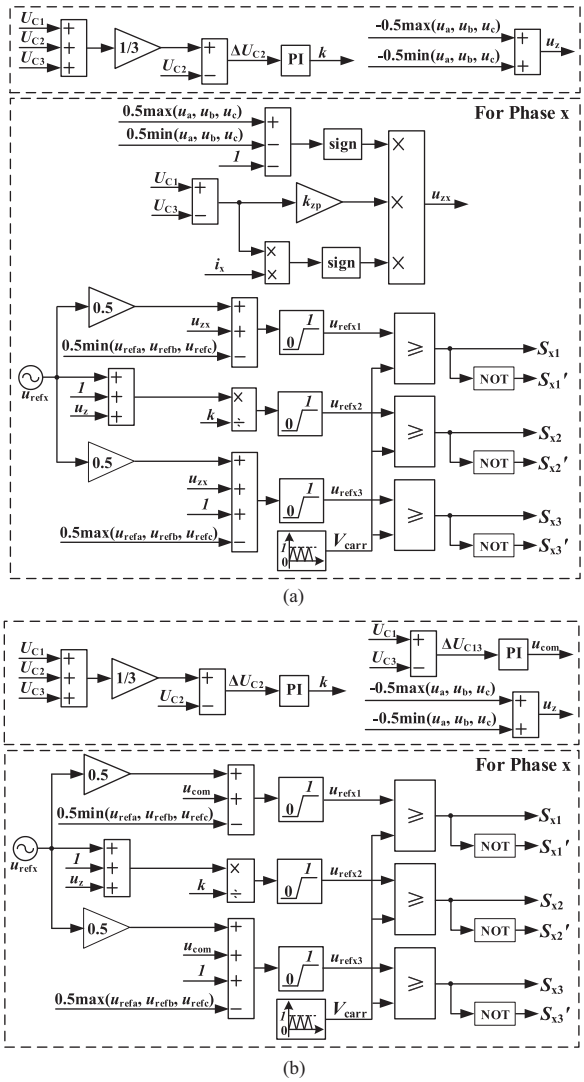

Fig. 6. Proposed voltage balancing methods. (a) Variable-reference + ZSV injection I. (b) Variable-reference + ZSV injection II.

and lower capacitor voltages. In addition, the ZSV signals are injected into $u_{\mathrm{refx}1}$ and $u_{\mathrm{refx}3}$, and a third harmonic voltage u_{Z} is injected into $u_{\mathrm{refx}2}$. They are effective to enhance the dc input voltage utilization ratio.

According to the proposed idea "4L = 2L + 3L," combining the variable-reference modulation scheme and two different ZSV injection methods can develop two different voltage balancing methods for the four-level NPC converters. The two voltage balancing methods are both decoupled into two parts.

1) The two-level converter unit in the four-level NPC converter contains the switches $S_{\mathrm{x}2}$, $S_{\mathrm{x}2}$' and the middle capacitor C_2. By regulating the reference signal $u_{\mathrm{refx}2}$ via a PI regulator, $U_{\mathrm{C}2}$ can be successfully balanced at $1/3U_{\mathrm{dc}}$.
2) The remained three-level converter unit in the four-level converter NPC contains C_1, C_3, $S_{\mathrm{x}1}$, $S_{\mathrm{x}1}$', $S_{\mathrm{x}3}$, and $S_{\mathrm{x}3}$'. With ZSV injected into $u_{\mathrm{refx}1}$ and $u_{\mathrm{refx}3}$, the capacitor voltage imbalance issue and the low-frequency voltage fluctuation issue of C_1 and C_3 can be solved well.

C. Comparative Analysis and Discussion

Most of the existing voltage balancing methods for four-level NPC are fundamentally decoupled into two parts: 1) the middle capacitor voltage balancing control and 2) the upper and lower capacitor voltage balancing control. But the basic ideas and implementation ways of them are different. Comparison of the existing carrier modulation methods and the proposed voltage balancing methods are presented in Table II.

The carrier-overlapped modulation method [20], variable-carrier method [8], [9], [21], variable-reference method [22], [23], and variable-angle method [24] can partially realize closed loop control of the capacitor voltages. Comparatively, the redundant level modulation [25], the voltage balancing methods [26], [27], [28], and the proposed methods can realize closed loop control of all the three capacitor voltages. Better dynamic voltage balancing performance can be guaranteed when using the closed loop control methods [25], [26], [27], [28].

Similar to the existing methods in [26] and [27], the proposed voltage balancing methods have the same feature that they aim to slightly modify the modulation signal amplitude via PI compensators. Specifically, the voltage balancing method in [26] and [27] and the proposed method II both use two compensators. However, the proposed method II does not use any complex and decoupling matrix, which makes it easier to implement in digital chips.

In addition, the proposed methods are different from the closed-loop voltage balancing method in [28]. The proposed methods modify the modulation signal amplitude to realize balancing control while the method in [28] modifies the switching angle values. As a result, the resulting variation of the phase voltages are different than that in [28].

Overall, the proposed voltage balancing methods are the extension of the variable-carrier, variable-reference, and variable-angle voltage balancing methods. With the proposed idea "4L = 2L + 3L," the proposed methods are easy to understand and implement in practical applications. More importantly, more 3L ZSV injection methods can be introduced to develop new four-level voltage balancing methods. This advantage makes the proposed methods more flexible.

IV. Simulation Analysis

Taking the 4L-ANPC converter as an example, simulation results of it are provided to verify the proposed idea and the proposed voltage balancing control methods. According to the simulation parameters in Table III, the simulation results of the 4L-ANPC converter with the existing method and the proposed methods are presented in Fig. 7.

Taking Phase C as an example, the voltage and current waveforms of the switches of the 4L-ANPC converter with the proposed method I are presented in Fig. 8. Besides, the power loss distribution of the 4L-ANPC converter is given in Fig. 9. Finally, performance comparison of the 4L-ANPC converter with different voltage balancing methods is shown in Table IV.

It can be found that there is about 162V triple-fundamental-frequency voltage oscillations on $U_{\mathrm{C}1}$ and $U_{\mathrm{C}3}$ when using

TABLE II
COMPARISON OF THE EXISTING CARRIER MODULATION METHODS AND THE PROPOSED VOLTAGE BALANCING METHODS

Voltage Balancing Method	Middle Capacitor Voltage Control	Upper and Lower Capacitor Voltage Control
Carrier-overlapped [20]	Carrier-overlapped modulation (open loop)	LS-PWM + Optimum ZSV injection (closed loop)
Variable-carrier [8], [9], [21]	Modify carrier signal amplitude (closed loop)	LS-PWM (open loop)
Variable-reference [22], [23]	Modify modulation signal amplitude (closed loop)	LS-PWM (open loop)
Variable-angle [24]	Modify modulation signal angle (closed loop)	LS-PWM (open loop)
Redundant level modulation [25]	Redundant level modulation (closed loop)	LS-PWM + Optimal ZSV injection (closed loop)
The methods in [26], [27]	Modify modulation signal amplitude (closed loop)	Modify modulation signal amplitude (closed loop)
The method in [28]	Modify switching angle values (closed loop)	Modify switching angle values (closed loop)
The proposed methods	Modify modulation signal amplitude (closed loop)	LS-PWM + 3L ZSV injection (closed loop)

TABLE III
SIMULATION PARAMETERS OF THE 4L-ANPC CONVERTER

Main Component	Parameter
DC-link voltage U_{dc}	1200 V
DC-link capacitors C_1, C_2, C_3	1.32 mF
Switching frequency f_s	10 kHz
Switches S_{x1}, S_{x1}', S_{x3}, S_{x3}'	UF3SC065007K4S
Switches S_{x2}, S_{x2}'	UF3SC120009K4S
LR load	2 mH, 7.2 Ω

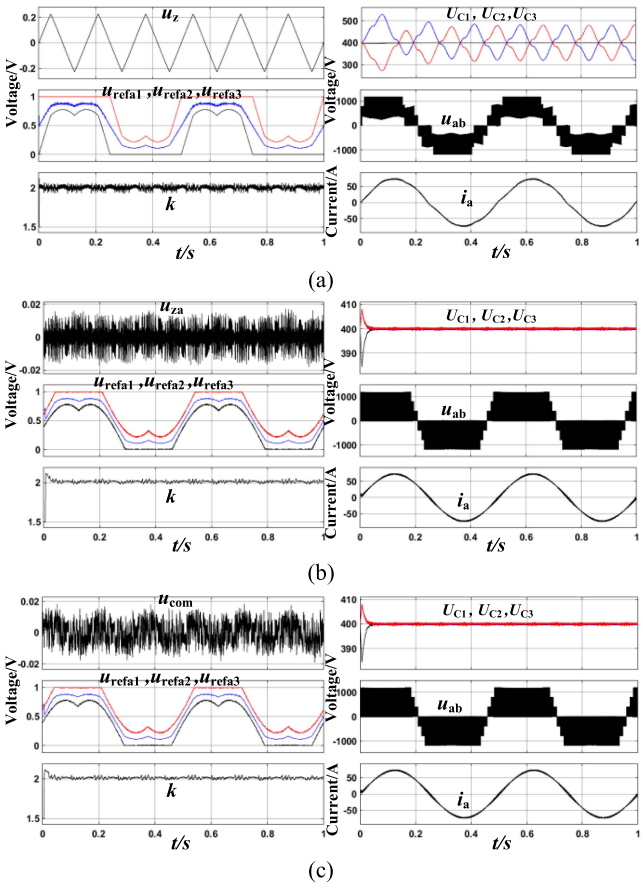

Fig. 7. Key simulation results when f_m is 2 Hz and m is 0.9. (a) Existing method "variable-reference + 3rd harmonic injection." (b) Proposed method "variable-reference + ZSV injection I." (c) Proposed method "variable-reference + ZSV injection II."

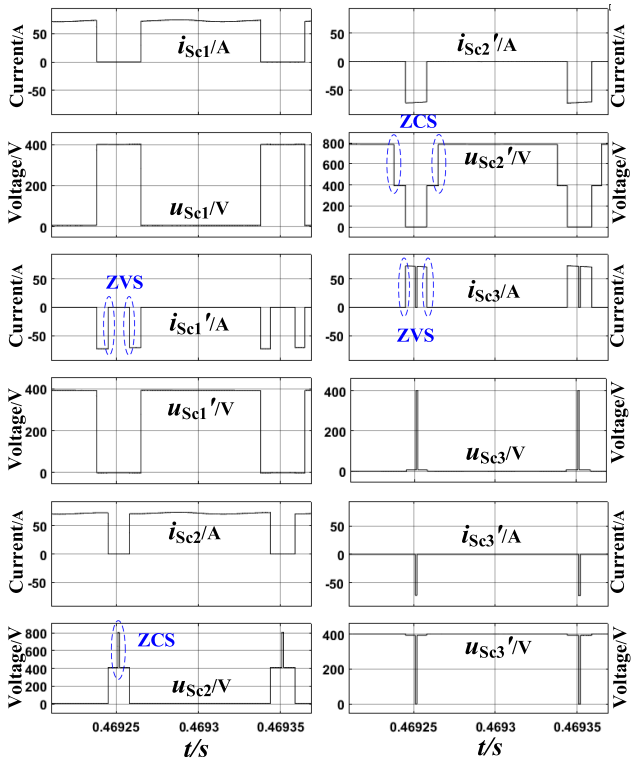

Fig. 8. Voltage and current waveforms of each switch of the 4L-ANPC converter with the proposed method I.

TABLE IV
COMPARISON OF THE EXISTING METHOD AND THE PROPOSED METHODS

Control Method	Total Loss	Oscillation	THD
The existing method	215.4 W	162 V	2.94%
Proposed method I	232.2 W	2 V	2.19%
Proposed method II	232.8 W	2 V	2.18%

the existing method "variable-reference + 3rd harmonic injection." The large low-frequency voltage oscillations lead to high blocking voltages across the power switches and high output current harmonics. However, with the proposed methods, the low-frequency voltage oscillations on U_{C1} and U_{C3} are nearly zero. Furthermore, the total harmonic distortion (THD) of the phase current is reduced by about 0.76% when using the proposed voltage balancing methods.

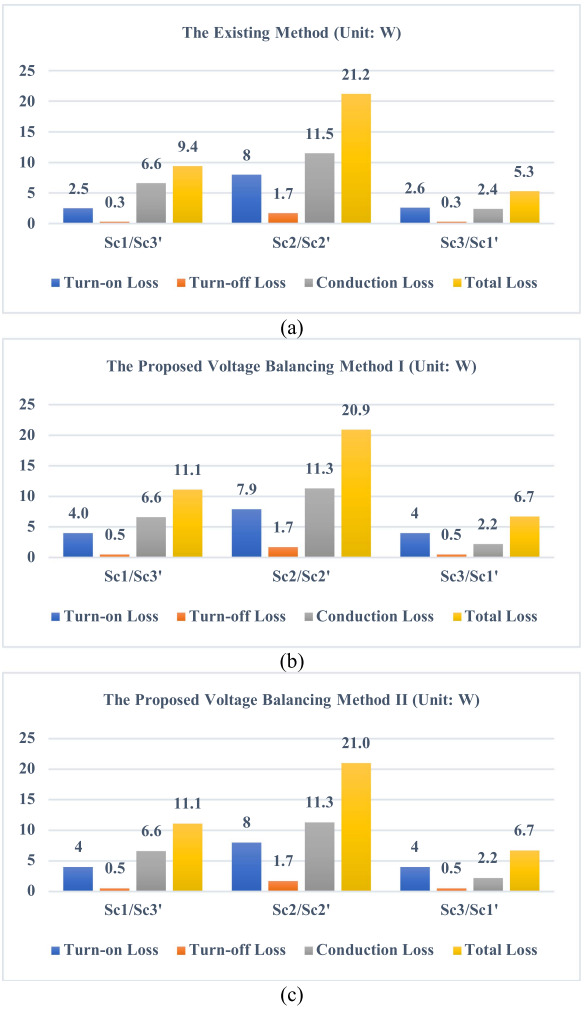

Fig. 9. Power loss distribution of the 4L-ANPC converter when f_{m} is 2 Hz and m is 0.9. (a) Existing method "variable-reference + 3rd harmonic injection." (b) Proposed method I. (c) Proposed method II.

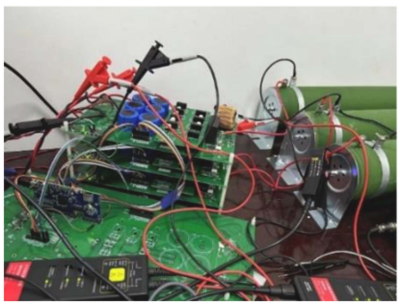

Fig. 10. Experimental prototype of the 4L-ANPC converter.

Compared to the existing method, the proposed methods I and II show more switching transitions of the power switches in the 4L-ANPC converter. However, the increased power losses are not such much because of soft switching. The variable-reference modulation in the proposed methods aim to regulate the dwell time of the switches S_{x2} and S_{x2}' to balance the middle capacitor voltage U_{C2}. As a result, there are two switching times for each switch of S_{x2} and S_{x2}' during one switching period. The switching losses of S_{x2} and S_{x2}' should increases theoretically

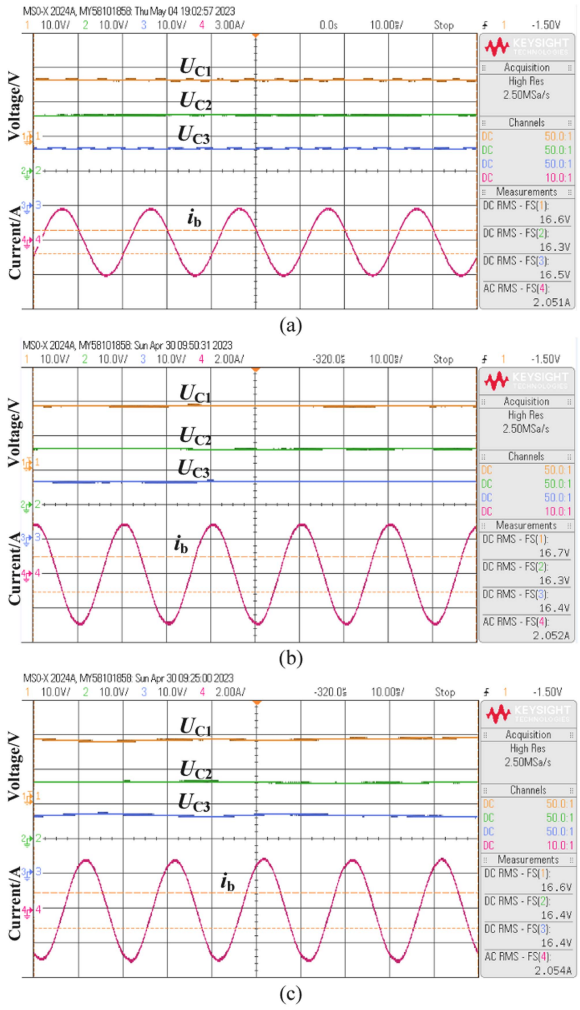

Fig. 11. Key results of the 4L-ANPC converter with different methods when f_{m} is 50 Hz and m is 0.9. (a) Existing method. (b) Proposed method I. (c) Proposed method II.

but the switching losses of them do not increase. Because S_{x2} and S_{x2}' turn ON and OFF with zero current switching (ZCS), which can be further verified from Fig. 8.

In addition, S_{x1}' and S_{x3} turn ON and OFF with zero voltage switching. Since the proposed methods and the existing method all contain a common variable-reference scheme, the total power losses of S_{x2} and S_{x2}' are nearly the same, which can be seen from Fig. 9. But there is a little difference on the power loss distribution of the other four switches per phase leg due to ZSV injection in the proposed methods. Specifically, both the ZSV injection methods lead to turn-ON loss increase in proposed two methods. As a result, the proposed methods lead to about 17 W power loss increase compared to the existing method "variable-reference + 3rd harmonic injection." Fortunately, the increased 17 W power loss could be nearly neglected when it is compared to the power rating 50 kW. Finally, the efficiency of the 4L-ANPC converter using the existing method "variable-reference + 3rd harmonic injection," the proposed method I, and the proposed method II is 99.57%, 99.54%, and 99.54%, respectively.

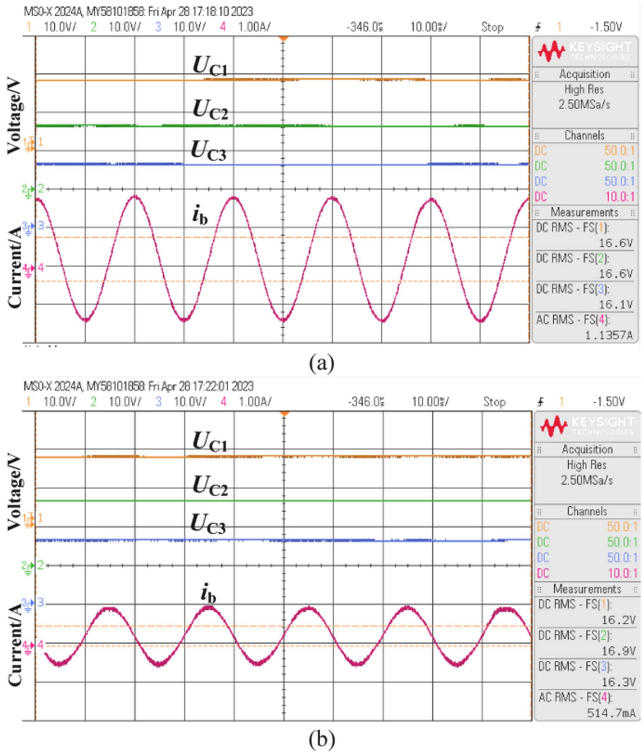

Fig. 12. Key results of the 4L-ANPC converter with the proposed method II when f_m is 50 Hz. (a) m is 0.5. (b) m is 0.2.

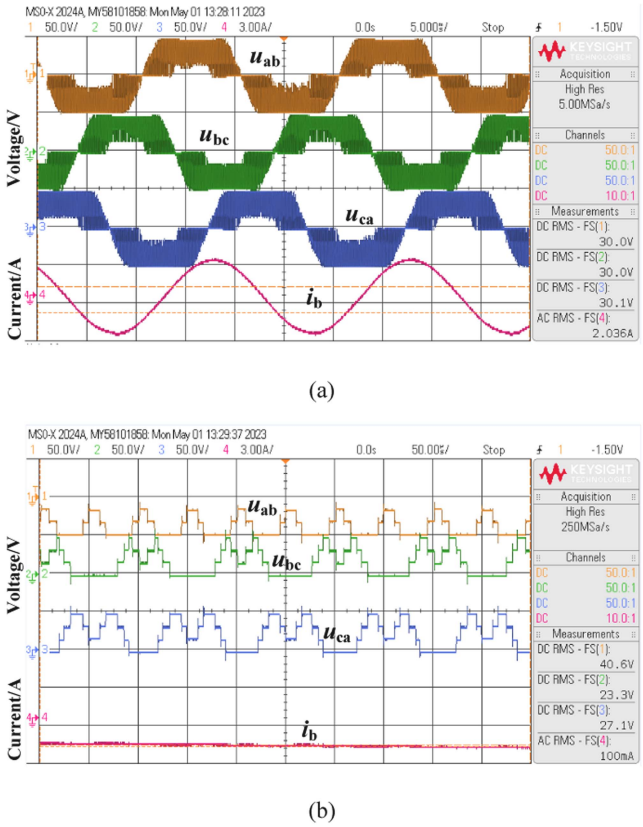

Fig. 13. Key results of the 4L-ANPC converter with the proposed method I when f_m is 50 Hz and m is 0.9. (a) Line voltages and phase current. (c) Zoomed-in line voltages and phase current.

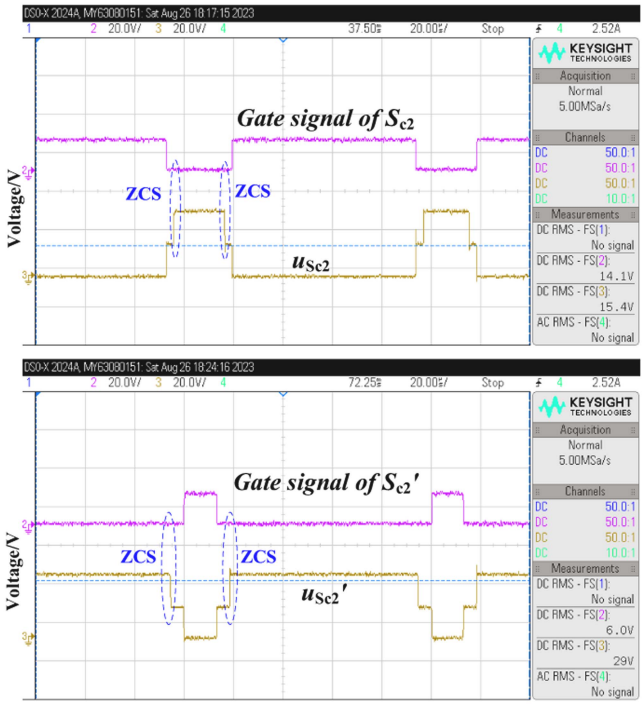

Fig. 14. Gate signal and voltage waveforms of S_{c2} and S_{c2}'.

TABLE V
EXPERIMENTAL SPECIFICATIONS OF THE 4L-ANPC CONVERTER

Component	Total Loss
DC-link voltage U_{dc}	50 V
DC-link capacitors C_1, C_2, C_3	1.32 mF
Switching frequency f_s	10 kHz
LR Load	5 mH, 10 Ω

V. EXPERIMENTAL VERIFICATION

To further verify the proposed voltage balancing methods, an experimental prototype of the 4L-ANPC converter is built according to the specifications in Table V. The experimental prototype in Fig. 10 is implemented with the help of the DSP chip TMS320F28379.

Taking the operating condition (f_m = 50 Hz and m is 0.9) as an example, the experimental results of the 4L-ANPC converter are presented in Fig. 11. The three capacitor voltages are all balanced at 16.7 V, which is 1/3 of the dc-link voltage of 50 V. There are nearly no low-frequency voltage fluctuations on U_{C1} and U_{C3}. Under this condition, the three voltage balancing methods does not bring in much difference on the output performances of the 4L-ANPC converter. In addition, taking the proposed method II as an example, the experimental results of the 4L-ANPC converter with different modulation indices are presented in Fig. 12. Though the 4L-ANPC converter operates at low modulation indices, the proposed methods can still balance the three capacitor voltages well. Taking the proposed method I as an example, the line voltages and zoomed-in waveforms are presented in Fig. 13. The switching voltage is kept at $1/3U_{dc}$ well, which is helpful to reduce switching loss and EMI.

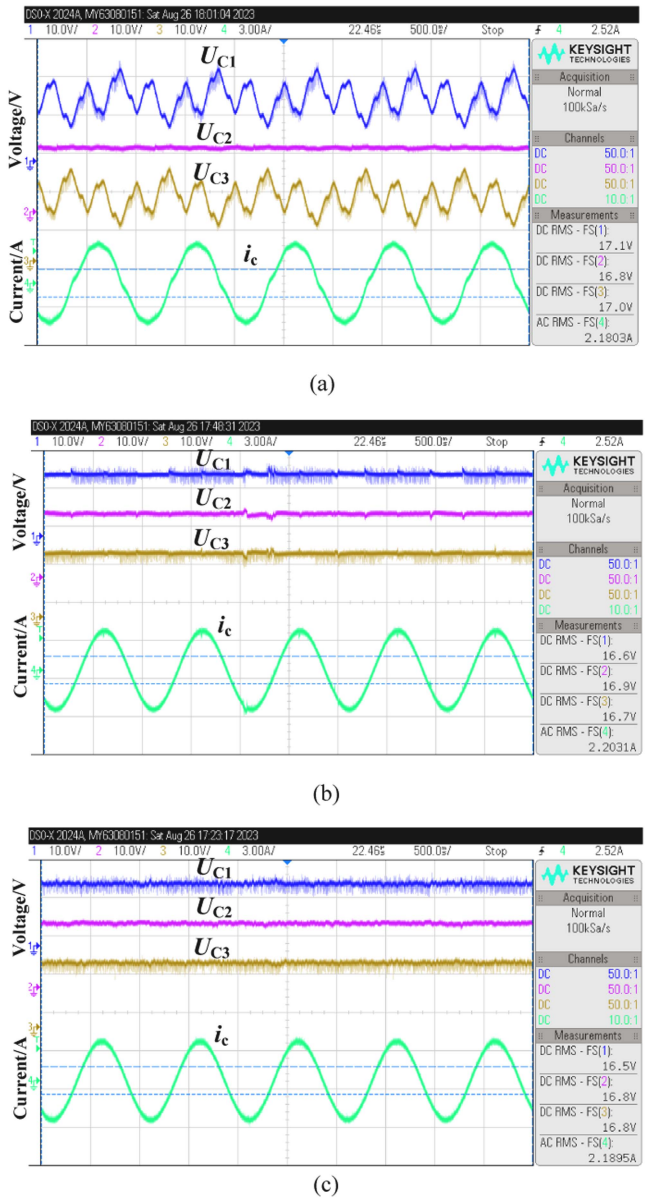

Fig. 15. Key results of the 4L-ANPC converter with the proposed method I when f_m is 1 Hz and m is 0.9. (a) Existing method. (b) Proposed method I. (c) Proposed method II.

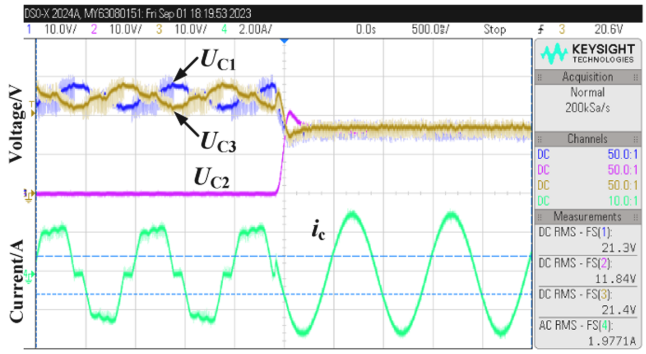

Fig. 16. Key experimental results of the 4L-ANPC converter when it operates from the traditional level-shifted carrier modulation method to the proposed method II.

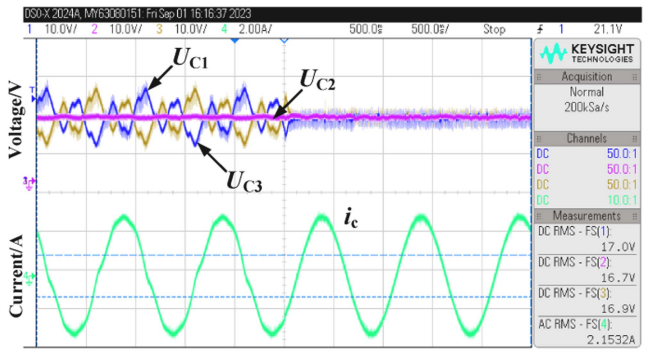

Fig. 17. Key experimental results of the 4L-ANPC converter when it operates from the existing method "variable-reference + 3rd harmonic injection" to the proposed method II.

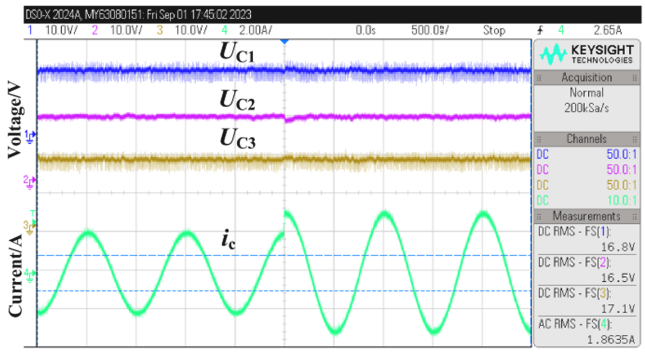

Fig. 18. Key experimental results when the modulation index m changes from 0.6 to 0.9.

Additionally, the gate signals and voltage waveforms of the switches S_{c2} and S_{c2}' are provided in Fig. 14 when f_m is 50 Hz and m is 0.9. It can be observed that the two switches S_{c2} and S_{c2}' are turned ON and OFF with ZCS when the voltage level changes between $1/3U_{dc}$ and $2/3U_{dc}$. Therefore, though the switching transitions of the switches S_{c2} and S_{c2}' increase by one time, the switching losses of them does not increase, which supports the simulation results and analysis in Section IV.

Taking the operating condition (f_m = 1 Hz and m is 0.9) as an example, the experimental waveforms of the 4L-ANPC converter with different voltage balancing methods are presented in Fig. 15. Though the three capacitor voltages are all balanced at about 16.7 V, the existing method leads to the largest low-frequency voltage fluctuations on U_{C1} and U_{C3}. In contrast, the proposed methods I and II can greatly suppress the low-frequency voltage fluctuations. Because the dual-reference signals u_{refx1} and u_{refx3} in the proposed voltage balancing methods can suppress the low-frequency voltage fluctuations on U_{C1} and U_{C3} while the ZSV injection methods can eliminate the voltage drift between them.

Furthermore, Fig. 16 shows the experimental waveforms of the 4L-ANPC converter when it operates from the traditional level-shifted carrier modulation scheme to the proposed method II. Fig. 17 shows the experimental waveforms of the 4L-ANPC converter when it operates from the existing method "variable-reference + 3rd harmonic injection" to the proposed method II. With the traditional level-shifted carrier modulation scheme,

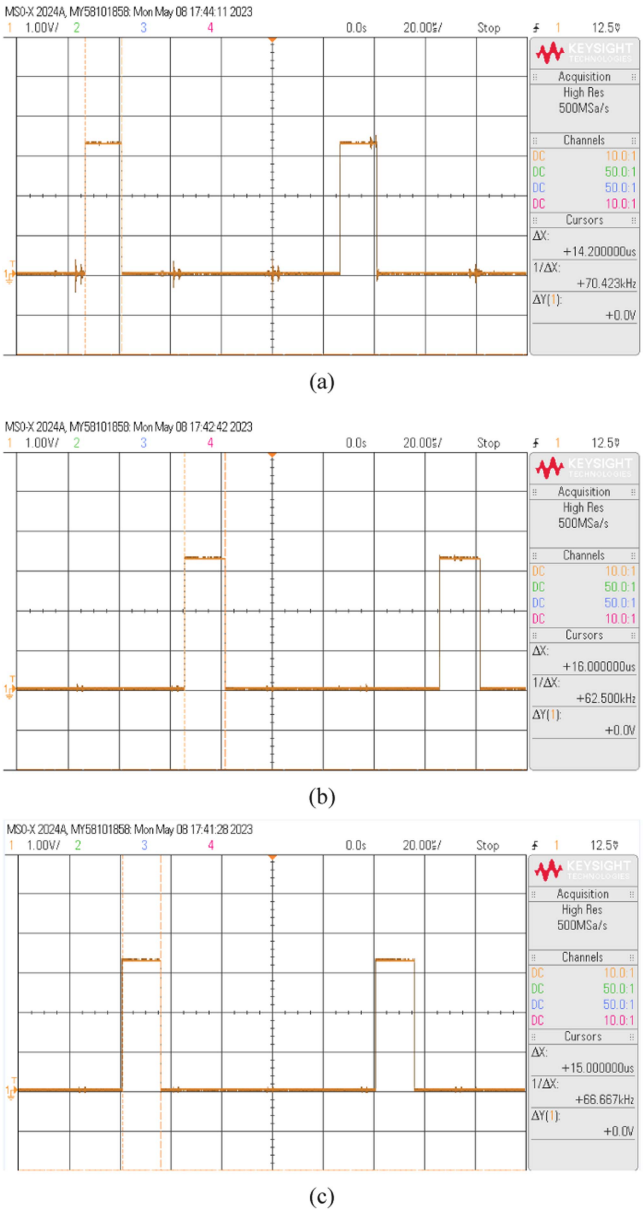

Fig. 19. Code executing time. (a) Existing method. (b) Proposed method I. (c) Proposed method II.

U_{C2} is zero while U_{C1} and U_{C3} share the input voltage with large low-frequency voltage fluctuations. These results basically verify the theoretical analysis result in Section II-B. Once using the existing method "variable-reference + 3rd harmonic injection," the three capacitor voltages are all balanced but there are still large low-frequency voltage fluctuations on U_{C1} and U_{C3}. With the proposed method II, the low-frequency voltage fluctuations are greatly suppressed.

At the condition of 1 Hz, the experimental waveforms of the capacitor voltages and phase current of i_c when the modulation index changes from 0.6 to 0.9 are presented in Fig. 18. It can be found that the capacitor voltages can be still stable at about 16.7 V even after the modulation index changes. In addition, as shown in Fig. 19, the code executing time of the existing method, the proposed method I and the proposed method II is, respectively, 14.2 μs, 16 μs, and 15 μs during the switching period of 100 μs. Compared to the existing method, the proposed methods increase slight computation burden. Furthermore, the proposed method II shows slightly lower computation burden than method I. Because three proportional regulators and three phase current information are required to achieve three ZSV injection signals u_{za}, u_{zb}, u_{zc} in the proposed method I, while only one PI regulator is utilized to achieve a common ZSV injection signal u_{com} in the proposed method II.

Overall, the proposed two voltage balancing methods cannot only balance dc-link capacitor voltages of the 4L-ANPC converter, but also suppress the low-frequency voltage fluctuations on the upper and lower capacitors. Comparatively, the proposed method II is easier to implement in digital controller systems.

VI. Conclusion

This article proposes a new insight on four-level NPC converters that every four-level NPC converter is a hybrid combination of a two-level converter unit and a three-level converter unit. With the proposed idea, the complex voltage balancing control can be simplified into two parts.

1) The middle capacitor voltage balancing control is realized based on a variable-reference scheme for the two-level converter unit. It is implemented by regulating the amplitude of the reference signal u_{refx2} via a PI compensator based voltage loop.
2) The upper and lower capacitor voltages are balanced based on ZSV injection methods for the three-level converter unit. Low-frequency voltage fluctuations are eliminated because of dual-reference-signal modulation (u_{refx1} and u_{refx3}) for this three-level converter unit.

Compared to the existing method "variable-reference + 3rd harmonic injection," the proposed methods can further reduce THD and eliminate low-frequency voltage fluctuations at the expense of slightly increased power losses. More importantly, with the proposed idea "4L = 2L + 3L," more voltage balancing control methods could be developed by referencing to the existing voltage balancing methods for three-level converters.

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