A Multi-Mode Full-Bridge/Modified-Stacked-Switches Structured CLLC Resonant Converter for Energy Storage Applications

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***Abstract*—In this article, a new full-bridge/modified-stacked-switches multimode *CLLC* isolated resonant converter is presented for energy storage applications. In particular, a multimode wide voltage gain control system is proposed, which takes advantage of the topology reconfiguration method in both the inverter and the rectifier blocks in the proposed circuit to regulate the output voltage while preventing the switching frequency from drifting away far from the resonant frequency. The impact of the parasitic elements in the isolated *CLLC* resonant circuit is also investigated in this article. In addition, a smooth mode transition is provided to avoid any transients caused by a rapid frequency change. The operating principles of the control system is analyzed extensively. Compared with the traditional pulsefrequency modulated resonant converters, the proposed control system attains enhanced efficiency even at extremely low voltage gains while sustaining a nearly consistent high-efficiency profile. Furthermore, it mitigates voltage regulation instability under light loads attributed to parasitic components by constraining the frequency spectrum. The proposed control system presents an appealing solution for high-voltage, high-power energy storage applications that demand a broad range of voltage gains and where the influence of switch $R_{ds\mathrm{ON}}$ is reduced due to the low current characteristics typical of these applications. Finally, a 500 W 100 V-350 V input, 96 V output prototype has been built to verify the performance of the proposed converter system.**

***Index Terms*—*CLLC* resonant circuit, dc/dc converters, hybrid control, multimode control, reconfigurable dc/dc converter, soft switching, wide voltage gain.**

I. Introduction

HIGH frequency, wide input/output voltage bidirectional dc/dc power converters are being used in many applications such as energy storage [1], [2], renewable energy sources [3], [4], and consumer electronics [5] due to their small size and high power density.

There are several types of dc/dc converters available as given in Fig. 1, each with its own characteristics and applications. Due to their effectiveness, high efficiency, high power density, and compact size, resonant converters have been widely adopted in many high-frequency wide gain applications, such as energy storage systems (ESSs) demonstrated in Fig. 2. CLLC resonant converters are among the popular topologies due to their zero-voltage switching (ZVS) feature, symmetric structure, and bidirectional power transfer ability. Yet, in wide voltage gain applications e.g., ESS due to wide battery voltage charging profile (see Fig. 3), with conventional pulse frequency modulation (PFM) control, in which the output voltage is adjusted by changing the load output impedance through switching frequency variation, the converter suffers from: limited light load operation; wide switching frequency range to meet the voltage

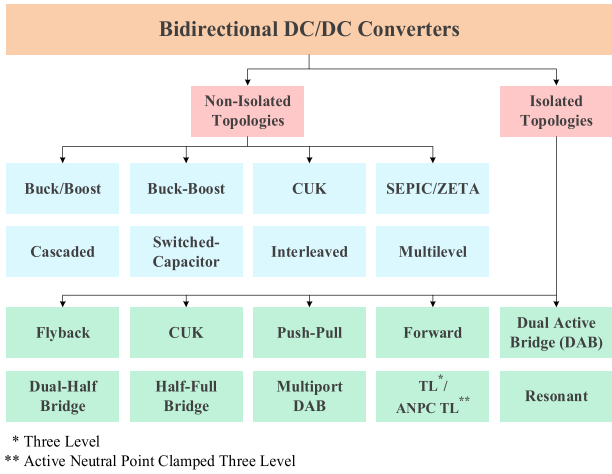

Fig. 1. Classification of bidirectional DC/DC converters.

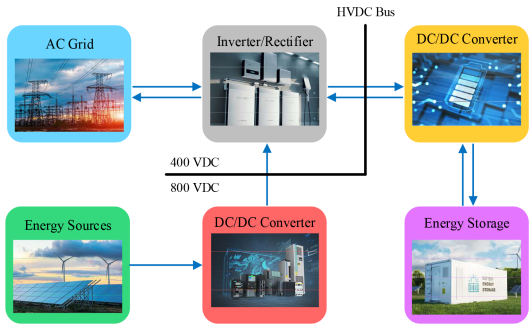

Fig. 2. System diagram of a typical ESS.

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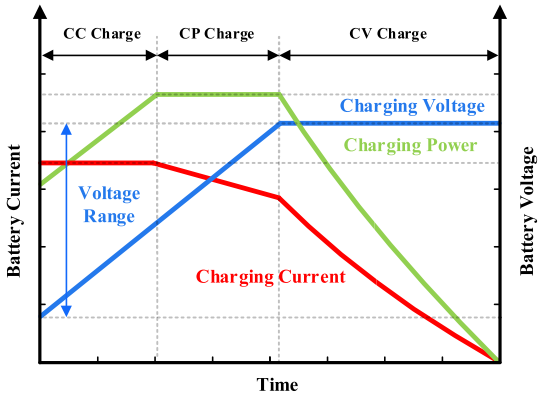

Fig. 3. Battery charging profile.

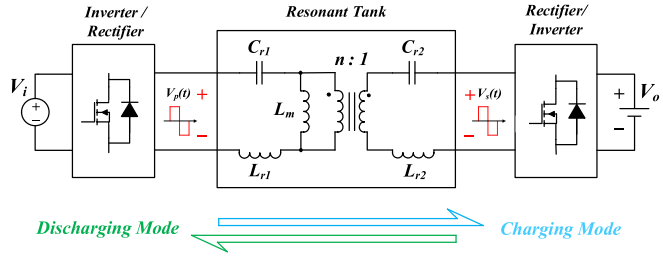

Fig. 4. Simplified circuit topology of a *CLLC* converter.

gain requirements; and challenges with the electromagnetic interference, etc. [6], [7].

As a result, the above challenges hinder the operation of the converter in light load or ultralow voltage gain conditions. This is because the switching frequency must deviate away from the resonant frequency to satisfy the output voltage and load requirements. Consequently, with a greater switching frequency at light loads, the overall efficiency of the converter is severely compromised.

Furthermore, with the continuous increase in the number of appliances and development of electronic devices, standby function and therefore standby losses have become an inherent part of any electronic devices [8]. According to literature, it has been found that in practice, with a significant increase in the switching frequency in the resonant converters during light load operation, instead of a reduction in the voltage gain, the output voltage increases due to parasitic capacitances especially in very high switching frequency (500 kHz+) applications [9].

Therefore, a detailed analysis must be conducted and a comprehensive mathematical model of the *CLLC* resonant converter must be obtained. Consequently, depending on the application, parasitic elements must be considered in the design and development of the control system.

In this regard, Arshadi et al. [10], Kim [11], Noah et al. [12] obtained the mathematical model of the resonant circuit and analyzed the voltage gain characteristic by adding the parasitic capacitances of the output-side switches to the fundamental equivalent circuit. However, they failed to consider the influence of the distributed capacitance of the transformer on the converter.

Further, based on the proposed model, to provide proper voltage regulation in wide voltage gain applications and improve the converter efficiency in light loads, alternative methods are required to prevent the switching frequency from drifting away from the resonant frequency.

The simplified system diagram of a *CLLC* bidirectional dc/dc converter has been given in Fig. 4. In general, there are two approaches to extending the voltage gain range of the resonant converter while addressing the previously-mentioned challenges. The first approach involves topology morphing and modifying the converter topology, which includes a change in: the primary inverter [13], [14], [15], [16], [17]; the secondary rectifier [18], [19], [20]; and the resonant tank topology [21], [22], [23]. While restructuring inverter and rectifier topologies is more common in practice, some literature focuses solely on resonant tank reconfiguration.

To enhance the hold-up time and modify the characteristics of the resonant converter, Wang et al. [23] introduced an additional resonant capacitor and auxiliary switch in the *LLC* tank. However, this frequent resonant circuit reconfiguration results in transients, spikes, increased losses, and reduced converter efficiency. Sha and Yang [14] and Jovanović and Irving [15] suggested that on the inverter side, by applying proper gate signals, the conventional full-bridge (FB) converter can switch to half-bridge (HB) operation mode to extend the voltage gain range. The FB inverter operates in the low input voltage range and switches to an HB when the input voltage increases beyond a certain level. In [18], by adding a switch in the rectifier block, the rectifier can switch between a full bridge and a voltage doubler (VD).

The second approach to achieve a wider voltage gain operation in the resonant converters is taking advantage of hybrid modulation techniques. Many control freedoms exist in *CLLC* resonant converters, including the switching frequency, phase shift angle, duty ratio, etc. Typical modulation techniques in resonant converters are PFM, phase shift modulation (PSM), symmetric and asymmetric pulsewidth modulation (PWM), and burst-in control [24], [25], [26].

To solve the aforementioned challenges, a new multi-mode controlled FB/modified-stacked-switches *CLLC* resonant converter is proposed in this article. The impact of the parasitic elements in the isolated *CLLC* resonant circuit is investigated in this article. To support the proposed topology, a multimode wide voltage gain control system is proposed which takes advantage of the topology reconfiguration method in both the inverter (FB circuit) and the rectifier (the modified-stacked-switches leg) blocks to regulate the output voltage while avoiding the switching frequency from drifting away far from the resonant frequency. Having a wide switching frequency range contributes to an increased core size in the design process. Therefore, by limiting the switching frequency range, the design of the magnetic components will be optimized. In addition, by means of the proposed control system, the switching frequency varies smoothly throughout the voltage gain range to avoid any transients caused by a rapid frequency change. Furthermore, by limiting the range of the switching frequency control spectrum, the impact of the parasitic elements on the converter's performance is minimized and a high-efficiency profile is achieved throughout the entire voltage gain range with the proposed topology.

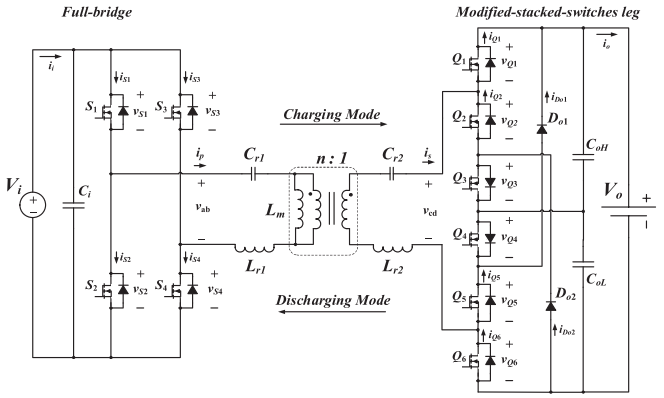

Fig. 5. Topology of the proposed *CLLC* resonant converter employing a FB circuit on the primary and a modified-stacked-switches leg on the secondary side.

The rest of this article is organized as follows. In Section II, the overall voltage gain characteristics of the *CLLC* converter are investigated by considering the impact of parasitic capacitances of the rectifier switches and the influence of distributed capacitance of the high-frequency transformer. A new hybrid control strategy is developed in Section III by combining the topology morphing methods and the available modulation techniques to enhance the voltage gain range of the *CLLC* converter and improve the efficiency profile of the converter in light load conditions. In Section IV, the design scheme, along with the process of obtaining the optimal circuit parameters are covered to meet the voltage gain requirements at full load and light load. The experimental results of a proof-of-concept prototype with an input voltage of 100 to 350 V, an output voltage of 96 V, and a rated output power of 500 W are provided in Section V to verify the performance of the developed hybrid control system. Finally, Section VI concludes the article.

II. Mathematical Model of the *CLLC* Converter With Parasitic Elements

The proposed multimode *CLLC* resonant converter topology and its key waveforms in steady-state operation have been provided in Figs. 5 and 6, respectively. The topology consists of: a FB inverter; a CLLC resonant tank; and a modified-stacked-switch rectifier network [27].

As mentioned in the previous section, in the inverter block, by using an h-bridge at the front-end side of the dc/dc converter, the overall voltage gain of the converter can be extended by switching from a FB to an HB. In addition, in the stacked-switch rectifier in Fig. 5, by switching between various operating modes, namely VD and full-wave (FW), the voltage gain range of the converter can be further extended.

To increase the power density and enable operating in high switching frequencies, a *CLLC* resonant circuit has been used due to its ZVS, soft-switching feature and symmetric structure. The resonant tank in Fig. 5 includes L_{r1} and L_{r2} as the resonant inductors, C_{r1} and C_{r2} as the resonant capacitors, and a high-frequency transformer with magnetizing inductance L_m and primary to secondary turn ratio of n to provide galvanic isolation. The equivalent circuit of the *CLLC* resonant tank in charging

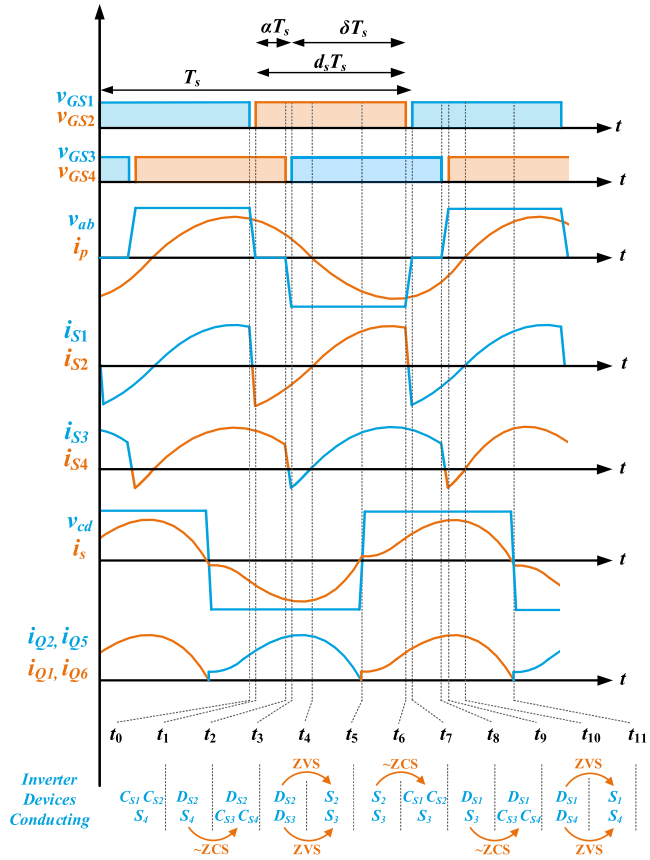

Fig. 6. Key waveforms of the converter in steady-state operation.

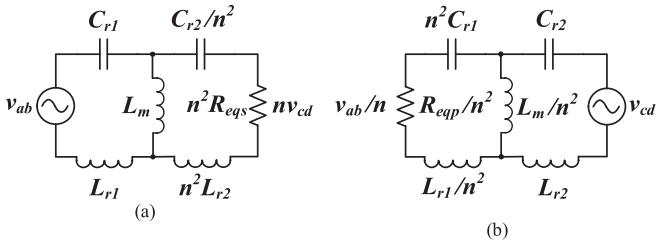

Fig. 7. Simplified equivalent circuit of the *CLLC* resonant tank in (a) charging and (b) discharging modes.

and discharging modes are demonstrated in Fig. 7 where R_{eqp} and R_{eqs} are the primary and secondary side equivalent loads, respectively.

In conventional resonant converters with PFM, the output voltage is regulated by adjusting the operating frequency and modifying the impedance of the circuit components and the load. In the soft-switching area, as the switching frequency increases, the output voltage drops, and this lays the foundation of the control system. Yet, with the recent development of semiconductor devices, to increase the power density of the power converters, the switching frequency has been pushed towards the MHz range. One of the major drawbacks of the conventional resonant converters with PFM is the limited voltage gain range since the switching frequency needs to stray away from the resonant frequency. However, according to the literature, due to the parasitic parameters of the overall converter, under light

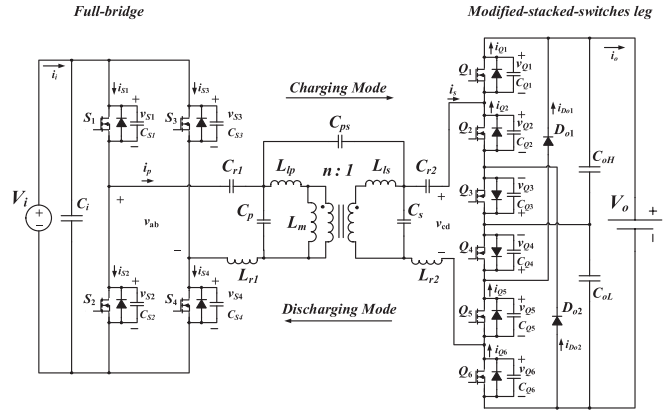

Fig. 8. Topology of the *CLLC* resonant converter with the parasitic elements.

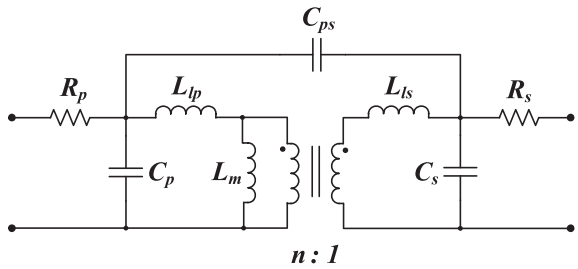

Fig. 9. Equivalent circuit of the high frequency transformer with parasitic elements.

load conditions, at above 500 kHz, as the switching frequency increases, instead of a drop in the voltage gain, the output voltage increases, which leads to unstable operation of the control system and high oscillations in the output voltage [9], [11]. As a result, in high frequency and power density applications, the parasitic parameters of the circuit components have to be included in the analysis, and to prevent unstable operation of the control system, the switching frequency spectrum has to be kept within a relatively narrow range and deviating from the resonant frequency has to be prevented.

A. Equivalent Circuit Model With Parasitic Elements

Traditionally, the parasitic parameters are ignored to simplify the design process. The topology of the *CLLC* converter with the parasitic circuit components has been given in Fig. 8 which includes the parasitic capacitances of the primary winding (C_p), the secondary winding (C_s), and the parasitic capacitance between the primary and the secondary windings (C_{ps}). In addition, L_{lp} and L_{ls} are primary and secondary winding leakage inductances, respectively. While in many applications, the leakage inductances of the high-frequency transformer (L_{lp} and L_{ls}) are utilized solely as the series inductances to form the resonant circuit, in this article, $L_{r1,}$ and $L_{\mathrm{r}2}$ are added as separate components to the *CLLC* resonant circuit. The equivalent model of the high-frequency transformer is demonstrated in Fig. 9.

The primary and secondary leakage inductances can be directly measured at low frequencies using short-circuit and open-circuit tests and can be summed up and represented by a single

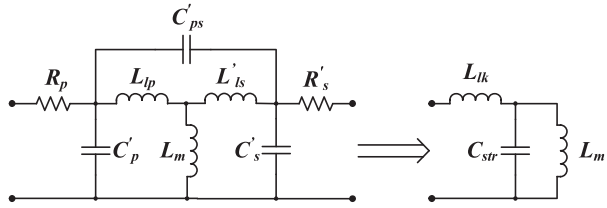

Fig. 10. Equivalent circuit of the high-frequency transformer with parasitic elements.

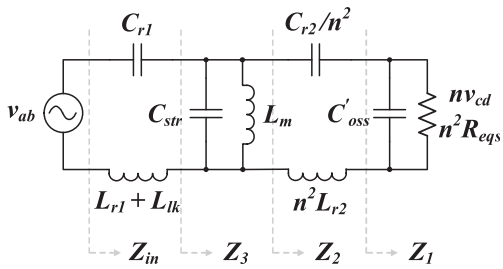

Fig. 11. Simplified equivalent circuit of the *CLLC* resonant tank in charging mode.

equivalent inductance L_{lk} referred to the primary side as demonstrated in Fig. 10

$$L_{lk} = L_{lp} + n^2 L_{ls}. \tag{1}$$

According to [28], in the same manner, the primary, secondary, and the coupling parasitic capacitances of the transformer can be modeled by an equivalent parasitic capacitance C_{str} on the primary side as

$$C_p^{'} = C_p + \left(\frac{n-1}{n}\right) \cdot C_{ps} \tag{2}$$

$$C_s^{'} = \frac{1}{n^2} C_s + \frac{1-n}{n^2} C_{ps} \tag{3}$$

$$C_{ps}^{'} = \frac{1}{n} C_{ps} \tag{4}$$

$$C_{str} \cong C_p^{'} + C_s^{'}. \tag{5}$$

With (1) to (5), the equivalent model of the high-frequency transformer can be simplified as illustrated in Fig. 10. The overall equivalent model of the *CLLC* resonant circuit with the parasitic components has been illustrated in Fig. 11.

In Fig. 11, $c_{\mathrm{oss}}^{'}$ represents the equivalent stray and snubber capacitors of the rectifier switches transferred to the primary side of the resonant tank.

B. Voltage Gain Formulas Derivation

As demonstrated in Fig. 8, in charging mode, the h-bridge operates as an inverter, the stacked-switch leg operates as a rectifier, and the power is transferred from the input dc to the battery pack. To obtain a detailed voltage gain formula for the *CLLC* resonant converter, seven parameters must be considered in the transfer function including resonant inductors L_{r1} and L_{r2}, resonant capacitors C_{r1} and C_{r2}, magnetizing inductor L_m, the turn ratio of the high-frequency transformer n, and the equivalent parasitic capacitance C_{str}.

Considering that the *CLLC* resonant tank in Fig. 8 is composed of two *LC* tanks, two quality factors have been defined in (6). Typically, the leakage inductance of the high-frequency transformer is less than 2% of the magnetizing inductance. Considering that the values of L_{r1} and L_{r2} are much greater than those of the leakage inductances, the leakage inductances can be neglected in the equivalent circuit. Yet, in this manuscript, to increase the accuracy of the obtained model and to investigate the impact of the leakage inductances of the high-frequency transformer, L_{lp} and L_{ls} have been combined and modeled as L_{lk} which has been brought to the primary side. Although in defining Q_1 and Q_2, L_{lk} has not been included, it has been considered in obtaining the total voltage gain formula of the proposed converter

$$Q_1 = \frac{\sqrt{\frac{L_{r1}}{C_{r1}}}}{n^2 R_{\text{eqs}}}\ ,\ Q_2 = \frac{n^2 \cdot \sqrt{\frac{L_{r2}}{C_{r2}}}}{R_{\text{eqp}}} \tag{6}$$

$$L_{r1} = kL_m,\ C_{r2} = mC_{r1},\ L_{r2} = \frac{1}{m} L_{r1} \tag{7}$$

$$\omega_0 = \frac{1}{\sqrt{L_{r1}C_{r1}}} = \frac{1}{\sqrt{L_{r2}C_{r2}}}\ ,\ \omega_r = \frac{\omega_s}{\omega_0}\ ,\ R_{\text{eqs}} = \frac{8R_L}{\pi^2} \tag{8}$$

$$X_{Lr1} = n^2\,\omega_r Q_1 R_{\text{eq}S},\ X_{Cr1} = \frac{n^2 Q_1 R_{eqS}}{\omega_r} \tag{9}$$

$$C_{\text{str}} = p_1\,C_{r1},\ C'_{\text{oss}} = \frac{p_2}{n^2}\,C_{r1},\ L_{lk} = p_3\,L_{r1}. \tag{10}$$

In the above equations k is the ratio between the magnetizing inductance (L_m) and the primary resonant inductance (L_{r1}), m is the ratio between the primary (C_{r1}) and secondary (C_{r2}) resonant capacitors, p_1 represents the ratio of the equivalent parasitic capacitance on the primary side (C_{str}) to C_{r1}, p_2 is the ratio of the equivalent stray and snubber capacitors of the rectifier switches (C_{oss}) to C_{r1}, p_3 represents the ratio between the primary winding leakage inductance to L_{r1}, and Q_1 and Q_2 are the charging and discharging quality factors, respectively. The voltage gain of the *CLLC* resonant circuit demonstrated in Fig. 11 can be obtained as

$$H\left(j\omega_s\right) = \frac{n \cdot v_{cd}}{v_{ab}} = \frac{Z_1}{Z_2} \cdot \frac{Z_3}{Z_{\text{in}}} \tag{11}$$

where

$$Z_{1,pu} = \frac{-jQ_1}{-jQ_1 + \frac{p_2}{n^2}\omega_r} \tag{12}$$

$$Z_{2,pu} = \frac{-jQ_1}{\frac{p_2}{n^2}\omega_r - jQ_1} + \frac{jn^2\omega_r Q_1}{m} - \frac{jn^2 Q_1}{m\omega_r} \tag{13}$$

$$Z_{3,pu} = \frac{-jQ_1}{p_1\omega_r - \frac{k}{\omega_r}} \,||Z_{2,pu} \tag{14}$$

$$Z_{\text{in},pu} = j\left(1 + p_3\right) \cdot \omega_r Q_1 - \frac{jQ_1}{\omega_r} + Z_{3,pu}. \tag{15}$$

To obtain the no-load voltage gain curve of the *CLLC* converter, the quality factor is set to 0 and the impact of each of the parasitic capacitive elements can be investigated.

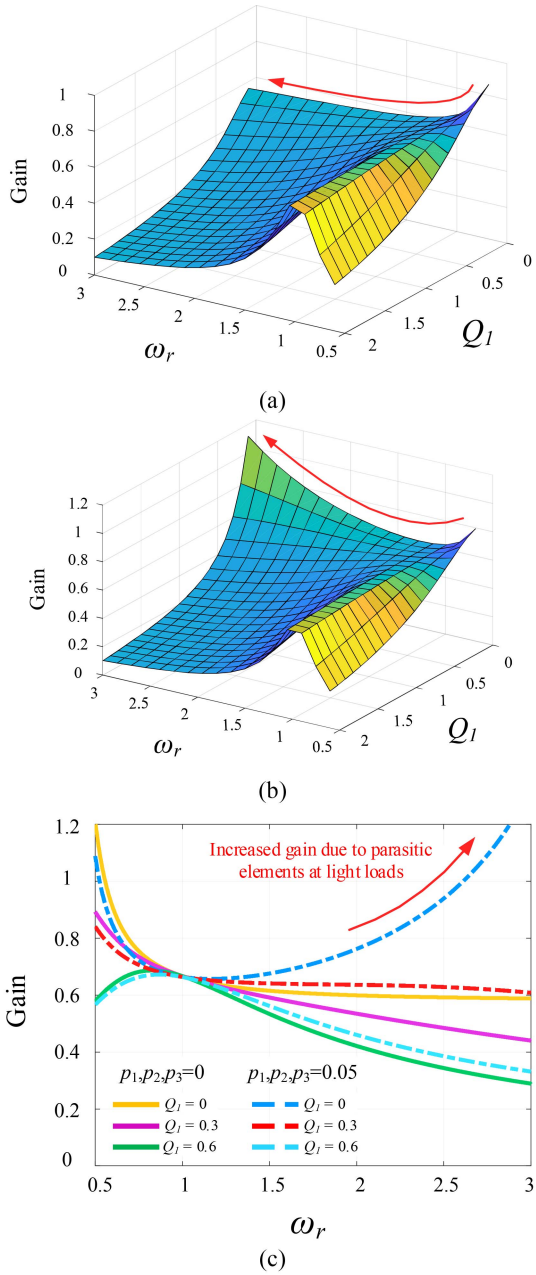

Fig. 12. Voltage gain plot of the *CLLC* resonant circuit in charging mode. (a) Without parasitic elements. (b) With parasitic elements. (c) Combined plots for $Q_1 = 0$, $Q_1 = 0.3$, $Q_1 = 0.6$.

As can be seen in Figs. 12 and 13, in the case of high parasitic capacitive ratios, with an increase in the switching frequency, the overall voltage gain of the converter increases. This behavior may lead to unstable operation of the control system and may cause the output voltage to diverge from its reference. To avoid this, proper insulation should be used between the transformer's primary and secondary windings, and switches with smaller parasitic capacitances must be used in the rectifier block. In addition to the part selection, in the design of the control system and the selection of the resonant components, the switching frequency must be limited to prevent the converter from moving into the unstable region.

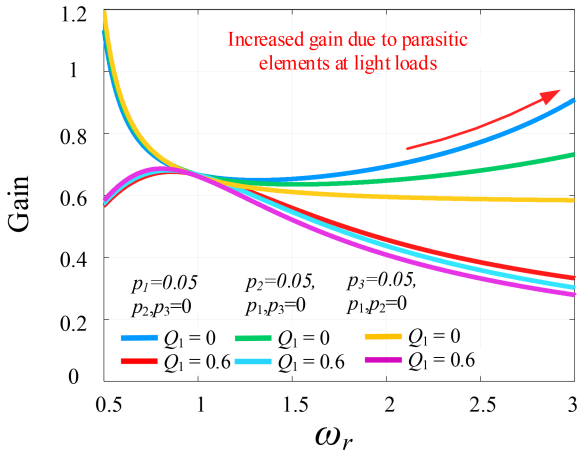

Fig. 13. Voltage gain plot of the *CLLC* resonant circuit with parasitic elements for $Q_1 = 0$ and $Q_1 = 0.6$.

The simplified model of the proposed converter in charging mode is demonstrated in Fig. 14, where the inverter block is an h-bridge, and the rectifier network is composed of a stacked-switch leg. Q_3 and Q_4 provide an additional current path for the secondary resonant current and enable the rectifier to switch between multiple operating points. To ensure that the converter operates within the inductive region and soft-switching is realized throughout the whole output power range including the light loads, the design has been conducted in the full-load condition.

To obtain the voltage gain formula in steady-state operation, it is assumed that the inverter operates as a FB and there is proper insulation between the primary and secondary of the high frequency transformer and the switching frequency range will be limited. Also, considering the parasitic elements have little impact on the voltage gain curve in full load, the equivalent circuit of the *CLLC* resonant tank becomes as illustrated in Fig. 5. The Fourier series representation of the voltage at the primary of the resonant tank in Fig. 5 is given as

$$v_{ab} = \sum_{h=1,3,5,\ldots}^{\infty} \left(\frac{4V_i}{h\pi} \sin(\delta h\pi) \sin\left(\frac{h\pi}{2}\right) \sin\left(h\omega_s t - \frac{\alpha T_s}{2}\right) \right) \tag{16}$$

where

$$\delta = d_s - \alpha. \tag{17}$$

In the above equations, h represents the harmonic order, d_s is the duty ratio of the gate signals in each leg, α is the phase shift between the gate signals of the first leg and second leg of the FB and δ is the equivalent ON time duty ratio of the generated voltage at the output of the inverter.

Considering the topology of the *CLLC* resonant tank and its filtering nature, the higher order harmonics can be ignored, and therefore using fundamental harmonic approximation (FHA), the inverter output voltage can be written as

$$v_{ab} = \frac{4V_i}{\pi} \sin(\delta\pi) \sin\left(\omega_s t - \frac{\alpha T_s}{2}\right). \tag{18}$$

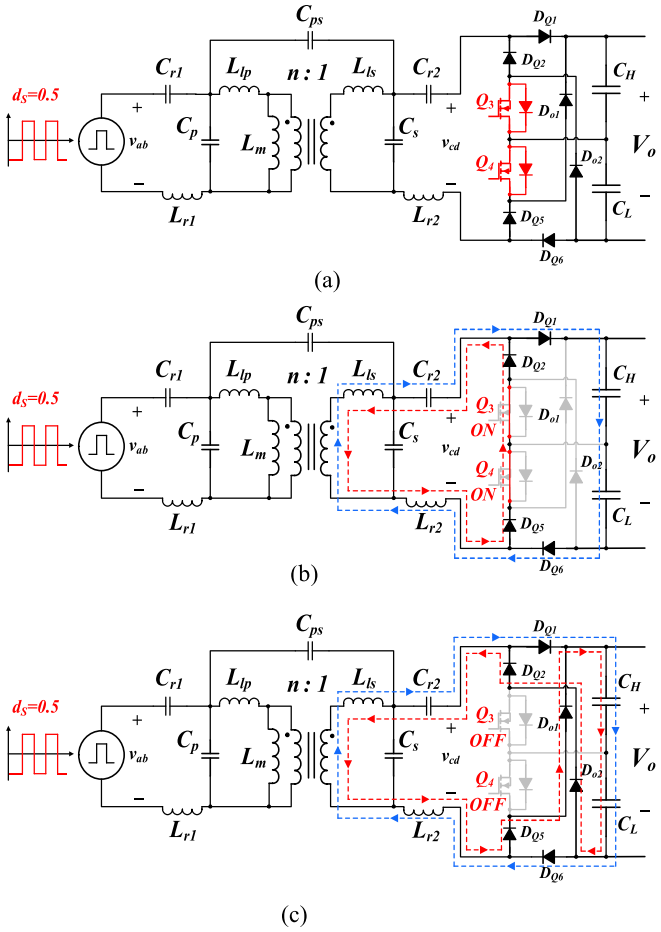

Fig. 14. Different modes of operation of the wide voltage gain multi-mode converter in the rectifier block (i.e., the modified-stacked-switches leg). (a) VD+FW rectifier with PWM+PFM control. (b) VD rectifier with PFM control. (c) FW rectifier with PFM control.

Consequently, the rms value of v_{ab} can be obtained as

$$v_{ab\_\mathrm{rms}} = \frac{2\sqrt{2}V_i}{\pi} \sin(\delta\pi). \tag{19}$$

The overall voltage gain of the resonant tank when charging G_C is

$$G_C = \frac{nv_{cd}}{v_{ab}} = \frac{mQ_1\omega_r^3}{\sqrt{\left[\omega_r^3\sigma_3 + \omega_r\sigma_1\right]^2 + \left[\omega_r^4\sigma_4 + \omega_r^2\sigma_2 + \sigma_0\right]^2}} \tag{20}$$

where

$$\sigma_4 = \left(m + (k+1)\,n^2\right)\, Q_1^2 \tag{21}$$

$$\sigma_3 = m\,(k+1)\,Q_1 \tag{22}$$

$$\sigma_2 = -\omega_r^2\left(m + (2k+1)\,n^2\right) Q_1^2 \tag{23}$$

$$\sigma_1 = -mkQ_1 \tag{24}$$

$$\sigma_0 = kn^2Q_1^2. \tag{25}$$

In the rectifier block, depending on the rectifier topology, the rectifier voltage gain will be different. In FW, the RMS value of

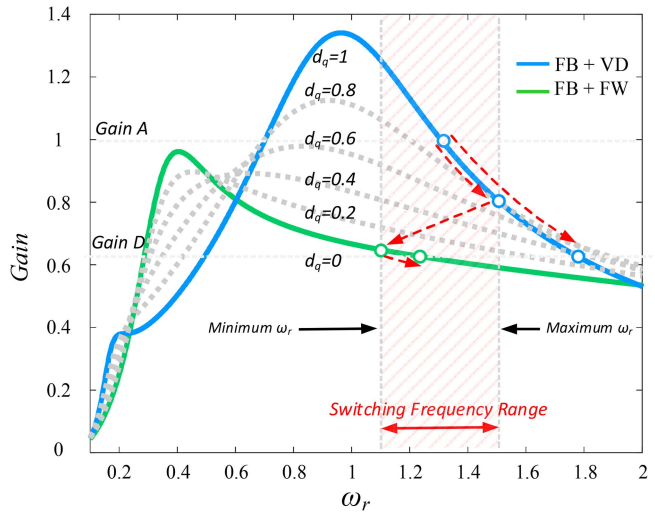

Fig. 15. Voltage gain plot of the proposed stacked-switch converter for various duty ratios in the rectifier block.

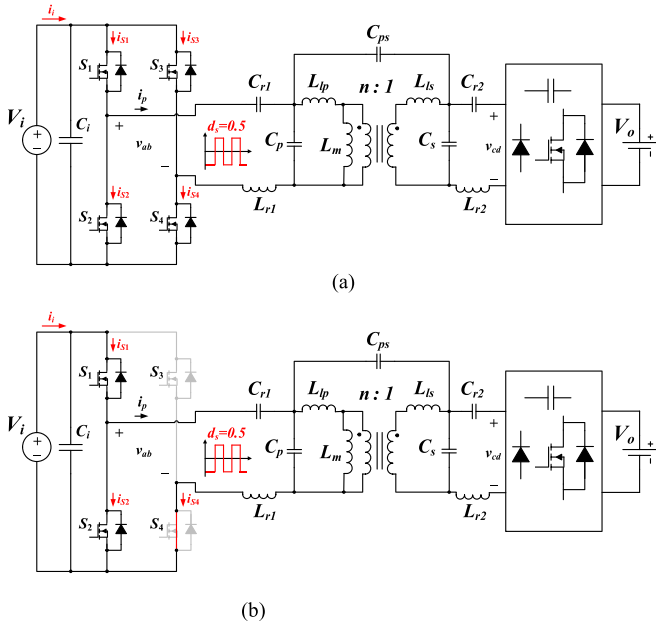

Fig. 16. Different modes of operation of the multimode wide voltage gain converter in the inverter block. (a) FB inverter in mode I and mode II. (b) HB inverter in mode II to mode VI.

the voltage and current are given as

$$V_{cd}\,(\text{rms})\,|_{FW} = \frac{2\sqrt{2}}{\pi}\,V_o \tag{26}$$

$$I_s\,(\text{rms})\,|_{FW} = \frac{\pi}{2\sqrt{2}}\,I_o. \tag{27}$$

In the case of turning Q_3 and Q_4 ON in VD, the above equations change to

$$V_{cd}\,(\text{rms})\,|_{HW} = \frac{\sqrt{2}}{\pi}\,V_o \tag{28}$$

$$I_s\,(\text{rms})\,|_{HW} = \frac{\pi}{\sqrt{2}}\,I_o \tag{29}$$

where the equivalent resistance is given as

$$R_{\text{eq}s}|_{VD} = \frac{2}{\pi^2}\,R_L. \tag{30}$$

As a result, by means of (16) to (30), the overall voltage gain curve of the converter in FW and VD have been provided in Fig. 15. Yet, as can be seen in Fig. 15, by applying PWM signals to Q_3 and Q_4, multiple voltage gain curves can be obtained between the FW and VD curves. Assuming PWM signals with switching frequency of f_s and a duty ratio of d_q are applied to the middle switches in the rectifier block, (26) to (29) will be changed as given

$$V_{cd}\,(\text{rms})\;|_{\text{PWM}} = \frac{(2-d_q)\,\sqrt{2}}{\pi}\,V_o \tag{31}$$

$$I_s\,(\text{rms})\;|_{\text{PWM}} = \frac{\pi}{(2-d_q)\,\sqrt{2}}\,I_o \tag{32}$$

$$R_{\text{eqs}}\;|_{\text{PWM}} = \frac{2(2-d_q)^2}{\pi^2}\,R_L. \tag{33}$$

III. Proposed Multi-Mode Control Scheme for Extended Voltage Gain

As demonstrated in Section II-A, due to the existence of parasitic elements, in addition to proper insulation of the high-frequency windings, the switching frequency of the *CLLC* converter must be limited to prevent the unstable operation of the control system.

Further, as illustrated in Fig. 15, by varying d_q in the rectifier block, several voltage gain curves can be obtained in the converter. Consequently, as demonstrated in Fig. 15, by properly switching between different operating modes, the overall voltage gain of the converter can be extended while limiting the switching frequency spectrum.

However, the voltage gain plot shown in Fig. 15 only takes advantage of the reconfiguration of the rectifier block. In many industrial ac/dc power supplies, the input ac voltage is universal and supports both 120 V_{rms} 60 Hz and 220 V_{rms} 50 Hz sources. Therefore, depending on the application, the converter covers a typical minimum input ac voltage of 90 V_{rms} and a maximum input ac voltage of 240 V_{rms} before the under-voltage ac or over-voltage ac protection is triggered. Consequently, in these applications, one of the approaches to adapt to the input ac voltage while maintaining the same performance is to switch from FB in 120 V_{rms} to HB in 220 V_{rms} input. As demonstrated in Fig. 16, the same approach can be used in dc/dc resonant converters to extend the overall voltage gain of the converter.

A. Description of the Wide Voltage Gain Control System

Fig. 17 demonstrates the overall voltage gain plot of the proposed multi-mode converter system. In Fig. 17, in mode I, the inverter operates in FB and the rectifier acts as a VD with Q_3 and Q_4 turned ON while the output voltage is regulated through

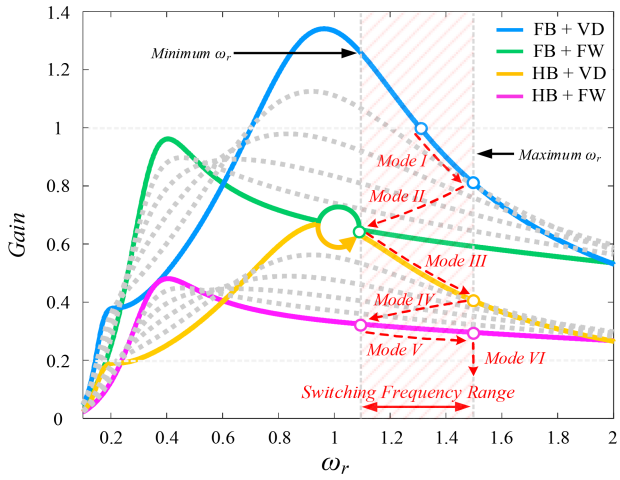

Fig. 17. Voltage gain plot and multimode operation of the proposed converter.

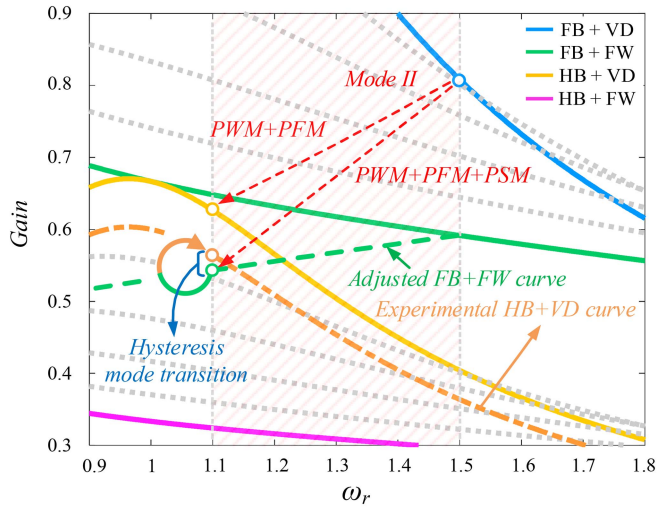

Fig. 18. Voltage gain plot and multimode operation of the proposed converter with adjustments in mode II.

PFM. Once the switching frequency hits the upper limit, the control system switches to mode II.

In mode II, while the inverter continues to operate as a FB, PWM signals are applied to Q_3 and Q_4 making the rectifier operate between VD with $d_q = 1$ and FW with $d_q = 0$. At the same time, to provide a smooth transition between VD to FW, as d_q is reduced, the switching frequency is decreased linearly. In this mode, by exceeding $d_{q\max}$ the control moves back to mode I, and by hitting $d_{q\min}$, the control moves to mode III. Yet, as can be seen in Fig. 17, the voltage gain curve of FB+FW intersects with HB+VD at $f_{s\min}$. Consequently, to increase the voltage gain range of the overall control system, when d_q hits the bottom limit, the inverter switches from FB to HB and the topology of the rectifier changes from FW back to VD. However, as illustrated in Fig. 18, in practice and especially in light loads, the HB+VD curve peaks slightly below FB+FW. As a result, to address this, in mode II, in addition to reducing d_q and the switching frequency, the phase shift between the first and second leg of the FB is adjusted in a way to make the curves intersect at $f_{s\min}$. Adding the PSM in mode II not only enables a smooth transition, but also provides a hysteresis feature preventing the converter from switching back and forth around the border of mode II and mode III.

TABLE I
SUMMARY OF THE MULTI-MODE WIDE VOLTAGE GAIN CONTROL SYSTEM

Mode	Modulation Method	Inverter Structure		Rectifier Structure
I	PFM	FB		VD
II	PWM+PFM+PSM	FB	T1	$VD\|_{PWM}$
III	PFM	HB	T2	VD
IV	PWM+PFM	HB	T3	$VD\|_{PWM}$
V	PFM	HB	T4	FW
VI	APWM	HB	T5	FW

The operation of the multimode control in mode III is the same as mode I but S_3 is turned OFF while S_4 is turned ON to enable the inverter to operate as an HB. In the same manner by hitting $f_{s\max}$, the control moves to mode IV.

Similarly, in mode IV, by applying PWM signals to Q_3 and Q_4, the control in the rectifier block smoothly transitions from VD to FW. However, considering that the inverter operates as an HB, there is no PSM included in the control. By hitting $d_{q\min}$, the control switches from $HB+VD|_{PWM}$ to HB+FW in mode V.

In mode V, Q_3 and Q_4 are turned OFF and the inverter and rectifier operate in HB and FW respectively while the voltage is regulated through PFM. By exceeding f_{smax} the control moves to mode V.

In mode VI, the converter continues to operate in HB+FW, however, to limit the switching frequency, the control system operates in APWM mode regulating the output voltage by adjusting the duty ratio of the inverter side switches (d_s) while keeping f_s at $f_{s\max}$.

Table I gives the operating modes of the proposed wide voltage gain control system along with the structure of the inverter and the rectifier blocks with the modulation techniques used in each mode while showing the main changes at each transition.

Although there are 6 different operating modes in the proposed control system, according to Fig. 17, the main challenge with the transient and the accuracy of the control system at borders happen when transitioning from mode II to mode III where the inverter switches from FB to HB, while in other mode changes, the transition happens smoothly and minor changes happens in the control parameters.

*T*1: In the transition from mode I to mode II, while the inverter and its modulation stay the same, the control system regulates the output by modifying the topology of the rectifier circuit. As the control moves from mode I to mode II, PWM signal are applied to Q_3 and Q_4, yet the transition is smooth, and the change in the duty ratio is minimal. Hence, even in the case of operating at the border, there will be no unstable and inaccurate operation.

*T*2: In switching from mode II to mode III, the converter undergoes a major transition in which the configuration of both the inverter and rectifier changes where the inverter switches from FB to HB and the rectifier switches from FW rectifier to VD. As a result, proper design of the control and operating

TABLE II
VOLTAGE GAIN FORMULA IN EACH MODE OF OPERATION

Mode	Voltage Gain	Quality Factor
I	$\frac{V_o}{V_i}=\frac{2G_C}{n}\sqrt{\sum_{h=1,3,5,\ldots}^{\infty}\left[\frac{1}{h}\right]^2}$	$Q_1=\frac{\pi^2\sqrt{\frac{L_{r1}}{C_{r1}}}}{2n^2R_L}$
II	$\frac{V_o}{V_i}=\frac{2G_C\sqrt{\sum_{h=1,3,5,\ldots}^{\infty}\left[\frac{1}{h}\sin(h\pi\delta)\right]^2}}{n(2-d_q)}$	$Q_1=\frac{\pi^2\sqrt{\frac{L_{r1}}{C_{r1}}}}{2n^2(2-d_q)^2R_L}$
III	$\frac{V_o}{V_i}=\frac{G_C}{n}\sqrt{\sum_{h=1,3,5,\ldots}^{\infty}\left[\frac{1}{h}\right]^2}$	$Q_1=\frac{\pi^2\sqrt{\frac{L_{r1}}{C_{r1}}}}{2n^2R_L}$
IV	$\frac{V_o}{V_i}=\frac{G_C\sqrt{\sum_{h=1,3,5,\ldots}^{\infty}\left[\frac{1}{h}\right]^2}}{n(2-d_q)}$	$Q_1=\frac{\pi^2\sqrt{\frac{L_{r1}}{C_{r1}}}}{2n^2(2-d_q)^2R_L}$
V	$\frac{V_o}{V_i}=\frac{G_C}{2n}\sqrt{\sum_{h=1,3,5,\ldots}^{\infty}\left[\frac{1}{h}\right]^2}$	$Q_1=\frac{\pi^2\sqrt{\frac{L_{r1}}{C_{r1}}}}{8n^2R_L}$
VI	$\frac{V_o}{V_i}=\frac{G_C}{2n}\sqrt{\sum_{h=1,3,5,\ldots}^{\infty}\left[\frac{1}{h}\sqrt{\frac{1-\cos(2h\pi d_s)}{2}}\right]^2}$	$Q_1=\frac{\pi^2\sqrt{\frac{L_{r1}}{C_{r1}}}}{8n^2R_L}$

limits is necessary to avoid mode oscillations at the border to avoid inaccurate and unstable operation.

To achieve this, a hysteresis operation has been considered in the design by adding the phase-shift modulation in the overall control in mode II. As a result, as can be seen in Fig. 18, by adding a phase shift between the left and right leg switches of the inverter, the voltage gain curve is adjusted (dashed green) in a way to bring the gain curve in mode II much lower that the starting point in mode III. Consequently, the hysteresis area between the voltage gain in mode II and mode II prevents the control from oscillating between the two modes at around the border. The depth of the hysteresis area can be adjusted by modifying the phase shift between the legs of the FB inverter.

*T*3: The transition in T3 is quite identical to that of T1. After hitting the upper-frequency limit, the control moves to mode IV where PWM signals are applied to the middle switches. Considering the modulation, by properly designing the control, the transition can be done smoothly without negatively impacting the accuracy or the stability of the control system.

*T*4: Transitioning from mode IV to V is similar to T2. However, the main difference is no major transient is imposed on the converter since there is no reconfiguration on the inverter side and there is a smooth transition between the two modes.

*T*5: Considering that in T5, the topology of both the inverter and rectifier blocks remain unchanged and only the modulation technique changes, the transients are minimized, and mode transition happens smoothly.

The overall voltage gain formula of the converter in different operating modes and its associated quality factor expressions have been given in Table II.

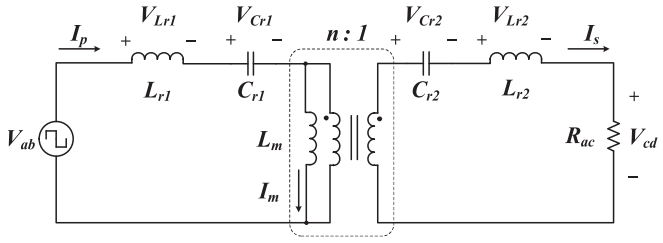

Fig. 19. Equivalent circuit of the proposed *CLLC* converter.

To provide closed-loop analysis for the proposed converter, four PI controllers have been developed depending on the main modulation technique (PFM, PSM, PWM, and APWM) used in various operating modes. FHA has been used to calculate the controller voltage gain along with the Control System Analysis Toolbox in MATLAB. Since there are two subsystems in the closed-loop system with high-frequency (converter) and low-frequency (PI controller) performance, developing a comprehensive model of the high-frequency converter only results in a complicated design process. As a result, an average model has been used to design the low-frequency controller. Consequently, the use of FHA is reasonable to design the control system in the proposed converter.

In doing so, the equivalent circuit of the proposed *CLLC* converter has been provided in Fig. 19. The following differential equations have been obtained by using the KVL and KCL laws

$$\begin{aligned} &-V_{ab}+L_{r1}\dot{I}_p+V_{Cr1}+L_m\dot{I}_m=0 && I_p=C_{r1}\dot{V}_{Cr1}\\ &-V_{ab}+L_{r1}\dot{I}_p+V_{Cr1}+L_{r2}\dot{I}_s+V_{Cr2}+V_{cd}=0 && I_s=C_{r2}\dot{V}_{Cr2}.\\ &V_{cd}=R_{ac}I_s && I_p=I_m+I_s \end{aligned} \tag{34}$$

As given in (18), based on FHA, $V_{ab}=\frac{4V_i}{\pi}\sin(\delta\pi)\sin(\omega_s t-\frac{\alpha T_s}{2})$ can be approximated as the input to the resonant converter. Considering that f_s, d_s, and d_q have been considered as the main control inputs of the system and the fact that these parameters do not exist in the equations independently, and they are implicitly present in (17) and (18), the system will have a general form as

$$\frac{dx}{dt}=f(x)+g(x,u). \tag{35}$$

To design PI controllers to provide voltage regulation, the nonlinear system (34) has been linearized using Control System Analysis Toolbox in MATLAB, and the frequency response of the system is achieved. Then, its frequency response has been analyzed based on the utilized modulation technique. In each mode, to neutralize the harmful effect of PI controller's pole at the origin, the controller's zero has been considered to be close to the origin (i.e., $s=0.1$). Using Control System Analysis Toolbox, at each operating mode, K_d and K_l have been modified to achieve the damping ratio of $\zeta=0.5$ and based on that, the values of K_p and K_i have been obtained.

The block diagram of the proposed control system is demonstrated in Fig. 20. Considering having different ground at the primary and secondary side of the resonant current, the output voltage is sampled through isolated amplifier and after passing through a low-pass filter being compared to the reference, the

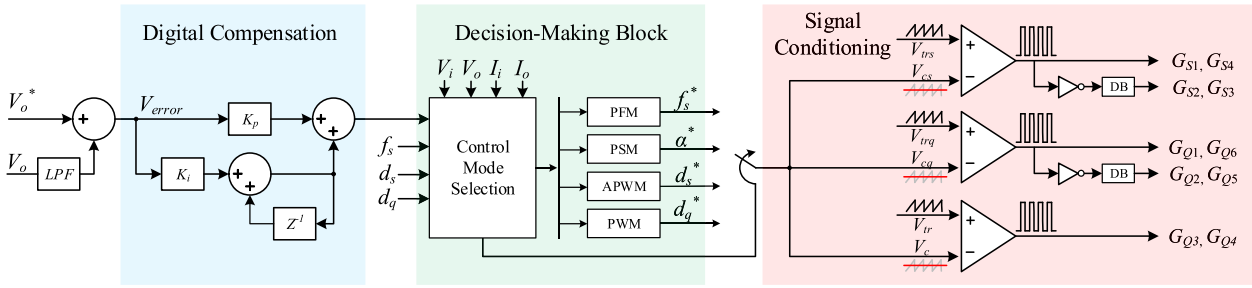

Fig. 20. Block diagram of the multimode control system.

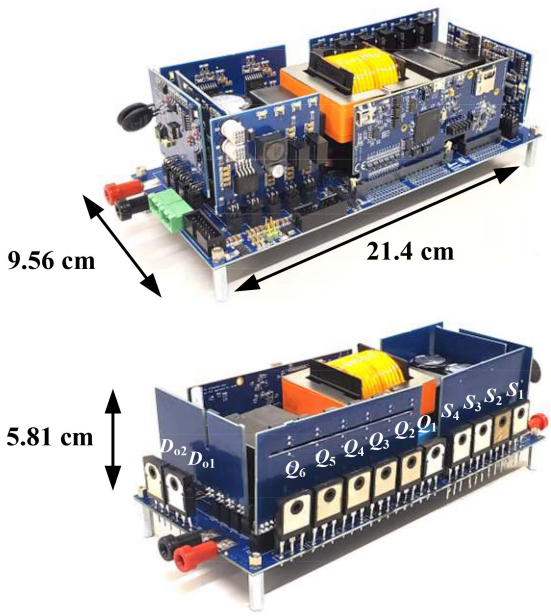

Fig. 21. Proof-of-concept 500 W, 100–350 V input 96 V output prototype.

TABLE III
DESIGN SPECIFICATIONS AND CIRCUIT PARAMETERS

	Qty	Vendor	Part No.	Value	Desc.
L_M	1	Custom	Custom	108.8 µH	16T primary
n_p/n_s	-	-	-	1.5	-
L_{r1}	1	Coilcraft	SER2918H-153	~16 µH	-
L_{r2}	1	Coilcraft	SER2915L-332	~ 3 µH	-
C_{r1}	1	KEMET	PHE450RB5150	150 nF	1.6 kV, PP
C_{r2}	3	KEMET	PHE845VZ6470	1.57 µF	1.5 kV, PP
f_s	-	-	-	100 kHz to 125 kHz	-
S_1-S_4, Q_1-Q_6	10	United SiC	UJ4C075033K3S	SiC MOSFET	-
FET Driver	10	Toshiba	TLP155E	170ns, 15kV/us Optocoupler	-
D_{o1}, D_{o2}	2	Infineon	AIDW40S65C5	SiC Schottky Diode	-
C_{i1}	2	Nichicon	LGL2G391MELA	390 uF	400 V, Alum
C_{i2}	1	Panasonic	EZP-E50106LTA	10 uF	500V, PP
C_o	2	Panasonic	EZP-E50256LTA	25 uF	500V, PP
C_{S1}-C_{S4}	4	KEMET	PHE448SB3100	100 pF	2 kV, PP
C_{O1}-C_{O6}	6	KEMET	PHE448SB3330	330 pF	2 kV, PP
MCU	1	TI	TMS320F28379	-	200MHz
P_o	-	-	-	500 W	-
V_o	-	-	-	96 V	-
V_i	-	-	-	100 V ~ 350 V	-

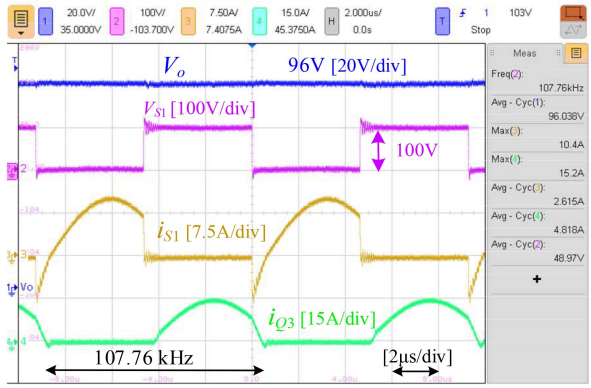

Fig. 22. Experimental waveforms of the converter in mode I. Input and output voltage and the current passing through S_1 and Q_3.

error goes through digital compensation and output is fed to the decision-making block along with the output current and the input voltage and current.

While initially the control starts from mode I, at each digital interrupt, the decision-making block reads the input and output voltage and current and depending on the current mode, f_s, α, d_s, and d_q, it determines the next operating mode and generates the reference signals for the next cycle and through the signal conditioning block, gate signals are applied to the corresponding switches.

IV. Experimental Results

To investigate the performance of the proposed wide voltage gain multi-mode control system, a 500 W, 100–350 V input 96 V output dc/dc prototype with *CLLC* resonant tank shown in Fig. 21 has been designed and developed. The parameters and specifications of the converter in Fig. 21 are given in Table III.

The key waveforms of the converter are demonstrated in Figs. 22, 23, and 24. The control starts in mode I (FB + VD). Fig. 22 illustrates the output voltage, the drain to source voltage and current of S_1, and the current passing through Q_3 where the input voltage is 100 V and the output load is 18.5 Ω.

The resonant current passing through the primary and the secondary of the resonant tank are given in Fig. 23.

To fully investigate the performance of the multimode control system, as depicted in Fig. 25, the input voltage is increased from 100 V and consequently, the voltage gain is reduced from point A to point L while the output is regulated at 96 V.

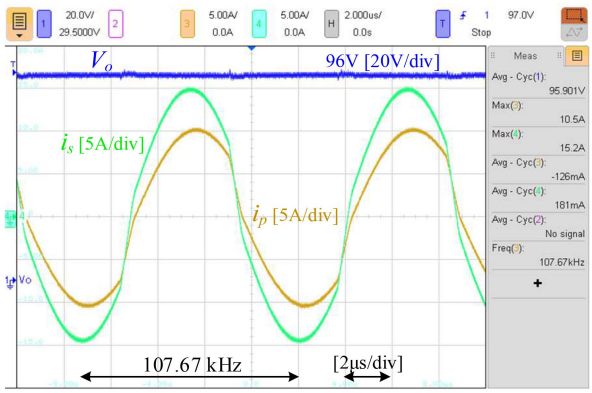

Fig. 23. Experimental waveforms of the converter in mode I. Input and output voltage and the current passing through S_1 and Q_3.

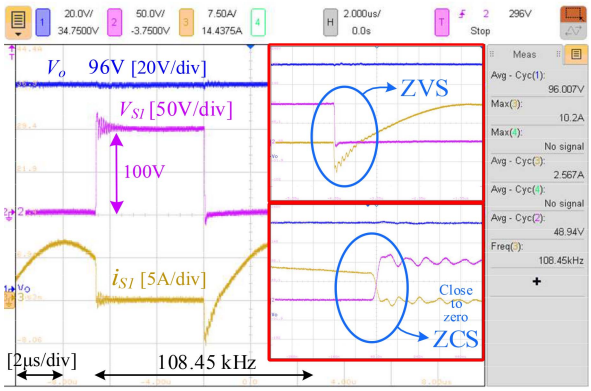

Fig. 24. Experimental waveforms of the converter in mode I. Output voltage and voltage and current of S_1 in the inverter block.

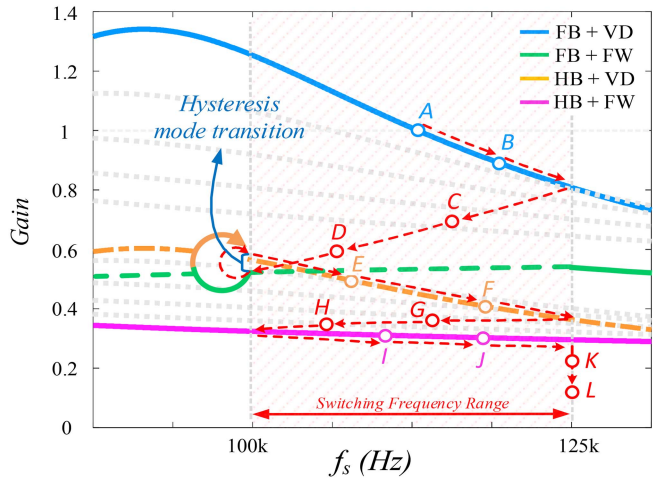

Fig. 25. Overall voltage gain plot of the *CLLC* resonant circuit with different scenarios moving from a gain of A to a gain of L.

The dynamic response of the multi-mode control is provided in Fig. 26. In mode I, the input is increased from 100 to 110 V going from point A to B and the output is regulated at 96 V through PFM in FB+VD.

In Fig. 27, the input goes from 110 to 130 V moving from a gain of B to C. By switching from mode I to mode II, the

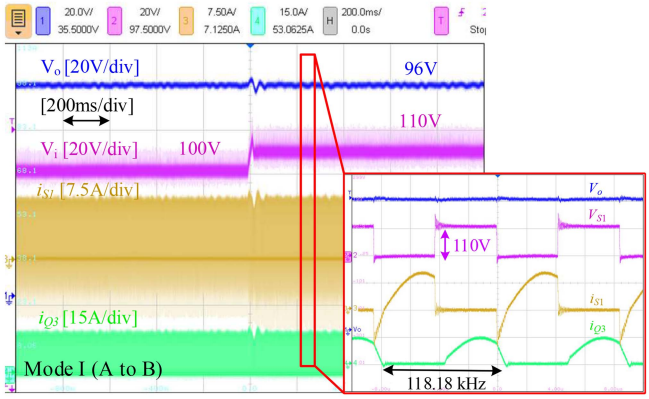

Fig. 26. Dynamic response of the converter in mode I for a step change in V_i (100 to 110 V).

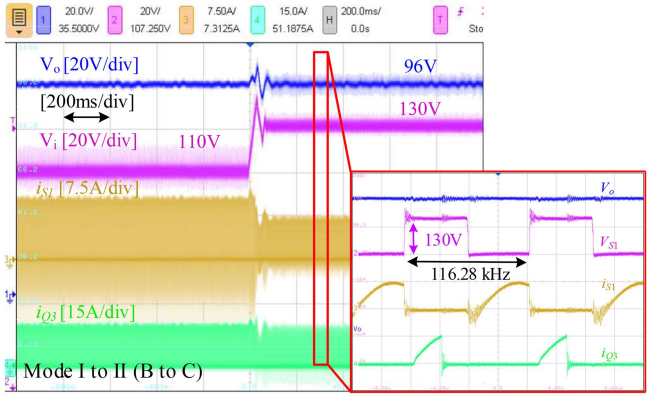

Fig. 27. Dynamic performance of the converter transitioning from mode I to mode II for a step change in V_i (110 to 130 V).

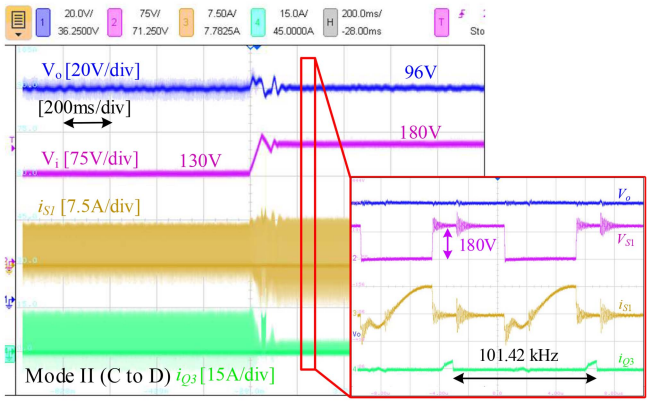

Fig. 28. Dynamic response of the converter in mode II for a step change in V_i (130 to 180 V).

control regulates the output voltage through PWM+PFM+PSM in FB+VD$|_{\text{PWM}}$ by changing the duty cycle and adjusting the switching frequency and the phase shift accordingly.

To investigate the performance of the control in mode II, the voltage is further increased from 130 to 180 V in Fig. 28. As demonstrated, the output is regulated at 96 V.

Fig. 29 shows the control system's ability to regulate the voltage by switching from FB to HB in the inverter block and at the

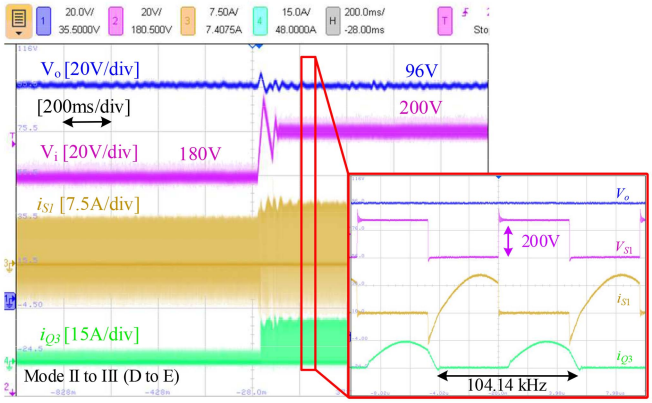

Fig. 29. Dynamic performance of the converter transitioning from mode II to mode III for a step change in V_i (180 to 200 V).

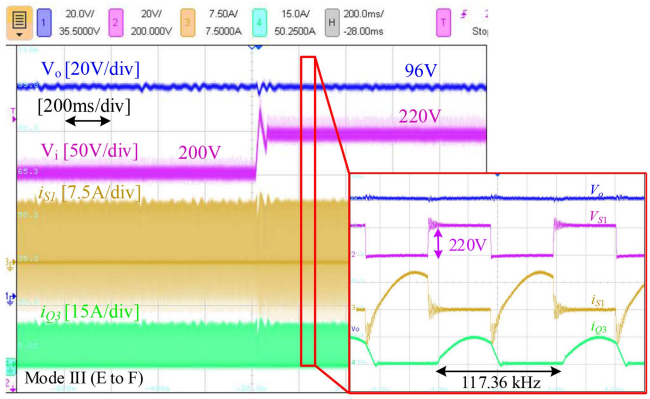

Fig. 30. Dynamic response of the converter in mode III for a step change in V_i (200 to 220 V).

same time switching to VD in the rectifier block in transitioning from mode II ($V_i = 180$ V) to mode III ($V_i = 200$ V). As can be seen, the output voltage is regulated through PFM.

In mode III, the operation of the control system is similar to mode I with only the inverter operating as a HB. The dynamic response of the control after applying a step change in V_i going from 200 to 220 V has been given in Fig. 30.

In the same manner that was described in mode II, by applying PWM signals to Q_3 and Q_4 and adjusting the duty ratio, the output voltage is regulated. However, unlike mode II, considering that the inverter is operating as an HB, PSM is not included in this mode. The performance of the control system in the case of increasing V_i from 220 to 240 V moving from mode III to mode IV has been provided in Fig. 31.

Fig. 32 demonstrates the dynamic response of the control system in mode IV with a step voltage change from 240 to 300 V.

By further increasing the input voltage and reducing the voltage gain from point H to point I, as illustrated in Fig. 33, the control moves from mode IV to mode V where Q_3 and Q_4 are turned OFF and the rectifier switches to FW and the output voltage is regulated through PFM. Fig. 33 shows the transition by increasing the input from 300 to 330 V.

The dynamic performance of the control system in mode V moving from point I to J has been given in Fig. 34.

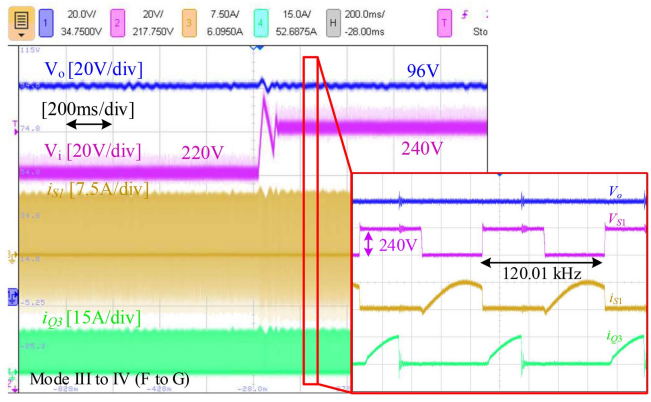

Fig. 31. Dynamic performance of the converter transitioning from mode III to mode IV for a step change in V_i (220 to 240 V).

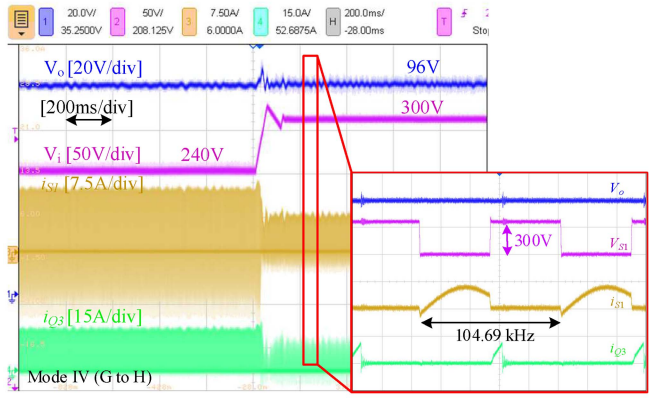

Fig. 32. Dynamic response of the converter in mode IV for a step change in V_i (240 to 300 V).

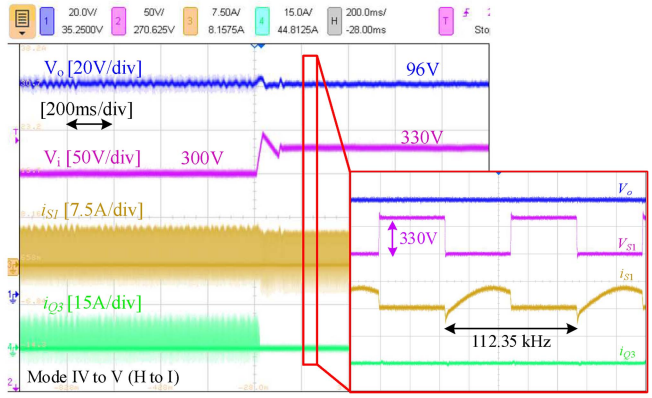

Fig. 33. Dynamic performance of the converter transitioning from mode IV to mode V for a step change in V_i (300 to 330 V).

Similarly, by further increasing the input voltage the switching frequency hits the upper limit and the control moves from point J in mode V to point K in mode VI shown in Fig. 35. In mode VI, the switching frequency is kept constant at f_{smax} and the output voltage is regulated through APWM by adjusting the duty ratio of the inverter side switches.

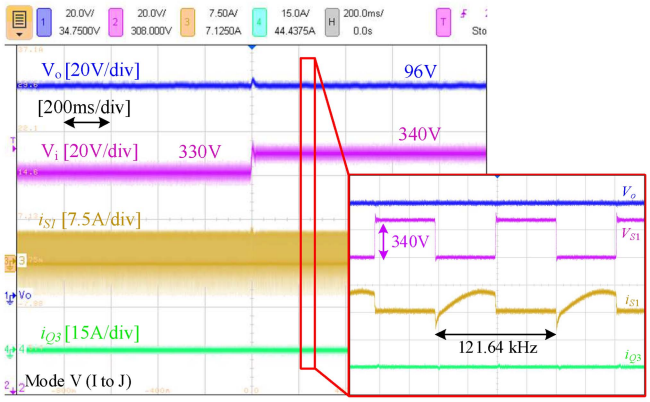

Fig. 34. Dynamic response of the converter in mode V for a step change in V_i (330 to 340 V).

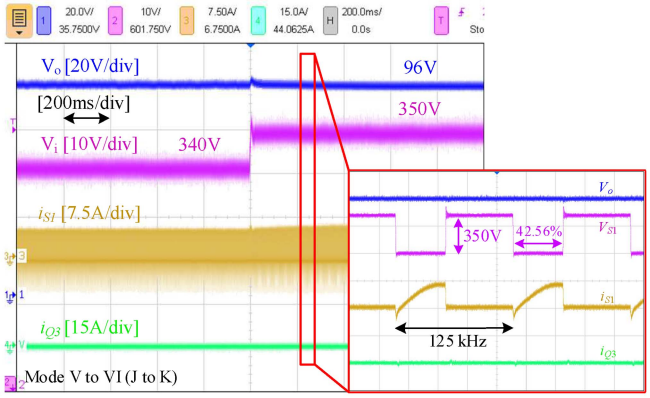

Fig. 35. Dynamic performance of the converter transitioning from mode V to mode VI for a step change in V_i (340 to 350 V).

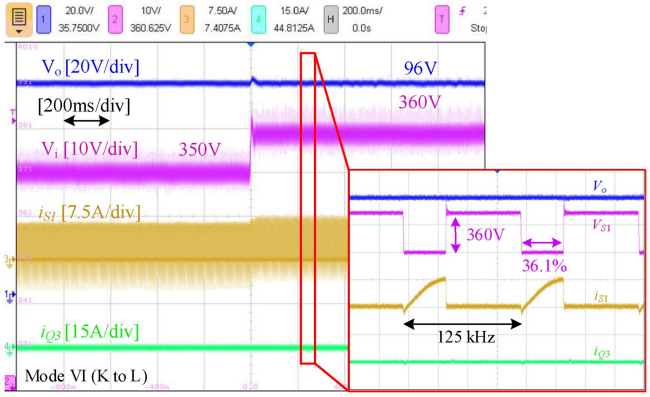

Fig. 36. Dynamic response of the converter in mode VI for a step change in V_i (350 to 360 V).

Fig. 36 illustrates the performance of the APWM loop in mode VI going from 350 to 360 V while regulating the output at 96 V by keeping f_s at $f_{s\max}$ and reducing the duty ratio of the gate signals at the inverter block.

As demonstrated in previous operating points, the proposed control is able to regulate the output voltage for a wide input voltage range while keeping the switching frequency within a narrow operating range.

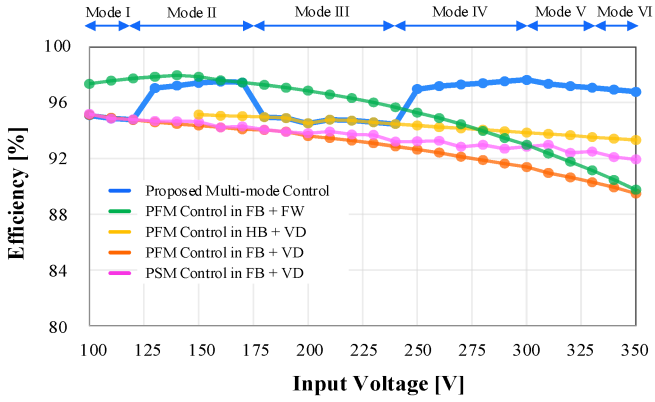

Fig. 37. Efficiency comparison of various control modulation approaches with the same rated power.

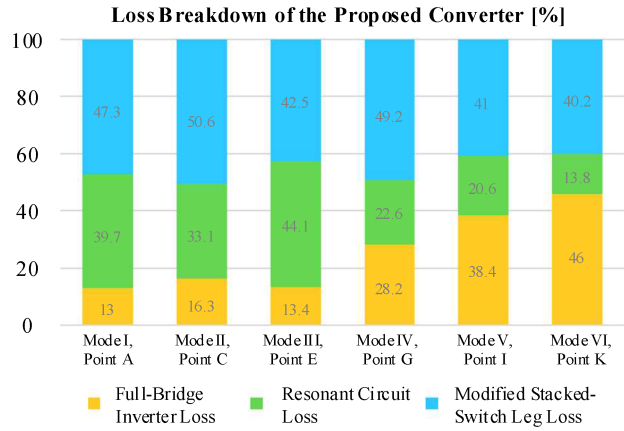

Fig. 38. Loss breakdown of converter at rated power.

The efficiency plot of the proposed control system compared with various control modulation techniques in terms of the input voltage at full load has been given in Fig. 37. Also, the loss breakdown of the proposed converter in various operating modes has been provided in Fig. 38. In addition, the performance of the proposed converter is compared with the popular bidirectional isolated dc/dc converters in Table IV.

Although the proposed FB-Stacked-Switch Converter employs a higher number of active switches compared to the DAB converter, it maintains fewer overall switches and passive components than the active neutral point clamped TL converter with a flying capacitor (FC).

Despite potentially exhibiting slightly reduced efficiency at rated power due to switch $R_{ds\mathrm{ON}}$, the converter offers a wide operating voltage gain range through topology morphing and mode switching. This approach restricts the switching frequency and prevents substantial deviation from the resonant frequency.

As a result, the converter achieves improved efficiency at very low voltage gains and maintains an almost flat efficiency profile. Moreover, it prevents voltage regulation instability at light loads caused by parasitic components by confining the switching

TABLE IV
COMPARISON OF ISOLATED BIDIRECTIONAL CONVERTERS [29]

Topology	Voltage Gain	No. of Switches	No. of Passive Elements	No. of Windings	Power Density	V_{in} (V)	P_o (W)	Max η	Applications
Flyback [30]	$\frac{ND}{1-D}$	2	2	2	Low to Medium	12	25	90%	Uninterruptable Power Supplies
CUK [31]	$\frac{ND}{1-D}$	2	6	2	Low to Medium	440	2200	89%	Photovoltaic Systems
Push-Pull [32]	ND	4	2	4	Medium	20 to 45	600	94%	PV generated system for residential applications, UPSs
Forward [33]	ND	4	2	2	Low to Medium	12	20	94%	RESs, BESSs, EVs, UPSs
Dual Active Bridge [34]	M.D.*	8	2	2	High	500	1000	95%	Automotive, BESSs
Dual-Half Bridge [34]	M.D.	4	6	2	High	500	1000	94%	Automotive, Fuel Cell, BESSs
Half-Full Bridge [35]	M.D.	6	4	2	High	60	320	94%	Uninterruptable Power Supplies, EVs
Multiport (DAB) [36]	M.D.	4n	n	n	High	9	500	96%	Multi Sustainable Sources Generation Systems
Three Level (TL) [37]	M.D.	8	6	2	High	100	600	97%	RESs, BESSs, EVs, UPSs
ANPC TL with FC [38]	M.D.	12	8	2	High	500	3500	97%	Automotive, Fuel Cell, BESSs
Half-Bridge CLLC [34]	M.D	8	7	2	High	500	1000	97%	Automotive, Fuel Cell, BESSs
Full-Bridge CLLC [34]	M.D	8	5	2	High	500	1000	96%	Automotive, BESSs
Dual Stacked Switch CLLC [27]	M.D.	12	9	2	High	1000	1000	97%	Automotive, BESSs
The Proposed Converter	M.D.	10	8	2	High	400	500	97%	Battery Energy Storage Systems

* N is the transformer ratio
** Modulation Dependent

frequency spectrum. This developed converter presents an appealing solution for high-voltage, high-power energy storage applications where a wide voltage gain range is required and the impact of switch R_{dsON} is minimized due to the low current characteristics of these applications.

The thermal image of the converter operating at rated power has been provided in Fig. 39. To properly demonstrate the loss distribution at rated power, the heatsinks and fans were removed. Fig. 39(a) illustrates the heat distribution in mode I where Q_3 and Q_4 are turned ON, and Fig. 39(b) demonstrates the heat distribution in mode II where PWM signals are applied to Q_3 and Q_4. As can be seen, due to soft switching, the introduction of Q_3 and Q_4 does not contribute to any significant drop in the overall efficiency.

V. CONCLUSION

A new multimode controlled *CLLC* resonant converter that utilizes a FB circuit on the primary side and a modified-stacked-switches leg on the secondary side has been presented in this article for energy storage applications. The impact of the parasitic elements on the *CLLC* resonant converter has first been studied. The investigation showed that to ensure a stable operation within the whole loading profile, the converter's switching frequency needs to be restricted and prevented from drifting away from the resonant frequency.

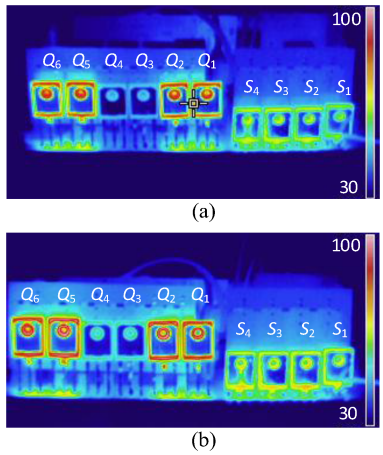

Fig. 39. Thermal image of the proposed converter at rated power. (a) Mode I. b) Mode II.

To overcome the above issue, a multimode control scheme has been presented to regulate the output voltage for wide voltage gain applications within a narrow switching frequency spectrum by taking advantage of the reconfigurable structure of both the inverter side and the rectifier side circuits. A 100 V∼350 V/96 V, 500 W, 100–125 kHz proof of concept prototype has been developed and a comparative analysis and experimental studies have been performed to investigate the performance of the proposed converter system. The results confirmed that the converter regulates the output voltage within a wide input voltage range while providing soft switching for all of the semiconductor devices.

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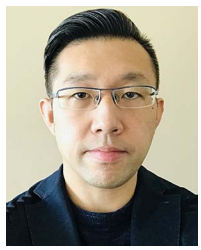

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