A Low Computing FCS-MPC Based on Voltage Vector Tracking Algorithm With CMVs Suppression and Capacitor Charging Balance Algorithm Without Weight Factors for ANPC 3P-5L Converters

Shaomin Yan, Chengmin Li, Yue Cui, Hao Zhang, and Qingyun Yang

***Abstract*—Active neutral-point clamped three-phase five-level (3P-5L) converter system under conventional FCS-MPC algorithm is subjected to high computational burden, large common mode voltages (CMVs), unfixed switching frequency, and cumbersome weight factor design. To tackle above defects, in this article, a low computing FCS-MPC based on voltage vector tracking algorithm with CMVs suppression and capacitor charging balance algorithm without weight factors is proposed for ANPC 3P-5L converters. First, a voltage vector tracking algorithm with CMVs suppression is adopted, which filtrates 64 redundant voltage vectors to reduce CMVs, selects voltage vector by sector boundary conditions to lower computational burden, and enhances vector tracking accuracy with fixed switching frequency. Second, a capacitor charging balance algorithm is proposed to balance flying capacitor voltages (FCVs) and dc capacitor voltages (DCVs) without weight factors, which adjusts operation time of redundant switch states to balance FCVs according to each phase flying capacitor charges, and selects redundant switch states to balance DCVs according to upper and lower capacitor charges. Finally, advantages of proposed MPC are verified in experiment, where the errors of current, FCVs and DCVs are decreased by 1.4 A, 1.2 V and 0.2 V, and current THD, transient time and code execution time are decreased by 2.25%, 20 ms and 151.5 μs respectively.**

***Index Terms*—Active neutral-point clamped (ANPC), capacitor charging balance algorithm, common mode voltages (CMVs) suppression, finite-control set model predictive control (FCS-MPC), fixed switching frequency, three-phase five-level (3P-5L) converter, voltage vector tracking algorithm.**

I. Introduction

THREE-PHASE five-level (3P-5L) power electronic converters have been increasingly applied in wind power generation, high-voltage flexible ac/dc transmission, high-performance motor system, and other fields with the advantages of high voltage and power levels [1], [2], [3], [4], which includes topology structures of cascaded H-bridge, flying capacitor, neutral point clamped (NPC), and active neutral point clamped (ANPC) [5], [6]. Compared to other 3P-5L converters, ANPC 3P-5L converter has advantages of simple structure and flexible control, which combines of NPC and flying capacitor 3P-3L converter [7], [8], [9]. Therefore, ANPC 3P-5L converter system with an optimal FCS-MPC algorithm is carried out in this article in Fig. 1.

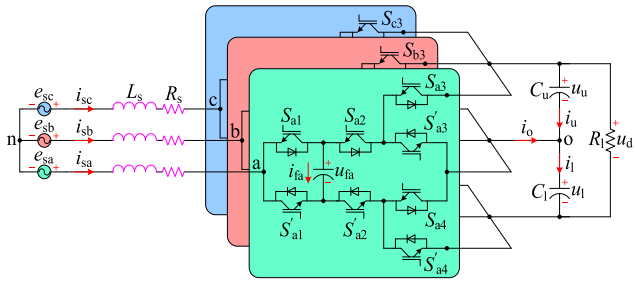

Fig. 1. ANPC 3P-5L converter topology.

Traditional linear control strategies are difficult to meet the dynamic and decoupling requirements of ANPC 3P-5L converter system [10]. Finite-control set model predictive control (FCS-MPC) has been widely applied in power converter system with its fast dynamic response, flexible multi-objective and multiconstraint synchronization processing, no modulation, and simplified controller design [12], [13], [14], which could overcome the mentioned problem of traditional linear control strategies and improves system performance [14]. However, traditional FCS-MPC has some disadvantages of low control accuracy, high computational burden and cumbersome weight factor design [15], [16]. Thus, relevant optimization researches on FCS-MPC are carried out for 3P-2L converter, 3P-3L converter and 3P-5L converter.

For 3P-2L converter, some researches are carried out to improve control accuracy and reduce computational burden in [17] and [18]. In [17], a low complexity MPC algorithm is proposed, which determines the optimal voltage vector directly

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Shaomin Yan, Chengmin Li, Hao Zhang, and Qingyun Yang are with the School of Engineering, Qufu Normal University, Rizhao 276827, China (e-mail: yansm@qfnu.edu.cn; lichengmin@qfnu.edu.cn; h_zhang1128@qfnu.edu.cn; yang_qy@qfnu.edu.cn).

Yue Cui is with the School of Electrical Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: cuiyue@hust.edu.cn).

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to reduce computational burden and operational time. However, single vector output mode leads to low control accuracy. In [18], a sector optimization method based on effective vector radiation range is applied to directly determine the optimal vector without vector traversal, which reduces computational burden and improves control accuracy.

For 3P-3L converter, some researches are carried out to improve control accuracy, fix switching frequency, reduce computational complexity, and eliminate weight factor in [19], [20], and [21]. In [19], a fast finite-switching-state MPC algorithm without weighting factor is proposed, which reduces the number of voltage vector from 27 to 3, avoids cumbersome weight factors design and lowers computational burden. An FCS-MPC algorithm is designed in [20] to realize dc-capacitor voltage balance with basic voltage vectors and virtual voltage vectors that do not affect midpoint potential. In [21], an optimization method of sector is designed to select the optimal vector of current targets without traversal optimization, and a dc-capacitor voltage balance method is adopted to determine the optimal vector for neutral-point potential balance without weight factors. In [19], [20], and [21], computational burden is reduced and weight factors are eliminated, but their switching frequency is not fixed. A modulated FCS-MPC strategy is designed in [22] to obtain fixed switching frequency, and weight factor is eliminated based on capacitor charging balance algorithm.

For 3P-5L converter, the issues of high accuracy, fixed switching frequency, low computational complexity, low CMVs and no weight factors are mainly focused on in [23], [24], and [25]. In [23], a MPC strategy based on SVPWM algorithm with fixed switching frequency is proposed, which adds CMVs term into cost function to reduce CMVs, but weight factors design is complex and cumbersome. In [24], a fast MPC strategy is proposed, which eliminates CMVs according to vector traversal optimization of zero CMVs vectors, and reduces the number of weight factors according to two-step prediction. To eliminate weight factors, in [25], a computation-efficient MPC without CMVs is proposed, which balances flying and dc-link capacitor voltages by selecting appropriate switching combinations of optimal voltage vectors, eliminates CMVs by zero CMVs vectors and only selects five voltage vectors for MPC optimization according to the location of voltage vector targets.

Different from the balance method of dc capacitor voltage (DCVs) and FCVs by comparing their voltage values without accurate action time in [26], a capacitor charging balance algorithm is proposed, which calculates action time of two redundant switch states accurately and balances DCVs and FCVs effectively. Different from dual vector synthesis method in [27], a three voltage vector synthesis mode is adopted in voltage vector tracking algorithm to improve reference current tracking accuracy. Different from CMVs suppression method that only remains 19 zero CMVs vectors for voltage targets in [28], a CMVs suppression method is applied by 61 voltage vectors with small CMVs and has high control accuracy.

In this article, the main innovation points are as follows.

1) Vector tracking algorithm with CMVs suppression is proposed, which filters 64 redundant vectors to reduce its fluctuation by their effects on CMVs. And three voltage vector synthesis mode is applied to improve reference vector tracking accuracy and fixe switching frequency.
2) Voltage vector is selected directly by sector boundary conditions to reduce computational burden.
3) A capacitor charging balance algorithm is proposed, which adjusts redundant switch state operation time to balance FCV and DCV.

TABLE I
U_{ao}, I_{fa}, AND I_{o} UNDER EIGHT SWITCH STATES

u_{ao}	i_{fa}	i_{o}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	State
$u_{\mathrm{d}}/2$	0	0	1	1	1	1	SS_{a1}
$u_{\mathrm{d}}/4$	i_{sa}	i_{sa}	1	0	1	1	SS_{a2}
$u_{\mathrm{d}}/4$	-i_{sa}	0	0	1	1	1	SS_{a3}
0	0	i_{sa}	1	1	0	0	SS_{a4}
0	0	i_{sa}	0	0	1	1	SS_{a5}
-$u_{\mathrm{d}}/4$	-i_{sa}	i_{sa}	0	1	0	0	SS_{a6}
-$u_{\mathrm{d}}/4$	i_{sa}	0	1	0	0	0	SS_{a7}
-$u_{\mathrm{d}}/2$	0	0	0	0	0	0	SS_{a8}

II. Converter Topology and System Modeling

The ANPC 3P-5L converter topology is depicted in Fig. 1, where e_{sx} and i_{sx} ($x = a,b,c$) are grid voltage and current; u_{fx} and i_{fx} ($x = a,b,c$) are floating capacitor voltages and currents; i_{o} is neutral-point current; u_{d} is dc-link voltage; u_u, u_l, i_l and i_u are lower and upper DCVs and currents; u_{xo} ($x = a,b,c$) is output voltage of phase-x; u_{on} is CMVs; R_s and L_s are resistance and inductance of ac-side inductors; C_{fx} ($x = a,b,c$) is phase-x flying capacitor; C_u and C_l are dc-link upper and lower capacitors; and R_l is dc-link resistance load.

Taking phase-a for an example, the switching rules of power converter are as follows.

1) Switch states of S_{a1} and S'_{a1}, S_{a2} and S'_{a2}, S_{a3} and S'_{a3}, and S_{a4} and S'_{a4} are complementary, respectively.
2) Switch states S_{a3} and S_{a4} are same.

Assuming FCVs and DCVs are stable at $u_d/4$ and $u_d/2$, 8 switch states with their abbreviation of SS_{a1}-SS_{a8} generate five voltage levels including "$u_d/2$," "$u_d/4$," "0," "-$u_d/4$," and "-$u_d/2$," and the corresponding u_{ao}, i_{fa}, and i_o are given in Table I.

The same rules are also suitable for phase-b and phase-c. Thus, ANPC 3P-5L converter has 512 switch states, which generates 125 voltage vectors in $\alpha\beta$ coordinate frame in Fig. 2.

In Fig. 1, ac-side inductor equations are expressed as

$$R_s i_{sx} + L_s di_{sx}/dt = -u_{xo} + e_{sx} - u_{\mathrm{on}} (x = a, b, c). \quad (1)$$

To easily represent converter output voltages under different switch states, switching function s_x ($x = a,b,c$) is defined as

$$s_x = \begin{cases} 2 & SS_{a1} & & u_{xo} = u_d/2 \\ 1 & SS_{a2} & \text{or } SS_{a3} & u_{xo} = u_d/4 \\ 0 & SS_{a4} & \text{or } SS_{a4} & u_{xo} = 0 \\ -1 & SS_{a6} & \text{or } SS_{a7} & u_{xo} = -u_d/4 \\ -2 & SS_{a8} & & u_{xo} = -u_d/2 \end{cases} \quad (2)$$

and converter output voltages are expressed as

$$u_{xo} = u_d s_x/4 (x = a, b, c). \quad (3)$$

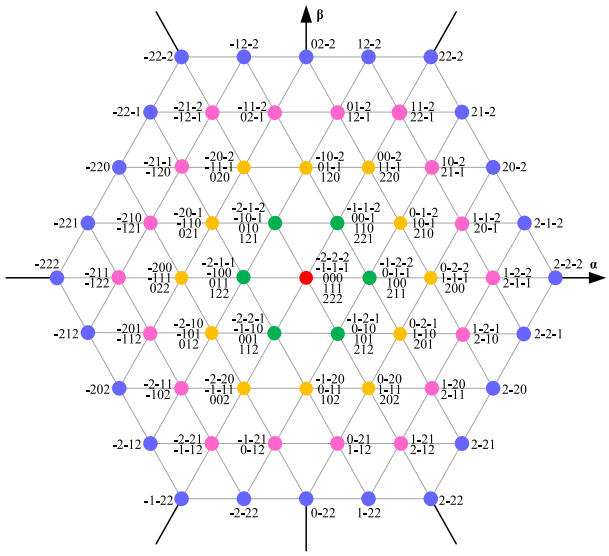

Fig. 2. Total voltage vectors in $\alpha\beta$ coordinate frame.

When grid currents are balanced, CMV is derived by (1) and (3) as [25]

$$u_{\text{on}} = -u_d(s_a + s_b + s_c)/12. \tag{4}$$

To reduce computational complexity, ac-side equation and output voltage of converter in coordinate frame $\alpha\beta$ are given as [26], [28]

$$\begin{cases} e_\alpha - u_\alpha = L_s di_\alpha/dt + R_s i_\alpha \\ e_\beta - u_\beta = L_s di_\beta/dt + R_s i_\beta \end{cases} \tag{5}$$

$$\begin{cases} u_\alpha = u_d(-s_c - s_b + 2s_a)/12 \\ u_\beta = \sqrt{3}u_d(-s_c + s_b)/12 \end{cases} \tag{6}$$

where i_α, i_β, u_α, u_β, e_α, and e_β are $\alpha\beta$ components of inductance currents, converter and grid voltages.

Besides, flying capacitor currents and neutral-point current are related to switch states in Table I, and expressed as [27]

$$i_{fx} = (S_{x1} - S_{x2})\, i_{sx}(x = a, b, c) \tag{7}$$

$$i_o = |S_{a2} - S_{a3}|\, i_{sa} + |S_{b2} - S_{b3}|\, i_{sb} + |S_{c2} - S_{c3}|\, i_{sc}. \tag{8}$$

Accordingly, flying capacitor equations and dc-link upper and lower capacitor equations are expressed as

$$C_{fx} du_{fx}/dt = (S_{x1} - S_{x2}) i_{sx}(x = a, b, c) \tag{9}$$

$$C_u du_u/dt - C_l du_l/dt = -\sum_{x=a,b,c} |S_{x2} - S_{x3}|\, i_{sx}. \tag{10}$$

For the traditional FCS-MPC algorithm, predictive equations and cost function are expressed as follows [27].

Predictive current and FCV equations are discretized from (5) and (9) as

$$i_y^P(k) = i_y(k+1) = i_y(k) + \frac{T_s}{L_s}\left(e_y(k) - u_y(k) - R_s i_y(k)\right)(y = \alpha, \beta) \tag{11}$$

$$u_{fx}(k+1) = u_{fx}(k) + \frac{T_s(S_{x1} - S_{x2}) i_{sx}(k)}{C_{fx}}(x = a, b, c) \tag{12}$$

where T_s is sampling period.

Assuming $C_u = C_l = C_d$, predictive DCV equations are discretized from (10) as

$$u_u(k+1) - u_l(k+1) = u_u(k) - u_l(k) - \frac{\sum_{x=a,b,c} |S_{x2} - S_{x3}|\, i_{sx}(k)}{C_d/T_s}. \tag{13}$$

Cost function is defined as (14) to track current targets and balance FCVs and DCVs

$$J = \sum_{y=\alpha,\beta} \left|i_y^R(k+1) - i_y(k+1)\right| + \lambda_d \left|u_u(k+1) - u_l(k+1)\right| + \lambda_f \sum_{x=a,b,c} \left|u_{fx}^R(k+1) - u_{fx}(k+1)\right| \tag{14}$$

where i_y^R ($y = \alpha,\beta$) are $\alpha\beta$ components of reference currents; u_{fx}^R ($x = a,b,c$) are phase-x reference FCVs; and λ_f and λ_d are weight factors of FCVs and DCVs.

Therefore, after the evaluation for total switch states by (12), (13), and (14), switch state that minimizes (14) is selected as the optimal switch state.

However, traditional FCS-MPC algorithm has some defects.

1) The optimal switch state is selected from total 512 switch states, which results in huge computational burden.
2) Only one switch state is applied per control period, which results in low control accuracy, unfixed switching frequency and dispersed current harmonics.
3) Two weight factors in cost function are determined by cumbersome trial and error, which increases design complexity.

III. Improved FCS-MPC Algorithm

To tackle the defects of traditional FCS-MPC algorithm, an improved FCS-MPC algorithm is implemented in two stages, namely voltage vector tracking stage and capacitor charging balance stage. First, voltage vector tracing algorithm with CMVs suppression is designed to enhance vector tracking accuracy, reduce CMVs and fix switching frequency. Second, weight factors are eliminated by capacitor charging balance algorithm, which balances FCVs and DCVs simultaneously.

A. Voltage Vector Tracking Algorithm With Reduced CMVs and Fixed Switching Frequency for Tracking Current Targets

Voltage vector tracking algorithm is implemented as follows. First, redundant voltage vectors that produce large CMVs are filtered according to their effects on CMVs. Second, according to current targets, reference voltage vector is derived, and its sector and subsector are efficiently determined by sector conversion and sector boundary conditions. Third, voltage vectors are selected according to derived sector and subsector, and their

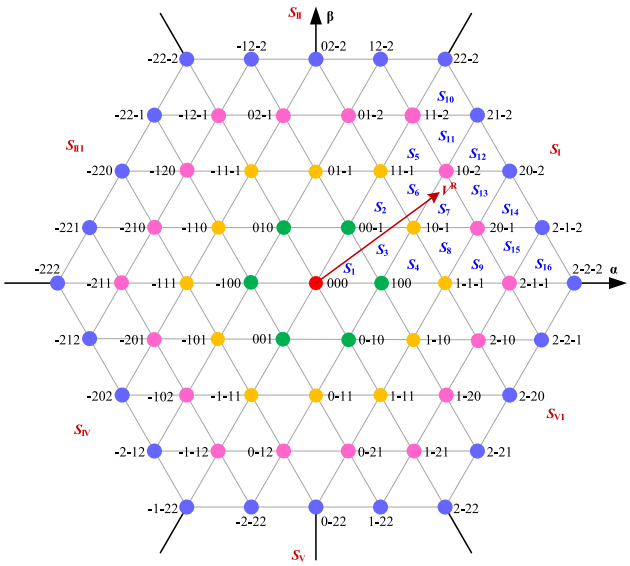

Fig. 3. Selected voltage vectors for reduced CMVs.

operation sequences are set for a fixed switching frequency; Finally, voltage vector operation time is derived by its cost function.

1) Redundant Voltage Vectors Filtration for CMVs: From (4), CMVs under total 125 voltage vectors have different fluctuation range from $-u_d/2$ to $u_d/2$. And from (11), redundant voltage vectors have same current tracking effects. Since redundant voltage vector selection and their operation time calculation are complex and time-consuming, 64 voltage vectors that generate larger fluctuations are filtrated. Thus, CMVs under the remained 61 voltage vectors in Fig. 3 have smaller fluctuations from $-u_d/6$ to $u_d/6$.

2) Reference Voltage Vectors and Sector Determination: Current tracking targets are expressed as

$$i_y^R(k+1) = i_y(k+1)(y = \alpha, \beta). \tag{15}$$

Reference voltage vector $V^R(k)$ is derived by (11) and (15) as

$$\begin{aligned} u_y^R(k) = {} & L_s(i_y(k) - i_y^R(k+1))/T_s \\ & - R_s i_y(k) + e_y(k)\,(y = \alpha, \beta) \end{aligned} \tag{16}$$

where u_y^R $(y = \alpha,\beta)$ are $\alpha\beta$ components of $V^R(k)$.

To easily select voltage vectors to track $V^R(k)$, the coordinate frame is divided into six sectors $S_{\rm I}$-$S_{\rm VI}$ in Fig. 3, and each sector is divided into 16 subsectors S_1-S_{16}. The sector of $V^R(k)$ is derived by its angle, and given as

$$\theta^R(k) = \arctan\left(u_\beta^R(k)/u_\alpha^R(k)\right). \tag{17}$$

Relationships between sector of $V^R(k)$ and $\theta^R(k)$ are given in Table II, where n is defined as sector number.

TABLE II
RELATIONSHIP BETWEEN SECTOR OF $V^R(K)$ AND $\theta^R(K)$

Value of $\theta^R(k)$	Sector of $V^R(k)$	Value of n
$[0, \pi/3]$	Sector $S_{\rm I}$	n=1
$[\pi/3, 2\pi/3]$	Sector $S_{\rm II}$	n=2
$[2\pi/3, \pi]$	Sector $S_{\rm III}$	n=3
$[\pi, 4\pi/3]$	Sector $S_{\rm IV}$	n=4
$[4\pi/3, 5\pi/3]$	Sector $S_{\rm V}$	n=5
$[5\pi/3, 2\pi]$	Sector $S_{\rm VI}$	n=6

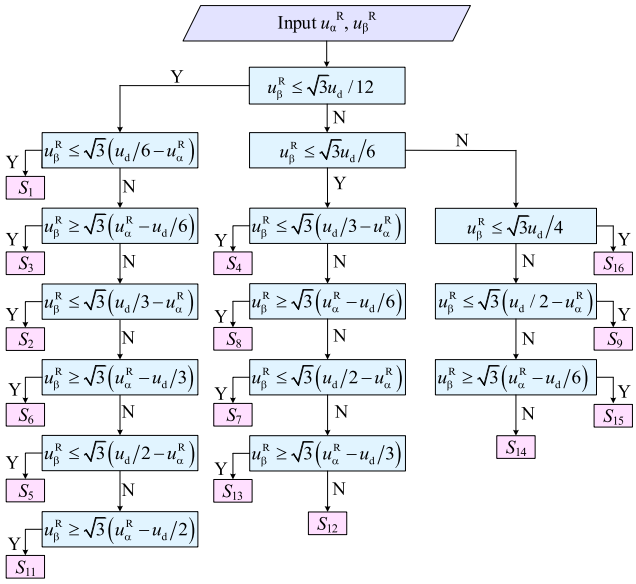

Fig. 4. Subsector derivation flowchart.

When $V^R(k)$ is in sector $S_{\rm II}$-$S_{\rm VI}$, $V^R(k)$ is converted to sector $S_{\rm I}$ uniformly. The conversion equations are given as

$$\begin{cases} u_\alpha^T(k) = \sqrt{u_\beta^R(k)^2 + u_\alpha^R(k)^2}\cos\left(\theta^R(k) - (n-1)\pi/3\right) \\ u_\beta^T(k) = \sqrt{u_\beta^R(k)^2 + u_\alpha^R(k)^2}\sin\left(\theta^R(k) - (n-1)\pi/3\right) \end{cases} \tag{18}$$

where $u_\alpha^T(k)$ and $u_\beta^T(k)$ are $\alpha\beta$ components of virtual reference voltage vector after conversion to sector $S_{\rm I}$.

The subsector of $V^R(k)$ is determined by $u_\alpha^T(k)$ and $u_\beta^T(k)$ in Fig. 4. voltage vectors for tracking $V^R(k)$ are selected by three voltage vector synthesis mode as follows.

3) Three Voltage Vector Synthesis Mode: Compared with conventional single voltage vector operation mode, three voltage vector synthesis mode is designed to improve control accuracy. Three voltage vectors are synthesized together in one control cycle to track its targets. Taking sector $S_{\rm I}$ for example, the selected voltage vectors and their operation sequence for each subsector are set in Table III according to the principle of only one phase switching function changing at same time.

Thus, each phase output voltage has a fixed switching frequency, which reduces current harmonics.

4) Voltage Vector Operation Time Calculation: Voltage vector with its operation time in subsector S_1 is marked in Fig. 5, and its operation time is determined by cost function to track its

TABLE III
VOLTAGE VECTOR OPERATION SEQUENCE IN SECTOR S_I

Subsector	Voltage vector operation sequence
Subsector S_1	00-1_000_100_000_00-1
Subsector S_2	00-1_10-1_11-1_10-1_00-1
Subsector S_3	00-1_10-1_100_10-1_00-1
Subsector S_4	1-1-1_10-1_100_10-1_1-1-1
Subsector S_5	10-2_11-2_11-1_11-2_10-2
Subsector S_6	10-2_10-1_11-1_10-1_10-2
Subsector S_7	10-2_10-1_20-1_10-1_10-2
Subsector S_8	1-1-1_10-1_20-1_10-1_1-1-1
Subsector S_9	1-1-1_2-1-1_20-1_2-1-1_1-1-1
Subsector S_{10}	11-2_21-2_22-2_21-2_11-2
Subsector S_{11}	10-2_11-2_21-2_11-2_10-2
Subsector S_{12}	10-2_20-2_21-2_20-2_10-2
Subsector S_{13}	10-2_20-2_20-1_20-2_10-2
Subsector S_{14}	2-1-2_20-2_20-1_20-2_2-1-2
Subsector S_{15}	2-1-2_2-1-1_20-1_2-1-1_2-1-2
Subsector S_{16}	2-2-2_2-1-2_2-1-1_2-1-2_2-2-2

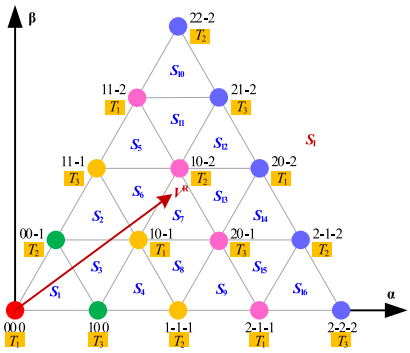

Fig. 5. Voltage vector operation time in sector S_I.

targets accurately. And cost function G is set as

$$G = \sqrt{\left(u_\alpha^R(k) - u_\alpha(k)\right)^2 + \left(u_\beta^R(k) - u_\beta(k)\right)^2}. \tag{19}$$

Assuming three voltage vectors are V_1, V_2 and V_3 with their operation times (T_1,T_2,T_3) and G values (G_1,G_2,G_3), the following equations are derived:

$$\begin{cases} T_1 : T_2 : T_3 = 1/G_1 : 1/G_2 : 1/G_3 \\ T_1 + T_2 + T_3 = T_c \end{cases} \tag{20}$$

where T_c is control period.

Accordingly, T_1, T_2, and T_3 are calculated as

$$\begin{cases} T_1 = G_2G_3T_c/(G_1G_2 + G_1G_3 + G_2G_3) \\ T_2 = G_1G_3T_c/(G_1G_2 + G_1G_3 + G_2G_3) \\ T_3 = G_1G_2T_c/(G_1G_2 + G_1G_3 + G_2G_3) \end{cases}. \tag{21}$$

Therefore, voltage vector tracking algorithm reduces CMVs by redundant voltage vector filtration, and improves vector tracking accuracy with fixed switching frequency by three voltage vector synthesis mode in Table III. Besides, due to the filtration of 64 redundant voltage vectors, reference voltage vector sector location by boundary conditions, and simple operation time calculation, this algorithm has lower computational burden compared with traditional FCS-MPC algorithm.

TABLE IV
EFFECTS ON DCVS AND FCVS UNDER REDUNDANT SWITCH STATES

Switch state	i_{fx}	i_o	$i_{sx}>0$	$i_{sx}<0$
SS_{x2}	i_{sx}	i_{sx}	$u_{fx}\uparrow u_l\uparrow u_u\downarrow$	$u_{fx}\downarrow u_l\downarrow u_u\uparrow$
SS_{x3}	$-i_{sx}$	0	$u_{fx}\downarrow u_l- u_u-$	$u_{fx}\uparrow u_l- u_u-$
SS_{x4}	0	i_{sx}	$u_{fx}- u_l\uparrow u_u\downarrow$	$u_{fx}- u_l\downarrow u_u\uparrow$
SS_{x5}	0	i_{sx}	$u_{fx}- u_l\uparrow u_u\downarrow$	$u_{fx}- u_l\downarrow u_u\uparrow$
SS_{x6}	$-i_{sx}$	i_{sx}	$u_{fx}\downarrow u_l\uparrow u_u\downarrow$	$u_{fx}\uparrow u_l\downarrow u_u\uparrow$
SS_{x7}	i_{sx}	0	$u_{fx}\uparrow u_l- u_u-$	$u_{fx}\downarrow u_l- u_u-$

B. Capacitor Charging Balance Algorithm to Eliminate Weight Factors for FCVs and DCVs Balance

Based on above operation sequence setting and operation time calculation in the voltage vector tracking algorithm, a capacitor charging balance algorithm without weight factor is designed as follows to balance FCVs and DCVs by redundant switch state selection and operation time adjustment during $s_x = 1$ and $s_x = -1$.

From Table I and (3), the effects on FCVs and DCVs are analyzed as follows under some redundant switch states (SS_{x2} or SS_{x3}, SS_{x6} or SS_{x7}) with same s_x. Taking SS_{x2} and SS_{x3} for examples, their s_x is 1 and generated voltage is $u_d/4$, while their flying capacitor currents are i_{sx} and $-i_{sx}$, and neutral-point currents are i_{sx} and 0.

FCVs increase and decrease under SS_{x2} and SS_{x3} when $i_{sx}>0$, and increase and decrease under SS_{x3} and SS_{x2} when $i_{sx}<0$, respectively. For DCVs, SS_{x2} and SS_{x6} increase lower capacitor voltage and decrease upper capacitor voltage when $i_{sx}>0$, and decrease lower capacitor voltage and increase upper capacitor voltage when $i_{sx}<0$. Besides, SS_{x3} and SS_{x7} have no effects on DCVs. The switch state effects on FCVs and DCVs are given in Table IV.

Capacitor charging balance algorithm consists of three parts: FCV balance method; DCV balance method; and switching method, which are designed as follows.

1) FCV Balance Method: Take the operation time adjustment of SS_{x2} and SS_{x3} during $s_x = 1$ for an example. Flying capacitor charge is expressed as

$$q_{fx}(k) = C_{fx}u_{fx}(k)(x = a, b, c). \tag{22}$$

Accordingly, ideal average charging currents are given as

$$i_{fx\_c}(k) = \left(C_{fx}u_{fx}^R(k) - C_{fx}u_{fx}(k)\right)/T_{x\_1} \quad (x = a, b, c) \tag{23}$$

where T_{x_1} represents the operation time of $s_x = 1$.

When $i_{fx\_c}(k)\cdot i_{sx}(k) = 0$, there exists two cases $i_{fx\_c}(k) = 0$ or $i_{sx}(k) = 0$. When $i_{fx\_c}(k) = 0$, DCVs are balanced, and operation time of SS_{x2} and SS_{x3} are set equally to avoid destroying balanced DCVs. When $i_{sx}(k) = 0$, SS_{x2} and SS_{x3} are unable to change DCVs, and operation time (T_{ssx2} and T_{ssx3}) of SS_{x2} and SS_{x3} are also set equally to reduce computational complexity.

TABLE V
REDUNDANT SWITCH STATE OPERATION TIME FOR FCV BALANCE

Select condition	Switch state and operation time
$i_{fx\_c}(k)i_{sx}(k)=0$	$\begin{cases}T_{ssx2}=T_{x\_1}/2\\T_{ssx3}=T_{x\_1}/2\end{cases}$ or $\begin{cases}T_{ssx7}=T_{x\_-1}/2\\T_{ssx6}=T_{x\_-1}/2\end{cases}$
$\begin{cases}0\le T_{ssx2}\le T_{x\_1}\\0\le T_{ssx3}\le T_{x\_1}\end{cases}$ and $i_{fx\_c}(k)i_{sx}(k)\neq 0$	$\begin{cases}T_{ssx2}=(T_{x\_1}+i_{fx\_c}(k)T_{x\_1}/i_{sx}(k))/2\\T_{ssx3}=(T_{x\_1}-i_{fx\_c}(k)T_{x\_1}/i_{sx}(k))/2\end{cases}$
$\begin{cases}0\le T_{ssx7}\le T_{x\_-1}\\0\le T_{ssx6}\le T_{x\_-1}\end{cases}$ and $i_{fx\_c}(k)i_{sx}(k)\neq 0$	$\begin{cases}T_{ssx7}=(T_{x\_-1}+i_{fx\_c}(k)T_{x\_-1}/i_{sx}(k))/2\\T_{ssx6}=(T_{x\_-1}-i_{fx\_c}(k)T_{x\_-1}/i_{sx}(k))/2\end{cases}$
$\begin{cases}T_{ssx2}<0 \text{ or } T_{ssx2}>T_{x\_1}\\T_{ssx3}<0 \text{ or } T_{ssx3}>T_{x\_1}\end{cases}$ and $i_{fx\_c}(k)i_{sx}(k)\neq 0$	$\begin{cases}T_{ssx2}=T_{x\_1}\\T_{ssx3}=0\end{cases}$
$\begin{cases}T_{ssx7}<0 \text{ or } T_{ssx7}>T_{x\_-1}\\T_{ssx6}<0 \text{ or } T_{ssx6}>T_{x\_-1}\end{cases}$ and $i_{fx\_c}(k)i_{sx}(k)\neq 0$	$\begin{cases}T_{ssx7}=T_{x\_-1}\\T_{ssx6}=0\end{cases}$

Thus, their operation times are set as

$$\begin{cases}T_{ssx2}=T_{x\_1}/2\\T_{ssx3}=T_{x\_1}/2\end{cases}(x=a,b,c). \tag{24}$$

When $i_{fx\_c}(k)\cdot i_{sx}(k)>0$, compared with SS_{x3}, SS_{x2} contributes to reducing FCV deviations, and T_{ssx2} and T_{ssx3} satisfy

$$\begin{cases}i_{fx\_c}(k)T_{x\_1}=i_{sx}(k)\,(T_{ssx2}-T_{ssx3})\\T_{ssx2}+T_{ssx3}=T_{x\_1}\end{cases}(x=a,b,c). \tag{25}$$

When $i_{fx\_c}(k)\cdot i_{sx}(k)<0$, compared with SS_{x2}, SS_{x3} contributes to reducing FCV deviations, and T_{ssx2} and T_{ssx3} satisfy

$$\begin{cases}i_{fx\_c}(k)T_{x\_1}=-i_{sx}(k)\,(T_{\mathrm{ssx3}}-T_{\mathrm{ssx2}})\\T_{ssx2}+T_{ssx3}=T_{x\_1}\end{cases}(x=a,b,c). \tag{26}$$

Thus, when $i_{fx\_c}(k)\cdot i_{sx}(k)\neq 0$, T_{ssx2} and T_{ssx3} are uniformly calculated from (25) and (26) as

$$\begin{cases}T_{ssx2}=(T_{x\_1}+i_{fx\_c}(k)T_{x\_1}/i_{sx}(k))/2\\T_{ssx3}=(T_{x\_1}-i_{fx\_c}(k)T_{x\_1}/i_{sx}(k))/2\end{cases}(x=a,b,c). \tag{27}$$

Besides, T_{ssx2} and T_{ssx3} might exceed the effective range of [0, $T_{\mathrm{x\_1}}$], which indicates that their operation times are not sufficient to fully balance FCVs during $s_x=1$. At this time, to reduce FCV deviations as much as possible, under two cases $i_{fx\_c}(k)\cdot i_{sx}(k)>0$ and $i_{fx\_c}(k)\cdot i_{sx}(k)<0$, T_{ssx2} and T_{ssx3} are set as

$$\begin{cases}T_{ssx2}=T_{x\_1}\\T_{ssx3}=0\end{cases}i_{fx\_c}(k)\cdot i_{sx}(k)>0(x=a,b,c) \tag{28}$$

$$\begin{cases}T_{ssx2}=0\\T_{ssx3}=T_{x\_1}\end{cases}i_{fx\_c}(k)\cdot i_{sx}(k)<0(x=a,b,c). \tag{29}$$

Similarly, the selection of redundant switch state (SS_{x6} or SS_{x7}) with their operation time adjustments are given in Table V.

2) DCV Balance Method: DCVs are inevitably affected by neutral-point currents ($i_{sx}\neq 0$) under SS_{x4} and SS_{x5} in Table IV. When $i_{sx}>0$, SS_{x4} and SS_{x5} increase lower capacitor voltage and decrease upper capacitor voltage. When $i_{sx}<0$, SS_{x4} and SS_{x5} decrease lower capacitor voltage and increase upper capacitor voltage.

TABLE VI
REDUNDANT SWITCH STATE SELECTION FOR DCVS BALANCE

Select condition	Switch state
$\Delta q_c(k)+\Delta q(k)=0$	SS_{x3} or SS_{x7}
$i_x(\Delta q_c(k)+\Delta q(k))<0$	SS_{x2} or SS_{x6}
$i_x(\Delta q_c(k)+\Delta q(k))>0$	SS_{x3} or SS_{x7}

Reasonable selection of redundant switch states (SS_{x2} or SS_{x3}, SS_{x6} or SS_{x7}) is conducive to balance DCVs during $s_x=1$ and $s_x=-1$. Two factors of initial capacitor charges and charging effects under SS_{x4} and SS_{x5} should be considered. The selection of switch states (SS_{x2} or SS_{x3}) is implemented to balance DCVs during $s_x=1$ as follows.

The initial capacitance charge deviation is expressed as

$$\Delta q_c(k)=C_l u_l(k)-C_u u_u(k). \tag{30}$$

The effects under SS_{x4} and SS_{x5} for upper and lower capacitors charge deviation during $s_x=0$ are expressed as

$$\Delta q(k)=\sum_{x=a,b,c}T_{x\_0}i_{sx}(k). \tag{31}$$

When $\Delta q_c(k)+\Delta q(k)=0$, DCVs have been balanced, and SS_{x3} is selected and does not affect DCVs.

When $i_x(\Delta q_c(k)+\Delta q(k))<0$, SS_{x2} is selected for its generated neutral-point current (i_x) contributes to balancing DCVs.

When $i_x(\Delta q_c(k)+\Delta q(k))>0$, SS_{x3} is selected for its generated neutral-point current (0) does not effect DCVs.

The same analysis is also suitable for SS_{x6} or SS_{x7}, and redundant switch state selection for DCVs balance are given in Table VI.

3) Switching Method: DCVs are affected by three phase neutral-point currents, while FCVs are only affected by local phase currents. So, FCV balance has higher priority than DCV balance. When FCVs maintain within a reasonable range of Δu, appropriate switching state is selected to balance DCVs. From above analysis, capacitor charging balance algorithm are shown in Fig. 6.

C. System Control Block Diagram

In Fig. 7, the improved algorithm is implemented from two progressive stages. First, the voltage vector tracking algorithm with CMVs suppression is implemented to reduce CMVs, improve vector tracking accuracy, fix switching frequency, and lower computational burden. By this algorithm, the duration time (T_{x_1}, T_{x_0} and T_{x_-1}) of $s_x=1$, $s_x=0$, and $s_x=-1$ is obtained. Second, the capacitor charging balance algorithm is implemented to balance FCVs and DCVs without weight factors by redundant switch state selection and operation time adjustment according to each phase flying capacitor charges, and upper and lower capacitor charges. By the algorithms, the redundant switch state operation times (T_{ssx2}, T_{ssx3}, T_{ssx6}, and T_{ssx7}) are obtained by (22) to (31) and Table V and VI, and the corresponding 24-channel switching signals are produced for converter system.

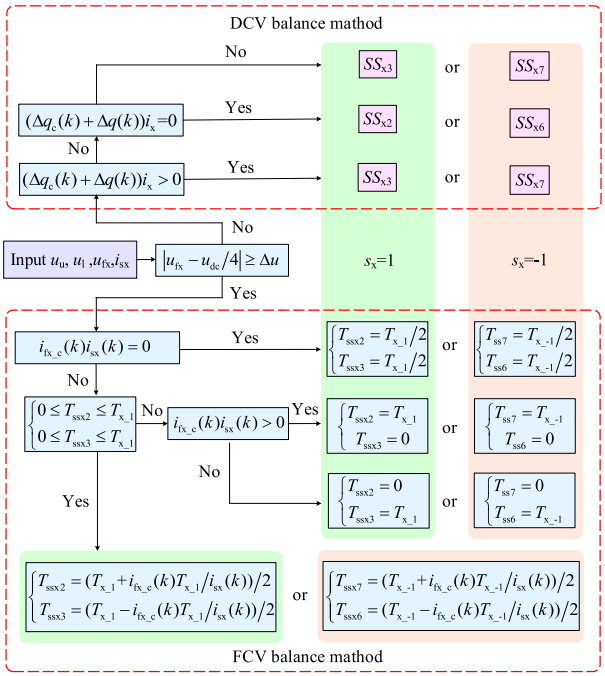

Fig. 6. Capacitor charging balance algorithm flowchart.

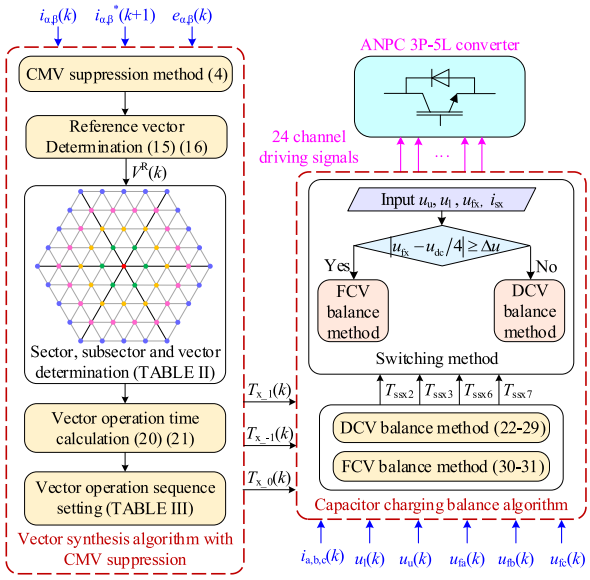

Fig. 7. System control block diagram.

IV. System Experiment

An experimental system of 3P-5L-ANPC converter based on dSPACE is carried out to verify the improved algorithm in Fig. 8. The primary circuit of experimental platform includes transformers, inductors, converters, flying capacitors, dc capacitors and driving circuit. The secondary circuit includes signal acquisition circuit, and signal processing circuit. The output signals from dSPACE are transmitted to the driving circuit through optical fibers. The system parameters and control parameters are given in Table VII.

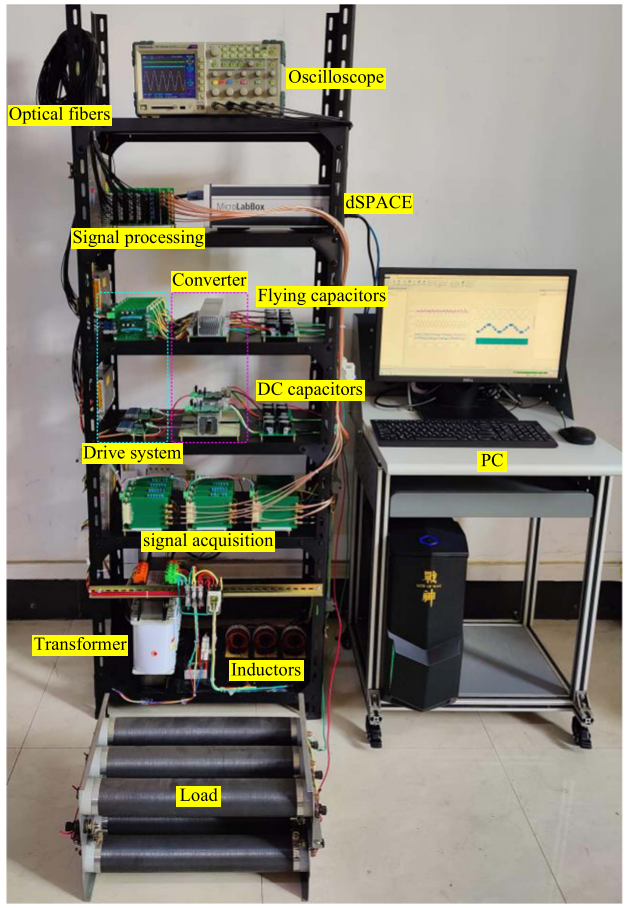

Fig. 8. Experimental 3P-5L-ANPC system.

TABLE VII
System Parameters and Control Parameters

Parameter	Description	Value
f	Grid voltage frequency	50 Hz
e_x	Phase voltage amplitude	311 V
k_T	Transformer ratio	380/110
R_s	Inductor internal resistance	0.1 Ω
L_s	Inductor inductance	8 mH
R_L	DC load resistance	100 Ω
$C_{fx(x=a,b,c)}$	Phase (a, b, c) flying capacitor	2240 μF
P_N	System rated power	3 kW
i_q^*	Reactive current reference	0
U_{dc}^*	DC voltage reference	250 V
T_c	Control period	100 μs
T_s	Sampling period	50 μs

A. System Steady Performance Evaluation

When R_L is 50 Ω, system steady performance and FFTs under proposed and conventional FCS-MPC algorithm are shown in Figs. 9–14 respectively.

In Figs. 9–11, u_{dc} stabilizes at 250 V with its error about 0.21 V; DCVs are about 0.3 V according to the difference of u_u and u_l; FCVs (u_{fa}, u_{fb}, and u_{fc}) is stable at 62.5 V with their maximum fluctuation of 0.2 V; the maximum error of i_a, i_b, and

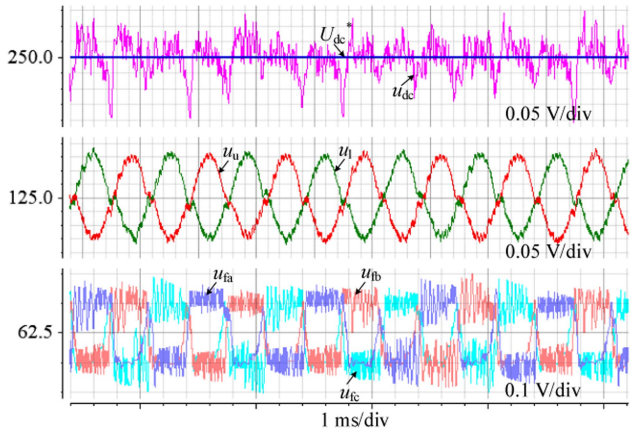

Fig. 9. Steady curves (u_u, u_l, u_{dc}, u_{fa}, u_{fb}, u_{fc}) under proposed FCS-MPC.

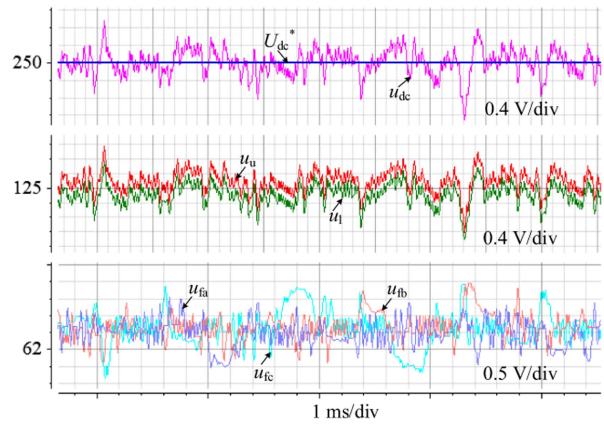

Fig. 12. Steady curves (u_u, u_l, u_{dc}, u_{fa}, u_{fb}, u_{fc}) under conventional FCS-MPC.

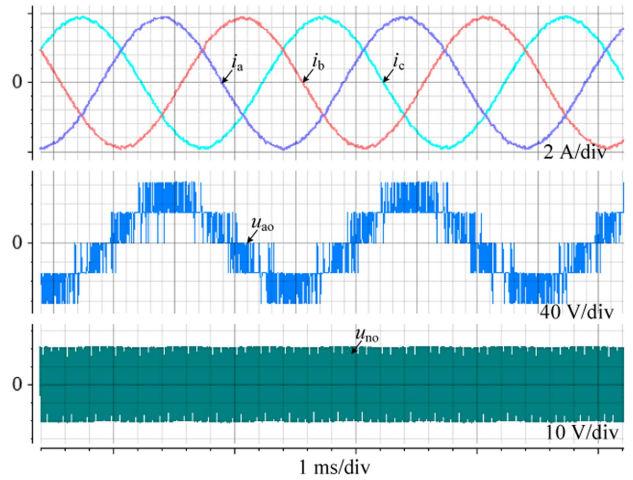

Fig. 10. Steady curves (i_c, i_b, i_a, u_{ao}, u_{no}) under proposed FCS-MPC.

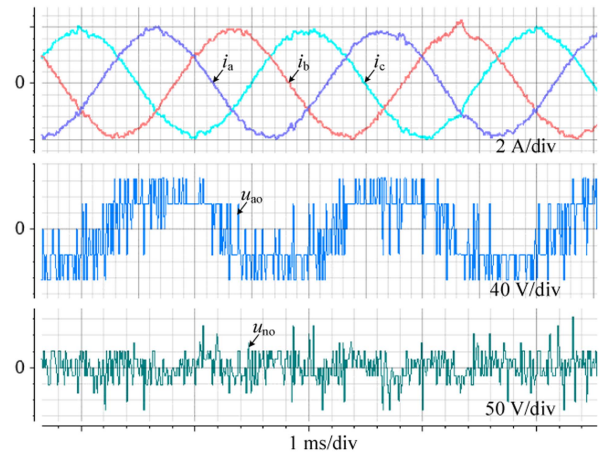

Fig. 13. Steady curves (i_c, i_b, i_a, u_{ao}, u_{no}) under conventional FCS-MPC.

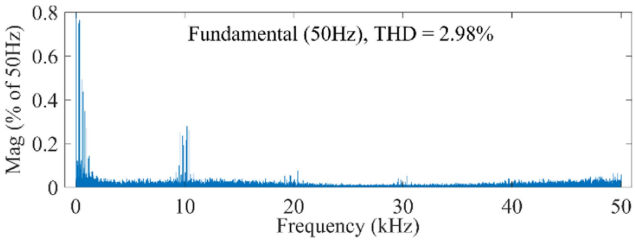

Fig. 11. System steady current FFT result under proposed FCS-MPC.

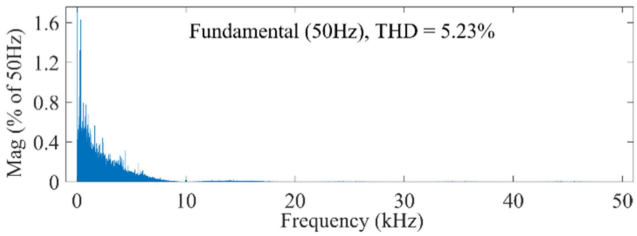

Fig. 14. System steady current FFT result under conventional FCS-MPC.

i_c are about 0.6 A; u_{ao} has five voltage output levels, which verifies five voltage output mode; the maximum value of CMVs (u_{no}) is about 22 V; current THD is about 2.98%.

Correspondingly, in Figs. 12–14, u_{dc} stabilizes at 250 V with its error about 1.2 V; DCVs are about 0.5 V according to the difference of u_u and u_l; FCVs (u_{fa}, u_{fb}, and u_{fc}) is stable at 62.5 V with their maximum fluctuation of 1.4V; the maximum error of i_a, i_b, and i_c are about 2 A; the maximum value of CMVs (u_{no}) is about 150 V; current THD is about 5.23%.

Compared with conventional FCS-MPC, the errors of dc-link voltage, DCVs, FCVs and current are reduced by 0.99 V, 0.2 V, 1.2 V and 1.4 A, respectively; CMVs and current THDs are reduced by 128 V and 2.25%, respectively. Therefore, the system has better steady performance under proposed FCS-MPC due to three voltage vector synthesis mode and capacitor charging balance algorithm.

B. System Transient Performance Evaluation

When R_L increases from 50 to 100 Ω, system transient performance under proposed and conventional FCS-MPC algorithms are shown in Figs. 15–18, respectively.

In Figs. 15 and 16, u_{dc} recovers to 250 V within 80 ms with its maximum deflection of 1.7 V; the maximum deflection of u_l, u_u

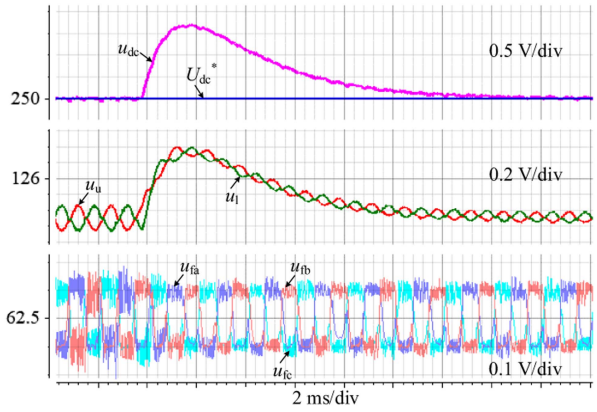

Fig. 15. Transient curves (u_u, u_l, u_{dc}, u_{fa}, u_{fb}, u_{fc}) under proposed FCS-MPC.

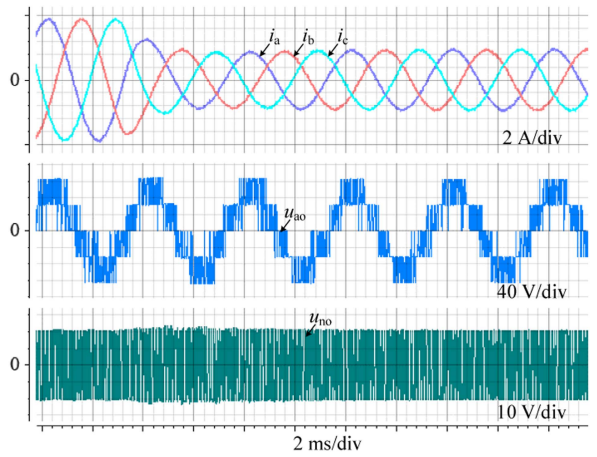

Fig. 16. Transient curves (i_c, i_b, i_a, u_{ao}, u_{no}) under proposed FCS-MPC.

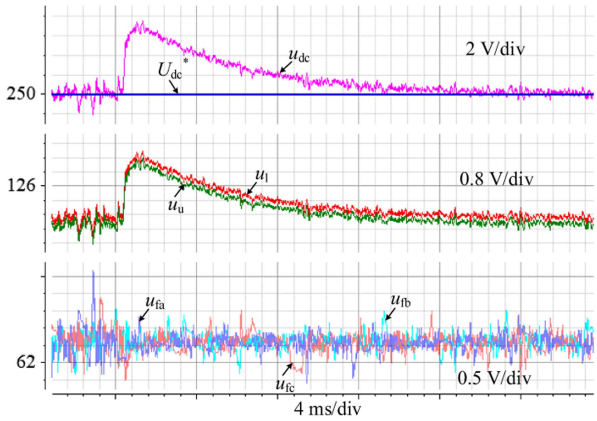

Fig. 17. Transient curves (u_u, u_l, u_{dc}, u_{fa}, u_{fb}, u_{fc}) under conventional FCS-MPC.

is 0.85 V; the maximum fluctuation of u_{fa}, u_{fb}, and u_{fc} decreases from 0.18 V to 0.12 V; i_c, i_b, and i_a track the targets smoothly.

Corresponding, in Figs. 17 and 18, $u_{\rm dc}$ recovers to 250 V within 100 ms with its maximum deflection of 6.4 V; the maximum deflection of u_u and u_l is 3.2 V; the maximum fluctuation of u_{fa}, u_{fb}, and u_{fc} decreases from about 2 V to 1.2 V; i_c, i_b, and i_a track their targets with fluctuation of 0.8 A.

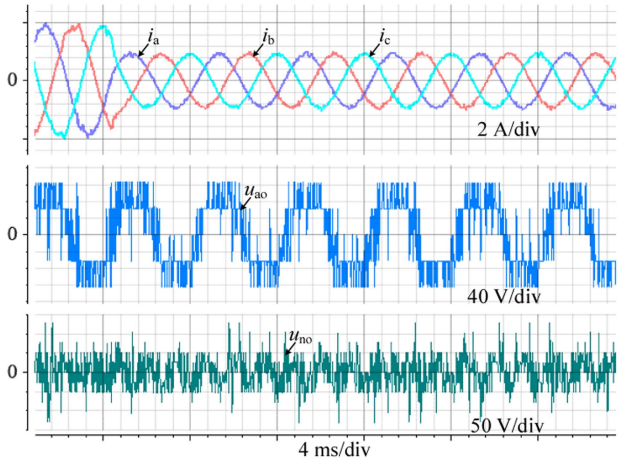

Fig. 18. Transient curves (i_c, i_b, i_a, u_{ao}, u_{no}) under conventional FCS-MPC.

TABLE VIII
CODE EXECUTION TIME OF TWO FCS-MPC ALGORITHMS

Algorithm	Code execution time
Proposed FCS-MPC	40.5 μs
Conventional FCS-MPC	192 μs

Compared with conventional FCS-MPC, the recovery time of $u_{\rm dc}$ is reduced by 20 ms; the maximum deflection is reduced by 4.7 V; i_c, i_b, and i_a track the targets smoother. Therefore, the proposed FCS-MPC makes system have better transient performance due to three voltage vector synthesis mode and capacitor charging balance algorithm.

C. Algorithm Computational Burden Evaluation

Computational burden of proposed and conventional FCS-MPC algorithms could be evaluated by code execution time of TMS320F28335 [21], [22], [30], [31], and their execution times are 40.5 and 192 μs in Table VIII. So, the proposed FCS-MPC has smaller execution time with decreases by about 151.5 μs due to the filtration of 64 redundant voltage vectors, reference voltage vector sector location by boundary conditions, and simple operation time calculation.

VI. CONCLUSION

According to above experiment results, we could draw the following conclusions.

1) The proposed voltage vector tracking algorithm selects the optimal voltage vector directly, which reduces the system computational burden by 151.5 μs due to the filtration of 64 redundant voltage vectors, reference voltage vector sector location by boundary conditions, and simple operation time calculation compared with conventional vector traversal algorithm.
2) The proposed vector synthesis algorithm reduces system current steady error by 1.4 A according to three voltage vector synthesis mode, lowers CMVs by 128 V according to selecting small CMVs vectors, and fixes switching

frequency by operation sequence setting compared with conventional single vector output mode.

3) The proposed capacitor charging balance algorithm reduces system steady errors of DCVs and FCVs by 0.2 and 1.2 V, respectively, and lowers system transient voltage recovery time by 20 ms according to redundant switch state selection and their operation time adjustment compared with conventional FCS-MPC.

VII. Discussion

The improved FCS-MPC algorithm is manly to reduce CMV, improve system control accuracy, fix switching frequency, remove weighted factors and lower computational burden without consideration of dead-time effects and switching loss. The study of dead-time effects and switching loss are necessary and important in high power and low switching frequency converter system. Therefore, the improved FCS-MPC algorithm for dead-time effects and switching loss would be carried out in the future.

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