A Low-Complexity Pure-MOS Sliding-Frequency Semi-Digital Buck DC-DC Converter Based on a Triple-Comparator Structure

Bo Zhou, Xinyuan Han, Yifan Li, Zhaoyuan Wang, Ling Fu, Zhihua Wang, *Fellow, IEEE*, and Huikai Xie, *Fellow, IEEE*

***Abstract*—Based on a triple comparator and several digital modules, a semidigital buck dc–dc converter is proposed and fabricated in 65-nm CMOS, for SoC power management. The switching frequency is automatically sliding from dozen kHz to sub-MHz for different load conditions. Experimental results show that the presented dc–dc converter has a high efficiency up to 93%, with an active area less than 0.03 mm^2, and achieves a peak-to-peak ripple voltage smaller than 3.92 mV and a load-step over/under-shoot voltage lower than 10 mV and the switching frequency of 20–578 kHz, with the supply voltage of 1.8–3.3 V and load current of 1–50 mA. The proposed dc–dc converter with the output voltage covering 1.2–1.8 V also accomplishes a linear regulation less than 0.167% and a load regulation lower than 0.208%. This converter has advantages of small area and low complexity due to semidigital structure, high efficiency and low ripple with a sliding-frequency scheme, and pure-MOS design without on-chip passive devices. The proposed triple-comparator structure based on two groups of offset voltages, benefits the digital implementations of buck dc–dc converters.**

***Index Terms*—Buck, dc–dc converter, high efficiency, low complexity, low ripple, pure-MOS, semidigital, sliding-frequency, triple-comparator.**

I. Introduction

With rapid development of information technology, dc–dc converters are widely used in portable and wearable electronic devices such as mobile phones, earbuds, smart bracelets, laptops and tablets, and also used in power management for SoC. Buck dc–dc converter has a wide load range, where the conduction and switching losses dominate at heavy and light loads, respectively, which inversely requires a varying switching frequency for high conversion efficiency [1]. To aim at low-complexity and high-efficiency application scenarios, buck dc–dc converters need to employ digital modulation schemes and dynamic switching frequency techniques, and eliminate large-size on-chip passive devices (resistors / capacitors / diodes).

The existing converters [2], [3] based on the conventional pulse-width modulation (PWM) technique with active ramp tracking or current-mode controls, have a high efficiency in heavy loads while encounter a low efficiency under light ones. The reported prototypes [4], [5], [6], [7] based on the traditional pulse-frequency modulation (PFM) scheme with voltage-mode ripple-based control or constant-on-time inductor-current based regulation, improve the efficiency in light loads, while the switching frequency depends on the load current that degrades the robustness. The existing works optimize the PFM switching-frequency stabilization by introducing the adaptive-on-time [8], [9], [10] or frequency locking [11], [12], [13] skills (for example, current-sensing hysteretic window), but degrade the converter design complexity. In addition, the PFM has no efficiency and ripple advantages in heavy loads, when compared to the PWM. Therefore, the mainstream buck converters utilize multi-mode schemes with varying switching frequencies for different load conditions.

The existing dual-mode converters [14], [15], [16], [17], [18] with PWM for heavy load and PFM / double clock time (DCT) / pulse-skip modulation / advanced burst mode for light one, obtain high efficiency within full-range load. The reported triple-mode ones [19], [20], [21], [22] introduce an additional modulation type (multiple-sawtooth PWM / deep-green mode / economy mode / retention), to the PWM and PFM, achieving both ultra-low quiescent current and high efficiency over a wide load range. However, multimode schemes encounter ultra-high hardware complexity due to multiple groups of mode controllers. In addition, digital-controlled dc–dc converters are presented in [23], [24], [25], [26], [27], [28], [29], [30], [31], by utilizing a digital modulator, such as the digital PWM (DPWM) or a power-driving-tracked-duration (PDTD) scheme. Nevertheless, an analog-to-digital or digital-to-analog converter, or a delay-locked loop, is necessary in these converters, which increases

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hardware complexity and power consumption. The existing works always need an error amplifier (EA) followed by a large-size capacitor, and also require current / voltage sensors with lots of resistors to accomplish multi-mode control. Therefore, large-size passive components are inevitable in the traditional architectures.

In conclusion, the mentioned designs either use complex digital modulation structures or employ complicated multimode operation schemes for the dynamic switching frequency, and also require numerous on-chip passive components that occupy a large silicon area, which are not fit for low-cost applications such as SoC power management.

In this article, a semidigital buck dc–dc converter, based on pure-MOS devices and triple-comparator structure, is proposed. The switching frequency is automatically sliding to support high efficiency and low ripple for both heavy and light loads.

The rest of this article is organized as follows. Section II clarifies the proposed triple-comparator architecture, and Section III presents the detailed circuit implementations, followed by experimental results in Section IV. Finally, Section V concludes this article.

II. Proposed Architecture

Both the on-time of the power stage and the loop-bandwidth of the buck converter set an upper limit of the converter switching frequency, and the external filtering inductors and capacitors set a floor value of the switching frequency [32]. Under a heavy load, to avoid the conduction loss that degrades the conversion efficiency, high switching frequency is required. While for a light load, the switching loss is dominant and thus low switching frequency is needed. In this article, the switching frequency is automatically sliding from dozen kHz to sub-MHz for different load conditions.

A semidigital structure made of simple comparators and digital units, is proposed to accomplish a digital modulation scheme and dynamic switching frequency, by introducing a sleep status where the external filtering capacitor supplies the load and thus the switching frequency varies with the load current. The comparator offset voltages protect the power stage from damage and affect its conduction time that inversely decides the load current range. The presented structure with two groups of offset voltages, does not use any on-chip passive components, which is fully different from the existing literature.

Fig. 1 gives the proposed converter architecture based on a triple comparator (Tri-COMP), which consists of a control logic, a power driver, an error comparator (EC), a peak-voltage comparator (PC), a zero-voltage comparator (ZC), a power stage, and three identical delay units, followed by the external *LC* filtering and resistive-feedback networks. By using several digital units and three simplified comparators, the output signals from EC, PC, and ZC, alternately turn the push-pull power transistors M_P-M_N ON and OFF. A stable output voltage $V_{\rm OUT}$ is achieved, via a voltage negative-feedback loop with the 1-V reference voltage $V_{\rm REF}$.

Conventional EAs with a large capacitor for frequency compensation, and traditional ramp generators based on capacitor

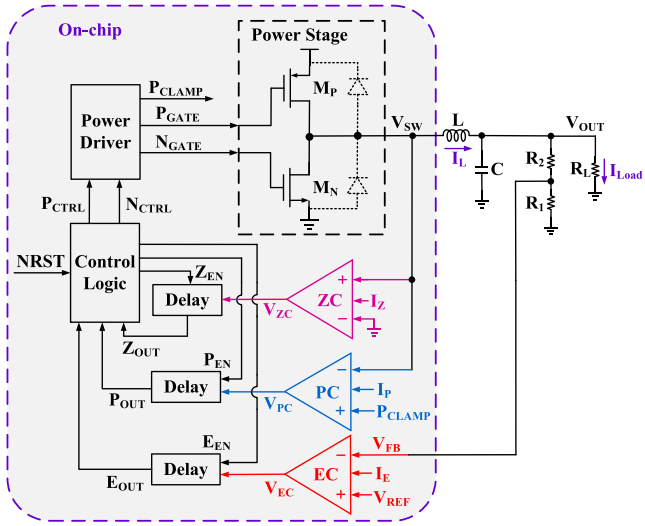


Fig. 1. Proposed architecture based on a Tri-COMP.

charging-discharging, are replaced by the EC that compares the feedback voltage $V_{\rm FB}$ with $V_{\rm REF}$, to eliminate the requirement for on-chip capacitors. The existing inductor-current / output-voltage detectors for mode swapping, are replaced by the proposed triple comparator. Both PC and ZC, used to clamp the output signal $V_{\rm SW}$ of power stage between the supply voltage $V_{\rm DD}$ and ground signal GND, employ two groups of offset voltages due to asymmetric input-pair sizes. All these make on-chip resistors absent. The Tri-COMP architecture contributes to small silicon size, low complexity, high efficiency, and semidigital design, which does not use on-chip passive components.

Fig. 2 shows the operating principles of proposed converter. The digital signals ($E_{\rm OUT}$ / $P_{\rm OUT}$ / $Z_{\rm OUT}$) are set to GND or the comparator outputs (V_{EC} / V_{PC} / V_{ZC}), that is, the comparators (EC / PC / ZC) are enabled or disabled, under the control of the high-level non-overlapping signals (E_{EN} / P_{EN} / Z_{EN}), respectively. This inversely decides the signals $\rm P_{CTRL}$ / $\rm N_{CTRL}$ and thus gets $P_{\rm GATE}$ / $N_{\rm GATE}$ / $P_{\rm CLAMP}$. As a result, M_P and M_N are ON or OFF sequentially and affected by E_{EN}/P_{EN}/Z_{EN}, where $P_{EN} = 1$ is for M_P on and M_N OFF, $Z_{EN} = 1$ makes M_N ON and M_P OFF, and $E_{EN} = 1$ disables M_P / M_N to get the sleep zone.

The converter transient behavior is divided into two states: rising and steady ones. The former operates in continuous conduction mode, and M_P-M_N turn ON or OFF alternately with a fixed time slot, where the inductor current $I_L \geq 0$ and $V_{\rm OUT}$ continuously increases and $V_{\rm FB}$ approaches $\rm V_{REF}$. The latter works in discontinuous conduction mode, and each ripple period t_R includes the inductor L charging time t_L (the sum of M_P on slot and M_N on period) and the sleep-zone time t_S, according to three comparator outputs. During t_L period, M_P-M_N turn ON or OFF sequentially with a fixed time slot, and I_L charges the capacitor C and the load R_L. Within t_S period, M_P-M_N are OFF and I_L is damped to zero, and C is discharged to provide the load current, $I_{\rm Load}$. The sleep-zone time is decided by $I_{\rm Load}$ and thus the steady-state switching frequency, $f_{\rm SW}$, varies with the load condition. The output ripple voltage, $V_{\rm ripple}$, is also affected

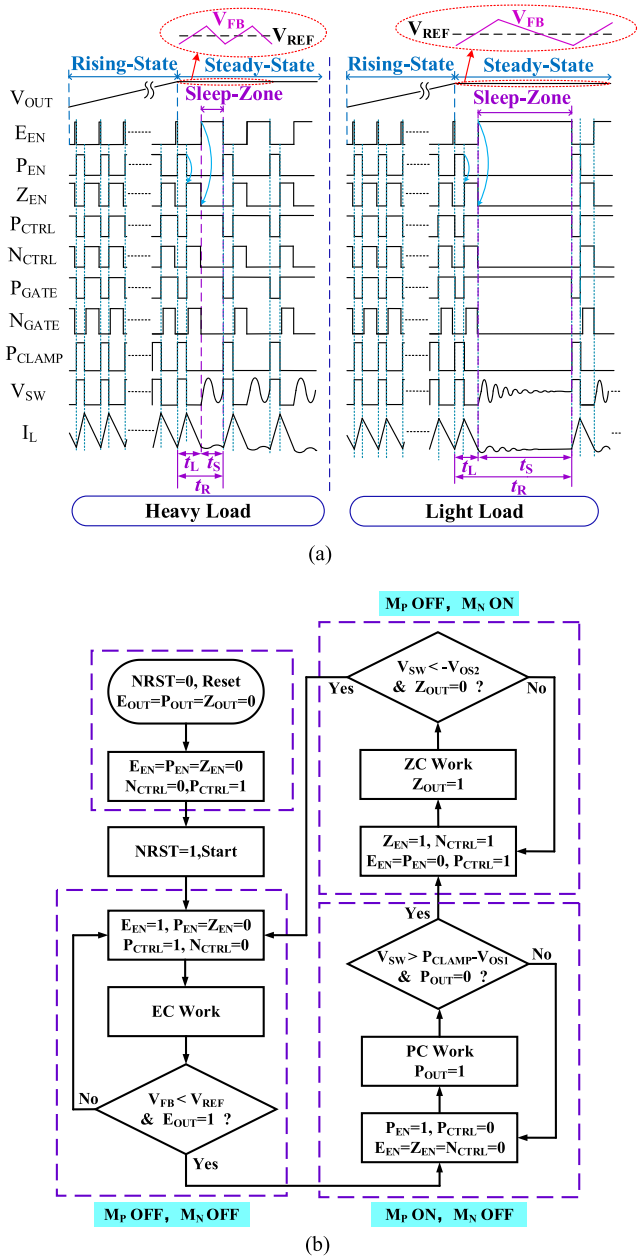


Fig. 2. Operating principles of the proposed converter. (a) Timing sequence. (b) State diagram.

by the I_L ring duration, T_{ring}, which is related to I_{Load}. The relationship between the switching frequency, ripple voltage, and load current, is given in (1) and (2). Therefore, the ripple voltage increases and the switching frequency decreases, as I_{Load} goes down, vice versa.

$$f_{\mathbf{SW}} = \frac{1}{t_{\mathbf{R}}} = \frac{1}{t_{\mathbf{L}} + t_{\mathbf{S}}}, t_{\mathbf{S}} \alpha \frac{1}{I_{\mathbf{Load}}} \tag{1}$$

$$V_{\mathbf{ripple}} = \frac{1}{\mathbf{C}} \int_0^{T_{ring}} I_{\mathbf{L}} dt \alpha \int_0^{1/I_{\mathbf{Load}}} I_{\mathbf{L}} dt. \tag{2}$$

The power stage of the converter has three alternate work statuses: sleeping, charging, and discharging, where M_P-M_N are ON /OFF, controlled by the control logic and thus decided by these three comparators, according to the V_{SW} clamping condition and the comparison result between V_{FB} and V_{REF}. During the rising and steady states of the converter, the power stage always alternately works in these three statuses, where the sleep-zone duration is small / medium / large for the rising / heavy-load steady / light-load steady states, respectively. While charging and discharging statuses have the fixed durations, which are not affected by I_{Load}. Each ripple period is composed of M_P on time (triggered by EC and ended by PC), M_N on slot (triggered by PC and ended by ZC), and sleeping zone (triggered by ZC and ended by EC). That is, the frequency-sliding scheme is conducted by all the digital modules and three comparators. A low-level-effective reset signal (NRST) is introduced to set the initial values of the control signals, which inversely triggers the buck converter.

According to the operating principles shown in Fig. 2, the three comparators work alternately. That is, when EC is activated, PC and ZC are disabled, vice versa. Moreover, EC with the input voltage, compared to 1-V V_{REF}, has a similar amplifier structure, as PC with a comparison voltage of P_{CLAMP} ($= V_{\text{DD}}$ with PC enabled or GND with PC disabled). All these make it feasible that EC and PC are highly reused and employ the same two-stage cascaded structure with an NMOS input-pair, to save one comparator and one delay unit. That is, the triple comparator is further simplified to a double one, which will be considered as a future work to lower quiescent current.

III. Circuit Implementation

Regardless of external resistive-feedback and *LC* filtering networks, the proposed converter consists of a power stage, a triple comparator, and three digital modules, which is indeed regarded as an ultra-low-cost digital implementation.

A. Comparators

Fig. 3 gives the proposed PC / ZC / EC comparators, based on two-stage cascaded structure of a fold-cascode amplifier followed by a common-source one, to reduce comparator propagation delay. Both PC and ZC have input offset voltages of V_{OS1} and V_{OS2}, respectively, while EC never does.

Both EC and PC employ NMOS input pairs with different transistor size ratios between M_1 and M_2, to achieve the input offset voltages close to 0 and of V_{OS1}, respectively. The input-pair (M_1 and M_2) having a size ratio k_1 of 10:2 for V_{OS1} with a typical value of 70 mV, is introduced in the PC to avoid the reverse conduction current of M_P parasitic body diode into V_{DD}. The ZC uses an asymmetric PMOS input pair with a size ratio k_2 of 10:8 to generate V_{OS2} with a typical value of 15 mV, which prevents the reverse conduction current of M_N parasitic body diode from GND.

V_{OS1} and V_{OS2} are optimized to make a tradeoff between the output voltage ripple and I_{Load} range, by setting a perfect M_P-M_N conduction time, since $V_{\text{SW}}+V_{\text{OS1}}$ is compared to P_{CLAMP} ($= V_{\text{DD}}$ with PC enabled or GND with PC disabled), and $V_{\text{SW}} + V_{\text{OS2}}$ is compared to GND, via the PC and ZC to turn ON/OFF M_P and M_N, respectively. On one hand, when V_{OS1} is small, V_{SW} approximates V_{DD} and the M_P conduction (charging) time is

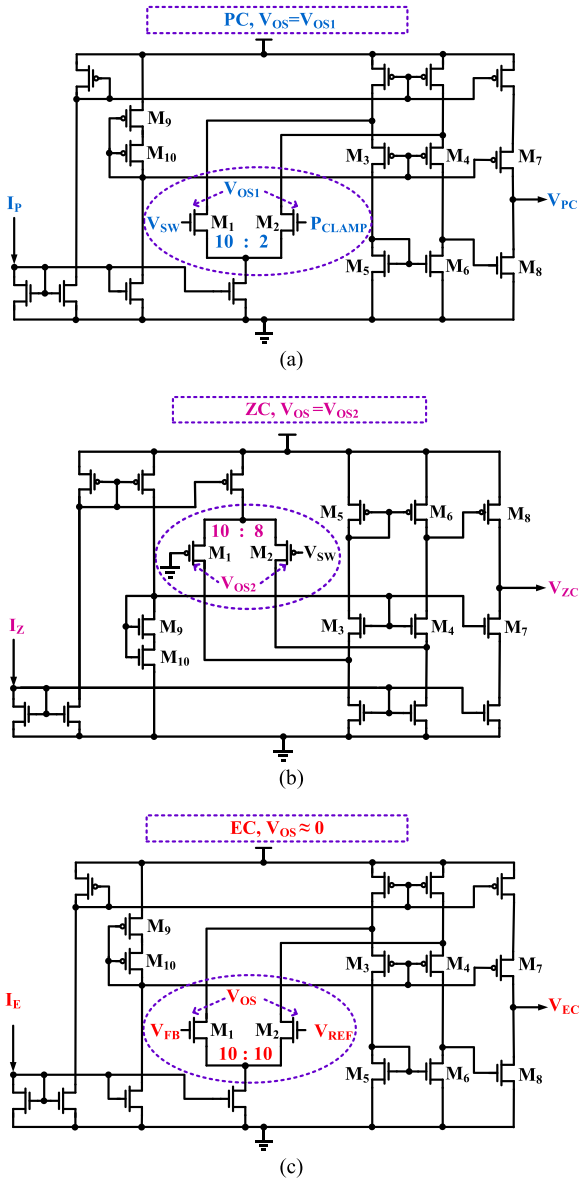


Fig. 3. Proposed comparator circuits. (a) Peak-voltage comparator. (b) Zero-voltage comparator. (c) Error comparator.

long, which inversely improves I_{Load} upper limit but degrades the output ripple. When V_{OS1} is too large, V_{SW} is far below V_{DD}, causing the converter to malfunction in heavy loads. On the other hand, when V_{OS2} is large, V_{SW} goes away from GND and the $\mathrm{M_N}$ conduction (discharging) time is long, which inversely degrades the output ripple. In this article, low V_{OS2} (15 mV) and medium V_{OS1} (70 mV) values are chosen, to aim at 50-mA load range and mV-level ripple voltage. Lower V_{OS1} (<70 mV) and lower V_{OS2} (<15 mV) will be considered as a future work to aim at a larger I_{Load} range with slight ripple degradation.

B. Digital Modules

Fig. 4 shows the proposed digital circuits of control logic, power driver, and delay unit. As depicted in Fig. 4(a), the control logic made of basic logic gates and four delay cells, generates

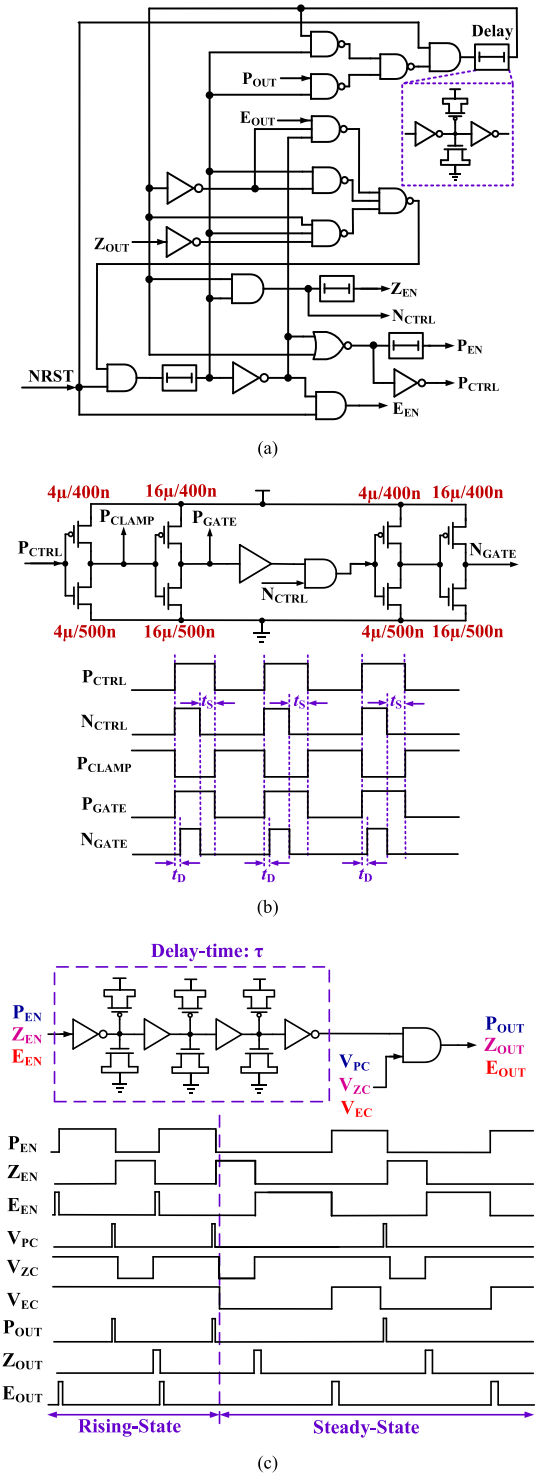


Fig. 4. Digital modules. (a) Control. (b) Driver. (c) Delay unit.

five paths of control signals in accordance with Fig. 2 to regulate the converter. The delay cells made of complementary MOS capacitors and two inverters, are for the high-level nonoverlapping generation of E_{EN} / P_{EN} / Z_{EN} signals and also for the sleep zone t_{S} of N_{CTRL} / P_{CTRL} signals.

The power driver employs the inverter / buffer chain with transistor-size scale-up by four, to generate the driving signals

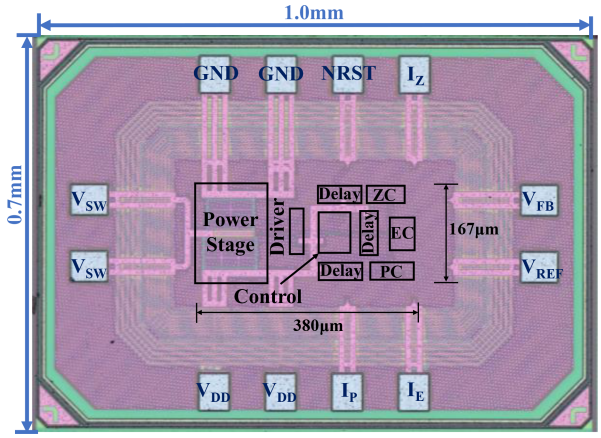


Fig. 5. Chip micrograph in 65-nm CMOS process.

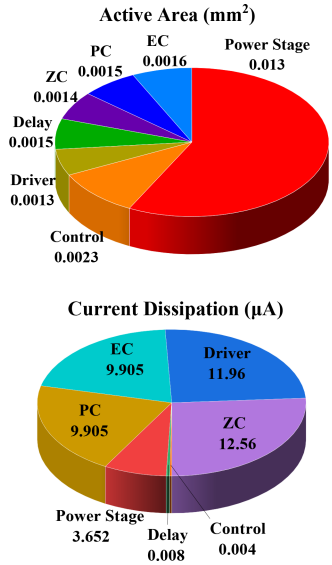


Fig. 6. Measured converter breakdowns in active area and current dissipation.

P_{GATE} and N_{GATE} for the large-size transistors M_P-M_N, and get the clamping signal P_{CLAMP} for the PC. As given in Fig. 4(b), the embedded digital buffer and AND gate form the dead-zone time t_D of 6 ns, together with the sleep-zone time t_S generated by the control logic, to avoid synchronous conduction between M_P and M_N. In this article, P_{CLAMP} is fixed to V_{DD} when PC is activated ($P_{\mathrm{CTRL}} = 0$), and is then switched to GND when PC is disabled ($P_{\mathrm{CTRL}} = 1$). That is the reason why P_{CLAMP} is the inverse of P_{CTRL} rather than fixed to V_{DD}.

Identical delay modules inserted between the comparators and control logic, play a role as comparator enable triggers, and utilize three pairs of complementary MOS capacitors as delay components. As shown in Fig. 4(c), the delay component with a typical value of $\tau = 90$ ns, makes the comparators work alternately and control logic sequentially respond to single-path signal related to one comparator. That is, the delay units with their signal waveforms are clearly demonstrated in Fig. 4(c), ensure three alternate work statuses shown in Fig. 2(b).

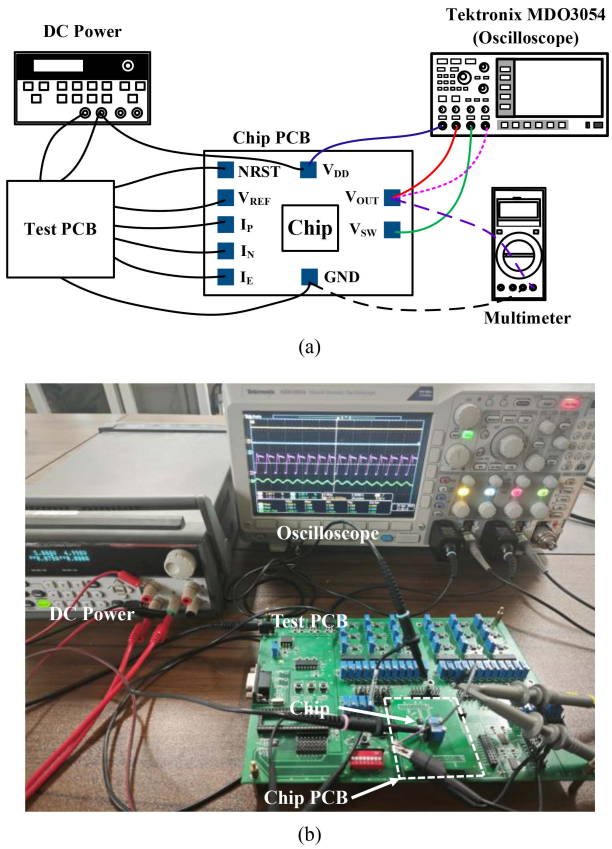


Fig. 7. DC–DC converter chip test benches. (a) Measurement setup block diagram. (b) Chip test environment.

C. Power Stage

As shown in Fig. 1, the power stage only consists of push-pull transistors M_P and M_N. The power transistors $\mathrm{M_P}$ with the size ratio of 5400 μm/0.4 μm and $\mathrm{M_N}$ with the size ratio of 4230 μm/0.5 μm, to achieve the conduction impedances (R_{ON}) less than 0.7 and 0.4 Ω, respectively, which are driven by the P_{GATE} and N_{GATE} signals with a dead zone for M_P OFF and M_N ON and a sleep zone for M_N OFF and M_P on, as shown in Fig. 4(b). Small R_{ON} value benefits a high conversion efficiency but consumes a large silicon area, vice versa. Therefore, R_{ON} has to make a compromise between efficiency and area. In this article, sub-Ω level is chosen and enough for $I_{\mathrm{Load}} \leq 50$ mA and efficiency up to 93%, to evidently save the silicon area.

IV. Experimental Results

The proposed buck dc–dc converter based on the triple-comparator structure is fabricated in a 65-nm CMOS process. Fig. 5 gives the chip micrograph of the prototype buck dc–dc converter, where all the modules of the dc–dc converter and all the pads of the power and IO are clearly demonstrated, with the chip size of 1.0 mm $\times$ 0.7 mm and core area less than 380 μm $\times$ 167 μm.

The chip breakdowns in active area and current dissipation are summarized in Fig. 6, with the detailed submodule silicon size and power consumption. The total quiescent current and

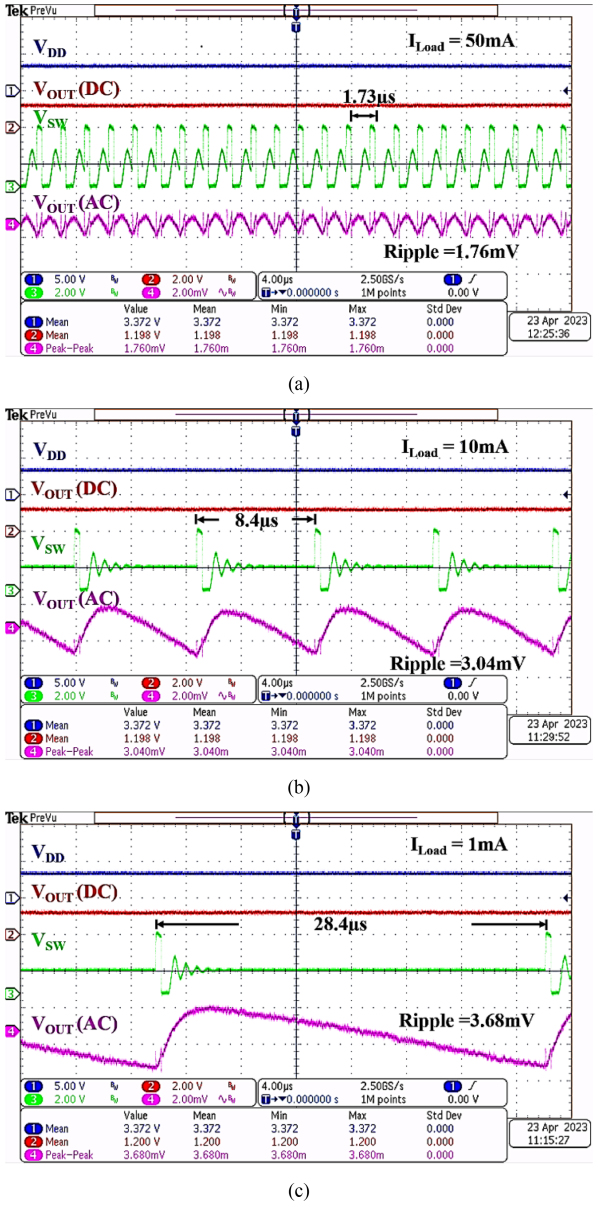


Fig. 8. Steady-state behaviors with 3.3-V V_{DD} and 1.2-V V_{OUT}, under different loads. (a) 50 mA. (b) 10 mA. (c) 1 mA.

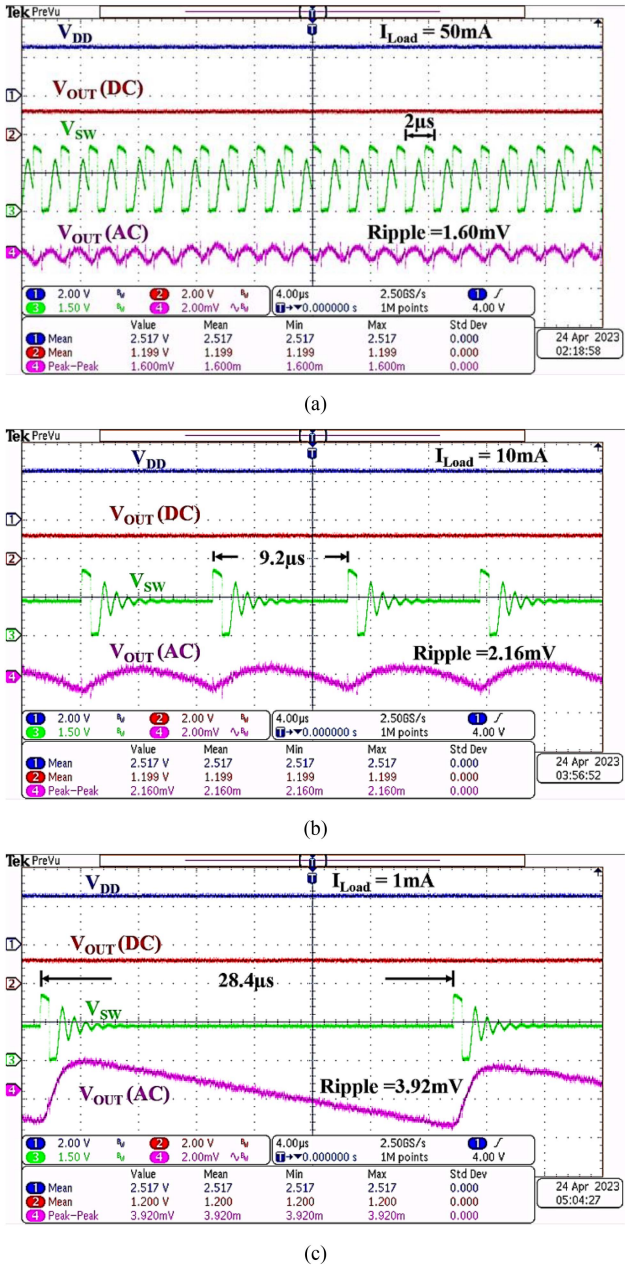


Fig. 9. Steady-state behaviors with 2.5-V V_{DD} and 1.2-V V_{OUT}, under different loads. (a) 50 mA. (b) 10 mA. (c) 1 mA.

active area are 48 μA and 0.03 mm^2, respectively. The power stage occupies the majority of silicon size and the comparators dominate current dissipation. Further power optimization will be done by using the comparator multiplexing scheme.

Fig. 7 gives the converter chip test benches with the detailed connection relationship. A Tektronix MDO3054 oscilloscope is used to observe the signal waveforms. A printed circuit board (PCB) is designed to generate the biasing currents and supply voltages for the measured chip, and is supplied by a dc power. A high-precision multimeter is used to measure the line / load regulations and the efficiency.

Oscilloscopes use the default (dc) coupling mode to track the real-time signal waveforms and utilize the ac coupling one to observe the ripple voltages. Figs. 8, 9, and 10 show the measured converter steady-state behaviors, with V_{OUT} centered at 1.2 V, V_{DD} variation of 1.8–3.3 V, and I_{Load} range of 1–50 mA. It can be seen that V_{OUT} varies from 1.198 to 1.201 V and achieves a peak-to-peak ripple voltage with the minimum and maximum values of 1.20 mV for heavy loads and 3.92 mV for light ones, respectively. The measured switching frequency is automatic sliding, with the lower and upper limits of 35 and 578 kHz for small and large I_{Load}, respectively. V_{SW} waveforms in accordance with Fig. 2, are also observed under different I_{Load} conditions.

The measured load regulation (LDR) and linear regulation (LNR) performances are given in Fig. 11. The converter with V_{OUT} centered at 1.2 V, achieves the LDR variation from

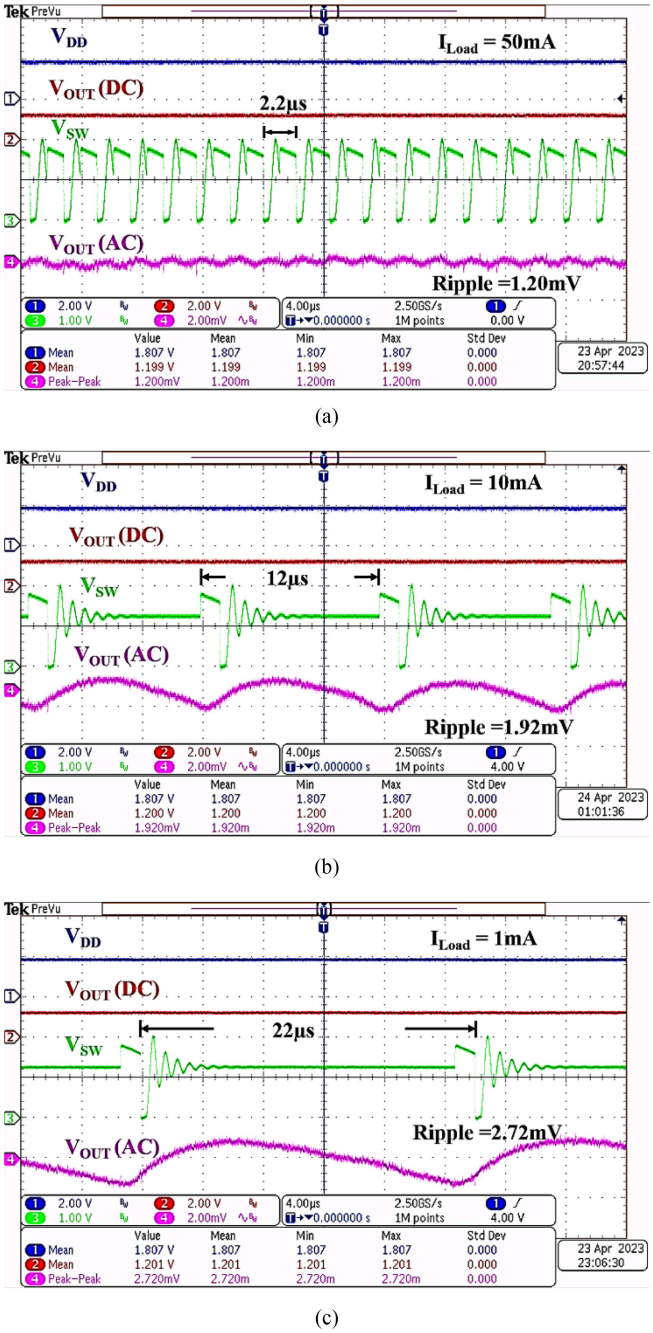


Fig. 10. Steady-state behaviors with 1.8-V V_{DD} and 1.2-V V_{OUT}, under different loads. (a) 50 mA. (b) 10 mA. (c) 1 mA.

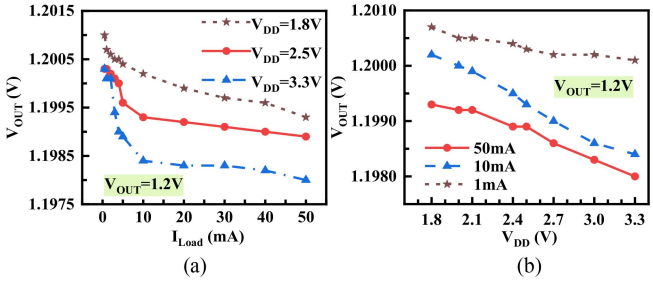


Fig. 11. Measured LDR and LNR of 1.2-V V_{OUT}. (a) Load regulation. (b) Linear regulation.

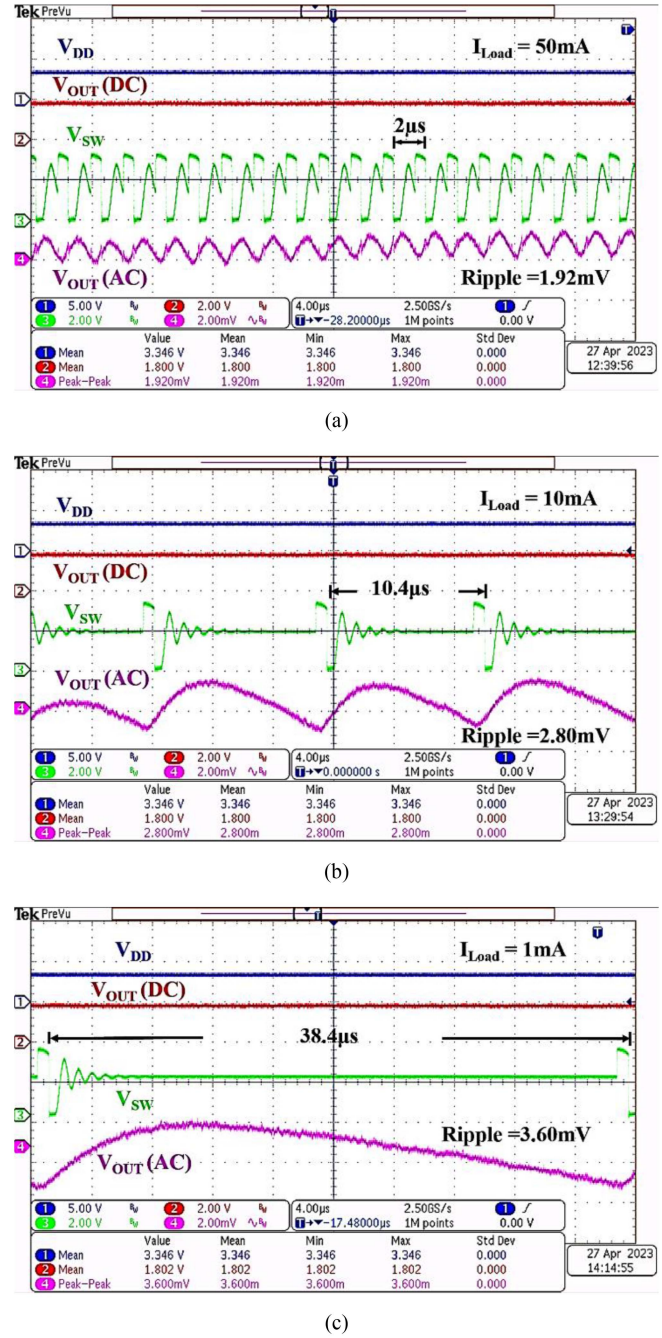
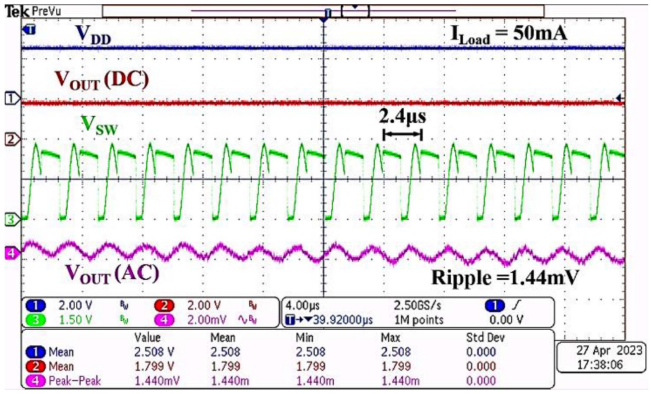


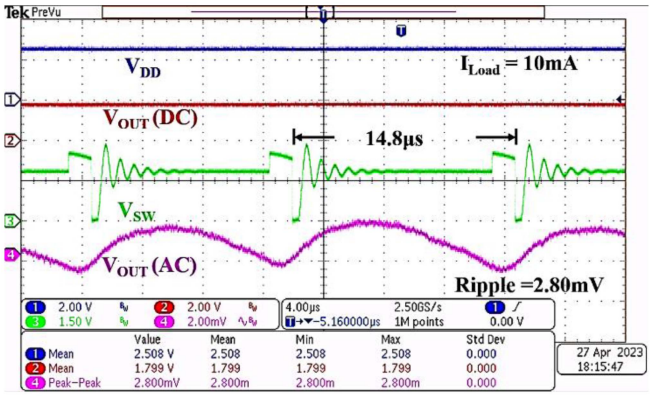
Fig. 12. Steady-state behaviors with 3.3-V V_{DD} and 1.8-V V_{OUT}, under different loads. (a) 50 mA. (b) 10 mA. (c) 1 mA.

0.117% to 0.192% and the LNR range of 0.058%–0.158%, with V_{DD} of 1.8–3.3 V and I_{Load} of 1–50 mA.

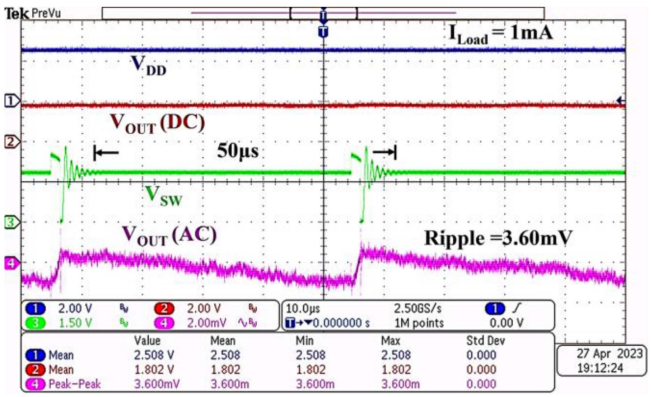
Figs. 12 and 13 show the measured converter steady-state behaviors, with V_{OUT} centered at 1.8 V, V_{DD} variation of 2.5–3.3 V, and I_{Load} range of 1–50 mA. It can be seen that V_{OUT} varies from 1.799 to 1.802 V and achieves a peak-to-peak ripple voltage with the minimum and maximum values of 1.44 mV for heavy loads and 3.60 mV for light ones, respectively. The measured switching frequency is automatic sliding, with the lower and upper limits of 20 and 500 kHz for small and large



(a)



(b)



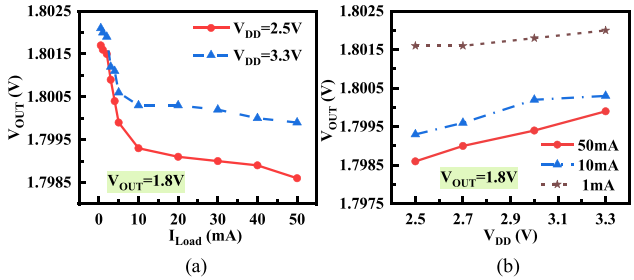
(c)

Fig. 13. Steady-state behaviors with 2.5-V V_{DD} and 1.8-V V_{OUT}, under different loads. (a) 50 mA. (b) 10 mA. (c) 1 mA.

I_{Load}, respectively. V_{SW} waveforms in according to Fig. 2 under heavy and light loads, are also observed.

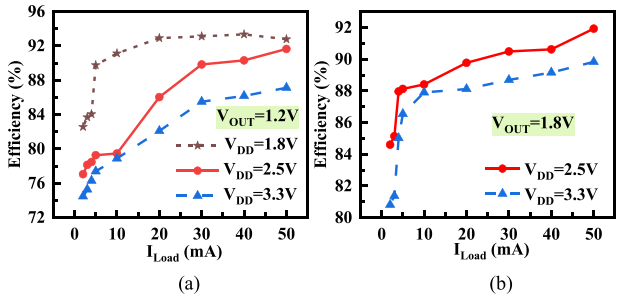
Fig. 14 gives the measured LDR and LNR performances for 1.8-V V_{OUT}. The LDR and LNR are 0.122%–0.172% and 0.022%–0.072%, respectively, under V_{DD} varying from 2.5 to 3.3 V and I_{Load} increasing from 1 to 50 mA. Measured results verify that the presented converter has high robustness over supply voltage and load current variations.

Fig. 15 shows the measured conversion efficiencies with V_{DD} and I_{Load} variations. The converter accomplishes the light-load



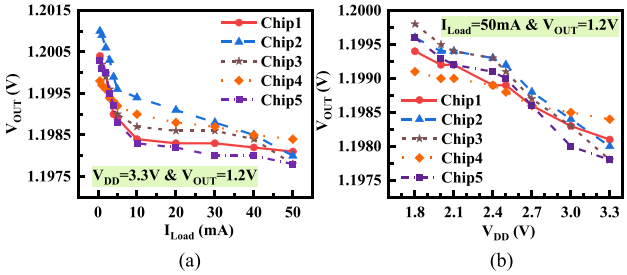
(a) (b)

Fig. 14. Measured LDR and LNR of 1.8-V V_{OUT}. (a) Load regulation. (b) Linear regulation.



(a) (b)

Fig. 15. Measured efficiencies with varying V_{OUT}. (a) 1.2 V. (b) 1.8 V.



(a) (b)

Fig. 16. Measured LDR and LNR performances across multiple chips. (a) 1.2-V LDR. (b) 1.2-V LNR.

efficiency of 81% and heavy-load one of 92% for 1.8-V V_{OUT}, and achieves the minimum and maximum efficiencies of 74% for small I_{Load} and 93% for large I_{Load} with 1.2-V V_{OUT}, respectively. Measured results prove that the proposed sliding-frequency scheme ensures high conversion efficiency (η_{buck}) over a wide load range.

Both Figs. 16 and 17 give the measured LDR and LNR performances across multiple chips. With V_{OUT} centered at 1.2 V, the converter achieves the LDR of 0.117%–0.208% under 3.3-V V_{DD} and the LNR of 0.058%–0.167% under 50-mA I_{Load}, respectively. While for V_{OUT} centered at 1.8 V, both the LDR of 0.094%–0.172% under 3.3-V V_{DD} and the LNR of 0.022%–0.095% under 50-mA I_{Load}, are accomplished. Five chips have the similar LDR / LNR regulation performances and trends, which verifies that the proposed converter is immune to process variations.

Based on the data above, it is concluded that V_{OUT} and ripple voltage slightly decrease, the conversion efficiency is lightly

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This article	[2]	[6]	[12]	[16]	[21]	[26]	[30]
Process (nm)	65 CMOS	65 CMOS	28 CMOS	65 CMOS	180 CMOS	180 BCD	55 CMOS	40 CMOS
Architecture	Tri-COMP	PWM	COT	Hysteretic	DCT+PWM	Tri-Mode	DPWM	PDTD
Supply Voltage (V)	1.8–3.3	3.3	3.3	3.3	2–5	2.7–4.7	1.5–3	2.5
Output Voltage (V)	1.2–1.8	1.0–2.5	1.05	0.6–2.0	0.8–3	1.6	1.2	1.2
Max. I_{Load} (mA)	50	900	1700	1500	50	100	10	300
Max. V_{Ripple} (mV)	3.92	40*	20	150*	25	40	20	60
Max. f_{SW} (MHz)	0.578	1	2.5	1	2.6	4	2	1.45
Max. LDR (%)	0.208# / 0.192	-	-	0.667*	2	0.519*	-	-
Max. LNR (%)	0.167# / 0.158	-	-	0.600*	-	0.050	-	-
Peak η_{buck} (%)	93	92	94	96	93	92	91	93
Total Area (mm²)	0.7	1.10	2.5	2.14	1.10	0.55	-	0.51
Active Area (mm²)	0.03	-	-	0.54	-	-	0.15	-
Undershoot/time (mV/µs)@Load step	8/14 @ 1–50mA	85/4 @ 50–500mA	75/4 @ 0.3–1.7A	106/3.4 @ 0.2–1.1A	80/11 @ 6.67µA–50mA	48/8 @ 5µA–80mA	-	73/0.369 @ 60–300mA
Overshoot/time (mV/ µs)@Load step	10/16 @ 50–1mA	70/4 @ 500–50mA	90/5 @ 1.7–0.3A	87/3.6 @ 1.1–0.2A	30/60 @ 50mA–6.67µA	26/2.6 @ 80mA–5µA	-	72/0.335 @ 300–60mA
Auto Frequency Switching	Yes	No	No	No	Yes	Yes	No	No
Passive Device Used	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FoM[a] (pJ/1mW)	4.05	17.39	8.11	78.13	3.45	6.79	9.16	37.08

* Calculation according to the data in the literature # Multiple-chip results [a] Smaller value is better under the maximum output voltage

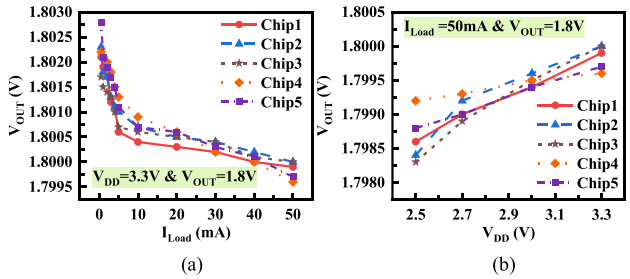


Fig. 17. Measured LDR and LNR performances across multiple chips. (a) 1.8-V LDR. (b) 1.8-V LNR.

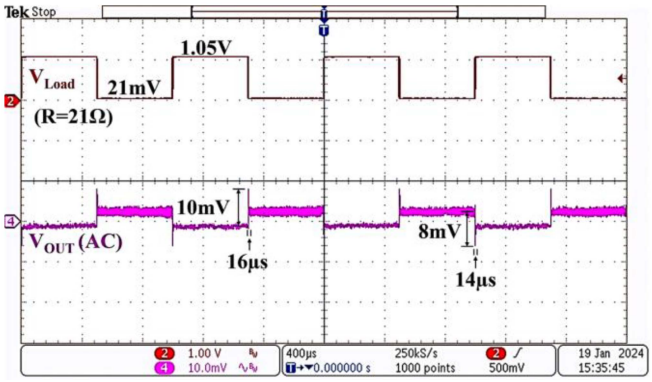


Fig. 18. Measured load transient response with load current step.

improved, and the switching frequency evidently increases, as $I_{\rm Load}$ goes up, vice versa. In addition, the conversion efficiency also slightly grows up as $V_{\rm DD}$ decreases. The proposed design has an autosliding switching frequency from 20 to 578 kHz for different load conditions, to ensure high conversion efficiency up to 93% and low ripple voltage less than 3.92 mV.

Fig. 18 gives the measured load transient response between 1 and 50 mA, with 3.3-V V_{DD} and 1.2-V $V_{\rm OUT}$. By using an external voltage-to-current converter ($V_{\rm Load}/R$) as the load for the load current step, the measured overshoot and undershoot voltages are 10 and 8 mV, while the recovery time are 16 and 14 μs, respectively.

The dc–dc converter performances are summarized and compared to the existing designs in Table I. The proposed converter benefits a small overshoot/overshoot voltage, at the cost of the recovery time, in comparison to the traditional structures. The figure of merit (FoM), to calculate the consumed energy from the supply voltage per switching cycle to supply the unit output power ($P_{\rm Load}$) [33], is given in (3), to consider conversion efficiency, load capacity, switching frequency, and output ripple. The presented design with fairly good LNR / LDR and ripple features, contributes to ultra-low-cost ultrasmall-area semidigital implementation with a better FoM value, by employing the presented triple-comparator architecture, and also benefits pure-MOS design without any on-chip passive components

$$\text{FoM(pJ/1mW)} = \frac{1}{\eta_{\rm buck}} \frac{I_{\rm Load(mA)} \times V_{\rm ripple(mV)}}{f_{\rm SW(MHz)}} \times \frac{1}{P_{\rm Load(mW)}}. \tag{3}$$

V. CONCLUSION

Based on a new triple-comparator architecture, a low-cost pure-MOS sliding-frequency semidigital buck dc–dc converter is proposed for applications in SoC power management. The

converter has been fabricated in a 65-nm CMOS technology. Test experiments show that the converter achieves a peak efficiency up to 93%, a peak-to-peak ripple less than 3.92 mV, an LNR / LDR less than 0.208%, a load-step overshoot/undershoot voltage lower than 10 mV, a FoM value less than 4.1 pJ/1mW, and an ultra-low active area smaller than 0.03 mm^2. The presented converter has the following advantages: low-complexity digitalized structure only with a triple comparator and several digital units; automatic-sliding switching frequency for high efficiency and low ripple; and no use of on-chip passive components for low hardware cost. The proposed mechanism, which is fully different from the existing operational schemes, leads to low-complexity digital designs.

Both power optimization, with a reuse scheme of three comparators, and reconfigurable offset voltages, using multiple groups of input-pair size ratios, will be considered as future works to aim at a lower quiescent current and a larger load range, respectively.

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