A High Conversion Ratio Converter Based on Tapped-Series Capacitor Circuit

Tingting Yao, *Member, IEEE*, Mingfei Ban, *Member, IEEE*, and Yiqi Liu, *Member, IEEE*

***Abstract*—A high conversion ratio converter is detailed analyzed in this article. Inspired by partial power structure, the proposed topology can be divided into two circuits: *LLC* circuit and tapped-series capacitor (TSC) step-down circuit. The *LLC* converter operates under a constant operating frequency. The tapped-series capacitor converter is paralleled to output of *LLC* converter with closed-loop control to regulate the total output voltage with the high conversion ratio ability. The operational principle and parameter design method of proposed topology are explained in detail, especially the operating modes of TSC circuit. Meanwhile the structure of matrix transformer adopted in the *LLC* converter is optimized. The proposed converter can achieve both high conversion ratio ability as well as high efficiency with a wide input voltage range. A 400–5 V prototype is built and the testing results verify the advantages of the proposed converter.**

***Index Terms*—High conversion ratio, tapped-series capacitor, zero voltage switching.**

I. Introduction

FOR dc–dc converters, one great challenge of the topology is to realize high conversion ratio, such as in the application of auxiliary power module in electrical vehicle, which needs to convert high input voltage to low output voltage by more than 50 times. For high input voltage and low output voltage topology, usually two kinds of structures are used from the perspective of energy conversion times, namely single-stage one and multiple-stage one [1], [2], [3], [4], [5], [6], [7], [8], [9].

For the multiple-stage structure, the high conversion ratio can be divided into several different parts. Kasper et al. [10] adopted a cascade converter architecture, while a large number of passive components is utilized, which increases the system size and cost [11], [12]. Chuang et al. [13] proposed an interleaved high step-down Buck topology, which can reduce switching stress. Junfeng et al. [14] improved the topology with multilevel circuit using an inductor, which reduces the volume. Also, new material component is also used to improve power density [15]. However, efficiency is limited by multiple conversion stages.

Manuscript received 4 January 2024; revised 5 February 2024; accepted 17 February 2024. Date of publication 23 February 2024; date of current version 20 March 2024. This work was supported by the Fundamental Research Funds for the Central Universities. Recommended for publication by Associate Editor D. Qiu. *(Corresponding author: Yiqi Liu.)*

The authors are with the College of Computer and Control Engineering, Northeast Forestry University, Harbin 150001, China (e-mail: yaotingting@nefu.edu.cn; banmingfei@nefu.edu.cn; ee_617@nefu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3369051.

Digital Object Identifier 10.1109/TPEL.2024.3369051

To reduce the number of power conversion, many scholars have proposed various novel single-stage step-down topologies, and the most typical one is *LLC* circuit. Besides it, tapped inductor Buck converter with a simple structure is proposed in [16], but the switch has a large voltage stress and operates under hard switching conditions. Some topologies based switched capacitor and other modules have been proposed to reduce components voltage stress [17], [18], [19]. [20], [21], [22] add a switch and an inductor to form the hybrid-transformer-based Buck converter on the basis of [19] to achieve soft switching and suppress voltage oscillation. For the single-stage structure, though the energy conversion times can be reduced, it is difficult to achieve high efficiency within the various input or output situations. For example, in *LLC* converter, the switch can operate in the well soft-switching mode at the resonant frequency. However, when the input voltage or output voltage changes, the operating frequency must be adjusted, which is different from the optimal point, which leads to the decrement of the system efficiency. Based on above analysis, it can be summarized that for high conversion ratio single stage converter, one concern of these converters is that how to design a high-performance transformer with high turns ratio. Another concern of the single stage one is that how to guarantee a high performance within a certain voltage conversion range. As well know, the soft switching characteristics can only be achieved within a very narrow range, thus, how to achieve high and wide conversion requirement is a difficult and emerging topic, which needs to be addressed.

To solve the above mentioned problem, other advanced pre-single-stage structure is proposed in [23], [24], [25], [26], [27], [28], [29], [30], and [31], such as sigma structure. This presingle-stage one is similar as input series and output parallel. The most typical one is the combination of *LLC* circuit and Buck circuit, where the *LLC* circuit operates under the resonant frequency to achieve high efficiency. And when the input voltage various, the Buck circuit works with different duty cycle to regulate the output voltage. However, because the step-down ability of the Buck circuit is not very strong, when the input voltage of the Buck circuit is too high, it cannot realize the step-down conversion considering the effect of switch ON resistance, inductor series resistance, and other parasitic components. Meanwhile, the efficiency of the converter is poor under extreme conversion situation.

To achieve performance improvement of high conversion ratio converter, a novel step-down topology based on tapped-series capacitor circuit is proposed. For the proposed converter, the tapped series capacitor converter is adopted as a regulated stage,

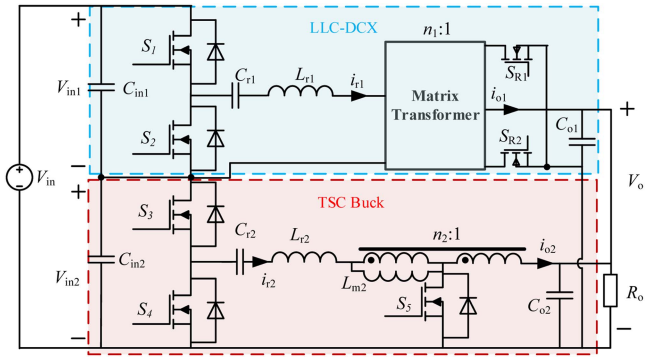

Fig. 1. Proposed single-stage high step-down DC–DC converter.

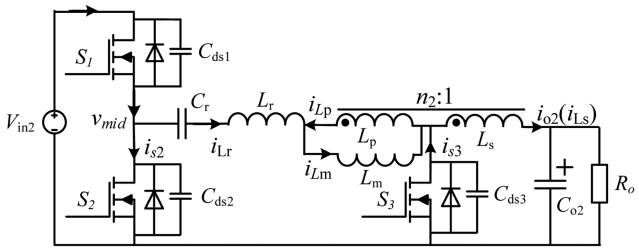

Fig. 2. TSC converter with ground referenced resonant path.

which can operate under soft-switching condition and realize higher conversion ratio. Based on the proposed topology, the converter can achieve 400 V–5 V step-down power conversion with 95.2% efficiency and the efficiency is always above 93.2% with input voltage varying from 360 V to 440 V.

The rest of this article is organized as follows. In this article, general structure and the operating modes are given in Section II. The matrix transformer with advanced structure is analyzed in Section III. The parameter design and calculation method are detailed analyzed in Section IV. The prototype and testing waveforms are given in Section V. Finally, Section VI concludes this article.

II. Operational Principle of the Proposed Converter

A. Introduction of the Proposed Topology's Structure

The topology of the high step-down dc–dc converter proposed in this article is shown in Fig. 1. It consists of two parts, *LLC* converter and resonant tapped-series capacitor (TSC) step-down converter, forming a stacked and quasi-parallel structure. The *LLC* plays as an dc transformer with constant conversion ratio and transfers most part of the input power to the load. The TSC step-down converter is adopted to maintain stable output voltage through closed-loop control by adjusting the duty cycle. It is possible to ensure that all switches realize soft switching through reasonable parameter design and control method.

Since the input side is connected in series, both converters can be regarded as voltage sources. Therefore, the total input voltage is equal to the sum of the respective input voltages. Assuming that the voltage gain expressions of *LLC*-DC transformer (DCX) and resonant TSC converter can be, as shown in (1) and (2), respectively, in the latter part, detailed theoretical derivations will be made for the specific gain expressions of the two parts of the circuit

$$\frac{V_o}{V_{\text{in1}}} = M_1 \tag{1}$$

$$\frac{V_o}{V_{\text{in2}}} = M_2 \tag{2}$$

where V_{in1} stands for the input side voltage of the *LLC* circuit and V_{in2} stands for that of TSC circuit. Since the input sides of the two converters are connected in series, they have the same input current, so the power distribution between them is proportional to their input voltage. The quantitative relationship between *LLC* circuit and TSC circuit is

$$\frac{P_{\text{in1}}}{P_{\text{in2}}} = \frac{V_{\text{in1}}}{V_{\text{in2}}} = \frac{M_2}{M_1}. \tag{3}$$

P_{in1} stands for the input side power of the *LLC* circuit and P_{in2} stands for that of TSC circuit. Furthermore, when η_1 and η_2 represents the corresponding efficiency; P_{o1} and P_{o2} represent the output power of the corresponding circuits, respectively; P_o is the system output power, the overall system efficiency can be expressed as

$$\eta = \frac{P_o}{P_{\text{in}}} = \frac{P_{o1} + P_{o2}}{P_{\text{in1}} + P_{\text{in2}}} = \frac{P_{\text{in1}}\eta_1 + P_{\text{in2}}\eta_2}{P_{\text{in1}} + P_{\text{in2}}}. \tag{4}$$

Combining above equations, the overall efficiency can be expressed as (5), where the efficiency is sum relationship

$$\eta = \frac{V_{\text{in1}}}{V_{\text{in}}}\eta_1 + \frac{V_{\text{in2}}}{V_{\text{in}}}\eta_2. \tag{5}$$

B. Operational Analysis of TSC Converter

1) Mode Analysis: The circuit diagram of resonant TSC converter is shown in Fig. 2, including a float switch S_1, two ground switches S_2, and switch S_3. There is a tapped coupled inductor in the circuit, where consists by primary side inductor L_{p} and secondary side inductor L_{s}. L_{m} is the magnetizing inductance. C_{r} is a series capacitor, which can block dc component and also plays the role of resonant. The leakage inductance of the tapped coupled inductor can be used as the resonant inductor L_{r}. The turns ratio of the coupled inductor is n_2:1 in the step-down situation where the turns ratio is larger than 1.

From a general perspective, the operating state can be divided into nonresonant one and resonant one. For the resonant one, it is based on the resonance between C_{r} and L_{r}, which can help to guarantee the soft-switching operating mode of the switches. The capacitor and the tapped coupled inductor can both help to achieve high step-down ability. Compared with the traditional Buck converter, this circuit utilizes the energy stored in the capacitor and the magnetic element, which can realize high performance.

The detailed current and voltage waveforms are shown in Fig. 3. To analyze the resonant circuit, there are seven different operating modes during one cycle. The specific circuit diagram can be seen by Fig. 4. The description is given in the following part.

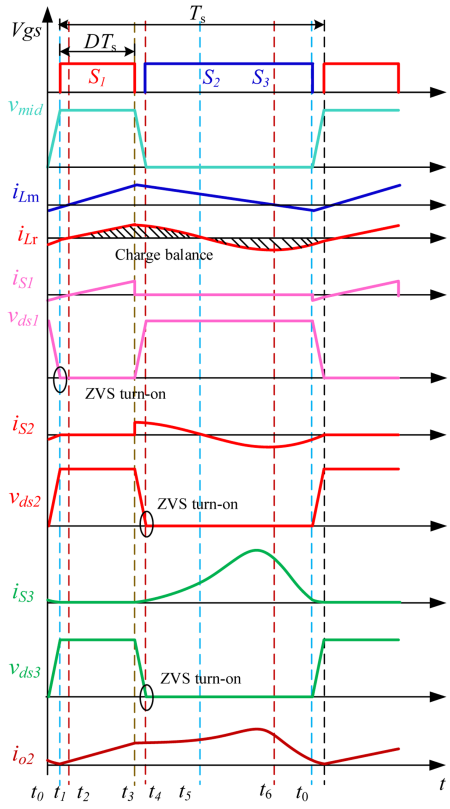

Fig. 3. Main waveforms of the TSC converter.

Mode 1 [t_0-t_1*]:* This mode starts when the driving signals of S_2 and S_3 disappear. The half bridge structure charges and discharges the parasitic capacitance with an inductive load and operate to guarantee the soft switching condition. When the driving signal of S_1 comes when the switch drain-source voltage is zero, this mode ends.

Mode 2 [t_1-t_2*]:* This mode starts when driving signal of S_1 comes. The magnetizing inductor continues to discharge the current from right to left direction in the diagram. The modes end when the magnetizing inductor is fully discharged and the current direction will be reverse in the following instant.

Mode 3 [t_2-t_3*]:* This mode starts when the input voltage begins to charge the resonant network. When assuming the constant voltage across the resonant capacitor, the current of the resonant inductor, and the magnetizing inductor will change linearly. The mode ends when the driving signal of S_1 disappears.

Mode 4 [t_3-t_4*]:* This mode starts when the driving signals of S_1 disappears. The half bridge structure charges and discharges the parasitic capacitance with an inductive load and operate to guarantee the soft switching condition. When the driving signal of S_2 and S_3 come when switch drain-source voltage is zero, this mode ends.

Mode 5 [t_4-t_5*]:* This mode starts when the driving signal of S_2 and S_3 come. The voltage across the primary side inductor and the magnetizing inductor keep constant. Thus, in the loop of resonant capacitor and resonant inductor, they operate in the resonant situation. This mode ends when the positive current resonates to zero.

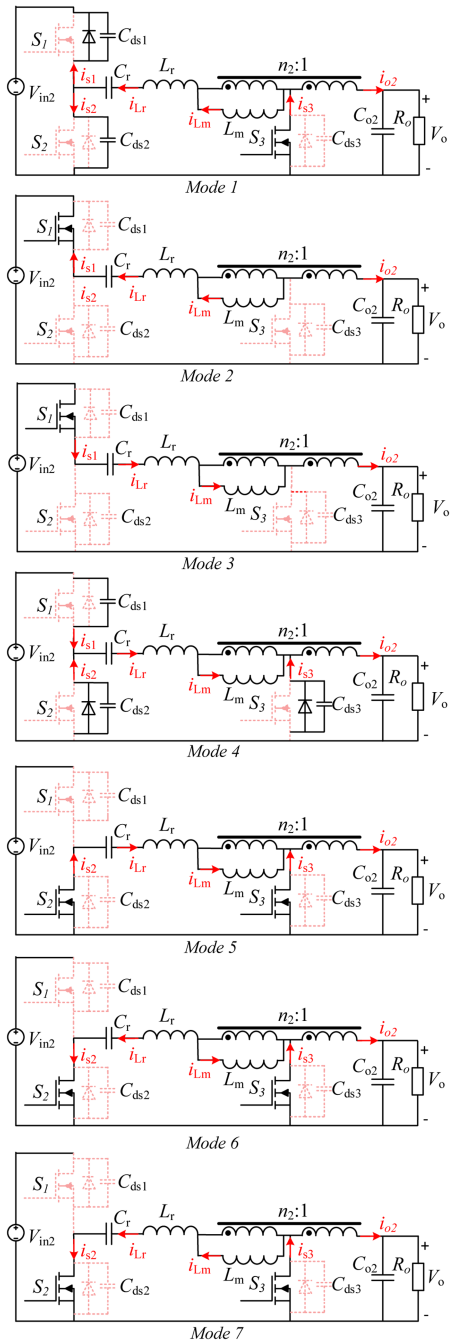

Fig. 4. Working modes of TSC converter.

Mode 6 [t_5-t_6*]:* This mode starts when the resonant current comes into the negative part. The magnetizing inductor voltage still keeps constant. This mode ends when the direction of the magnetizing inductance begins to be reverse.

Mode 7 [t_6-t_0*]:* This mode starts when direction of the magnetizing inductance begins to be reverse. This mode ends when the driving signals of S_2 and S_3 disappear.

2) Voltage Gain: According to mode 2 and mode 3, (6)–(9) can be obtained

$$i_{Lr} = i_{o2} = n_2 i_{Lp} \tag{6}$$

$$i_{Lm} = i_{Lp} + i_{Lr} \tag{7}$$

$$V_{Lm} = L_m \frac{di_{Lm}}{dt} = n_2 V_{Ls} \tag{8}$$

$$V_{Lr} = L_r \frac{di_{Lr}}{dt}. \tag{9}$$

According to Kirchhoff's voltage law, (10) can be obtained

$$V_{\text{in}2} - V_{Cr} - V_o = V_{Lr} + V_{Lm} + V_{Ls}. \tag{10}$$

Then, the magnetizing inductor voltage and resonant inductor voltage can be calculated as

$$V_{Lm} = \frac{(V_{\text{in}2} - V_o - V_{Cr}) n_2 (n_2 + 1) L_m}{L_m (n_2 + 1)^2 + n_2{}^2 V_{Cr}} \tag{11}$$

$$V_{Lr} = \frac{(V_{\text{in}2} - V_o - V_{Cr}) n_2{}^2 L_r}{L_m (n_2 + 1)^2 + n_2{}^2 L_r}. \tag{12}$$

During mode 5 and mode 6, the corresponding inductors voltage can be expressed as

$$V'_{Lm} = -n_2 V_o \tag{13}$$

$$V'_{Lr} = n_2 V_o - V_{Cr}. \tag{14}$$

The relationship between the currents can be expressed as

$$i_{s2} = i_{Lr} = i_{s3} - i_{o2} \tag{15}$$

$$i_{Lm} = i_{Lp} + i_{Lr} = \frac{1}{n_2} i_{io2} + i_{Lr}. \tag{16}$$

For the magnetizing inductor and the resonant inductor voltage, voltage-second-balance principle can be applied. Then, (17) and (18) can be given

$$V_{Lm} D = V'_{Lm} (1 - D) \tag{17}$$

$$V_{Lr} D = -V'_{Lr} (1 - D). \tag{18}$$

Combining (11)–(18), the voltage conversion ratio of resonant TSC converter can be obtained as follows:

$$M_2 = \frac{V_o}{V_{\text{in}2}} = \frac{(n_2 + 1) L_m D}{L_m (n_2 + 1)^2 + n_2{}^2 L_r}. \tag{19}$$

In general, $L_m \gg L_r$ in the actual design process, (19) can be expressed as

$$M_2 = \frac{V_o}{V_{\text{in}2}} = \frac{D}{n_2 + 1}. \tag{20}$$

According to the simplified (20), the relationship between the voltage conversion ratio M_2, the duty cycle D and the turns ratio n_2 can be obtained, as shown in Fig. 5. The appropriate D and n_2 can be determined according to the actual circuit parameters based on the surface.

III. Optimal Design of the Matrix Transformer

A. Magnetic Integration Design

The voltage gain of *LLC* circuit is determined by the turns ratio of transformer. For a high turns-ratio transformer, the print circuit board (PCB) winding structure meets great challenges.

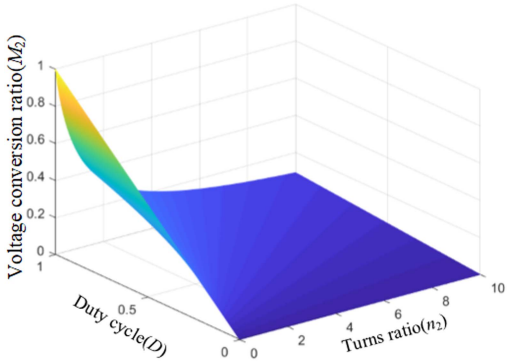

Fig. 5. Voltage conversion ratio M_2 versus dimension variable turns ratio n_2 and duty cycle D.

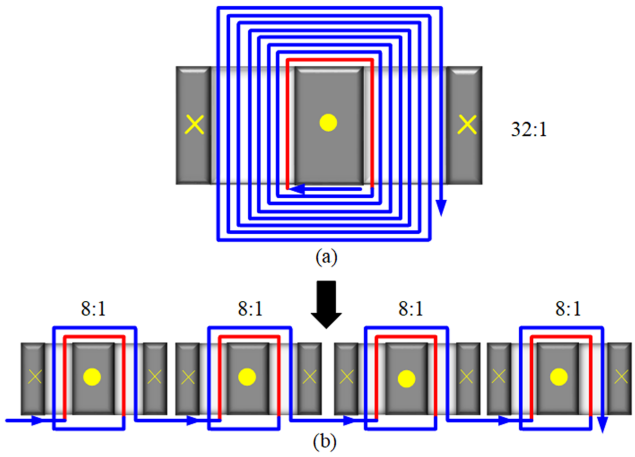

Fig. 6. Original matrix transformer magnetic integration process. (a) Only one magnetic core. (b) Original matrix transformer structure.

Taking a 32:1 transformer as an example, the winding arrangement method is shown in Fig. 6 under the traditional transformer design method. For convenience, only the primary and secondary windings of one layer are drawn to illustrate the magnetic integration process of the matrix transformer, where the primary winding, which is represented by the blue line occupying 4 series layers (8 turns in each layer). The secondary winding with a center tap is represented by the red line.

Owing to the limited window area of the magnetic core, the structure of Fig. 6(a) increases the area of the PCB. Therefore, four magnetic cores are used as the subunits of the matrix transformer, thereby changing the original eight-turn primary winding per layer to two turns per layer, as shown in Fig. 6(b). Nevertheless, the number of magnetic cores in this method is large and the utilization rate is low.

In order to reduce the number of magnetic cores, the magnetic integration method, as Fig. 7(a) show is adopted. In order to ensure that the magnetic flux does not circulate between the external magnetic legs, the air gap is set in the external magnetic core legs, and there is no air gap in the central magnetic core leg. Furthermore, the winding direction on one of the magnetic legs of each magnetic core is adjusted to change the magnetic flux

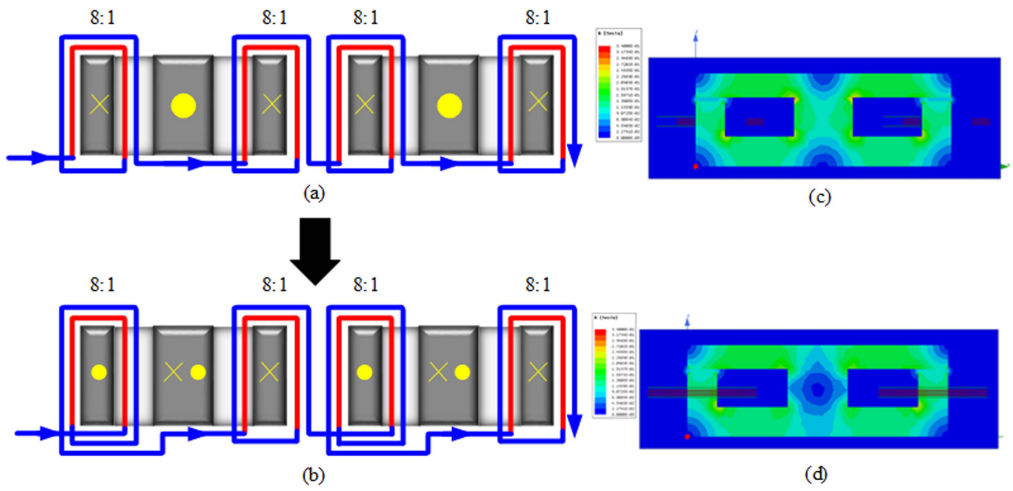

Fig. 7. Magnetic integration process based on the principle of magnetic flux cancellation. (a) No principle of magnetic flux cancellation. (b) Using the principle of magnetic flux cancellation. (c) FEA simulation result corresponding to (a). (d) FEA simulation result corresponding to (b).

direction in order to reduce the magnetic loss. The direction of the magnetic flux generated by the external magnetic legs can be designed opposite, as shown in Fig. 7(b). Fig. 7(c) and (d), respectively, shows the cross-sectional view of the finite element analysis (FEA) simulation under two winding methods. It can be seen that the optimized winding structure obviously weakens the ac magnetic flux of the central leg in order to reduce core loss.

B. Novel Windings Arrangement Design Scheme

The actual number of winding turns per layer should not be too much due to the limited window area of the magnetic core. Otherwise, the windings occupy larger PCB surface area outside window of the magnetic core, which is not beneficial to the layout of other components. Second, considering the design cost, each layer of windings is connected in series with via instead of blind holes or buried holes, which means that the position of the through hole used to realize the series connection of two adjacent layers of windings is not allowed to pass through the windings of other layers. This brings great limitations to the arrangement of the primary and secondary windings. Therefore, the novel winding layout design scheme is proposed in this article on the basis of the magnetic integration to ensure that the PCB surface area occupied by the windings can be decreased while reducing costs and using vias as few as possible.

The primary winding layout using the improved scheme is shown in Figs. 8 and 9. The turns ratio of each element transformer is 8:1. The red solid line and the brown dashed line represent the windings of the layer 1 and layer 2, respectively, and the blue solid line and the green dashed line represent the windings of the layer 3 and layer 4, respectively. The winding of layer 1 and layer 2 are connected in series for each element transformer. Then, the two layers windings of the four subunits are connected in series. The windings of layer 1 and layer 4 are connected through via 1. The winding methods of layer 3 and layer 4 are the same as above. The via Ax (x = 12,34) and the via Bx (x = 12,34) are, respectively, staggered in space. Compared

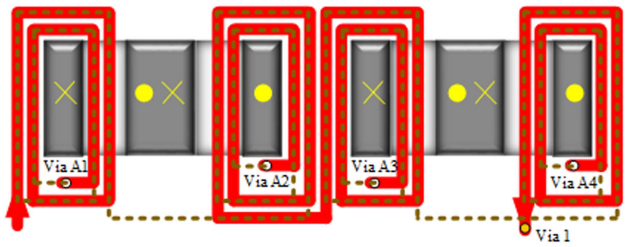

Fig. 8. Winding structure of layer 1 and layer 2 under the improved scheme.

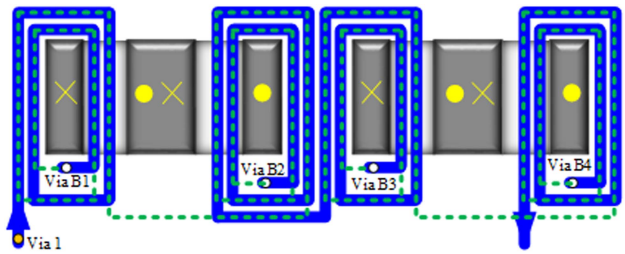

Fig. 9. Winding structure of layer 3 and layer 4 under the improved scheme.

with the original method, the number of vias reduces by 25%, and the PCB surface area occupied by the winding is smaller under the condition of constant line width and line spacing. The three-dimensional (3-D) diagram of the matrix transformer winding is shown in Fig. 10, the secondary windings of other subunits is hidden for easily reading.

IV. Parameter Design of the Proposed Converter

A. Turns Ratio of the Matrix Transformer

A 500 kHz 400 V to 5 V converter is designed based on above analysis. In order to transfer most of the power of the system through *LLC* circuit and reduce the effect of the TSC converter on the overall efficiency of the system. Here, the input voltages

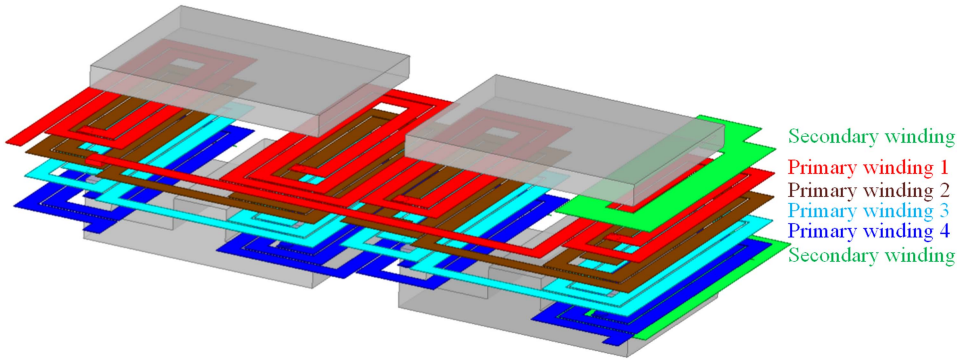

Fig. 10. Three-dimensional simulation schematic diagram of matrix transformer.

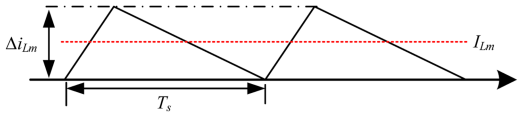

Fig. 11. Schematic diagram of magnetizing current waveform.

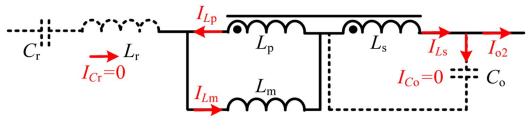

Fig. 12. DC equivalent circuit model of coupled inductor.

of *LLC* and TSC converters under rated conditions are designed to be 320 V and 80 V, respectively.

The larger turns ratio n_1 of *LLC* is, the smaller loss caused by TSC converter can be achieved. Meanwhile, the sum of both input voltage is always equal to the total input voltage, so V_{in1} must be less than the minimum input voltage V_{inmin}. Therefore, the turns ratio of *LLC* n_1 should satisfy

$$n_1 < \frac{V_{\mathrm{inmin}}}{2V_o}. \tag{21}$$

It is calculated that n_1<36, and it is actually determined that the total turns ratio of the matrix transformer is 32:1, i.e., the turns ratio of each element transformer is 8:1.

B. Parameter Design of TSC Converter

1) Magnetizing Inductance: According to the mode analysis, the negative magnetizing current i_{Lm} is not conducive for the energy transmission and efficiency improvement. Therefore, in order to ensure the magnetizing current always flows in the positive direction, the following requirements should be satisfied:

$$I_{Lm} \geq \frac{1}{T_s}\int_0^{T_s} i_{Lm}dt = \frac{1}{2}\Delta i_{Lm} \tag{22}$$

where I_{Lm} is the dc component of the magnetizing current as well as the average value. Δi_{Lm} represents the peak-to-peak value of the magnetizing current. T_s stands for the switching period, as shown in Fig. 11.

Assuming 100% efficiency, the equivalent dc circuit model of the coupled inductor is shown in Fig. 12, since the capacitor satisfies the ampere-second balance principle in the steady state. It can be seen that the average currents I_{Cr} and I_{Lr} flowing through the resonant capacitor and the resonant inductor are zero. Assuming that all ac components of the output current i_{Ls} flow through the output filter capacitor C_o. The dc component flows through the load. Therefore, the dc component I_{Lm} of the magnetizing inductance is equal to the dc component I_{Lp} of i_{Lp}, and the dc component I_{o2} of the output current is equal to the dc component I_{Ls} of i_{Ls}. Then, the following formula holds:

$$\langle i_{Lm}\rangle_{T_s} = \langle i_{Lp}\rangle_{T_s} + \langle i_{Lr}\rangle_{T_s} \Leftrightarrow I_{Lm} = I_{Lp} \tag{23}$$

$$\langle i_{Ls}\rangle = I_{Ls} = I_{o2}. \tag{24}$$

From the turns ratio, (25) can be obtained

$$I_{Lm} = I_{Lp} = \frac{1}{n_2}I_{o2} = \frac{1}{n_2} \times \frac{V_o}{R_o} = \frac{1}{n_2}I_{Ls}. \tag{25}$$

TABLE I
FUNDAMENTAL PARAMETERS OF THE PROPOSED TOPOLOGY

Description	Value or Part Number
Input voltage	360V~440V (rated 400V)
Output voltage/Output current	5V/20A
Output power	100W
Switching frequency	500kHz
Switches, $S_{1,2,3,4,5}$	GaN Systems GS66508B
SRs, $S_{R1\sim R8}$	Infineon BSZ019N03LS
Leakage inductance, L_{r1}	3.6μH
Resonant capacitor, C_{r1}	29nF
Magnetizing inductance, L_{m1}	52μH
Leakage inductance, L_{r2}	0.3μH
Resonant capacitor, C_{r2}	320nF
Magnetizing inductance, L_{m2}	2μH
Transformer Core (3F36)	EI22 (LLC), EQ20 (TSC Buck)
Output capacitance, $C_{o1,o2}$	300μF

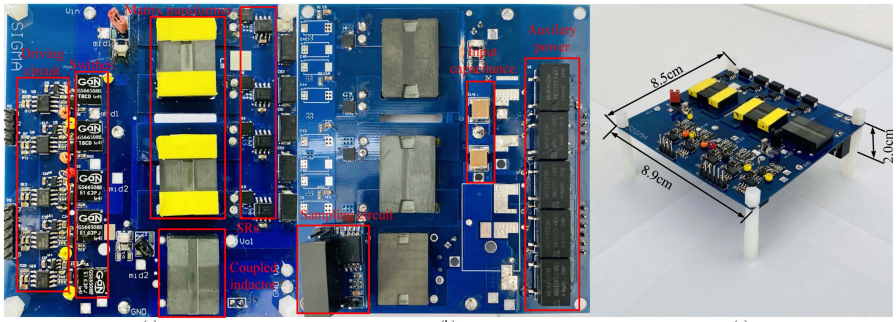

Fig. 13. Photos of experimental prototype. (a) Top view. (b) Bottom view. (c) Overall view.

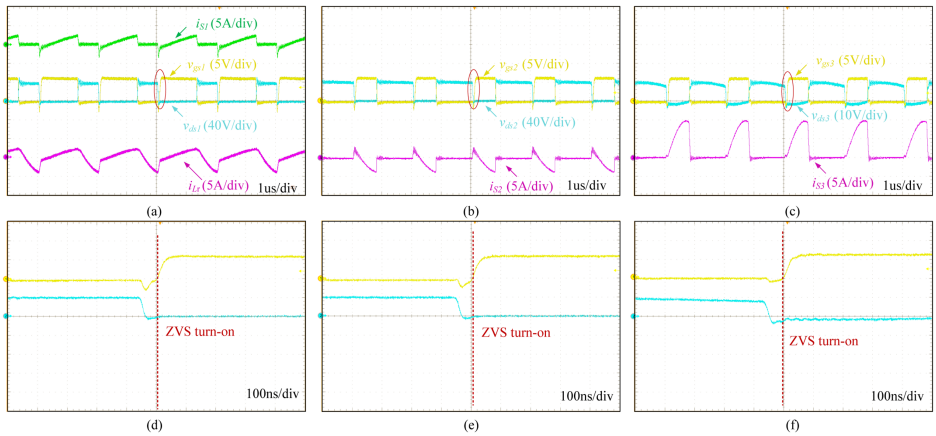

Fig. 14. Experimental waveforms of TSC converter under 360 V-input (40 V-input for TSC converter) conditions (The listed components correspond to the symbols in Fig. 2). (a) i_{S1}: current flowing through S_1; i_{Lr}: resonant current; v_{gs1} driving voltage of S_1; v_{ds1}: drain-to-source voltage of S_1. (b) i_{S2}: current flowing through S_2; v_{gs2} driving voltage of S_2; v_{ds2}: drain-to-source voltage of S_2. (c) i_{S3}: current flowing through S_3; v_{gs3} driving voltage of S_3; v_{ds3}: drain-to-source voltage of S_3. (d) Soft switching waveforms of S_1. (e) Soft switching waveforms of S_2. (f) Soft switching waveforms of S_3.

According to (8) and (23)–(25), Δi_{Lm} can be expressed as

$$\Delta i_{Lm} = \frac{\frac{n_2}{n_2+1} V_{\text{in2}} \cdot D\,(1-D)\,T_s}{L_m}. \tag{26}$$

According to (22), (27) can be obtained

$$L_m \geq \frac{{n_2}^2\,(1-D)\,T_s R_o}{2}. \tag{27}$$

Meanwhile, the overall input voltage variation causes the input voltage fluctuation of the TSC converter when duty cycle is adjusted to regulate output voltage, here $D_{\min}$ represents minimum duty cycle. Then, the critical value of the magnetizing inductance can be obtained by

$$L_m \geq \frac{{n_2}^2\,(1-D_{\min})\,T_s R_o}{2}. \tag{28}$$

V. Experimental Results

A 500 kHz 5 V/20 A 100 W experimental prototype is built to verify the above analysis. The devices types and values are shown in Table I, including the switches, coupled inductor, and capacitors. Fig. 13 shows the picture of the experimental prototype and the testing current and voltage waveforms are shown in Figs. 14–16.

As the picture shows, there are three components in the prototype, which occupy most of the place. In the future, the power density can be further improved by integrating the two magnetic cores of the matrix transformer. From another perspective, the operating frequency of the converter can be further increased, thus, the value and volume of the passive components can be further reduced. Meanwhile, as the prototype picture shows, the driving circuit of these switches also occupy a certain area, thus, the integrated chip for switch and driving circuit can be used to further improve the power density. Finally, in the current prototype, the components are placed in a horizontal layout, the layout can be further optimized into a vertical 3-D structure to reduce the volume.

It can be seen from Figs. 14–16 that all the switches of the TSC converter can realize ZVS turn-ON within the wide input range of 360 V to 440 V under rated load conditions. The experimental waveforms verify the correctness of the theoretical analysis. The overall efficiency of the system can reach 95.2% under rated working conditions.

The efficiency of the proposed topology and the rated 400 V/5 V *LLC* converter under the same input voltage range are compared, as shown in Fig. 17. The efficiency of the proposed topology is better than that of the *LLC*+Buck converter under the entire input voltage range. The peak efficiency at the rated

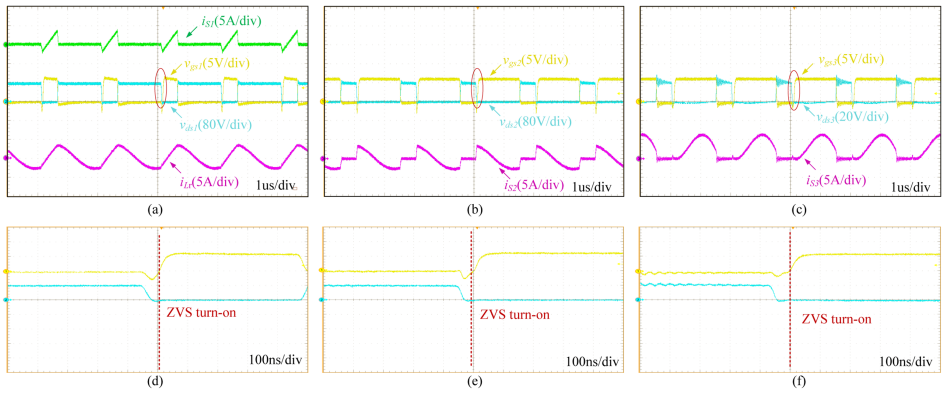

Fig. 15. Experimental waveforms of TSC converter under rated 400 V-input (80 V-input for TSC converter) conditions (The listed components correspond to the symbols in Fig. 2). (a) i_{S1}: current flowing through S_1; i_{Lr}: resonant current; v_{gs1} driving voltage of S_1; v_{ds1}: drain-to-source voltage of S_1. (b) i_{S2}: current flowing through S_2; v_{gs2} driving voltage of S_2; v_{ds2}: drain-to-source voltage of S_2. (c) i_{S3}: current flowing through S_3; v_{gs3} driving voltage of S_3; v_{ds3}: drain-to-source voltage of S_3. (d) Soft switching waveforms of S_1. (e) Soft switching waveforms of S_2. (f) Soft switching waveforms of S_3.

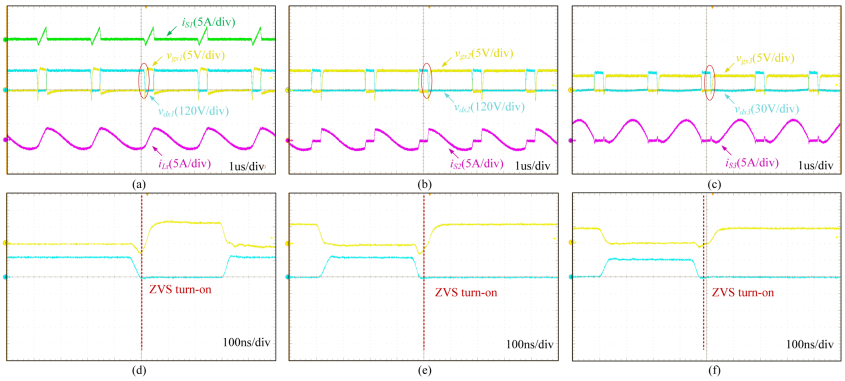

Fig. 16. Experimental waveforms of TSC converter under 440 V-input (120 V-input for TSC converter) conditions (The listed components correspond to the symbols in Fig. 2). (a) i_{S1}: current flowing through S_1; i_{Lr}: resonant current; v_{gs1} driving voltage of S_1; v_{ds1}: drain-to-source voltage of S_1. (b) i_{S2}: current flowing through S_2; v_{gs2} driving voltage of S_2; v_{ds2}: drain-to-source voltage of S_2. (c) i_{S3}: current flowing through S_3; v_{gs3} driving voltage of S_3; v_{ds3}: drain-to-source voltage of S_3. (d) Soft switching waveforms of S_1. (e) Soft switching waveforms of S_2. (f) Soft switching waveforms of S_3.

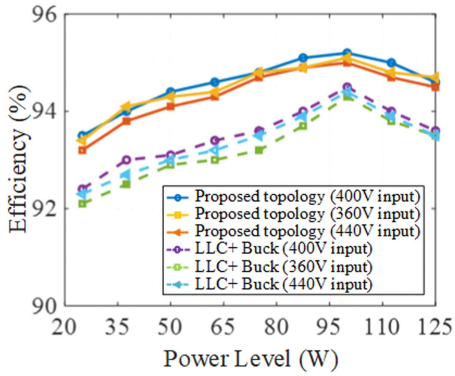

Fig. 17. Efficiency comparison of proposed topology and *LLC*+Buck converter.

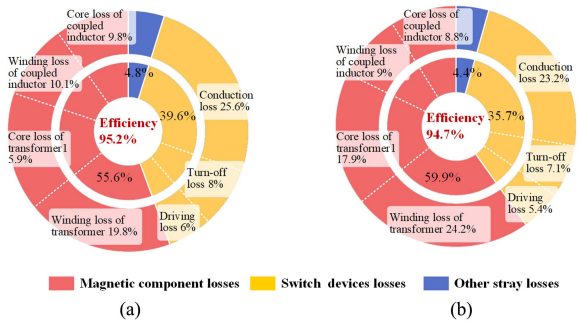

Fig. 18. Loss breakdown of prototypes with different matrix transformers. (a) Prototype based on proposed transformer winding connection structure. (b) Prototype based on conventional transformer winding connection structure.

working point is 0.7% higher than that of conventional topology. Within the wide input voltage range, the proposed topology always shows higher efficiency. The efficient operating range is greatly improved compared with other high conversion ratio converters [32], [33], [34].

The proposed topology is aiming for a "dc socket" for full dc building, where 400 Vdc or 375 Vdc are selected as the dc bus voltage across the whole building and 48 V, 12 V, and 5 V are typical load suppling voltage. In the future, 400 V to 1 V or even 0.7 V applications are necessary for XPU (CPU and GPU) power module, for higher conversion ratio condition, the stacked

the structure of the proposed converter, which use two or more proposed converter series in the input side and parallel in the output side can be further investigated.

The loss breakdown of the topology using the traditional transformer structure and the optimized transformer structure is compared, as shown in Fig. 18. The efficiency can be improved by 0.5%, and the loss of the matrix transformer is greatly reduced.

VI. Conclusion

A high conversion ratio (400 V–5 V) dc–dc converter with wide input voltage (360 V–440 V) based on TSC circuit is proposed. The operational principle and parameter design method of proposed topology especially TSC circuit are explained in detail. Meanwhile an optimal winding structure of matrix transformer is proposed. With the adoption of the TSC converter, all the semiconductor devices can operate in the soft switching condition. A prototype is built based on theoretical analysis, and the peak efficiency is 95.2% and the whole power range efficiency is above 93.2% with input voltage varying from 360 V to 440 V.

References

[1] P. Thummala, D. B. Yelaverthi, R. A. Zane, Z. Ouyang, and M. A. E. Andersen, "A 10-MHz GaNFET-based-isolated high step-down DC–DC converter: Design and magnetics investigation," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 3889–3900, Jul./Aug. 2019.

[2] C.-L. Wei, C.-H. Wu, L.-Y. Wu, and M.-H. Shih, "An integrated step-up/step-down DC–DC converter implemented with switched-capacitor circuits," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 10, pp. 813–817, Oct. 2010.

[3] T. Yao, Y. Guan, and W. Wang, "A high efficiency multi-module parallel RF inverter system for plasma induced hydrogen," *Protection Control Modern Power Syst.*, vol. 8, no. 1, pp. 152–162, 2023.

[4] Y. Li, X. Lyu, D. Cao, S. Jiang, and C. Nan, "A 98.55% efficiency switched-tank converter for data center application," *IEEE Trans. Ind. Appl.*, vol. 54, no. 6, pp. 6205–6222, Nov./Dec. 2018.

[5] S. Jiang, C. Nan, X. Li, C. Chung, and M. Yazdani, "Switched tank converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 81–90.

[6] R.-J. Wai and J.-J. Liaw, "High-efficiency coupled-inductor-based step-down converter," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4265–4279, Jun. 2016.

[7] X. Zhao, C.-S. Yeh, C.-W. Chen, and J.-S. Lai, "A comprehensive comparison of MHz GaN-based ZVS step-down converters for low power integrated on-chip applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 5271–5275.

[8] L. Zhu et al., "Buck-boost type high step-down low power modular converter for medium voltage DC systems," *IEEE Trans. Power Electron.*, vol. 38, no. 1, pp. 634–646, Jan. 2023.

[9] R. Guan et al., "A high step-down partial power processing switched-capacitor converter for wide input voltage range medium voltage DC applications," *IEEE Trans. Power Electron.*, vol. 38, no. 10, pp. 12265–12277, Oct. 2023.

[10] M. Kasper, D. Bortis, and J. W. Kolar, "Novel high voltage conversion ratio 'Rainstick' DC/DC converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 789–796.

[11] C. Chuang, C. Pan, and H. Cheng, "A novel transformer-less interleaved four-phase step-down DC converter with low switch voltage stress and automatic uniform current-sharing characteristics," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 406–417, Jan. 2016.

[12] S.-H. Kim, H. Cha, H. F. Ahmed, and H.-G. Kim, "Isolated double step-down DC-DC converter," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, 2015, pp. 2306–2311.

[13] C. Chuang, C. Pan, and H. Cheng, "A novel transformer-less interleaved four-phase step-down DC converter with low switch voltage stress and automatic uniform current-sharing characteristics," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 406–417, Jan. 2016.

[14] L. Junfeng, H. Renjun, and Z. Jun, "A non-isolated interleaved step-down DC-DC converter with high ratio," *Trans. China Electrotechnical Soc.*, vol. 33, no. 20, pp. 4763–4770, 2018.

[15] L. Wang, K. Sun, and R. Burgos, "Planar piezoelectric transformer-based high step-down voltage-ratio DC–DC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10833–10848, Sep. 2022.

[16] Y. Guan, P. Wang, M. Liu, D. Xu, and M. Chen, "MSP-LEGO: Modular series-parallel (MSP) architecture and LEGO building blocks for non-isolated high voltage conversion ratio hybrid DC-DC converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 143–150.

[17] C. Wei, Y. Zhao, Y. Zheng, L. Xie, and K. M. Smedley, "Analysis and design of a nonisolated high step-down converter with coupled inductor and ZVS operation," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 9007–9018, Sep. 2022.

[18] P. N. Truong, N. A. Dung, Y.-C. Liu, and H.-J. Chiu, "A nonisolated high step-down DC–DC converter with low voltage stress and zero voltage switching," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 3500–3512, Mar. 2023.

[19] M. Choi and D.-K. Jeong, "Design of high step-down ratio isolated three-level half-bridge DC–DC converter with balanced voltage on flying capacitor," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 10213–10225, Sep. 2022.

[20] Y. T. Yau, W. Z. Jiang, and K. I. Hwu, "Ultrahigh step-down converter with wide input voltage range based on topology exchange," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5341–5364, Jul. 2017.

[21] K. I. Hwu, W. Z. Jiang, and Y. T. Yau, "Ultrahigh step-down converter," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3262–3274, Jun. 2015.

[22] L. Zhang and S. Chakraborty, "An interleaved series-capacitor tapped buck converter for high step-down DC/DC application," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6565–6574, Jul. 2019.

[23] M. Ahmed, C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density 48/1V sigma converter voltage regulator module," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2017, pp. 2207–2212.

[24] M. H. Ahmed, F. C. Lee, and Q. Li, "Wide voltage range high-efficiency sigma converter 48V VRM with integrated magnetics," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 4701–4707.

[25] X. Xu, Y. Zhang, L. Zhu, H. Yu, Y. Zhang, and H. Wu, "A high step-down DC-DC converter with matrix-transformer and wide voltage gain for vehicle power supply applications," in *Proc. 22nd Int. Conf. Elect. Machines Syst.*, 2019, pp. 1–6.

[26] M. H. Ahmed, A. Nabih, F. C. Lee, and Q. Li, "Low-loss integrated inductor and transformer structure and in regulated LLC converter for 48-V bus converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 589–600, Mar. 2020.

[27] K. George and S. Ang, "Topology survey for GaN-based high voltage step-down single-input multi-output DC-DC converter systems," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl.*, 2016, pp. 340–343.

[28] C. Dong, W. Lei, and Z. Junjun, "Research of staggered parallel magnetic DC-DC converters based on improved average current control," *Power System Protection Control*, vol. 44, no. 24, pp. 58–65, 2016.

[29] W. Lin, X. Yuzhen, and Q. L. Zheng, "A high efficiency integrated step-down Cuk and flyback converter for LED power driver," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, 2015, pp. 60–64.

[30] M. Mu and F. C. Lee, "Design and optimization of a 380-12V high frequency, high-current LLC converter with GaN devices and planar matrix transformers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 854–862, Sep. 2016.

[31] S. Wang, H. Wu, F. C. Lee, and Q. Li, "Integrated matrix transformer with optimized PCB winding for high-efficiency high-power-density LLC resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 6621–6627.

[32] R. Guan et al., "A power self-balanced high step-down medium voltage DC converter with expandable soft-switching range," *IEEE Trans. Ind. Electron.*, vol. 71, no. 1, pp. 398–408, Jan. 2024.

[33] T. Jin, X. Yan, H. Li, J. Lin, Y. Weng, and Y. Zhang, "A new three-winding coupled inductor high step-up DC–DC converter integrating with switched-capacitor technique," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 14236–14248, Nov. 2023.

[34] Y. Wang, Z. Rong, Z. Sun, Y. Guan, S. Han, and D. Xu, "Analysis and implementation of a transformerless interleaved ZVS high-step-down DC-DC converter," *IEEE Trans. Power Electron.*, vol. 38, no. 11, pp. 13484–13495, Nov. 2023.

Tingting Yao (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2013, 2015, and 2023, respectively.

She is currently an Associate Professor with the College of Computer and Control Engineering, Northeast Forestry University, Harbin, China. Her research interests include the areas of high conversion ratio converters and high frequency resonant converters.

Mingfei Ban (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2011, 2013, and 2019, respectively.

He was a Visiting Ph.D. Student with the Illinois Institute of Technology, Chicago, IL, USA, in 2016 and 2017. He is currently an Associate Professor with the College of Computer and Control Engineering, Northeast Forestry University, Harbin, China. His research interests include economic-environmental dispatch, renewable energy, electric vehicles, and microgrids.

Yiqi Liu (Member, IEEE) received the Ph.D. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2016.

He was with the Northeast Forestry University, Harbin, China, in 2016, where he is currently a Professor. His current research interests include power electronics for renewable energy sources, multilevel converters, high-voltage direct-current transmission technology, dc microgrids, energy conversion, and wireless power transfer systems.