A DC Bus Oscillation Suppression Strategy Based on Series Voltage Compensator for Diode Rectifier

Ruidong Sun, *Graduate Student Member, IEEE*, Guohong Zeng, Wenzheng Xu, *Member, IEEE*, Zichao Zhang, Long Jing, Weige Zhang, and Xuezhi Wu, *Member, IEEE*

***Abstract*—Series compensation is an effective way to reduce the dc side passive filters of diode rectifier (DR), but the stability judgement of such series compensation system (SCS) by the impedance-ratio-based stability criteria is complicated, because this kind of system has many cascade forms and complex coupling interactions. This article proposes a stability analysis method for the SCS composed of DR and series voltage compensator, based on which an impedance optimization strategy is present to solve the instability problem. First, the simplified two-port small-signal model of SCS is established. The stability analysis is based on common characteristics of the system, which can fully reveal the dc bus oscillation mechanism combined with equivalent loop gain and the stable condition can be obtained for control system optimization. From the point of view of reshaping the impedance of series loop, a virtual-impedance-based control strategy with simple implementation is adopted to improve the system stability without affecting its dynamic performance, and the controller and parameters design are given considering the requirements of impedance optimization. An experimental prototype is established to validate the accuracy of stability analysis and the effectiveness of proposed control.**

***Index Terms*—DC bus oscillation, impedance optimization control, miniaturized passive filters, series compensation system (SCS) stability analysis, series voltage compensator (SVC).**

I. Introduction

DIODE rectifiers (DRs) are widely used in high-power applications, such as the aerospace, ships, and rail transit [1], [2], [3], which have the advantages over active rectifiers in efficiency, reliability, and power density because of simple structure, strong overload capacity, and low loss [4], [5]. The main drawback of DR is that dc side voltage ripple and grid current harmonics caused by rectification deteriorate the reliability of dc power supply and cannot meet the grid code [6], [7]. The most reliable and simplest method of meeting power supply standards is to use the high-capacity passive capacitors and inductors at dc output of DR. However, the passive filters are bulky and costly, and cause current total harmonic distortion (THDi) to increase dramatically during partial power operation [8], [9]. The large capacitors on dc bus will also raise the failure rate of power electronic systems and increase the difficulty of fault isolation under dc short [10], [11].

Active filters with power electronic circuits have been used as an alternative path to solve the issues caused by passive filters. A two-terminal active capacitor/inductor concept has been recently proposed in [11], [12], and [13]. The active filter consists of a small passive filter connected with an auxiliary circuit to achieve the same output characteristics as a large-capacity passive filter [11], and the apparent power and voltage of auxiliary circuit is significantly reduced [13]. This approaches retain the same convenience as passive filters without any external control signals and power supplies [12]. However, it is still necessary to use relatively large passive filters to reduce the capacity of power stage. An electronic inductor with harmonic suppression function is used to mitigate current harmonics in the same public grid [9], [14]. But the active circuit needs to carry full voltage and rated current and is not suitable for high-power applications.

To lower the voltage level and losses of active switches, a series type compensation circuit (electronic smoothing inductor) is inserted between DR output and dc bus to eliminate THDi and reduce dc capacitor current stress [15], [16]. However, the large capacitors are still needed to guarantee the dynamic behavior of dc voltage. The series voltage compensator (SVC) was proposed in [17] to eliminate the DR output voltage fluctuations by generating harmonic voltage. Thus, a stable dc bus voltage is obtained without capacitors. The discussions in [17] are confined to the case of no dc bus capacitors and verifies the feasibility of proposed voltage-current dual-loop (VCDL) control method. But it lacks a detailed analysis of system stability for most capacitive loads.

In [18] and [19], the stability of the series compensation system (SCS) consisting of source converter, load converter, and SVC was analyzed, and the impedance ratio of system was obtained by taking the load side bus as interfacing location. The system stability could be judged based on Middlebrook criterion. However, the impedance ratio in only one cascade mode was analyzed, which could not prove the whole system is stable. At present, the impedance-based methods are effective for stability assessment of multiconverters cascade systems [20], [21], [22]. But, the SCS has various cascade forms based on the different partition points. This means that all the impedance ratios at

Manuscript received 16 October 2023; revised 11 December 2023; accepted 22 January 2024. Date of publication 29 January 2024; date of current version 20 March 2024. This work was supported by the Delta Power Electronics Science and Education Development Program of Delta Group under Grant DREK2021005. Recommended for publication by Associate Editor M. Hartmann. *(Corresponding author: Guohong Zeng.)*

The authors are with the National Active Distribution Network Technology Research Center, Beijing Jiaotong University, Beijing 100044, China (e-mail: 20117025@bjtu.edu.cn; ghzeng@bjtu.edu.cn; xuwenzheng@bjtu.edu.cn; 20121537@bjtu.edu.cn; ljing@bjtu.edu.cn; wgzhang@bjtu.edu.cn; xzhwu@bjtu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2024.3359718.

Digital Object Identifier 10.1109/TPEL.2024.3359718

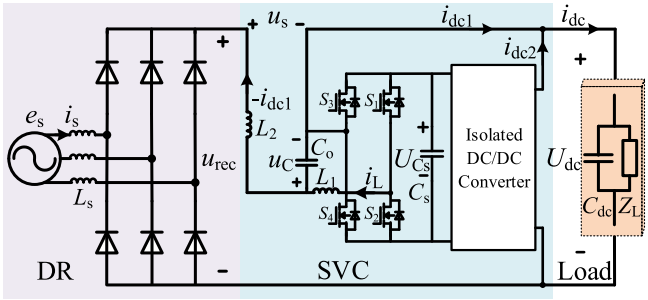

Fig. 1. Topology of DR with SVC.

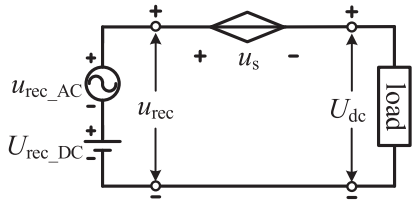

Fig. 2. Simplified circuit of the SCS.

different interfacing locations have to meet the forbidden-zone criteria to ensure SCS stability [23]. Meanwhile, the SCS is strongly coupled leading to difficulties in solving the converter impedance. Obviously, impedance-ratio-based stability criteria may not have the ability to judge stability very succinctly.

In order to solve this problem, Pan et al. [24] proposed a generic stability assessment methodology for the complex system, and the equivalent loop gain of the system is obtained based on a unified two-port small-signal model of the system. Then, the stability requirement of system is given by introducing the Nyquist criterion to the equivalent loop gain. On this basis, Mu et al. [25] clarified that the system equivalent loop gain and impedance-ratio type stability criterion at different interfacing locations, have the same stability results. However, the above stability criteria may not be able to visualize the factors affecting system stability, which does not provide guidance for solving the system stability problem.

Impedance is an intuitive and effective way for dynamic representation of power electronic devices [20]. The SVC replaces the bulky passive filter in the DR, unlike active capacitors/inductors in [11], [12], [13], [14], [15], and [16], its impedance characteristics cannot be equivalent to a fairly large-capacity passive filter. This may lead to system instability as the loop impedance characteristics of DR with conventional passive filters are changed [26]. Stability studies of cascaded systems have shown that the essential reason of system instability is that the system damping is reduced by the impedance of converter and causing dc bus oscillation [27], [28]. The virtual impedance control can improve the system stability at a very low cost, which is more promising [29]. Chen et al. [30] proposed an active damping control strategy and parameter design method to meet the diversified requirements of active damping configurations in a dc distribution system. However, active damping methods applied to SCS are rarely studied and the existing compensation controllers are complicated to design.

This article will study the stability of SCS composed of DR and SVC from the point of view of whole system, and the stability analysis methods in [24] and [25] are extended to SCS. The unified form, common transfer function, and equivalent loop gain of the SCS are derived, and this is used to analyze the dc bus oscillation mechanism. Furthermore, an impedance optimization based on voltage command compensation (IOVCC) control strategy with simple implementation and high parameter adaptability is presented to improve the SCS stability and have little impact on the dynamic performance of the system.

The rest of this article is organized as follows. The operating principle and design criteria of component sizing of SCS is presented in Section II. And the stability and dc bus oscillation mechanism of SCS with VCDL control are analysed and the oscillation suppression method is given in Section III. On this basis, Section IV gives the optimization process of SVC output impedance and the implementation of IOVCC control to improve system performance. Finally, Section V demonstrates the experimental verifications on a 2 kW prototype. Finally, Section VI concludes this article.

II. Operation and Component Sizing of the DR With SVC System

A. Topology and Operation Principle

The topology of the proposed DR with a SVC for dc filtering is shown in Fig. 1, where e_s and i_s are DR input voltage and current, respectively. The output pulsating voltage u_{rec} is generated by DR rectification. U_{dc} is the dc bus voltage. The SVC, which is a full-bridge converter with isolated power supply, is connected between DR and bus load to compensate the ripple voltage in u_{rec} by the output voltage u_s. Thus, the U_{dc} is equal to the average value of u_{rec}. A bidirectional isolated dc–dc converter is connected to dc bus to provide stable intermediate voltage U_{Cs} and electrical isolation. According to the series relationship, the i_{dc1} flowing through the SVC output terminals is both the output current of DR, and the load current i_{dc} is supplied by i_{dc1} and SVC input current i_{dc2}.

To facilitate the analysis of SCS's operating principle, the following assumptions are made.

1) The DR output current i_{dc1} is continuous.
2) The three-phase grid voltage is balanced, where phase voltage $e_{sa} = E_p \sin(\omega t)$, E_p is the amplitude of e_{sa}, $\omega = 2\pi f_o$ is fundamental angular frequenc, and f_o is fundamental frequency.
3) The influence of grid filter inductor L_s on the DR commutation process is ignored.

The simplified circuit of SCS is shown in Fig. 2. It can be seen that the DR, SVC, and load form a series loop.

According to [14], the DR output voltage u_{rec} can be expressed as

$$u_{rec} = \frac{3\sqrt{3}}{\pi} E_p \left[1 - \sum_{n=1,2,3,\cdots}^{\infty} \frac{2}{36n^2 - 1} \cos\left(6n\omega t - n\pi\right) \right]. \tag{1}$$

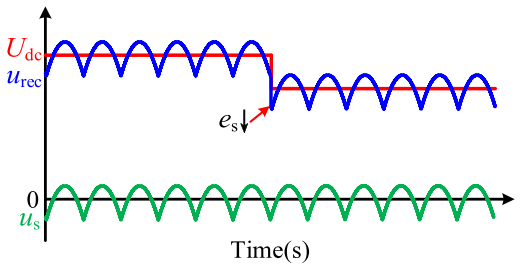

Fig. 3. Waveforms of system voltage during continuous operation.

The dc and ac components of u_{rec} can be calculated separately as follows:

$$U_{rec\_dc} = \frac{3\sqrt{3}}{\pi} E_p \tag{2}$$

$$u_{rec\_ac} = -\frac{3\sqrt{3}}{\pi} E_p \left[\sum_{n=1,2,3,\cdots}^{\infty} \frac{2}{36n^2-1} \cos(6n\omega t - n\pi) \right]. \tag{3}$$

The output voltage of the DR contains significant 6*n*th harmonics. Normally, the bus voltage of the dc power supply system is allowed to stabilize within a certain range as the grid voltage varies [16]. Therefore, the SVC handles only the ac component u_{rec_ac} in u_{rec}, implying a low VA rating, and a smooth U_{dc} is obtained instead of large-capacity passive filters. The u_s should be controlled as

$$u_s = u_{rec} - U_{rec\_dc}. \tag{4}$$

The main waveforms are shown in Fig. 3. The U_{dc} varies with e_s, and the u_s is pure ac voltage within allowed range of dc voltage. If its losses are neglected, the SVC is also a pure energy storage element compared to passive filters.

B. Design Criteria for System Component Sizing

System component sizing is presented considering the functionality, efficiency, and power density, which provide the basis for system stability analysis. Design guidelines for components in SVC, DR, and bus load are given, respectively.

1) Component Sizing for the SVC: First, the voltage and current stress on active devices of power stage are calculated. According to (2) and (3), the minimum value of U_{Cs} is $(3\sqrt{3}/\pi - 3/2)E_p \approx 0.093U_{dc}$ for controllability. Considering an adequate voltage margin in practice, the U_{Cs} is set typically to about 10%∼15% of U_{dc}. u_s has to be generated as the local pulse average value within the switching period $T = 1/f_s$ (switching frequency) by PWM using the duty ratio $d \in (0\sim1)$

$$u_s = dU_{Cs} - (1-d)U_{Cs}. \tag{5}$$

Combining (3) and (5) gives the relative turn-ON time of the transistors S_1, S_4

$$d(\varphi_N) = \frac{1}{2} + \frac{\sqrt{3}E_p}{2U_{Cs}} \left(\cos\varphi N - \frac{3}{\pi} \right) \varphi_N \in \left(-\frac{\pi}{6} \sim \frac{\pi}{6} \right) \tag{6}$$

which are required as weighting function for the calculation of average and rms values of the S_1, S_4 current

$$I_{S1S4,avg} = \frac{3}{\pi} \int_{-\pi/6}^{\pi/6} i_{dc1} \cdot d(\varphi_N) d\varphi_N = \frac{1}{2} i_{dc1} \tag{7}$$

$$I_{S1S4,rms} = \sqrt{\frac{3}{\pi} \int_{-\pi/6}^{\pi/6} {i_{dc1}}^2 \cdot d(\varphi_N) d\varphi_N} = \frac{1}{\sqrt{2}} i_{dc1}. \tag{8}$$

Due to pure ac characteristic of u_s, the average duty ratio is equal to 1/2. As a result, the current stress of S_1–S_4 are same.

Ideally, the SVC does not handle active power transfer (i.e., $i_{dc2} = 0$), so the capacity design of front-end dc–dc converter only needs to consider the SVC losses. The processed apparent power ratio of the compensator S_{SVC} to the main system S_{DR} can be derived as

$$\frac{S_{SVC}}{S_{DR}} = \frac{u_{s\_rms} \cdot i_{dc1}}{u_{rec\_rms} \cdot i_{dc1}} = \frac{\sqrt{\frac{3}{\pi} \int_{-\pi/6}^{\pi/6} {u_s(\varphi_N)}^2 d_{\varphi N}}}{\sqrt{\frac{3}{\pi} \int_{-\pi/6}^{\pi/6} \left[u_s(\varphi_N) + \frac{3\sqrt{3}}{\pi} \right]^2 d_{\varphi N}}}$$

$$\approx 4.2\% \tag{9}$$

where u_{s_rms} and u_{rec_rms} are the rms values of SVC and DR output voltages, respectively. The S_{SVC}/S_{DR} is independent of system power level and network voltage level by only 4.2%. Furthermore, due to the reduced voltage level, the SVC can be implemented with low-voltage high-current MOSFETS, and the $f_s \geq 100$ kHz, which allows the filters to be selected relatively small. While the low-voltage power semiconductors have lower on-state resistance, resulting in lower losses, which facilitates the realization of high power density rectifiers.

The capacitance of intermediate capacitor C_s has impact on the operation of SVC. The current of C_s can be obtained from

$$i_{Cs}(t) = \frac{u_{rec\_AC}(t)}{U_{Cs}} i_{dc1} \tag{10}$$

$$i_{dc1} = \frac{P_L}{U_{rec\_DC}} = \frac{P_L \cdot \pi}{3\sqrt{3} \cdot E_p} \tag{11}$$

where P_L is the power of DR system, to determine the value of C_s in terms of sixth-harmonic current. The voltage ripple across C_s is derived as

$$v_{Cs}(t) = \frac{1}{C_s} \int i_{Cs}(t) dt = \frac{P_L}{105\omega C_s U_{Cs}} \sin(6\omega t). \tag{12}$$

The peak voltage is

$$\Delta U_{Cs} = \frac{P_L}{105\omega C_s U_{Cs}}. \tag{13}$$

The design requires that $\Delta U_{Cs} \leq \gamma_v U_{Cs}$ (γ_v is the voltage ripple ratio). So the value of C_s should satisfy

$$C_s \geq \frac{P_L}{105\gamma_v \omega {U_{Cs}}^2}. \tag{14}$$

The full-bridge converter output *LCL* filter can be designed according to conventional procedure [31].

2) Input Inductor L_s: The increase of L_s is beneficial to reduce harmonic pollution to the grid and mitigate the adverse effects of both harmonic and unbalanced voltage on DR. But

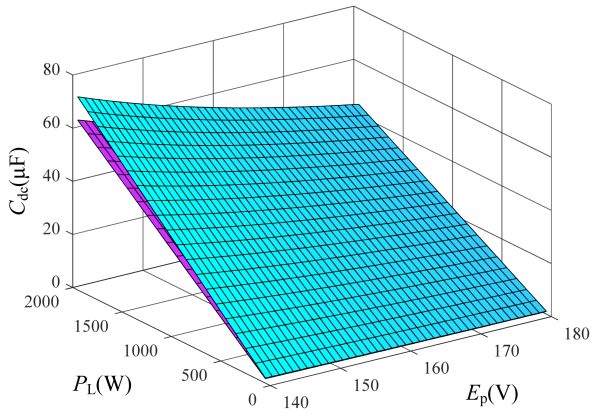

Fig. 4. Component sizing constraints of C_{dc}.

L_s affects the commutation process of DR to produce a non-negligible overlap angle, resulting in a voltage drop ΔU_{rec}

$$\Delta U_{rec} = \frac{3}{\pi} X_B \cdot i_{dc1} \tag{15}$$

where $X_B = \omega L_s$. The SVC needs to compensate for ΔU_{rec}, which generates active power transfer. Due to the small capacity of dc–dc converter, $\Delta U_{rec}/U_{dc}$ is limited to not exceed the overlap voltage drop factor α_v. The value of L_s should satisfy

$$L_s \le \frac{9\alpha_v {E_p}^2}{\omega \pi P_L}. \tag{16}$$

3) DC Bus Capacitor C_{dc}: The main purpose of SVC is to significantly lower the DR output capacitors. As a result of the limitation of control bandwidth, the SVC has poor ability to offset harmonic voltages above 18th order. For the higher harmonics suppression, the *LC* filter is still needed, which is composed of loop equivalent inductor $L_{eq} = 2L_s$ and C_{dc}, its cut-off frequency f_{LC} does not exceed $24f_o$. Therefore, the value of C_{dc} should satisfy

$$C_{dc} \ge \frac{1}{(24 \cdot 2\pi f_o)^2 L_{eq}}. \tag{17}$$

Also consider the dynamic response capability of rectifier, when the load power suddenly changes 50% of rated power, the dc bus voltage fluctuation ΔU_{dc} should be less than $\lambda_v U_{dc}$ (λ_v is the voltage fluctuation ratio). Based on the experience that the current loop response time is approximated by $10T_{eq}$, where T_{eq} is calculation period, assuming that the transient process is powered by C_{dc}. The value of C_{dc} also should satisfy

$$C_{dc} \ge \frac{5\pi^2 P_L T_{eq}}{54\lambda_v {E_q}^2}. \tag{18}$$

Fig. 4 shows the two constraint surfaces of size C_{dc}, with the minimum value of C_{dc} being dependent on P_L and E_p. The size of dc bus capacitors has been significantly reduced compared to conventional high-capacity electrolytic capacitors.

According to the above design criteria of component sizing, the design case of 2 kW prototype is given. The numerical results given in figures are based on the case with specifications described in Table I.

TABLE I
SPECIFICATIONS AND PARAMETERS OF THE DR WITH A SVC

	Parameters	Values
system	Source voltage $e_{s(rms)}$	110 V
	fundamental frequency f_o	50 Hz
	Dc bus voltage U_{dc}	256 V
	Power rating P_L	2000 W
	Overlap voltage drop ratio α_v	1%
	Voltage fluctuation ratio λ_v	5%
DR	Input inductor L_s	300 μH
	Dc bus capacitor C_{dc}	100 μF
	Rated load resistance R_L	33 Ω
SVC	Switching frequency f_s	100 kHz
	Intermediate dc voltage U_{Cs}	35 V
	Filter inductors L_1	80 μH
	Filter capacitor C_o	5.6 μF
	Filter inductors L_2	15 μH
	Voltage ripple ratio γ_v	2%
	Intermediate dc capacitor C_s	1 mF
DCX-LLC	Switching frequency	200 kHz
	Turns-ratio of LLC N	7:2
	Resonant inductor L_r	4.3 μH
	Resonant capacitor C_r	150 nF

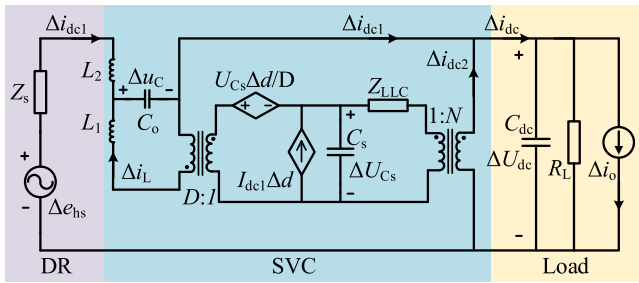

Fig. 5. Small-signal model of the SCS.

III. ANALYSIS OF SYSTEM STABILITY AND DC BUS OSCILLATION MECHANISM

A. Modeling and Stability Analysis for the SCS

The SCS could be modeled with three functional blocks: The DR can be equated to a Thevenin circuit with harmonic voltage source $e_{hs} = u_{rec\_ac}$ in series with line impedance $Z_s = 2sL_s$ [16], [32]. To simplify the stability analysis, the Z_L is resistive load R_L, which is in parallel with the dc bus capacitor C_{dc} as the dc bus equivalent load Z_{dc}, so $Z_{dc} = 1/(sC_{dc}+1/R_L)$. In the given case, a DCX-*LLC* resonant converter is used as front-end of SVC, and the SVC can take generic small-signal model [33]. The small-signal model of the SCS based on combination of these three blocks is shown in Fig. 5, where Δi_o is load current disturbance, U_{Cs} and I_{dc1} are steady-state values, D is average duty cycle, N is *LLC* turns-ratio, and Z_{LLC} is *LLC* equivalent impedance.

In order to effectively suppress the voltage harmonics of u_{rec}, the SVC adopts VCDL control to modulate the voltage u_C of filter capacitor C_o and the current i_L of filter inductor $L1$ [17]. From the point of view of whole system, using Δe_{hs} and Δi_o as input variables of system and ΔU_{dc} and Δi_{dc1} as the output variables, the small-signal control diagram of SCS is obtained, as shown in Fig. 6, where u_{ref} is the reference value of u_c, which

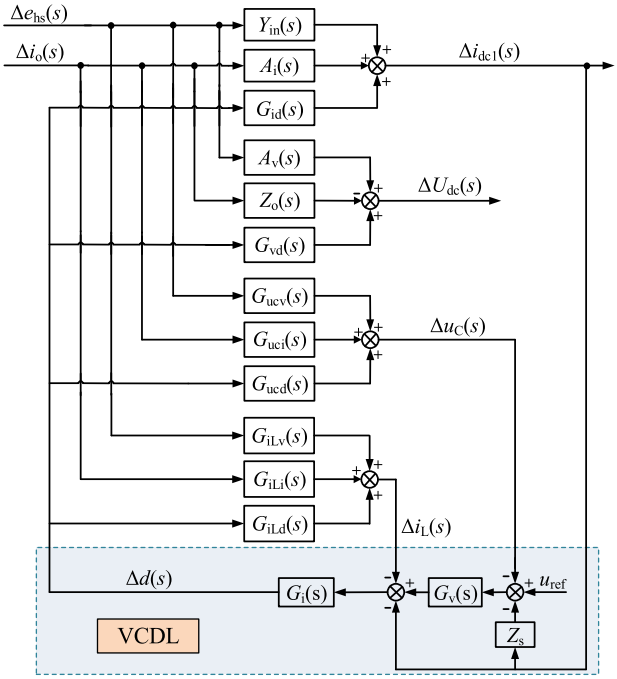

Fig. 6. Small-signal control block diagram of SCS with VCDL control.

TABLE II
PARAMETERS OF THE VCDL CONTROL OF SVC

Parameter	Value	Parameter	Value
k_{vp}	0.25	k_{r_1}	300
G_i	0.07	k_{r_2}	200
T_{eq}	40 μs	k_{r_3}	100

varies with e_s and is equal to u_{rec}-U_{rec_dc}. The G_v is voltage regulator, and the G_i is current regulator. Since the u_{ref} contains 6nth ac components, the G_v adopts proportional quasi-resonant controller to improve harmonic compensation. The G_v can be expressed as

$$G_v(s) = k_{vp} + \sum_{n=1,2,3} \frac{k_{r\_n} \cdot 2\omega_c s}{s^2 + 2\omega_c s + (6n\omega)^2} \tag{19}$$

where k_{vp} and k_{r_n} are gains of proportional and quasi-resonant links, respectively, and ω_c is bandwidth at resonant frequencies. The G_i adopts proportional controller. As i_L approximately equals -i_{dc1}, it follows that the load current feedforward is introduced to improve dynamic performance [34].

The parameters of G_v and G_i are designed to ensure that the SVC is independently stable. According to the controller design principle proposed in [34], a set of controller parameters that satisfy the design requirements is shown in Table II.

Furthermore, the expressions of open-loop transfer functions of the system can be all derived as shown in the Appendix with the small-signal model. It can be seen that these expressions are very complex and are not easy to analyze the system stability. Due to the coupling between front-end and downstream stages

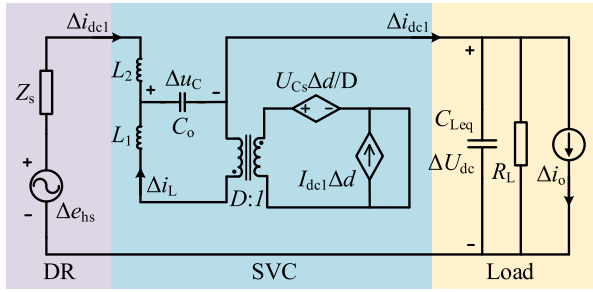

Fig. 7. Simplified small-signal model of the SCS.

of SVC and the large number of passive components, the small-signal model is complicated and the system order is high. So, to better characterize the system, the SVC is simplified as follows.

1) Considering C_s is large enough that the input voltage disturbance of downstream converter can is neglected, i.e., $\Delta U_{Cs} = 0$.
2) Considering the SVC hardly transmits active power, the load current disturbance is neglected for front-end converter.
3) Considering resonant inductor L_r is small enough in DCX-*LLC*, its output impedance Z_{LLC} is neglected [33].

The simplified small-signal model of whole system is shown in Fig. 7. The C_s is converted to dc bus to obtain the dc bus equivalent capacitor $C_{Leq} = C_{dc} + C_s/N^2$ and $Z_{dc} = 1/(sC_{Leq} + 1/R_L)$. The simplified expressions of open-loop transfer functions are then obtained as in Appendix. Furthermore, the simulation and comparison results in the Appendix verify the accuracy of the simplified model.

On this basis, the stability of SCS with VCDL control is analyzed in detail. The equivalent loop gain T_{VCDL} of SCS with VCDL control is established from Fig. 6 with the expression [35]

$$\begin{aligned} T_{VCDL} &= \frac{G_v G_i G_{ucd}}{G_i(G_{iLd} + G_{id} + G_v G_{id} Z_s) + 1} \\ &= \frac{G_v G_i U_{Cs} Z_{Co}(Z_{L2} + Z_s + Z_{dc})}{Z_{L1} Z_{Co} + (Z_{L1} + Z_{Co} + G_i U_{Cs})(Z_{L2} + Z_s + Z_{dc}) - G_v G_i U_{Cs} Z_{Co} Z_s} \end{aligned} \tag{20}$$

where $Z_{L1} = sL_1$, $Z_{L2} = sL_2$, $Z_{Co} = 1/(sC_o)$.

According to open-loop frequency-domain stability margin requirement, the phase margin of the frequency characteristic curve of T_{VCDL} is greater than 0° to ensure SCS stability, which is a sufficient condition for system stability.

On the other hand, in order to intuitively show the effect of system parameters on stability, the two-port small-signal model of the SCS obtained by integrating Fig. 6 is shown in Fig. 8, so the expressions of the four input-to-output transfer functions of the system can be derived as follows:

$$\begin{aligned} &Y_{in\_VCDL} \\ &= \frac{Y_{in} + G_i Y_{in}(G_{iLd} + G_v G_{ucd}) - G_i G_{id}(G_{iLv} + G_v G_{ucv})}{G_i(G_{iLd} + G_{id} + G_v G_{ucd} + G_v G_{id} Z_s) + 1} \end{aligned} \tag{21}$$

T_{ii_VCDL}

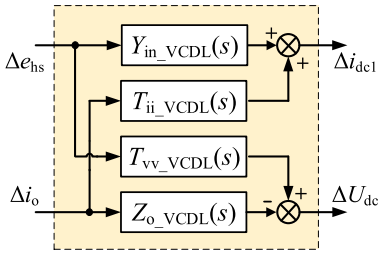

Fig. 8. Two-port small-signal model of the standard form of SCS.

$$= \frac{A_i + G_i A_i \left(G_{iLd} + G_v G_{ucd}\right) - G_i G_{id} \left(G_{iLi} + G_v G_{uci}\right)}{G_i \left(G_{iLd} + G_{id} + G_v G_{ucd} + G_v G_{id} Z_s\right) + 1} \tag{22}$$

$$T_{vv\_VCDL} = \frac{\begin{array}{l} A_v + G_i A_v \left[G_{iLd} + G_{id} + G_v (G_{ucd} + G_{id} Z_s)\right] \\ -G_i G_{vd} \left[G_{iLv} + Y_{in} + G_v (G_{ucv} + Y_{in} Z_s)\right] \end{array}}{G_i (G_{iLd} + G_{id} + G_v G_{ucd} + G_v G_{id} Z_s) + 1} \tag{23}$$

$$Z_{o\_VCDL} = \frac{\begin{array}{l} Z_o + G_i \left[\begin{array}{l} G_{vd}(A_i + G_{iLi}) + Z_o (G_{iLd} + G_{id}) + G_v \cdot \\ (G_{uci} G_{vd} + G_{ucd} Z_o + Z_s A_i G_{vd} + Z_s Z_o G_{id}) \end{array}\right] \end{array}}{G_i \left(G_{iLd} + G_{id} + G_v G_{ucd} + G_v G_{id} Z_s\right) + 1} \tag{24}$$

$$T_{m\_VCDL} = \frac{1}{G_i \left(G_{iLd} + G_{id} + G_v G_{ucd} + G_v G_{id} Z_s\right) + 1} \tag{25}$$

where Y_{in_VCDL} and Z_{o_VCDL} are the input admittance and output impedance of SCS, respectively, T_{ii_VCDL} and T_{vv_VCDL} are the current and voltage gain of SCS, separately. Then, the stability condition of the SCS can be obtained. If the SVC is stable when operating independently. According to the Nyquist criterion, the basic stability requirement for the SCS is that there are no right-half-plane (RHP) poles in the above input-to-output transfer functions (21)–(24). Consequently, there are no RHP poles in the common part T_{m_VCDL} is the sufficient and necessary condition for the stability of the SCS.

Using the equivalent loop gain T_{VCDL}, the system stability can be determined from the frequency-domain. The effect of parameters variation on system stability can be clearly obtained by utilizing the zero-pole distribution of T_{m_VCDL}. Comparing T_{VCDL} and T_{m_VCDL}, it can be found that the denominators of $1/(1+T_{VCDL})$ and T_{m_VCDL} are the same, in other words, they have the same poles. Therefore, the two approaches can be used to justify the stability of SCS and they have identical results.

It is important to note that the system remains stable and has sufficient harmonic suppression to ensure that the dc bus voltage is stabilized. When the system is stable, T_{vv_VCDL} can be used to measure the harmonic suppression capability of the system, and to ensure that the dc bus voltage ripple does not exceed $\pm 1\%$, T_{vv_VCDL} should satisfy

$$|T_{vv\_VCDL}(jk\omega)| \le \frac{1\%}{e_{hs\_k}} \tag{26}$$

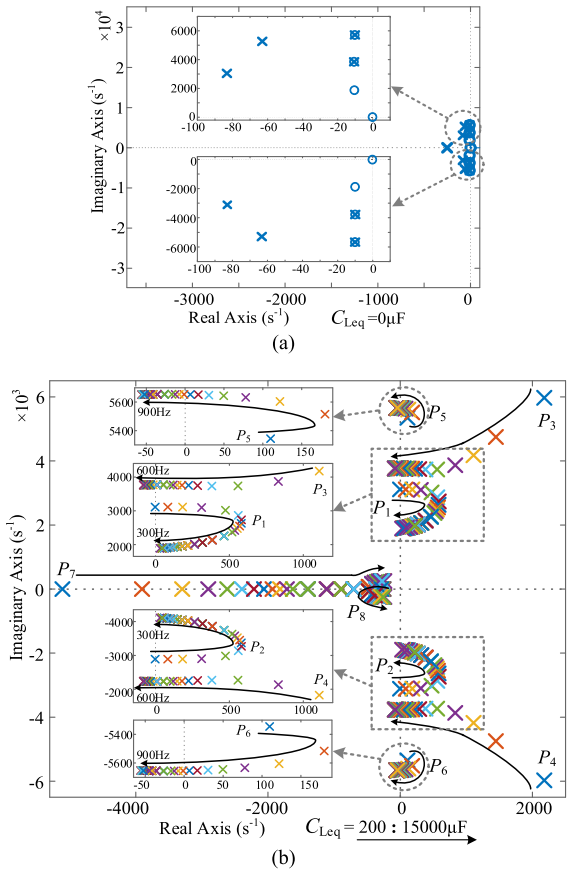

Fig. 9. Zero-pole distribution of the common transfer function T_{m_VCDL} with or without C_{Leq}. (a) $C_{Leq} = 0$ μF. (b) With increasing $C_{Leq} = 200{:}15000$ μF.

where e_{hs_k} indicates the kth harmonic percentage of e_{hs} in continuous mode.

B. Mechanism of the DC Bus Oscillation With VCDL Control

Existing studies have demonstrated that SVC with VCDL control can ensure stable operation of SCS when there are no dc bus capacitors [17]. However, based on the design criteria in Section II-B, the dc bus needs to be connected in parallel with capacitors to ensure the quality of power supply, which may affect system stability. Therefore, the effect of C_{Leq} on the stability of SCS is studied. Fig. 9 illustrates the zero-pole distribution of T_{m_VCDL} with or without the C_{Leq} on dc bus. When $C_{Leq} = 0$ μF, T_{m_VCDL} has no RHP poles, which indicates that the system is stable. When there are capacitors on dc bus, T_{m_VCDL} has three pairs of RHP conjugate poles (P_1–P_6), which means the system is unstable. As C_{Leq} increases, the RHP poles gradually approach the stable region, and the oscillation frequencies of P_1-P_2 tend to 300 Hz, that of P_3-P_4 tend to 600 Hz, and that of P_5-P_6 tend to 900 Hz, respectively, corresponding to the three resonant frequencies in G_v. Thus, it is considered that the quasi-resonant links cause the system instability.

Choosing $C_{Leq} = 200$ μF, the influence of quasi-resonant links in G_v on the system stability is analyzed. Fig. 10 presents

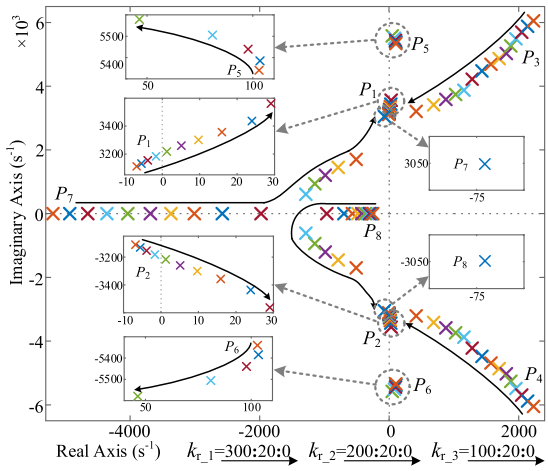

Fig. 10. Zero-pole distribution of the common transfer function $T_{\mathrm{m\_VCDL}}$ varying with $k_{\mathrm{r\_n}}$, $k_{\mathrm{r\_1}} = 300{:}20{:}0$, $k_{\mathrm{r\_2}} = 200{:}20{:}0$, $k_{\mathrm{r\_3}} = 100{:}20{:}0$.

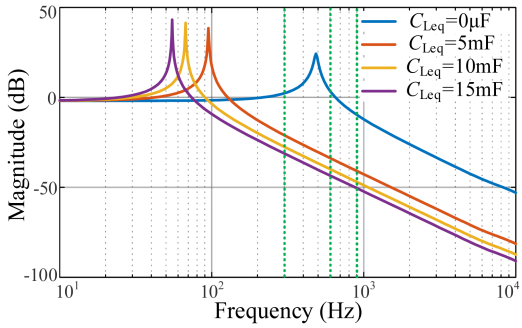

Fig. 11. Magnitude-frequency curves of $T_{\mathrm{vv\_VCDL}}$ with no quasi-resonant links in G_{v}.

the zero-pole distribution of $T_{\mathrm{m\_VCDL}}$ varying with the gains of quasi-resonant links ($k_{\mathrm{r\_n}}$, n = 1,2,3). From this, the following conclusions can be drawn.

1) As $k_{\mathrm{r\_n}}$ decreases, P_3–P_6 move closer to the stable region, while P_1-P_2 move towards the unstable region.
2) When $k_{\mathrm{r\_3}} = 0$, P_5-P_6 will not exist, when $k_{\mathrm{r\_3}} = 0$ and $k_{\mathrm{r\_2}} = 0$, P_1-P_2 will not exist, and when $k_{\mathrm{r\_3}} = 0$, $k_{\mathrm{r\_2}} = 0$ and $k_{\mathrm{r\_1}} = 0$, P_3-P_4 will not exist.
3) When there are no quasi-resonant links in G_{v}, the system can be stable.

Fig. 11 shows the magnitude-frequency curves of $T_{\mathrm{vv\_VCDL}}$ when there are no quasi-resonant links in G_{v}. Obviously, the SCS loses its harmonic compensation capability, analogous to the traditional DR, which suppresses 6nth harmonics by adding capacitors. However, this goes against the design goal of utilizing SVC to reduce passive filters.

From the above analysis, there is a contradiction between the stability and the harmonic suppression capability of SCS with

VCDL control. When both C_{Leq} and quasi-resonant links exist, the SCS is unstable, which will cause the dc bus oscillation and jeopardize the dc power supply system. But, according to the system operation principle, the dc bus capacitors and quasi-resonant links are indispensable. Therefore, the effect of

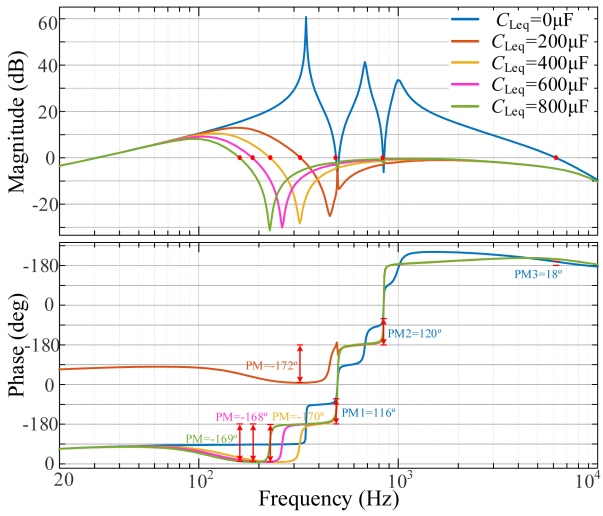

Fig. 12. Bode diagrams of T_{VCDL} varying with C_{Leq}.

the interaction of the dc bus capacitors and the quasi-resonant links on system stability needs to be further investigated to reveal the dc bus oscillation mechanism.

The open-loop frequency characteristics are used to infer the reasons affecting the system stability. Fig. 12 shows the bode diagrams of T_{VCDL} varying with C_{Leq}. It can be seen that when $C_{\mathrm{Leq}} = 0$ μF, i.e., Z_{dc} is resistive load, the phase margin of the system can meet the stability requirements (PM1–PM3>0), and the SCS is stable. When $C_{\mathrm{Leq}} \neq 0$ μF, i.e., Z_{dc} is a RC load, the phase margin cannot meet the stability requirements, and then the SCS is unstable.

Compare and analyze the expression (20) and bode diagrams of T_{VCDL}, where $Z_{\mathrm{L2}}+Z_{\mathrm{s}}+Z_{\mathrm{dc}}$ indicates the series loop impedance formed by L_2+L_{eq} and Z_{dc}. When there are capacitors in Z_{dc}, L_2+L_{eq}, and C_{Leq} will generate series resonance. According to design criteria of C_{dc}, the series resonance frequency does not exceed 1000 Hz, which will interact with the quasi-resonance frequencies in G_{v}.

From Fig. 12, it can be seen that the series resonance causes the frequency characteristic of T_{VCDL} to change significantly, and the common effect of the series impedance resonance and the quasi-resonant links in G_{v} results in phase margin of system not meeting the requirements. Also, the impedance resonance frequency decreases and moves away from the quasi-resonance frequencies as C_{Leq} increases, which will reduce the influence of series resonance on G_{v} and make the system tend to be stable. This is consistent with the conclusion in Fig. 9(b).

Combined with the analysis results of two stability criteria, the dc bus capacitors will resonate in series with the loop inductors, which will change the effect of the quasi-resonant links on stability, resulting in system instability. So, the dc bus oscillation is caused by the interaction of series impedance resonance and quasi-resonant links.

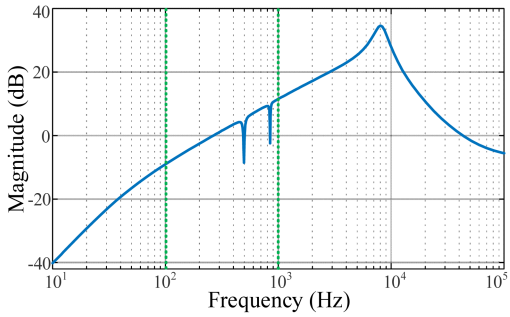

Fig. 13. Magnitude-frequency curve of Z_{o_SVC} under the Δi_o perturbation.

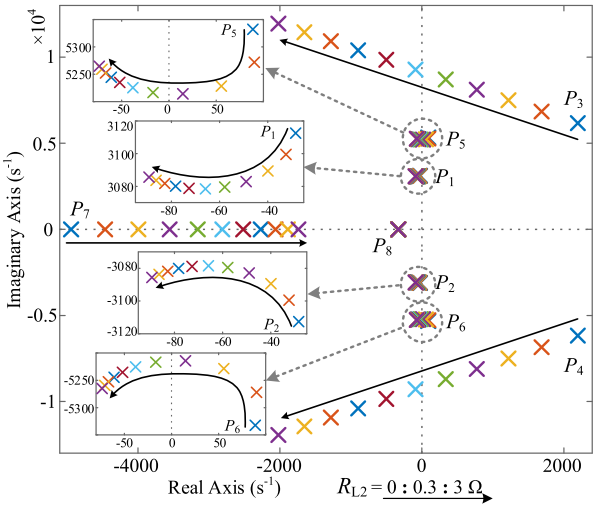

Fig. 14. Zero-pole distribution of T_{m_VCDL} varying with R_{L2}, $R_{L2}=0{:}0.3{:}3$.

C. Method for DC Bus Oscillation Suppression

The quasi-resonant links in G_v ensures sufficient harmonic suppression capability of the system. To avoid the interaction of series impedance resonance with G_v, it is necessary to reduce the series resonance effect. The equivalent output impedance of SVC with VCDL control is Z_{o_SVC}, the expression considering the Δi_o perturbation is as follows:

$$Z_{o\_SVC}=\frac{Z_{Co}\left(Z_{L1}-G_vG_iU_{Cs}Z_s\right)}{G_vG_iU_{Cs}Z_{Co}+G_iU_{Cs}+Z_{Co}+Z_{L1}}. \tag{27}$$

Fig. 13 shows the magnitude-frequency curves of Z_{o_SVC}, we can see that in series impedance resonance range (100–1000 Hz), the Z_{o_SVC} can be approximated as equivalent to a 600 μH inductor. However, this is not enough to suppress the series impedance resonance jeopardizing the system stability. By adding loop inductors and capacitors, it is possible to reduce the resonance frequency away from quasi-resonance frequencies and ensure system stability. But this requires the considerable capacity of passive components and loses the significance of series voltage compensation.

On the other hand, the system stability can also be improved by increasing the series loop damping to weaken the impedance resonance effect. Fig. 14 illustrates the effect of increasing the loop resistance R_{L2} (the series resistance of L_2) on the zero-pole distribution of T_{m_VCDL}. It is observed that increasing the series loop damping can bring RHP poles into the stable region and ensure the stable operation of the system.

However, the passive damping method brings additional losses and also affects the dynamic performance of the system. Therefore, an active damping method is considered to increase the loop impedance through optimal control, and the effect of series impedance resonance on stability is effectively improved without worsening system dynamic performance.

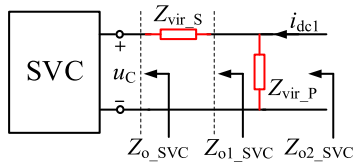

Fig. 15. Structure of the optimized SVC output impedance.

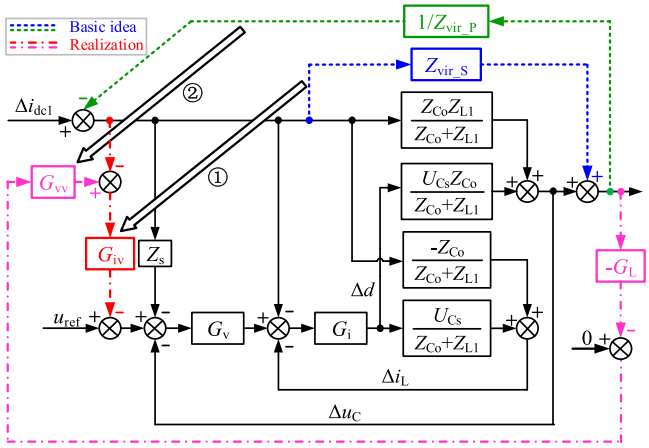

Fig. 16. Concept of IOVCC control strategy.

IV. Impedance Optimization Based on Voltage Command Compensation Control Strategy

By optimizing the output impedance of SVC, the series loop impedance characteristics can be improved. The IOVCC control strategy ensures the system stability by introducing a series-virtual-impedance Z_{vir_S}, and enhances system dynamic performance by introducing a parallel-virtual-impedance Z_{vir_p}. The optimized SVC output impedance structure is shown in Fig. 15.

Using the state variable feedback method [34], the virtual impedance is realized by equivalent transformation based on the small-signal control diagram (see Fig. 6) with VCDL control [36], [37]. Fig. 16 presents the implementation of the IOVCC control strategy, the dash line section shows an intuitive method of introducing Z_{vir_S} between the output current and voltage, and $1/Z_{vir\_P}$ between the output voltage and current. However, this method cannot be achieved by control directly. To make the same goal, the output of Z_{vir_S} is moved to the voltage reference and adjusting the transfer function to G_{iv}, futher moving the output

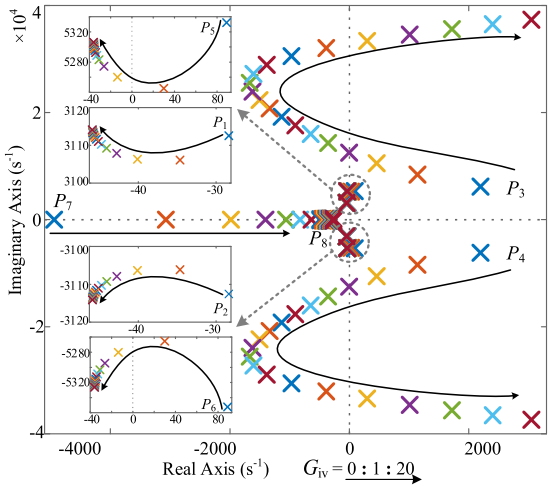

Fig. 17. Zero-pole distribution of T_{m_1} varying with G_{iv}, G_{iv} = 0:1:20.

of $1/Z_{vir\_P}$ to the input side of G_{iv} and adjusting the transfer function to $G_L G_{vv}$, as shown in the dot-dashed line section.

A. Implementation and Parameters Design of the Z_{vir_S}

In order to ensure the stable operation of the SCS, the output of SVC is connected in series with Z_{vir_S} to increase the series loop active damping, which can effectively suppress the series impedance resonance. According to the Fig. 16, the transfer function G_{iv} obtained by the equivalent transformation of Z_{vir_S} is expressed as

$$G_{iv} = (1 + G_{iv\_c})\, Z_{vir\_S}$$
$$G_{iv\_c} = \frac{G_i U_{Cs} + Z_{Co} + Z_{L1}}{G_v G_i U_{Cs} Z_{Co}}. \tag{28}$$

According to the dc bus oscillation suppression method, the introduced Z_{vir_S} can be set as a resistor. The derived expression for G_{iv} is too complex to implement. To ensure system stability, the Z_{vir_S} needs to be resistive at least in the series impedance resonance range (100–1000 Hz). The magnitude-frequency curve of G_{iv_c} in the above equation is shown in the Appendix. The $(1+G_{iv\_c})$ can be approximated as 1 in the 100–1000 Hz. Therefore, G_{iv} adopts proportional controller and uses i_{dc1} feedback control to realize Z_{vir_S} with the expression

$$Z_{vir\_S} = \frac{G_{iv} G_v G_i U_{Cs} Z_{Co}}{G_v G_i U_{Cs} Z_{Co} + G_i U_{Cs} + Z_{Co} + Z_{L1}}. \tag{29}$$

By adjusting G_{iv} to ensure system stability, the common part T_{m_1} of the input-to-output transfer functions of SCS after the introduction of Z_{vir_S} is expressed as

$$T_{m\_1} = \frac{1}{G_i\left[G_{iLd} + G_{id} + G_v G_{ucd} + G_v G_{id}(Z_s - G_{iv})\right] + 1}. \tag{30}$$

The zero-pole distribution of the T_{m_1} varying with G_{iv} is shown in Fig. 17, which shows that with the increase of G_{iv}, the unstable poles P_1-P_2 and P_5-P_6 tend to stabilize, and the P_3-P_4 first enter the stable region and then become unstable poles again. To ensure the system is stable, G_{iv} should be selected in range of 4 to 15, and $G_{iv} = 10$ is selected considering sufficient stability margin.

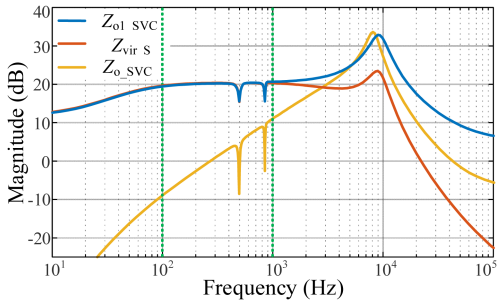

Fig. 18. Magnitude-frequency curves of the SVC output impedance with and without Z_{vir_S}.

After the introduction of the Z_{vir_S}, the output impedance of the SVC is $Z_{o1\_SVC} = Z_{o\_SVC} + Z_{vir\_S}$, and the optimized output impedance magnitude-frequency curves are shown in Fig. 18. It can be seen that Z_{vir_S} basically has resistance characteristics in the series resonance range, which effectively suppresses the adverse effect of series impedance resonance on stability.

B. Implementation and Parameters Design of the Z_{vir_P}

The introduction of Z_{vir_S} increases the output impedance of the SVC at low frequency, which reduces the load disturbance response capability of the SVC and thus affects the dynamic performance of the system. For this reason, Z_{vir_P} is connected in parallel to the output of SVC, as shown in Fig. 15. According to the Fig. 16, Z_{vir_P} is implemented through u_c feedback control as the command value of i_{dc1}, which implies control of the system power. When system is running stably, the closed-loop control ensures that the SVC does not output active power, so u_c does not contain dc component, and then $U_{dc} = U_{rec\_dc}$. The system control objective is to stabilize U_{dc}, so the U_{dc} is utilized instead of u_c feedback control to realize Z_{vir_P}.

In order to reduce only the low-frequency output impedance without changing the impedance in the series resonance range, a low-pass filter G_L is used to extract dc component of U_{dc} for feedback control. G_L is a second-order low-pass filter with the expression

$$G_L(s) = \frac{{\omega_n}^2}{s^2 + 2\omega_n s + {\omega_n}^2} \tag{31}$$

where ω_n is the cut-off angular frequency. To realize the stable control of U_{dc}, G_{vv} adopts a proportional-integral controller to realize Z_{vir_P} with the expression

$$G_{vv}(s) = k_p + \frac{k_i}{s} \tag{32}$$
$$Z_{vir\_P} = \frac{Z_{L1} + G_{iv} G_v G_i U_{Cs} - G_v G_i U_{Cs} Z_s}{G_L G_{vv} G_{iv} G_v G_i U_{Cs}}. \tag{33}$$

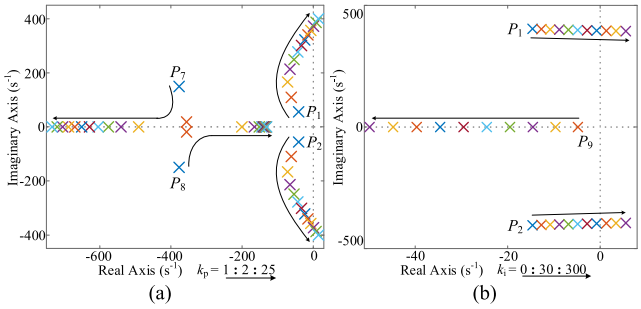

Fig. 19. Zero-pole distribution of T_{m_2} varying with G_{vv}. (a) $k_i = 0$, $k_v = 1{:}2{:}25$. (b) $k_v = 5$, $k_i = 0{:}30{:}300$.

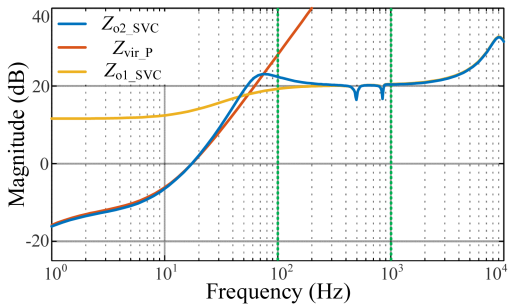

Fig. 20. Magnitude-frequency curves of the SVC output impedance with and without Z_{vir_P}.

The common part T_{m_2} of the input-to-output transfer functions of SCS after the introduction of Z_{vir_P} is expressed as

$$T_{m\_2} = \frac{1}{G_i\left[\begin{array}{l} G_{iLd} + G_{id} + G_v G_{ucd} + G_v G_{id}\cdot \\ (Z_s - G_{iv}) - G_L G_{vv} G_{iv} G_v G_{vd} \end{array}\right] + 1}. \quad (34)$$

First set $k_i = 0$, the zero-pole distribution of the T_{m_2} varying with k_p is shown in Fig. 19(a). With the increase of k_p, the P_1-P_2 go from stable region to unstable region, the system is stable when k_p<20. Considering enough stability margin setting $k_p = 5$, the zero-pole distribution of the T_{m_2} varying with k_i is shown in Fig. 19(b). Adding the integral link, the system adds a pole P_9, and with the increase of k_i, the P_1-P_2 go from stable region to unstable region, the system is stable when k_i<210. Increasing the gain of G_{vv} to reduce the magnitude of Z_{vir_P} can improve the dynamic performance of SVC, while considering the system stability, a compromise is chosen with $k_p = 5$ and $k_i = 30$.

After the introduction of the Z_{vir_P}, the output impedance of the SVC is $Z_{o2\_SVC} = Z_{o1\_SVC} // Z_{vir\_P}$, and the optimized output impedance magnitude-frequency curves are shown in Fig. 20. It can be seen that the magnitude of Z_{vir_P} is small enough at low frequency and large enough at high frequency. The optimized SVC output impedance Z_{o2_SVC} has a significantly lower magnitude at low frequency, which improves system dynamic performance; also, the magnitude in the series resonance range is large enough to effectively prevent the series impedance resonance from the system stability.

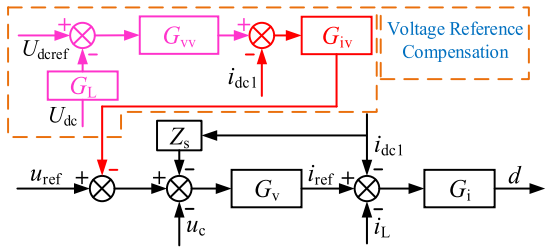

Fig. 21. Block diagram of the IOVCC control strategy.

TABLE III
PARAMETERS FOR IMPLEMENTING IOVCC

Parameter	Value	Parameter	Value
G_{iv}	10	ω_n	5×2π
k_p	5	k_i	30

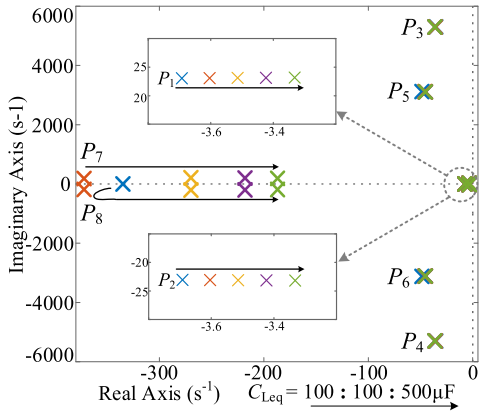

Fig. 22. Zero-pole distribution of T_{m_2} varying with C_{Leq}, C_{Leq} = 100:500 μF.

C. Stability of the SCS With IOVCC Control

The IOVCC control strategy is obtained through the above analysis. Based on the VCDL control, U_{dc} and i_{dc1} feedback control are added to compensate for the command value, and the optimized control block diagram is shown in Fig. 21.

Furthermore, the suppression effect of the IOVCC control strategy on the dc bus oscillation is verified. According to the optimized control parameters in Table III, the zero-pole distribution of T_{m_2} is shown in Fig. 22 when the C_{Leq} varies within a certain range. We can see that the IOVCC control strategy can ensure system stable operation. The optimized control strategy and parameter design method can provide enough stability margin.

The voltage gain T_{vv_IOVCC} of the SCS with optimized control can be expressed as

$$T_{vv\_IOVCC} = \frac{\begin{array}{l} A_v + G_i A_v\left[G_{iLd} + G_{id} + G_v G_{ucd} + G_v G_{id}(Z_s - G_{iv})\right] \\ +G_i G_{vd}\left[G_{iLv} + Y_{in} + G_v G_{ucv} + G_v Y_{in}(Z_s - G_{iv})\right] \end{array}}{G_i\left[\begin{array}{l} G_{iLd} + G_{id} + G_v G_{ucd} + G_v G_{id}\cdot \\ (Z_s - G_{iv}) - G_L G_{vv} G_{iv} G_v G_{vd} \end{array}\right] + 1}. \quad (35)$$

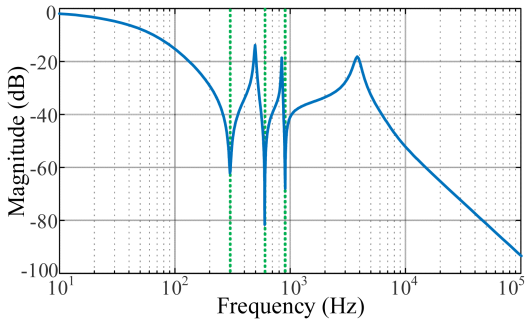

Fig. 23. Magnitude-frequency curve of the $T_{\mathrm{vv\_IOVCC}}$.

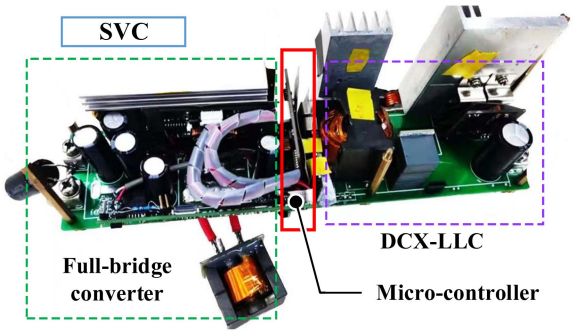

Fig. 24. Experimental prototype of the SVC.

The magnitude-frequency curve of $T_{\mathrm{vv\_IOVCC}}$ is shown in Fig. 23. The gains at the 6*n*th harmonic frequencies can make dc bus voltage ripple meet the requirements. Therefore, the IOVCC control strategy solves the dc bus oscillation problem of the SCS.

V. Experimental Verification

In order to verify the accuracy of the system stability and dc bus oscillation mechanism analysis, and the effectiveness of the IOVCC control strategy. The series compensation technique has been applied to a 2 kW, 110 V, 50 Hz DR with resistive load. The test bed for testing the experimental prototype is shown in Fig. 1. Table I gives the prototype design specifications. Fig. 24 illustrates the SVC prototype with the two-stage structure. Experimental cases of stability judgment under different working conditions with VCDL and IOVCC are completed. Meanwhile, the dynamic performance of SCS is tested during the source voltage and load transients.

A. Validation of Proposed Stability Assessment Methodology When the SVC Adopts VCDL Control

The dc bus capacitor C_{dc} is set to 0 μF, 100 μF and 1000 μF, respectively, to verify the effect of series impedance resonance on system stability. Fig. 25 shows the experimental waveforms of the SCS under different C_{dc}. Obviously, when the dc bus without capacitors, the SCS is stable, and the dc bus voltage harmonics are significantly suppressed. But there are obvious divergent oscillations in u_{rec}, U_{dc}, and i_{dc1} after the SVC input compensation when capacitors exist in the dc bus, this indicates

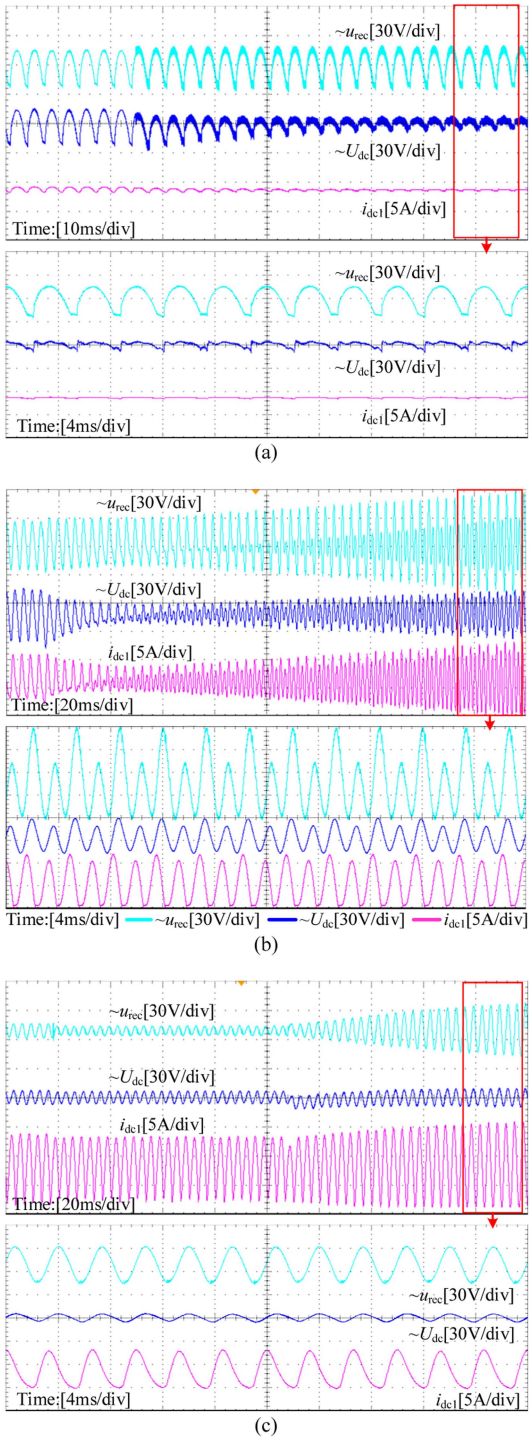

Fig. 25. Experimental waveforms of the SCS varying with C_{dc}. (a) $C_{\mathrm{dc}} = 0$ μF. (b) $C_{\mathrm{dc}} = 100$ μF. (c) $C_{\mathrm{dc}} = 1000$ μF.

that the system is unstable. Increasing the dc bus capacitors can mitigate the magnitude and frequency of system oscillation. The experimental results verify that the dc bus capacitors cause series impedance resonance, resulting in system instability, and that the effect of series resonance on stability can be mitigated by

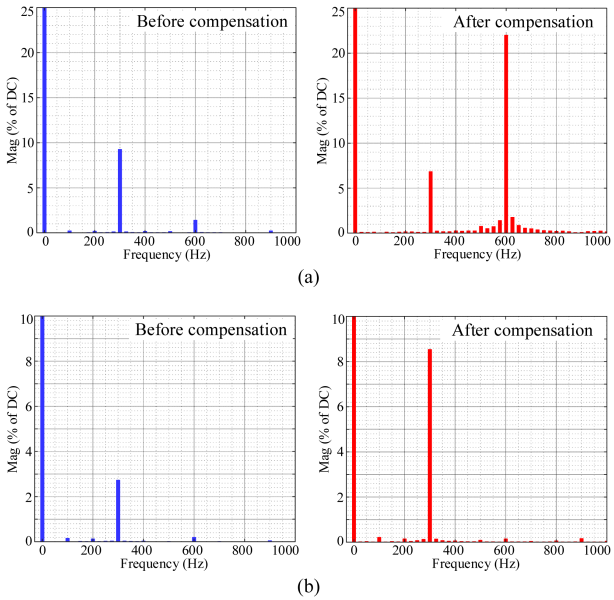

Fig. 26. Harmonic spectra of $u_{\rm rec}$ before and after compensation with different $C_{\rm dc}$. (a) $C_{\rm dc} = 100$ μF. (b) $C_{\rm dc} = 1000$ μF.

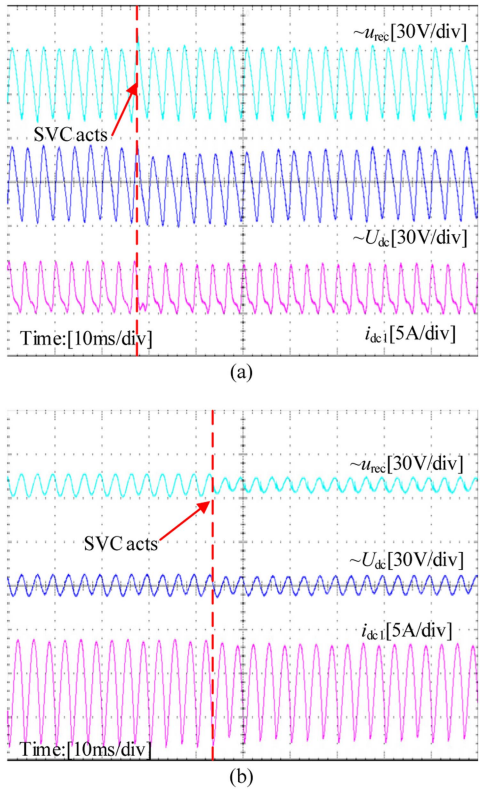

Fig. 27. Experimental waveforms of the SCS with no quasi-resonant links in $G_{\rm v}$. (a) $C_{\rm dc} = 100$ μF. (b) $C_{\rm dc} = 1000$ μF.

increasing capacitors to reduce the resonance frequency, corresponding to the judgment results of the SCS stability criterion in Section III.

Furthermore, the harmonic spectra of $u_{\rm rec}$ before and after SVC input compensation are shown in Fig. 26. When $C_{\rm dc} = 100$ μF, the harmonics in $u_{\rm rec}$ near 600 Hz increase significantly after the SVC input compensation; When $C_{\rm dc} = 1000$ μF, the harmonics in $u_{\rm rec}$ near 300 Hz increase significantly after the SVC input compensation. However, this deviates from the stability analysis results (the instability poles correspond to frequency near 900 Hz when $C_{\rm dc} = 100$ μF). The deviation of oscillation frequency obtained from theoretical analysis and experiments is due to the nonlinear DR being approximated as an ideal linear model. The stability analysis based on linearization modeling can still accurately derive the nature of system instability, since the trend of parameters variation on stability is consistent.

In order to verify that the interaction of the quasi-resonant links in $G_{\rm v}$ and series impedance resonance leads to the system instability. Fig. 27 shows the experimental waveforms of the SCS with no quasi-resonant links in $G_{\rm v}$ ($k_{\rm r\_n} = 0$, $n = 1,2,3$) when $C_{\rm dc}$ is 100 or 1000 μF. There are no divergent oscillations in $u_{\rm rec}$, $U_{\rm dc}$, and $i_{\rm dc1}$ after the SVC input compensation, which indicates that the system is stable. However, the system loses its harmonic suppression capability with no quasi-resonant links in $G_{\rm v}$, which causes $U_{\rm dc}$ and $i_{\rm dc1}$ containing abundant harmonic components. As $C_{\rm dc}$ increases, the harmonic contents of $U_{\rm dc}$ and $i_{\rm dc1}$ will decrease. The experimental results demonstrate that the SVC adopts VCDL control inevitably leads to the dc bus oscillation.

To show that increasing loop damping can effectively suppress the effect of series impedance resonance on system stability. Fig. 28 shows the experimental waveforms of the SCS with the addition of the L_2 series resistance $R_{\rm L2} = 3$ Ω when $C_{\rm dc}$ is 100 or 1000 μF. After the SVC input compensation, the system can operate stably, the dc bus voltage harmonics are obviously suppressed, and increasing $C_{\rm dc}$ can reduce the ripple of $U_{\rm dc}$. The experimental results confirm that increasing loop damping can suppresse the series impedance resonance, which can solve effectively the problem of dc bus oscillation induced by SVC with VCDL control. So, the experimental results are consistent with the analysis conclusions in Section III-C.

B. Validation of System Characteristics When the SVC Adopts Proposed IOVCC Control

To illustrate the effect of IOVCC control on system stability, Fig. 29 shows the experimental waveforms of the SCS with the IOVCC control when $C_{\rm dc}$ is 100 μF. It can be seen that the system can operate stably after the SVC input compensation, and the pulsation of the $i_{\rm dc1}$ is significantly suppressed and the ripple of the $U_{\rm dc}$ is reduced. This indicates that the proposed IOVCC control strategy can ensure stable operation of SCS by optimizing the output impedance characteristics of SVC.

In order to further illustrate the suppression effect of IOVCC control on dc bus oscillation, the $U_{\rm dc}$ harmonic contents before and after SVC input compensation for the different operating conditions mentioned above are compared, as shown in Table IV. From the data in the Table, it can be obtained that the SCS is stable when $C_{\rm dc} = 0$ μF, however, the THD of $U_{\rm dc}$ is still large due to limited harmonic compensation capability of SVC. Hence, the small dc bus capacitors are needed to stabilize the

TABLE IV
COMPARISON OF DC BUS VOLTAGE HARMONIC CONTENTS FOR DIFFERENT OPERATING CONDITIONS

Conditions \ System/U_{dc}		Stability	6th (%)		12th (%)		18th (%)		THD(%)	
			off	on	off	on	off	on	off	on
C_{dc}=0 μF	VCDL	Yes/Yes	6.05	1.24	1.55	0.49	0.62	0.50	6.32	1.57
C_{dc}=100 μF	VCDL	No/No	9.31	1.81	1.41	10.9	0.24	0.28	9.43	11.2
	VCDL/k_{r_n}=0	Yes/No	9.31	7.94	1.41	2.11	0.24	0.29	9.43	8.24
	VCDL/R_{L2}=3Ω	Yes/Yes	4.44	0.83	0.74	0.31	0.22	0.25	4.51	0.93
	IOVCC	Yes/Yes	9.31	0.41	1.41	0.08	0.24	0.05	9.43	0.43
C_{dc}=1 mF	VCDL	No/No	2.51	1.78	0.19	0.17	0.03	0.06	2.53	1.79
	VCDL/k_{r_n}=0	Yes/No	2.51	2.25	0.19	0.17	0.03	0.03	2.53	2.26
	VCDL/R_{L2}=3Ω	Yes/Yes	0.68	0.17	0.08	0.04	0.02	0.03	0.69	0.19

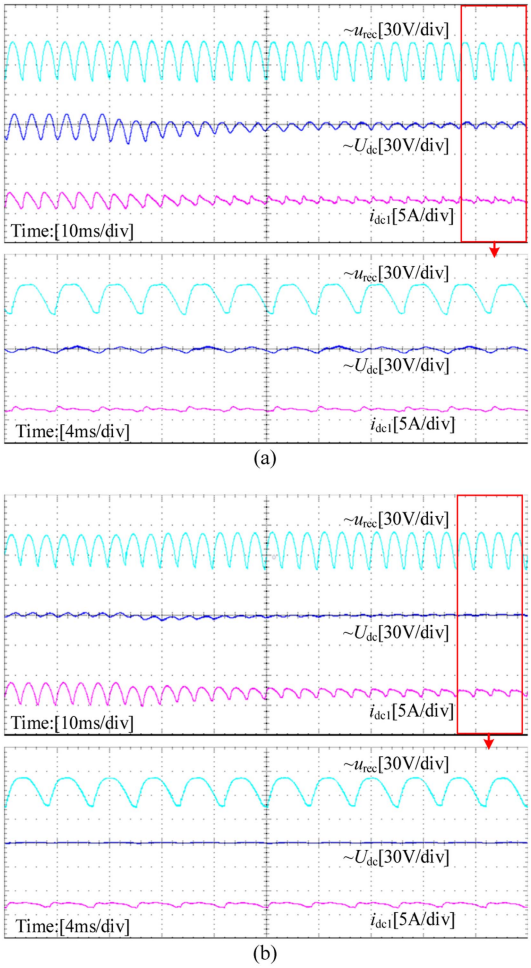

Fig. 28. Experimental waveforms of the SCS with the addition of $R_{L2} = 3\ \Omega$. (a) $C_{dc} = 100\ \mu$F. (b) $C_{dc} = 1000\ \mu$F.

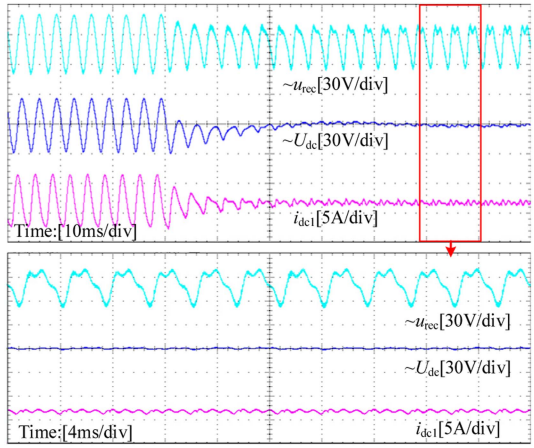

Fig. 29. Experimental waveforms of the SCS with the IOVCC control when $C_{dc} = 100\ \mu$F.

voltage ripple. Unfortunately, when there are dc bus capacitors, the SVC with VCDL control will inevitably lead to dc bus oscillation, which can not satisfy power supply requirements. As the capacitors increase, the dc bus voltage oscillation is mitigated, but this does not satisfy the design goals of SCS. By adding the loop resistor $R_{L2} = 3\ \Omega$, the SCS is stable and the THD of U_{dc} meets requirements. When SVC adopts IOVCC control, the SCS can operate stably, and only a small capacitor is needed to make the THD of U_{dc} meet requirements. The experimental data confirm the accuracy of the SCS stability analysis and verify the effectiveness of IOVCC control strategy.

Fig. 30 shows the load transient dynamic experimental waveforms with IOVCC. To verify the effect of command compensation link on SVC output impedance, an comparative experiment is performed. The dynamic waveforms of adding only Z_{vir_S} are shown in Fig. 30(a). As seen, when the load is stepped up from 30% to 100%, the undershoot of U_{dc} is about 18 V, and the recovering time is about 80 ms. The dynamic waveforms of adding Z_{vir_P} are shown in Fig. 30(b). The undershoot of U_{dc} is also about 14 V, and the recovering time is reduced to 20 ms.

Fig. 31 shows the source voltage e_s transient dynamic experimental waveforms with IOVCC. When e_s drops by 10%, The U_{dc} will follow the e_s to reach a new steady state, thereby ensuring the SVC barely takes on active power transfer. The dynamic waveforms for adding only Z_{vir_S} is shown in Fig. 31(a), the recovery time required for dynamic process is about 170 ms. The dynamic waveforms of adding Z_{vir_P} is shown in Fig. 31(b), the recovery time required for dynamic process is reduced to 40 ms.

Comparing Figs. 30(b) and 31(b) with 30(a) and 31(a), it can be seen that the parallel connection of Z_{vir_P} to the output of SVC

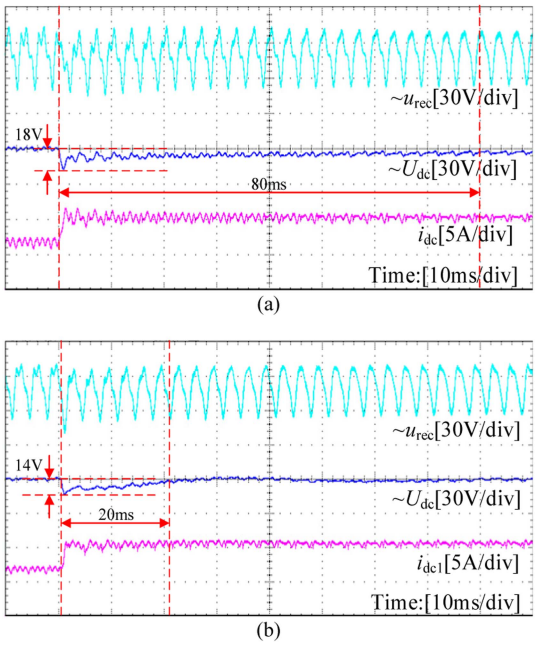

Fig. 30. Load transient dynamic experimental waveforms of the IOVCC. (a) Only add Z_{vir_S}. (b) Add Z_{vir_S} and Z_{vir_P}.

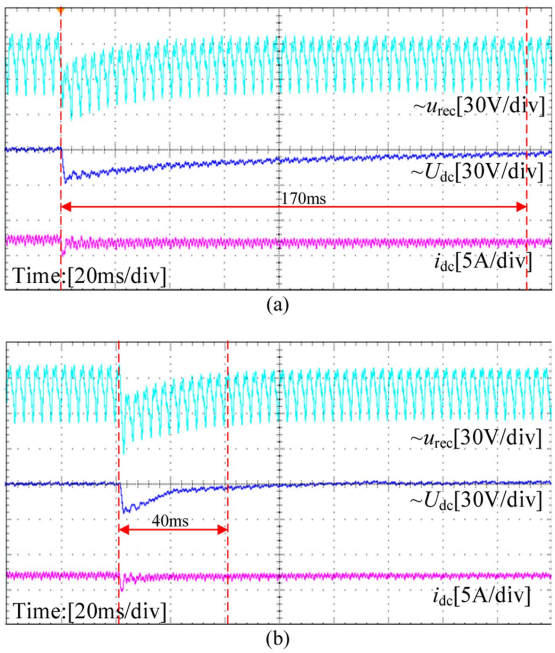

Fig. 31. Source voltage dynamic experimental waveforms of the IOVCC. (a) Only add Z_{vir_S}. (b) Add Z_{vir_S} and Z_{vir_P}.

effectively reduces the impedance of SVC at low frequency and improves the dynamic performance of the system compared to introducing only Z_{vir_S}. The experimental results are consistent with the theoretical analysis in Section IV.

Fig. 32 shows the ratio of the loss caused by SVC to total power of the system, it is clear that the added SVC based on partial-power compensation has little effect on efficiency advantage of DR. This also verifies that although the series

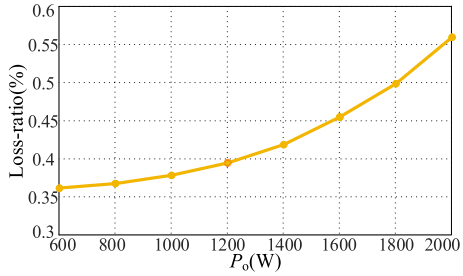

Fig. 32. Loss ratio of SVC.

structure allows SVC to flow through full load current, this partial power structure still has efficiency advantages due to the lower voltage levels and using smaller on-state resistance MOSFETS that can significantly reduce device losses.

VI. Conclusion

Impedance-based stability assessment methodology cannot succinctly judge the stability of SCS. In this article, the stability is analyzed based on the common characteristics of SCS, and the dc bus oscillation mechanism is discussed in detail. Then some conclusions can be obtained as follow.

1) The stability of the SCS can be judged by the common transfer function characterizing whole system, which is derived by calculating the input–output transfer functions of the unified form two-port small-signal model regardless of the coupling relationship between the parts.
2) According to the frequency characteristics of the equivalent loop gain, the dc bus oscillation is caused by the interaction of series impedance resonance and quasi-resonant links in G_v, and the stability results are consistent for the two methods.
3) The SVC adopts VCDL control, there is a contradiction between system stability and harmonic suppression capability, which will inevitably lead to dc bus oscillation, and system stability can be improved by adding loop damping.
4) The IOVCC control strategy solves dc bus oscillation by reshaping SVC output impedance. A series-virtual-impedance ensures system stability by adding loop damping, and a parallel-virtual-impedance improves dynamic performance by reducing impedance at low frequency.
5) The virtual impedances are achieved through state variable feedback, the straightforward controllers and the parameters design are applied to optimize system operation.

Finally, a 2 kW experimental prototype was developed and tested. The experimental results verified the accuracy and effectiveness of the proposed stability analysis methods and control strategy.

Appendix

The expressions of open-loop transfer functions of the SCS mentioned in Section III is shown in Table V, where $Z_{Cs} = 1/(sC_s)$. In order to verify the accuracy of the simplified model of the SCS, simulation sweep is performed for all the transfer functions in Fig. 6. The bode diagrams of the open-loop transfer

TABLE V
EXPRESSIONS FOR OPEN-LOOP TRANSFER FUNCTIONS FOR COMPLETE AND SIMPLIFIED SCS SMALL-SIGNAL MODELS

Definition	Transfer function	Simplified transfer function
$Y_{in}(s)=\dfrac{\Delta i_{dc1}(s)}{\Delta e_{hs}(s)}$	$\dfrac{Z_{dc}(Z_{L1}+Z_{Co}+D^2Z_{Cs})+N^2(Z_{L1}+Z_{Co})(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$\dfrac{Z_{L1}+Z_{Co}}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$A_i(s)=\dfrac{\Delta i_{dc1}(s)}{\Delta i_o(s)}$	$\dfrac{N^2Z_{dc}\left[(Z_{L1}+Z_{Co})(Z_{Cs}+Z_{LLC})+D^2Z_{Cs}Z_{LLC}+DZ_{Co}Z_{Cs}/N\right]}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$\dfrac{Z_{dc}(Z_{L1}+Z_{Co})}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$G_{id}(s)=\dfrac{\Delta i_{dc1}(s)}{\Delta d(s)}$	$\dfrac{N^2U_{Cs}Z_{Co}(Z_{Cs}+Z_{LLC})+Z_{Cs}Z_{dc}\left[NI_{dc1}(Z_{L1}+Z_{Co})+D(I_{dc1}Z_{Co}-NU_{Cs})\right]}{+Z_{Co}(U_{Cs}Z_{dc}+N^2DI_{dc1}Z_{Cs}Z_{LLC})}$ $\dfrac{}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$-\dfrac{U_{Cs}Z_{Co}}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$A_v(s)=\dfrac{\Delta U_{dc}(s)}{\Delta e_{hs}(s)}$	$\dfrac{N^2Z_{dc}\left[(Z_{L1}+Z_{Co})(Z_{Cs}+Z_{LLC})+D^2Z_{Cs}Z_{LLC}+DZ_{Co}Z_{Cs}/N\right]}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$\dfrac{Z_{dc}(Z_{L1}+Z_{Co})}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$Z_o(s)=\dfrac{\Delta U_{dc}(s)}{\Delta i_o(s)}$	$\dfrac{N^2Z_{dc}\left[(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}(Z_{Cs}+Z_{LLC})+D^2Z_{Cs}Z_{LLC})+Z_{Co}(Z_{Cs}+Z_{LLC})(Z_{L2}+Z_s)\right]}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$\dfrac{Z_{dc}\left[(Z_{L1}+Z_{Co})(Z_{L2}+Z_s)+Z_{L1}Z_{Co}\right]}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$G_{vd}(s)=\dfrac{\Delta U_{dc}(s)}{\Delta d(s)}$	$\dfrac{NZ_{dc}\left[Z_{Cs}(Z_{L2}+Z_{Co}+Z_s)(DU_{Cs}-I_{dc1}Z_{L1})-I_{dc1}Z_{Cs}Z_{Co}(Z_{L2}+Z_s)\right]}{+NZ_{Co}(U_{Cs}(Z_{Cs}+Z_{LLC})+DI_{dc1}Z_{Cs}Z_{LLC})}$ $\dfrac{}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$-\dfrac{U_{Cs}Z_{dc}Z_{Co}}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$G_{ucv}(s)=\dfrac{\Delta u_C(s)}{\Delta e_{hs}(s)}$	$\dfrac{Z_{Co}\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2Z_{Cs}(Z_{dc}+N^2Z_{LLC})+Z_{dc}(Z_{L1}+DNZ_{Cs})\right]}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$\dfrac{Z_{L1}Z_{Co}}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$G_{uci}(s)=\dfrac{\Delta u_C(s)}{\Delta i_o(s)}$	$\dfrac{NZ_{Co}Z_{dc}\left[NZ_{L1}(Z_{Cs}+Z_{LLC})-DZ_{Cs}(Z_{L2}+Z_s)+D^2NZ_{Cs}Z_{LLC}\right]}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$\dfrac{Z_{L1}Z_{dc}Z_{Co}}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$G_{ucd}(s)=\dfrac{\Delta u_C(s)}{\Delta d(s)}$	$\dfrac{Z_{Co}\left[N^2(Z_{L2}+Z_{dc}+Z_s)(DI_{dc1}Z_{Cs}Z_{LLC}+U_{Cs}(Z_{Cs}+Z_{LLC}))+U_{Cs}Z_{dc}(Z_{L2}+Z_s)\right]}{+Z_{Cs}Z_{dc}(DI_{dc1}(Z_{L2}+Z_s)+N(DU_{Cs}-I_{dc1}Z_{L1}))}$ $\dfrac{}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$\dfrac{U_{Cs}Z_{Co}(Z_{L2}+Z_{dc}+Z_s)}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$G_{iLv}(s)=\dfrac{\Delta i_L(s)}{\Delta e_{hs}(s)}$	$-\dfrac{Z_{dc}(Z_{Co}-DNZ_{Cs})+N^2Z_{Co}(Z_{Cs}+Z_{LLC})}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$-\dfrac{Z_{Co}}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$G_{iLi}(s)=\dfrac{\Delta i_L(s)}{\Delta i_o(s)}$	$-\dfrac{NZ_{dc}\left[DZ_{Cs}(Z_{L2}+Z_{Co}+Z_s)+NZ_{Co}(Z_{Cs}+Z_{LLC})\right]}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$-\dfrac{Z_{dc}Z_{Co}}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$
$G_{iLd}(s)=\dfrac{\Delta i_L(s)}{\Delta d(s)}$	$\dfrac{N^2(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[U_{Cs}(Z_{Cs}+Z_{LLC})+DI_{dc1}Z_{Cs}Z_{LLC}\right]}{+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)\left[U_{Cs}+DI_{dc1}Z_{Cs}\right]+NI_{dc1}Z_{Cs}Z_{Co}Z_{dc}}$ $\dfrac{}{(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)\left[N^2Z_{L1}(Z_{Cs}+Z_{LLC})+D^2N^2Z_{Cs}Z_{LLC}\right]}$ $+Z_{dc}(Z_{L2}+Z_{Co}+Z_s)(Z_{L1}+D^2Z_{Cs})+N^2Z_{Co}(Z_{L2}+Z_{dc}+Z_s)(Z_{Cs}+Z_{LLC})$ $+Z_{Co}Z_{dc}(Z_{L2}+Z_s+2DNZ_{Cs})$	$\dfrac{U_{Cs}(Z_{L2}+Z_{Co}+Z_{dc}+Z_s)}{(Z_{L1}+Z_{Co})(Z_{L2}+Z_{dc}+Z_s)+Z_{L1}Z_{Co}}$

functions obtained from complete model, simplified model, and simulation sweep are shown in Fig. 33. For A_i, A_v, Z_o, G_{vd}, G_{uci}, and G_{iLi}, there are differences between the simplified model and simulation sweep results at high frequency because of ignoring the Z_{LLC}, and since the deviation at high frequency do not affect the system stability, the Z_{LLC} can be neglected. For G_{id}, G_{ucv}, and G_{iLd}, there are differences between simplified model and simulation sweep results at low frequency because of ignoring

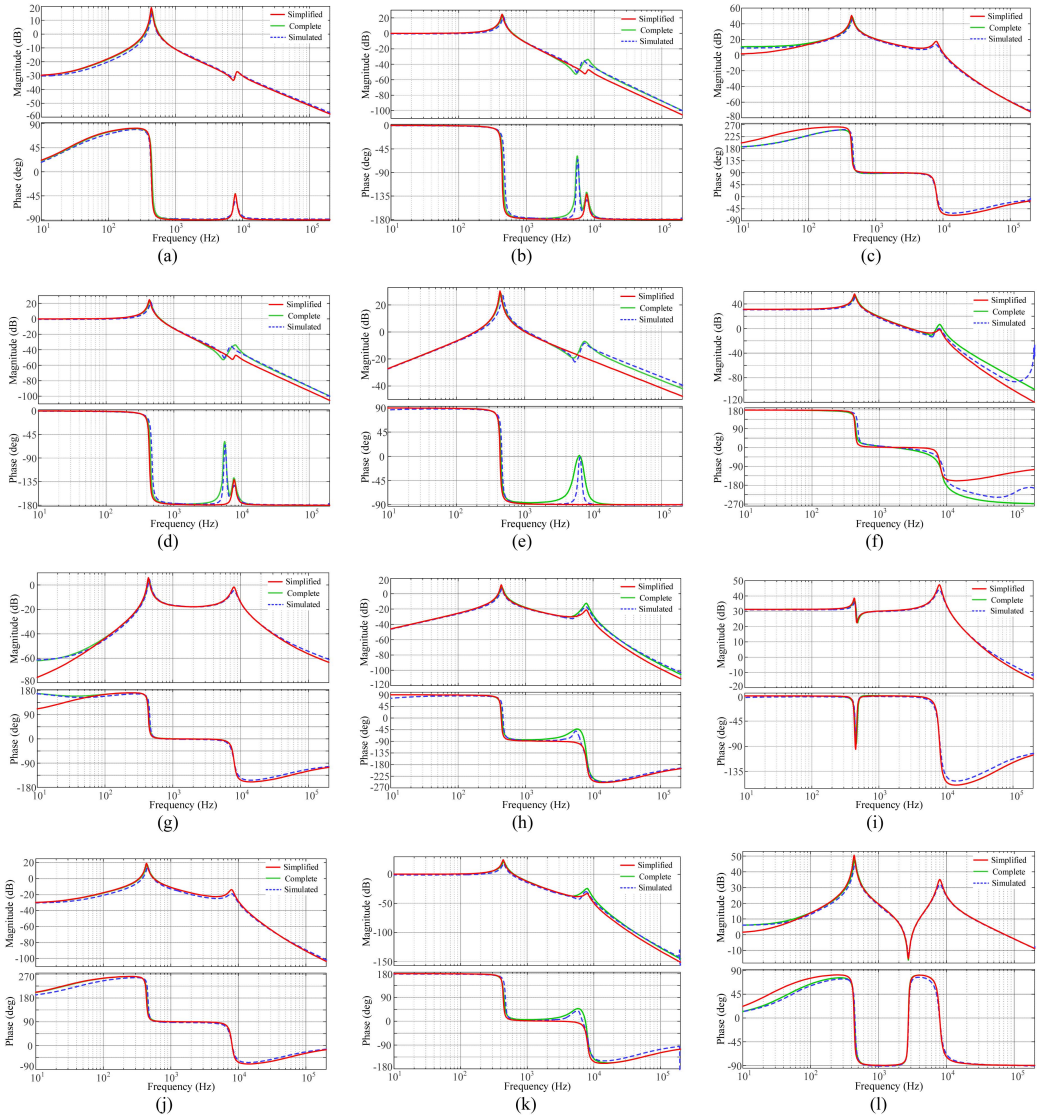

Fig. 33. Bode diagrams of transfer functions from complete model, simplified model, and simulation sweep. (a) Y_{in}. (b) A_{i}. (c) G_{id}. (d) A_{v}. (e) Z_{o}. (f) G_{vd}. (g) G_{ucv}. (h) G_{uci}. (i) G_{ucd}. (j) G_{iLv}. (k) G_{iLi}. (l) G_{iLd}.

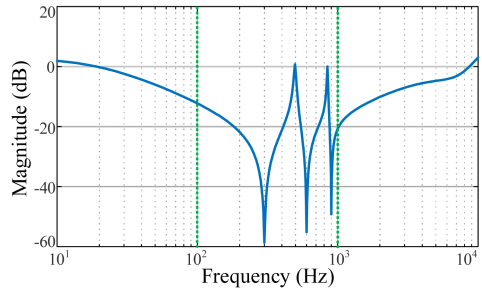

Fig. 34. Magnitude-frequency curve of the $G_{\mathrm{iv\_c}}$.

the load current of *LLC*. As the *LLC* carries almost no power and the system oscillation are not at low frequency, the load current of the *LLC* can be ignored. The simplified expressions of open-loop transfer functions is shown in Table IV.

The magnitude-frequency curve of the $G_{\mathrm{iv\_c}}$ mentioned in Section IV is shown in Fig. 34. It can be seen that $G_{\mathrm{iv\_c}}$ is approximately neglected compared to 1 in the series resonance range.

REFERENCES

[1] H. Yu, Y. Wang, and Z. Chen, "A novel renewable microgrid-enabled metro traction power system—Concepts, framework, and operation strategy," *IEEE Trans. Transport. Electrific.*, vol. 7, no. 3, pp. 1733–1749, Sep. 2021.

[2] P. Zhang, X. Wu, W. Xu, J. Liu, J. Qi, and A. Yang, "A compensation component injection method based on a hybrid modulation for minimizing the neutral-point voltage oscillations in a five-level flying capacitor rectifier," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2705–2718, Mar. 2022.

[3] L. Zhao, Z. Luo, Z. Fan, and Y. Shi, "A dual half-bridge converter with hybrid rectifier for DC power supply in railway systems," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4579–4587, May 2020.

[4] Y. Chang and X. Cai, "Hybrid topology of a diode-rectifier-based HVDC system for offshore wind farms," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 2116–2128, Sep. 2019.

[5] X. Meng, M. Chen, M. He, X. Wang, and J. Liu, "A novel high power hybrid rectifier with low cost and high grid current quality for improved efficiency of electrolytic hydrogen production," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3763–3768, Apr. 2022.

[6] W. Liu et al., "Power quality assessment in shipboard microgrids under unbalanced and harmonic AC bus voltage," *IEEE Trans. Ind. Appl.*, vol. 55, no. 1, pp. 765–775, Jan./Feb. 2019.
[7] S. Gupta, N. Vamanan, and V. John, "A diode bridge rectifier with improved power quality using the capacitive network," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1563–1572, Mar./Apr. 2018.
[8] F. Meng, X. Xu, L. Gao, Z. Man, and X. Cai, "Dual passive harmonic reduction at DC link of the double-star uncontrolled rectifier," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 3303–3309, Apr. 2019.
[9] F. Zare, P. Davari, and F. Blaabjerg, "A modular active front-end rectifier with electronic phase shifting for harmonic mitigation in motor drive applications," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5440–5450, Nov./Dec. 2017.
[10] C. Xu, B. Zhao, Z. Chen, J. Liu, Q. Song, and Z. Yu, "A novel converter-breaker integrated voltage source converter based on high-surge IGCT and fault self-clearing strategy for DC grid," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12668–12672, Dec. 2020.
[11] H. Wang and H. Wang, "A two-terminal active capacitor," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5893–5896, Aug. 2017.
[12] H. Wang, Y. Liu, and H. Wang, "On the practical design of a two-terminal active capacitor," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10006–10020, Oct. 2019.
[13] H. Wang and H. Wang, "A two-terminal active inductor with minimum apparent power for the auxiliary circuit," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1013–1016, Feb. 2019.
[14] A. Alduraibi, J. Yaghoobi, D. Solatialkaran, and F. Zare, "A modular power converter with active front-end system to mitigate harmonics in distribution networks," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1725–1735, Apr. 2021.
[15] X. Du, L. Zhou, and H. Tai, "Average current control of a series-type single-phase PFC with hybrid modulation," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2381–2385, Sep. 2011.
[16] H. Ertl and J. W. Kolar, "A constant output current three-phase diode bridge rectifier employing a novel 'electronic smoothing inductor'," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 454–461, Apr. 2005.
[17] R. Yang, Y. Yu, G. Wang, D. Wu, and W. Yu, "Series-connected DC voltage harmonics compensation circuit and application in multi-terminal DC," *Trans. China Electrotechnical Soc.*, vol. 36, pp. 554–562, Dec. 2021.
[18] W. Liu, K. Wang, H. S.-H. Chung, and S. T.-H. Chuang, "Modeling and design of series voltage compensator for reduction of DC-link capacitance in grid-tie solar inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2534–2548, May 2015.
[19] H. Wang, W. Liu, H. Chung, and F. Blaabjerg, "Stability analysis and dynamic response of a DC-link module with a series voltage compensator," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 2453–2460.
[20] C. Zhang, M. Molinas, A. Rygg, and X. Cai, "Impedance-based analysis of interconnected power electronics systems: Impedance network modeling and comparative studies of stability criteria," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 3, pp. 2520–2533, Sep. 2020.
[21] X. Wang et al., "Decentralized impedance specifications for small-signal stability of DC distributed power systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 4, pp. 1578–1588, Dec. 2017.
[22] W. Du, J. Zhang, Y. Zhang, and Z. Qian, "Stability criterion for cascaded system with constant power load," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1843–1851, Apr. 2013.
[23] X. Zhang, X. Ruan, and C. K. Tse, "Impedance-based local stability criterion for DC distributed power systems," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 62, no. 3, pp. 916–925, Mar. 2015.
[24] P. Pan et al., "An impedance-based stability assessment methodology for DC distribution power system with multivoltage levels," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4033–4047, Apr. 2020.
[25] H. Mu et al., "Impedance-based stability analysis methods for DC distribution power system with multivoltage levels," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9193–9208, Aug. 2021.
[26] L. Yu, L. Xu, J. Zhu, and R. Li, "Impedance modelling and stability analysis of diode-rectifier based HVDC connected offshore wind farms," *IEEE Trans. Power Del.*, vol. 37, no. 1, pp. 591–602, Feb. 2022.
[27] H. Liu, W. Guo, D. Cheng, Y. Wang, and M. Wang, "Stability and bifurcation analysis of DC microgrid with multiple droop control sources and loads," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2361–2372, Feb. 2021.
[28] Q. Xu, W. Jiang, F. Blaabjerg, C. Zhang, X. Zhang, and T. Fernando, "Backstepping control for large signal stability of high boost ratio interleaved converter interfaced DC microgrids with constant power loads," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5397–5407, May 2020.
[29] F. Feng, X. Zhang, J. Zhang, and H. B. Gooi, "Stability enhancement via controller optimization and impedance shaping for dual active bridge-based energy storage systems," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5863–5874, Jul. 2021.
[30] P. Chen, W. Jiang, X. Ruan, P. Zhao, and H. Li, "Active damping control and parameter design method for ISOP-based load converter in DC distribution system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 1, pp. 465–477, Feb. 2023.
[31] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Design of LCL filters with LCL resonance frequencies beyond the nyquist frequency for grid-connected converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 3–14, Mar. 2016.
[32] J. G. Mayordomo, L. F. Beites, X. Yang, and W. Xu, "A detailed procedure for harmonic analysis of three-phase diode rectifiers under discontinuous conduction mode and nonideal conditions," *IEEE Trans. Power Del.*, vol. 33, no. 2, pp. 741–751, Apr. 2018.
[33] F. Liu, X. Ruan, X. Huang, and Y. Qiu, "Second harmonic current reduction for two-stage inverter with DCX-LLC resonant converter in front-end DC–DC converter: Modeling and control," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4597–4609, Apr. 2021.
[34] G. Zhu, X. Ruan, L. Zhang, and X. Wang, "On the reduction of second harmonic current and improvement of dynamic response for two-stage single-phase inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1028–1041, Feb. 2015.
[35] Y. Cai, J. Xu, P. Yang, and G. Liu, "Design of double-line-frequency ripple controller for quasi-single-stage AC–DC converter with audio susceptibility model," *IEEE Trans. Ind. Electron.*, vol. 66, no. 12, pp. 9226–9237, Dec. 2019.
[36] X. Zhang, X. Ruan, and Q.-C. Zhong, "Improving the stability of cascaded DC/DC converter systems via shaping the input impedance of the load converter with a parallel or series virtual impedance," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7499–7512, Dec. 2015.
[37] B. He, W. Chen, X. Li, L. Shu, and X. Ruan, "A power adaptive impedance reshaping strategy for cascaded DC system with buck-type constant power load," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 8909–8920, Aug. 2022.

Ruidong Sun (Graduate Student Member, IEEE) was born in Yuncheng, China. He received the B.S. degree in electrical engineering from North University of China, Taiyuan, China, in 2018, and the M.S. degree in electrical engineering in 2020 from Beijing Jiaotong University, Beijing, China, where he is currently working toward the Ph.D. degree in electrical engineering with the School of Electrical Engineering.

His current research interests include hybrid rectifier, dc–dc converters, and renewable power generation.

Guohong Zeng received the B.S. degree in power drive control, the M.S. degree in power electronics and power drives, and the Ph.D. degree in automation of electric power system from Beijing Jiaotong University, Beijing, China, in 1988, 1991, and 2003, respectively.

He is currently an Associate Professor with the School of Electrical Engineering, Beijing Jiaotong University. His general research interests include power quality theory and improvement technology, high-power motor control technology, renewable energy, and energy storage technology.

Wenzheng Xu (Member, IEEE) received the B.Eng. degree in electrical engineering from Beijing Jiaotong University, Beijing, China, in 2012, the M.Sc. degree (with distinction) in energy engineering from The University of Hong Kong, Hong Kong, in 2013, and the Ph.D. degree in electrical engineering from The Hong Kong Polytechnic University (PolyU), Hong Kong, in 2020.

From 2013 to 2015 and March to June 2020, he was a Research Assistant and a Postdoctoral Fellow, respectively, with the Department of Electrical Engineering, PolyU, working on high-power converters and fast-charging devices for electric vehicles. He is currently a Lecturer with the School of Electrical Engineering, Beijing Jiaotong University. His research interests include power electronics, wireless power transfer, transportation electrification, and energy interconnection.

Zichao Zhang received the B.S. degree in Electrical Engineering and automation from China University of Petroleum, Qingdao, China, in 2020. He is currently working toward the M.S. degree with the School of Electrical Engineering, Beijing Jiaotong University, Beijing, China, both in electrical engineering.

His current research interests include hybrid rectifier and dc–dc converters.

Long Jing was born in Urumqi, China. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Beijing Jiaotong University, Beijing, China in 1999, 2002, and 2008, respectively.

He is currently an Associate Professor with the School of Electrical Engineering, Beijing Jiaotong University. He was engaged in the teaching and research of power electronics technology and new energy power generation. His current research interests include different ac–dc, dc–dc converters for energy storage, battery system control strategies, and modular multilevel converters.

Weige Zhang was born in Inner Mongolia, China. He received the B.S., M.S., and Ph.D. degrees in electrical engineering and automation from Beijing Jiaotong University, Beijing, China, in 1993, 1997, and 2013, respectively.

He is currently a Professor with the School of Electrical Engineering, Beijing Jiaotong University. His main research interests include power electronics technology, battery pack application technology, thermal management of battery packs, and distributed energy storage technology.

Xuezhi Wu (Member, IEEE) received the B.S. and M.S. degrees from Beijing Jiaotong University, Beijing, China, in 1996 and 1999, respectively, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2003, all in electrical engineering.

He is currently a Professor with the School of Electrical Engineering, Beijing Jiaotong University, Beijing, China. His current research interests include microgrids, wind power generation systems, power converters for renewable generation systems, power quality, and motor control.