Self-Synchronized Grid Impedance Estimation Unit Using Interpolated DFT Technique

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***Abstract*—Estimating the impedance of a grid-connected device or of a grid at the point of common coupling is important for evaluating the interaction between them. Impedance measurement involves a perturbation injection device, which perturbs the system, and a measurement device (impedance estimation unit), which acquires the grid voltages and currents to extract the impedance. When evaluating the grid impedance in the *dq* reference frame, the reference frame transformation requires estimating the grid angle. For a self-synchronized impedance estimation unit, angle estimation is typically performed by a phase-locked loop, but the presence of low-frequency voltage perturbations limits the accuracy of the results. This article proposes a method with a new approach, based on an interpolated discrete Fourier transform technique, to extract the grid angle. Conventional phase-locked loop and proposed interpolated-discrete-Fourier-transform-based techniques are compared experimentally and the proposed technique shows more accurate impedance estimation in the low frequency range, for comparable frequency tracking performance.**

***Index Terms*—Grid impedance estimation (IE), interpolated discrete Fourier transform (IpDFT), perturbation injection (PI), phase-locked loop (PLL).**

I. Introduction

THE use of power electronics converters in the grid for interfacing ac and dc grids [1], [2], renewable sources (wind turbine, PV source, etc.) [3], or battery storage systems [4] is growing. However, the power conversion action of those controller-based actively regulating devices may result in instabilities and large harmonic power flows [5] in the grid as reported in several incidents that occurred in Switzerland in 1995 [6], in Germany in 2013 [7], and in France and Spain in 2016 [8], [9]. The origin of those faults is the interaction between the grid and the converters, and more precisely, between the grid impedance and the converter admittances that were not passive in the expected frequency range.

This impedance–admittance interaction, first investigated for dc/dc converters in the 1970s [10], has since then been expanded to the three-phase grid systems [11], [12], [13] and used for converter controller design and impedance/admittance measurements. While the converter impedance can be estimated using small-signal models of the converter [14], the grid impedance is typically unknown at the point of common coupling (PCC) in the grid and, therefore, must be extracted by experimental means. To obtain experimentally an impedance, a typical method is to inject a perturbation (voltage or current) and measure the voltages and currents, as response of the injected perturbations. The voltages' and currents' values over the measurable frequency range are then extracted, allowing impedance computation in the frequency domain.

To perform the perturbation injection (PI) and the impedance extraction, several methods are possible using different sets of devices, as shown in Fig. 1. The perturbation source can either be generated by an ad-hoc converter with low-power requirements [as in Fig. 1(a), (b), and (e)] [15], [16] or be integrated into an existing grid-connected converter on top of its normal operation [as in Fig. 1(c) and (d)] [17], [18]. Similarly, the voltage/current measurements and the impedance estimation (IE) can either be integrated with the PI converter (PIC) [see Fig. 1(a) and (c)] [19] or be processed by an external IE unit (IEU) [as in Fig. 1(b), (d), and (e)] [16], [20].

Estimation of the impedance can be done in different reference frames: abc-frame [21], [22], [23], [24], $\alpha\beta$ (stationary) reference frame, or dq (synchronous) reference frame. In this last case, voltages and currents acquired are transformed in the dq-frame first, using an estimated grid angle, typically obtained with a phase-locked loop (PLL) computed by the PIC [15], [20], [25], [26], [27] or by one featured in the impedance measurement unit (IMU) [18], [28]. The PLL effect on the grid impedance computation has been extensively described in the literature [25], [28], [29]. Because the grid angle estimator (GAE) tracks the angle based on the voltages, perturbations on the grid voltages result in a distorted angle, impacting the grid IE, especially for low frequencies. A tradeoff between good grid angle tracking (large PLL bandwidth) and the quality of grid IE at low frequencies (small PLL bandwidth) must be found. The grid impedance at low frequencies is typically low (mainly comprised of the line resistance term) yet can still play a key role in the grid–converter interaction. It is, therefore, important to correctly estimate it. On the other hand, extensive research has been conducted in the power system community to develop phasor measurement units (PMUs) with high-speed acquisition systems, which can track the grid frequency with

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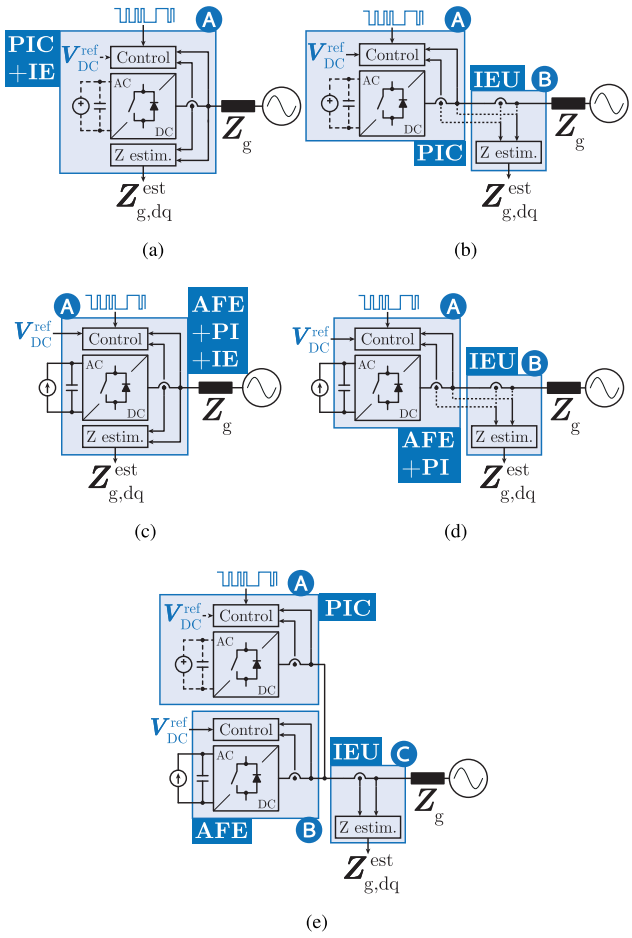

Fig. 1. IE systems: PIC with (a) internal grid IE capability, (b) independent IEU, (c) and (d) power-processing converter (AFE) with PI capability, and (e) power-processing converter, PIC, and independent IEU.

very good precision. Interpolation-based method [interpolated discrete Fourier transform (IpDFT)] has, for instance, been developed to determine accurately the frequency between two discrete Fourier transform (DFT) bins [30], [31]. PMU-based grid impedance measurement methods are also possible [32], [33], [34], [35], [36], but typically rely solely on grid voltage and current measurements, by extracting accurately the phasor at the fundamental frequency, without any perturbation being injected. Since the grid frequency is accurately estimated, by integrating it, it is consecutively possible to accurately estimate the grid angle, allowing for an IE in the dq reference frame. In the meantime, most of the research regarding grid IE relies on a grid angle estimated by real-time devices [16], [20], [26] where those DFT techniques are not conventionally implemented because of their large computational burden. However, when the impedance is estimated offline, after the PI, the estimation is typically performed by computers with a high computational capacity (when compared to embedded devices's computational power) and the objective is, in such applications, to reach high-quality estimation. Proper angle estimation is then key for low-frequency IE and the DFT-based approaches can be considered to improve the grid angle tracking.

This article proposes a technique for an impedance extraction unit (IEU) that can extract impedances in the dq-frame based on PMU phasor estimation techniques. Since the grid angle estimation is performed internally, the IE unit is self-synchronizing. Compared to a conventional PLL-based method with an equivalent grid frequency tracking speed, the proposed IpDFT-based method can estimate the grid impedance accurately for much lower frequencies, and the minimum frequency from which the impedance can be accurately estimated is clearly and simply defined. The rest of the article is organized as follows. In Section II, the effect of the grid angle estimation on the IE is introduced. In Section III, the proposed IpDFT-based method is presented. In Section IV, the experimental setup, including the PIC and the IEU, is described. In Section V, grid impedance is estimated using a state-of-the-art PLL method and the proposed IpDFT-based method as the GAE. Results are compared proving the proposed method to be a viable and convenient solution for gridIE in microgrids. Finally, Section VI concludes the article.

II. Impact of the Grid Angle Estimation on the IE

The IE in the dq frame is strictly linked to the knowledge of the fundamental grid angle. This is determined by a GAE that extracts the grid angle based on the grid voltages. The presence of perturbations (required for the IE) may alter the reliability of the results. This effect is here explained analytically.

Consider grid voltages and currents perturbed by a small-signal perturbation

$$\begin{cases} \boldsymbol{V}_{\mathrm{dq}}(t) = \boldsymbol{V}_{\mathrm{dq},0} + \boldsymbol{v}_{\mathrm{dq}}(t) \\ \boldsymbol{I}_{\mathrm{dq}}(t) = \boldsymbol{I}_{\mathrm{dq},0} + \boldsymbol{i}_{\mathrm{dq}}(t) \end{cases} \tag{1}$$

where $(\boldsymbol{V}_{\mathrm{dq},0}, \boldsymbol{I}_{\mathrm{dq},0})$ are the steady-state operating point and $(\boldsymbol{v}_{\mathrm{dq}}(t), \boldsymbol{i}_{\mathrm{dq}}(t))$ are the small-signal perturbations. Considering a GAE with the characteristic transfer function $G_{\mathrm{GAE}}(s)$

$$\Delta\theta^{\mathrm{cap}}_{\mathrm{g,p}}(s) = G_{\mathrm{GAE}}(s) \cdot \Delta\theta_{\mathrm{g,p}}(s) \tag{2}$$

where $\Delta\theta^{\mathrm{cap}}_{\mathrm{g,p}}(s)$ is the captured grid angle. It can be shown [25] that the GAE has an impact in the voltage and current estimation in the dq reference frame

$$\begin{cases} \boldsymbol{V}^{\mathrm{est}}_{\mathrm{dq}}(s) = \begin{bmatrix} 1 & 0 \\ 0 & 1 - G_{\mathrm{GAE}}(s) \end{bmatrix} \cdot \boldsymbol{V}_{\mathrm{dq}}(s) \\ \boldsymbol{I}^{\mathrm{est}}_{\mathrm{dq}}(s) = \boldsymbol{I}_{\mathrm{dq}}(s) + \begin{bmatrix} 0 & \frac{I_{\mathrm{q},0}}{V_{\mathrm{d},0}} \cdot G_{\mathrm{GAE}}(s) \\ 0 & -\frac{I_{\mathrm{d},0}}{V_{\mathrm{d},0}} \cdot G_{\mathrm{GAE}}(s) \end{bmatrix} \cdot \boldsymbol{V}_{\mathrm{dq}}(s). \end{cases} \tag{3}$$

Hence, the computation of the grid impedance becomes

$$\begin{aligned} \boldsymbol{Z}^{\mathrm{est}}_{\mathrm{dq}}(s) &= \boldsymbol{V}^{\mathrm{est}}_{\mathrm{dq}} \cdot \left(\boldsymbol{I}^{\mathrm{est}}_{\mathrm{dq}}\right)^{-1} \\ &= \begin{bmatrix} 1 & 0 \\ 0 & 1 - G_{\mathrm{GAE}}(s) \end{bmatrix} \\ &\quad \cdot \left(\boldsymbol{Z}^{-1}_{\mathrm{dq}}(s) + \begin{bmatrix} 0 & \frac{I_{\mathrm{q},0}}{V_{\mathrm{d},0}} \cdot G_{\mathrm{GAE}}(s) \\ 0 & -\frac{I_{\mathrm{d},0}}{V_{\mathrm{d},0}} \cdot G_{\mathrm{GAE}}(s) \end{bmatrix} \right)^{-1}. \end{aligned} \tag{4}$$

So, the estimation of $\boldsymbol{Z}_{\mathrm{dq}}$ is impacted by the response of the GAE, modeled by $G_{\mathrm{GAE}}(s)$. For an ideal grid IE, the GAE should have $G_{\mathrm{GAE}}(s) = 0$ for all frequencies, meaning that it should

TABLE I
PLL CONTROLLER GAINS

Gain	Value
t_{set}	100 ms
ξ	$\frac{1}{\sqrt{2}}$
ω_{n}	$\frac{1}{\xi\tau} = \frac{4.6}{\xi t_{\text{set}}} = 65\,\text{rad s}^{-1}$
$K_{\text{P,PLL}}$	$2\xi\omega_{\text{n}} = 92$
$K_{\text{I,PLL}}$	$\omega_{\text{n}}^2 = 4232$

only track the fundamental components of the grid voltages, and completely disregard any perturbation. However, since the GAE must correctly track the slow grid frequency changes, the GAE transfer function must tend to 1 at low frequencies. Therefore, a tradeoff between the transfer function tracking capability ($G_{\text{GAE}} \to 1$ at low frequencies) and good IE ($\boldsymbol{Z}_{\text{dq}}^{\text{est}} \to \boldsymbol{Z}_{\text{dq}}$ for all frequencies) must be found.

A. Conventional GAE: PLL

The conventional methods [15], [25], [28] employed for GAE mostly use PLL to track the grid angle. The selected PLL gains are introduced in Table I, based on two parameters: 1) the settling time t_{set} and 2) the damping ratio ξ.

As presented in the previous section, the estimation of Z_{dq} is impacted by the response of the GAE, modeled by G_{GAE}. Using a simple PLL [37], $G_{\text{GAE}}(s)$ can be written as

$$G_{\text{GAE}}(s) = G_{\text{PLL}}(s) = \frac{K_{\text{P}} \cdot s + K_{\text{I}}}{s^2 + K_{\text{P}} \cdot s + K_{\text{I}}}. \tag{5}$$

The PLL response is a low-pass filter, hence, when used to estimate the impedance in the dq reference frame, the grid impedance is filtered out by the PLL below its cut-off frequency as described and observed in [28]. In other words, in the low frequency range, the PLL would also track the perturbation introduced by the PIC (as $G_{\text{GAE}}(s) \to 1$) and, therefore, would introduce an error for the grid IE as per (4).

So, when tuning the PLL for IE, there is a tradeoff between a large PLL bandwidth frequency (to track fast frequency changes) and a small PLL bandwidth frequency (to track the impedance up to low frequencies). This can be well seen in Fig. 2 where, as t_{set} increases, the PLL minimum frequency $f_{\text{min,PLL}}$ decreases. In this article, the minimum frequency f_{min} is defined as the frequency point beyond which the magnitude is estimated with a $\pm 50\%$ accuracy.

Considering the injection of a perturbation with zero grid currents (no load steady-state conditions: $I_{\text{d},0} = 0, I_{\text{q},0} = 0$), according to (4) the grid impedance $Z_{\text{qq}}^{\text{est}}(s)$ would be

$$Z_{\text{qq}}^{\text{est}}(s) = (1 - G_{\text{PLL}}(s)) \cdot Z_{\text{qq}}(s). \tag{6}$$

So, in such conditions, the IE minimum frequency (beyond which the impedance is correctly estimated with a $\pm 50\%$ accuracy) is equal to the transfer function PLL minimum frequency $f_{\text{min,PLL}}$.

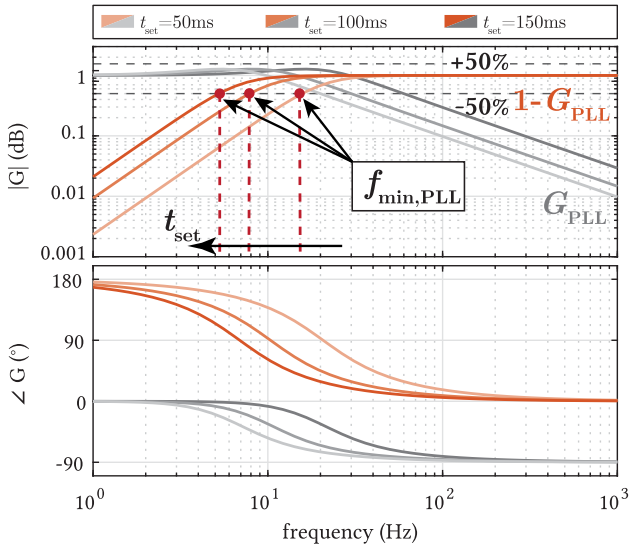

Fig. 2. Bode plot of the PLL transfer functions G_{PLL} and $1 - G_{\text{PLL}}$ for the PLL gains of Table I.

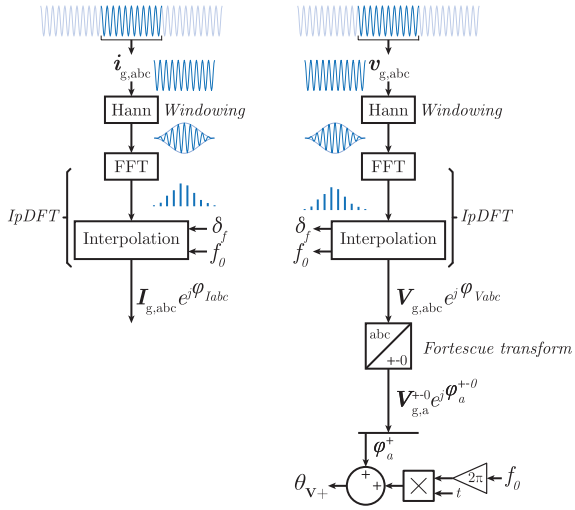

Fig. 3. Procedure for the IpDFT-based GAE. 1) Grid voltages are used to determine the grid voltage phasors and the grid frequency. 2) Grid frequency is then used to determine the grid current phasors. 3) Voltage phasor positive sequence is extracted to compute the grid angle.

III. IPDFT-BASED GRID ANGLE ESTIMATION

The proposed GAE aims at solving some of the PLL bandwidth limitations for IE: its high bandwidth frequency value and the dependence on multiple parameters (ξ, t_{set} for a simple PLL). In this article, we propose the use of the IpDFT method, developed for PMUs [30], [31] but never used before for grid IE. The working principle of the proposed approach is described hereafter.

A. Principle of the Method

In Fig. 3, the procedure for the IpDFT-based GAE is presented. It is based on a three-step procedure. First, the grid voltage and current measurements are windowed. Then, an

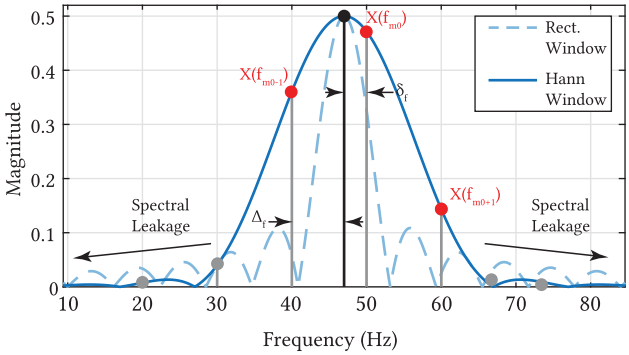

Fig. 4. Example of a frequency waveform of a pure 47-Hz sinusoid with a Hann window and a rectangular window.

FFT extracts the frequency components, and based on those, an interpolated IpDFT technique determines the grid frequency and the voltage and current phasors. Finally, the positive sequence phasor is extracted and used to compute the grid angle.

1) Windowing: To track precisely the grid frequency, the grid voltages are windowed around a small, moving, window of a few fundamental grid periods (2 to 10), with an update time T_{UP} of typically 1ms. This allows us to track the grid fundamental frequency f_{g} and voltage and current magnitudes $I_{\mathrm{g,abc}}$ and $V_{\mathrm{g,abc}}$ precisely over the whole PI time (here 8 s).

A Hann windowing [38] is applied to the sampled $V_{\mathrm{g,abc}}$ and $I_{\mathrm{g,abc}}$ to minimize the spectral leakage. Indeed, as shown in Fig. 4, the spectral energy of a pure sinusoid is more concentrated when a Hann window is applied than when a simple rectangular window is applied. Other windows can be used offering similar performance [39], [40]. An FFT is then applied to the windowed data around the grid frequency. Assuming that we are in a grid with known nominal grid frequency $f_{0,\mathrm{nom}}$ and with a maximum recordable time, or window time, T_{W} of 8 s, the frequency step between two bins Δ_{f} would be

$$\Delta_{\mathrm{f}} = \frac{1}{T_{\mathrm{W}}} \rightarrow \Delta_{\mathrm{f,MAX}} = \frac{1}{8} = 0.125 \text{ Hz}. \tag{7}$$

This precision is far below the potential variations of a conventional grid, where f_{g} would vary typically by tens of millihertz at most. Furthermore, an error in the grid angle estimation can lead to improper IE. To determine precisely the grid frequency, an interpolation technique can be employed to determine the grid frequency between two bins.

2) Interpolated DFT: IpDFT techniques have been developed by power system researchers and engineers [30], [31] for increasing the precision of the phasor identification of the grid PMUs.

The grid voltages are mainly sinusoids and small signal perturbations should not affect the overall grid voltage sinusoidal shape. As shown in Fig. 4, the DFT of a Hann-windowed sinusoid follows a certain curve. This curve is described as

$$X(k) = X((f - f_0) \cdot T_{\mathrm{W}}) = \frac{1}{2} \cdot \frac{\mathrm{sinc}(k)}{1 - k^2} \tag{8}$$

where k is the kth bin of the DFT.

Therefore, based on the two highest bins (here $X(f_{\mathrm{m0}})$ and $X(f_{\mathrm{m0\pm1}})$), by using the curve formula, it is possible to determine the fundamental frequency of a grid voltage V_{g} of unknown frequency [30], [31]

$$\begin{cases} f_{\mathrm{g},i} = (m0 + \delta^{\mathrm{est}}_{\mathrm{f},i}) \cdot \Delta f \\ \delta^{\mathrm{est}}_{\mathrm{f},i} = \epsilon \cdot \frac{2|V_{\mathrm{g},i}(m0+\epsilon)| - |V_{\mathrm{g},i}(m0)|}{|V_{\mathrm{g},i}(m0+\epsilon)| + |V_{\mathrm{g},i}(m0)|} \end{cases} \quad \text{for } i = \{a, b, c\}$$

$$\text{where } \epsilon = \begin{cases} +1 \text{ if } |V_{\mathrm{g},i}(m0+1)| > |V_{\mathrm{g},i}(m0-1)| \\ -1 \text{ if } |V_{\mathrm{g},i}(m0+1)| < |V_{\mathrm{g},i}(m0-1)| \end{cases}. \tag{9}$$

The frequency deviation is then averaged over the three phases a, b, and c to increase the precision

$$\Delta^{\mathrm{est}}_{\mathrm{f}} = \frac{\delta^{\mathrm{est}}_{\mathrm{f,a}} + \delta^{\mathrm{est}}_{\mathrm{f,b}} + \delta^{\mathrm{est}}_{\mathrm{f,c}}}{3} \tag{10}$$

and the estimated phasor $V^{\mathrm{est}}_{\mathrm{g},i} e^{j\angle V^{\mathrm{est}}_{\mathrm{g},i}}$ is

$$\begin{cases} |V^{\mathrm{est}}_{\mathrm{g},i}| = |V_{\mathrm{g},i}(m0)| \cdot \left| \frac{\pi \Delta^{\mathrm{est}}_{\mathrm{f}}}{\sin(\pi \Delta^{\mathrm{est}}_{\mathrm{f}})} \right| \cdot \left| (\Delta^{\mathrm{est}}_{\mathrm{f}})^2 - 1 \right| \\ \angle V^{\mathrm{est}}_{\mathrm{g},i} = \angle V_{\mathrm{g},i}(m0) - \pi \cdot \Delta^{\mathrm{est}}_{\mathrm{f}} \end{cases}. \tag{11}$$

3) Phasor Computation: As the phasors and the frequency are computed, the grid angle can be computed, based on the positive sequence phase a angle Φ^{+}_{a}. The Fortescue transform is applied to the grid voltage phasor $V_{\mathrm{g,abc}} e^{j\Phi_{\mathrm{g,abc}}}$ to obtain the phasor decomposition in the positive, negative, and zero sequences

$$\boldsymbol{V}_{\mathrm{g},+-0} e^{j\angle V_{\mathrm{g},+-0}} = \frac{1}{3} \cdot \begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix} \cdot \boldsymbol{V}_{\mathrm{g,abc}} e^{j\angle V_{\mathrm{g,abc}}} \tag{12}$$

with $\alpha = e^{j\frac{2\pi}{3}}$.

And the grid angle then becomes

$$\theta^{+}_{\mathrm{V}} = 2\pi f_0 t + \angle V_{\mathrm{g,a+}}. \tag{13}$$

The reason for using the phasor decomposition is not to extract the positive sequence (as we assume a balanced three-phase system) but instead to minimize the phase estimation error. In a balanced three-phase system, the positive sequence phase $\angle V_{\mathrm{g,a+}}$ is equal to the phase of the grid voltage a $\angle V_{\mathrm{g,a}}$. However, as we have computed the phase for the three phases, we can reduce the grid phase estimated error by utilizing the three grid angle phases, as

$$\angle V^{+,\mathrm{est}}_{\mathrm{g,a}} = \angle V^{\mathrm{est}}_{\mathrm{g,a}} + \left(\angle V^{\mathrm{est}}_{\mathrm{g,b}} + \frac{2\pi}{3} \right) + \left(\angle V^{\mathrm{est}}_{\mathrm{g,c}} - \frac{2\pi}{3} \right). \tag{14}$$

B. Parameters Selection

So, when the IpDFT is employed to estimate the grid angle, only three parameters have to be tuned: 1) the window size T_{W}, 2) the sampling frequency f_{S}, and 3) the update time T_{UP}. To select the parameter values, a perturbation is injected in the q-axis grid voltage and the grid angle is estimated with the proposed method. The perturbation is a single-tone, low-frequency (5 Hz), low-magnitude (10 V) signal and the perturbation is injected

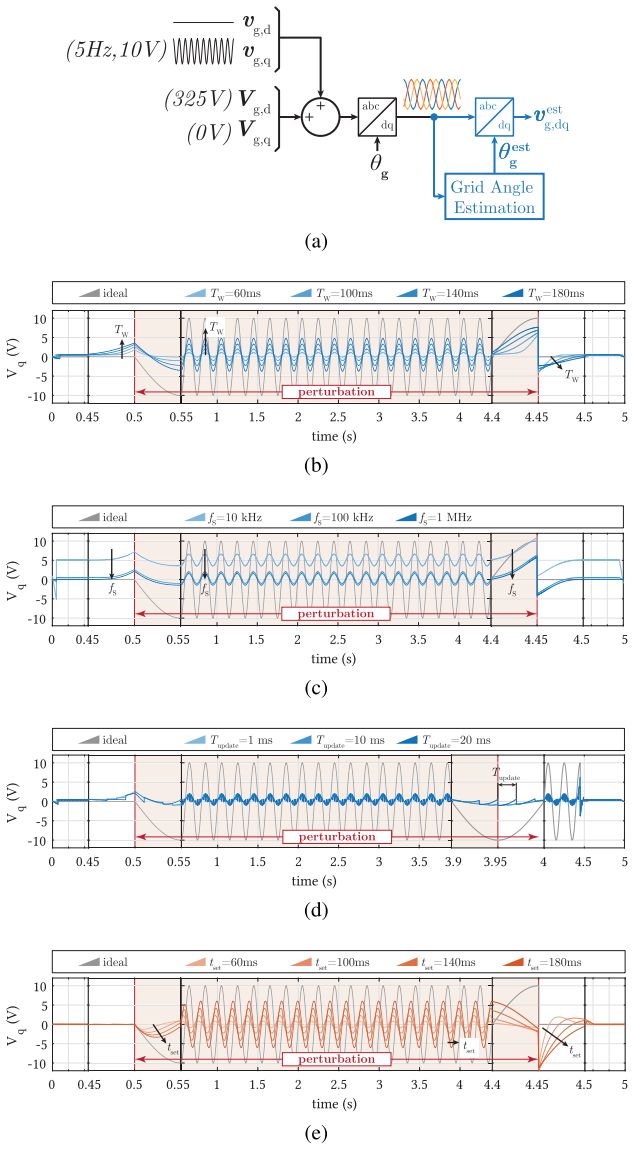

Fig. 5. V_q estimation using the IpDFT-based GAE technique during a 4.55-s perturbation (low frequency, low-magnitude single-tone signal). (a) and (b) Windowing time selection. (c) Sampling frequency selection. (d) Update time selection. (e) Comparison with a PLL-based GAE estimation for different settling times t_{set}.

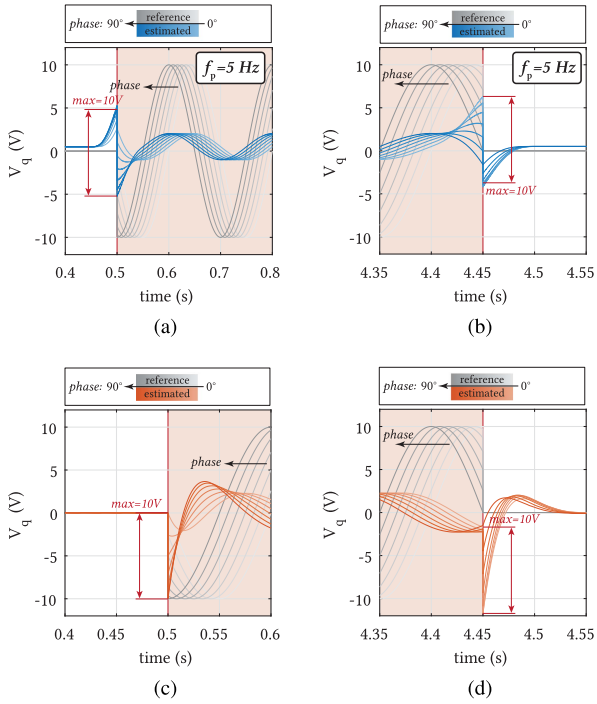

Fig. 6. Beginning and ending times of V_q estimated during a single-tone perturbation in the grid voltage q-axis for different phase angles using (a) and (b) the IpDFT and (c) and (d) the PLL techniques to estimate the grid angle.

during 0.95 s between the time 0.5 s and 4.45 s. The parameters selection must ensure reliable grid angle estimation tracking, meaning maintaining V_q close to 0 V.

1) *Window time selection:* As shown in Fig. 5(b), when the perturbation is injected, a small V_q overshoot is observed. The larger the window time is, the larger and longer this overshoot is. Meanwhile, the larger the window time is, the smaller the V_q magnitude is. The same is observed at the end of the PI. This results in a tradeoff where the window time must be selected small enough to reduce the initial and final overshoots while ensuring a large enough V_q magnitude for the desired frequency range of interest. In this example, a 100-ms time window is selected.
   This initial and final overshoot is dependent on two parameters: 1) the initial and 2) final perturbation phase and the window time width (or equivalently the settling time for the PLL). As shown in Fig. 6, a large initial or final phase can result in an overshoot of up to the perturbation signal magnitude in the case of a 90° phase. The length of the overshoot is however dependent solely on the window time. The initial and final overshoot widths are $\frac{T_W}{2}$, as witnessed in Fig. 5(b).
2) *Sampling frequency selection:* The IpDFT frequency (and phase) estimation error is mainly caused by the interference of the negative image, which is amplifying low-frequency bins magnitude. To reduce this effect, a larger sampling frequency can be employed. However, a higher sampling frequency would increase both the memory requirements and the computational burden for the postprocessing; therefore, a tradeoff must be found. As it can be seen in Fig. 5(c), at 100 kHz and 1 MHz sampling frequency, the voltage estimation is very close to 0, so a 100 kHz sampling frequency is selected.
3) *Update time selection:* Short update time allows for grid frequency and phase corrections at a high frequency. Large update time can reduce the computational burden but at the expense of potentially large errors on the grid angle estimation, caused by the error in the grid frequency. This, therefore, causes errors in the grid voltage estimation V_q, as shown in Fig. 5(d). An update time of 1 ms is selected as it does not show large V_q ripple or errors, compared to higher values.

All the selected values in this example have been summarized in Table II .

TABLE II
IPDFT PARAMETERS SELECTION VALUES

Steps	T_{W}	f_{S}	T_{UP}
1) T_{W} selection	[60 ms **100 ms** 140 ms 180 ms]	f_{S}=10 kHz	1 ms
2) f_{S} selection	**100 ms**	[10 kHz **100 kHz** 1 MHz)]	1 ms
3) T_{UP} selection	**100 ms**	**100 kHz**	[**1 ms** 10 ms 20 ms]

*Note 1: Corresponds to $(3-9\cdot T_{0,\mathrm{nom}})$.
Note 2: Selected values are in ***bold*.

As a comparison, PLL-based grid angle estimation is also performed and it shows similar overshoots at the end of the injection, which decreases in magnitude with the settling time. Compared to the IpDFT-based method, no overshoot is observed in the initial estimation but a certain time is necessary for V_{q} to settle at its nominal magnitude. And during operation, the grid voltage also has a delay that is dependent on the settling time, which is not the case of the IpDFT-based grid angle estimation. An initial comparison of the PLL-based and the IpDFT-based grid angle estimation can already be made, which is as follows.

1) At the beginning of the injection, a voltage overshoot is observed prior to the injection time when the IpDFT-based GAE is used.
2) During the injection, a voltage dephasing is observed when the PLL is used but not when the IpDFT-based GAE is used.
3) At the end of the injection, voltage overshoots are observed for the two grid angle estimation methods but the PLL provokes much larger and longer overshoots (equal to the settling time for the PLL and half the window time for the IpDFT).

C. Transfer Function

As shown in Fig. 5(b) for a single frequency, when an IpDFT-based GAE is used, the voltage $V_{\mathrm{g,q}}$ magnitude increases with the window time, however, no phase delay appears.

To evaluate the effect of the IpDFT-based GAE on a wide range of frequencies, the process shown in Fig. 7(a) is applied, with a wideband perturbation (chirp signal from 1 to 100 Hz) injected in the grid angle, generating a perturbed grid voltage that is then fed to the GAE. A fast Fourier transform (FFT) is then applied to the angle perturbation $\Delta\theta_g$ and the estimated grid angle perturbation $\Delta\theta_g$. The division of the two gives the equivalent transfer function, illustrating the impact of the GAE on the angle estimation for different frequencies.

The result is drawn in Fig. 7(b). As it can be seen, the IpDFT, similar to the PLL acts as a low-pass filter, with very small magnitudes of $1-G_{\mathrm{IpDFT}}$ for low frequencies but a magnitude closer to 1 for higher frequencies (above 20 Hz). The phase is always equal to 0, also observed for 5 Hz in Fig. 5(b).

This transfer function is estimated by the following analytical expression:

$$G_{\mathrm{IpDFT}}^{\mathrm{MODEL}}(s)=\frac{1}{sT_{\mathrm{W}}}\cdot\left(e^{\frac{sT_{\mathrm{W}}}{2}}-e^{-\frac{sT_{\mathrm{W}}}{2}}\right)\cdot\frac{\left(\frac{2\pi}{T_{\mathrm{W}}}\right)^2}{s^2+\left(\frac{2\pi}{T_{\mathrm{W}}}\right)^2}. \tag{15}$$

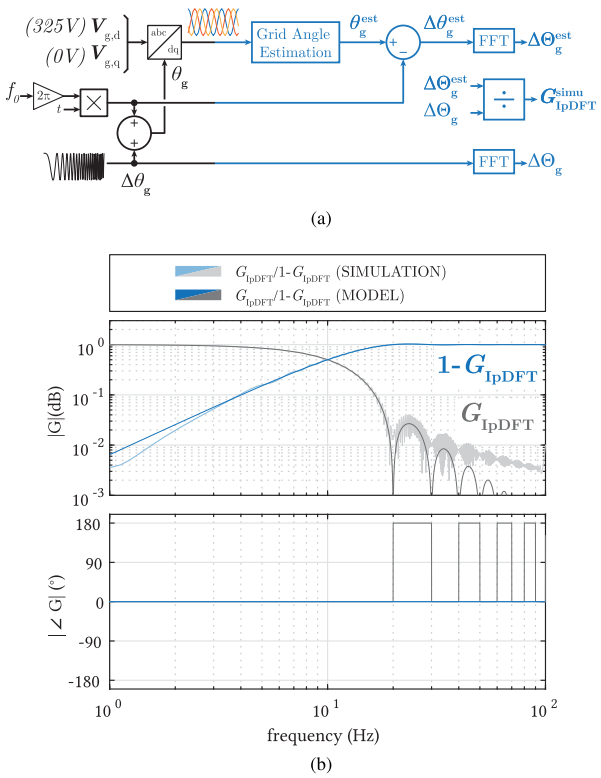

Fig. 7. IpDFT-based GAE transfer function. (a) Estimation process. (b) Transfer function model and simulation result comparison.

This transfer function is given by the product of the following two terms.

1) The first term represents the transfer function of an ideal moving average filter over a time window of length T_{W} (with the window centered between $t-T_{\mathrm{W}}/2$ and $t+T_{\mathrm{W}}/2$) and is responsible for all the antiresonances at the multiple integers of $\frac{1}{T_{\mathrm{W}}}$.
2) The second term is a resonance pole that takes into account the nonideal filtering at the frequency $\frac{1}{T_{\mathrm{W}}}$.

As can be noted, there is a good matching between the numerical data and the approximated formula. This transfer function with then be used to compensate the effect of the GAE, following the same approach as the works in [25] and [28] for the PLL.

IV. IMPEDANCE ESTIMATION UNIT

A. Procedure

A conventional method for the impedance measurement [20] shown in Fig. 8 is to inject two orthogonal perturbation signals in the grid line currents (typically in the d-axis and then

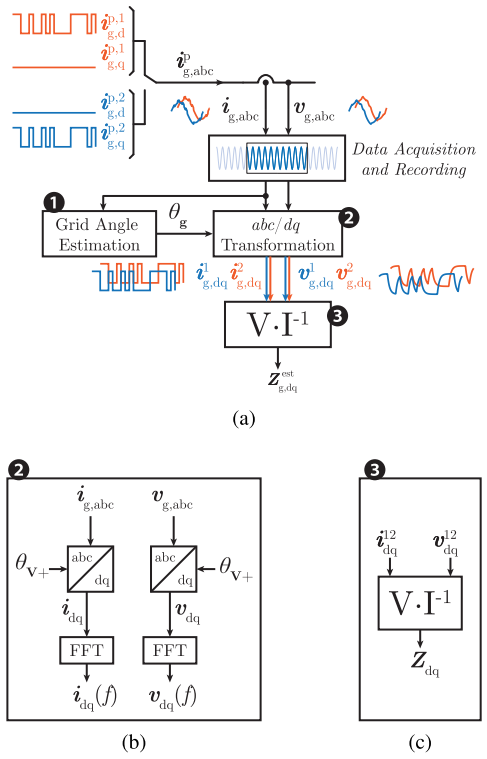

Fig. 8. Impedance measurement procedure. (a) Full procedure. (b) Detailed procedure for the abc/dq transformation. (c) Detailed procedure for the impedance computation.

in the q-axis) and then measure the perturbed voltages and currents and estimate the grid impedance. Various PI signals, sine-sweeps [19], single [17], and multitone signals [41] can be employed. However, when fast IE is required, pseudorandom binary signals (PRBS), with rich frequency content, are employed [18], [20]. An additional benefit of using such signals in this study is the concentration of the spectral power density in the low-frequency region [16]. Hence, in this study, a 2-A, 1-kHz PRBS12 (PRBS with a 12-b shift register [42]) signal is injected in the d and q current references. The grid impedance is estimated in the dq reference frame based on a three-step process illustrated in Fig. 8(a).

1) The grid angle is estimated with a GAE.
2) The measured voltages and currents $(\boldsymbol{v}_{\mathrm{g,abc}}, \boldsymbol{i}_{\mathrm{g,abc}})$ are transformed in their dq components $(\boldsymbol{v}_{\mathrm{dq}}, \boldsymbol{i}_{\mathrm{dq}})$ and the frequency components are extracted. The abc/dq transformation procedure is described in Fig. 8(b). The voltages and currents are first transformed in their dq components using the Clarke-Park transform

$$\boldsymbol{x}_{\mathrm{dq}} = \boldsymbol{T}_{\mathrm{abc\to dq}} \cdot \boldsymbol{x} f_{\mathrm{abc}} \tag{16}$$

where

$$\boldsymbol{T}_{\mathrm{abc\to dq}} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix}. \tag{17}$$

TABLE III
BASE VALUES FOR THE SYSTEM PARAMETERS

Parameter	Value
f_{g}	40.90 Hz
V_{g}	325 V
Z_{g}	1 Ω
f_{S}	100 kHz
t_{set}	100 ms
ξ	$\frac{1}{\sqrt{2}}$
T_{W}	100 ms
T_{UP}	1 ms

An FFT is then applied to the data.

3) The impedance is estimated using the data for both perturbation signals. Two sequential independent signals [27] are injected as grid current small-signal perturbations $\boldsymbol{i}^{p}_{\mathrm{g,dq}}$. By acquiring the voltage response $\boldsymbol{v}^{p}_{\mathrm{g,dq}}$, the grid impedance is then computed as

$$\boldsymbol{Z}_{\mathrm{g,dq}} = \begin{bmatrix} Z_{\mathrm{g,dd}} & Z_{\mathrm{g,dq}} \\ Z_{\mathrm{g,qd}} & Z_{\mathrm{g,qq}} \end{bmatrix} = \boldsymbol{V}_{\mathrm{g,dq}} \cdot \boldsymbol{I}^{-1}_{\mathrm{g,dq}} \tag{18}$$

where

$$\boldsymbol{V}_{\mathrm{g,dq}}(f) = \begin{bmatrix} v^{1}_{\mathrm{g,d}} & v^{2}_{\mathrm{g,d}} \\ v^{1}_{\mathrm{g,q}} & v^{2}_{\mathrm{g,q}} \end{bmatrix}, \boldsymbol{I}_{\mathrm{g,dq}}(f) = \begin{bmatrix} i^{1}_{\mathrm{g,d}} & i^{2}_{\mathrm{g,d}} \\ i^{1}_{\mathrm{g,q}} & i^{2}_{\mathrm{g,q}} \end{bmatrix}. \tag{19}$$

B. Experimental Setup

Results in this article are all based on experimental data from experiments conducted with the setup pictured in Fig. 9. The setup is composed of three elements: 1) a grid emulator, 2) a PIC, and 3) an IEU at the PCC between the converter and the grid emulator, as illustrated in Fig. 9(a). The grid emulator, pictured in Fig. 9(d), is based on the Regatron TC ACS grid simulator device controlled by a Plexim RT-Box device. Current measurements of the TC.ACS are read by the RT-Box that, according to the desired grid impedance, computes and generates analog voltage references for the TC.ACS device. By having the scheme of a grid with a certain grid impedance $\boldsymbol{Z}_g$ (pure resistance, in-series R+L, etc.) in the RT-Box, it is possible to emulate the grid behavior with any impedance value (compatible with the bandwidth of the power hardware: The total delay time is around 135μs so the system can emulate an impedance correctly up to 1.5 kHz ($\frac{1}{5 \cdot T_{\mathrm{W}}}$). The PI has been integrated on top of an active front-end (AFE) performing a standard control of the dc voltage and reactive power. The AFE current control bandwidth is around 1 kHz. PRBS signals are superimposed to the d and q axes current references (axes are determined by an internal PLL). Fig. 9(b) presents the PIC internal elements.

The IEU, illustrated in Fig. 9(c) is based on measurements from LEM IT 60-S Ultrastab current transducers and LEM CV 3-1000V 1:100 voltage modules. The acquisition device is a 32 14-b channels Elsys Tranet 408S. Data are sampled at a sampling rate of 20 MS/s; an averaging is performed using a 100-kHz

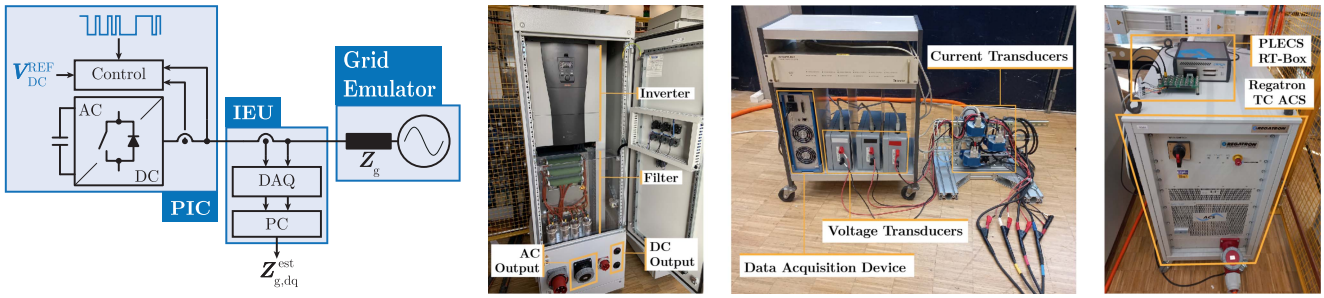

Fig. 9. Impedance measurement setup. (a) Scheme of operation, with (b) the PIC injecting currents perturbations into the grid, (c) an IEU measuring and recording the currents and voltages and computing the estimated impedance, and (d) the grid emulator (Regatron TC ACS) emulating a grid with a given $\boldsymbol{Z}_g$.

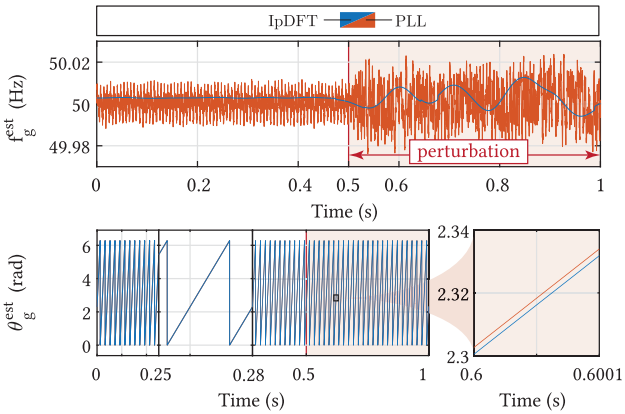

Fig. 10. PLL and IpDFT-based grid frequency and angle estimation before and during voltage perturbation (in the q-axis).

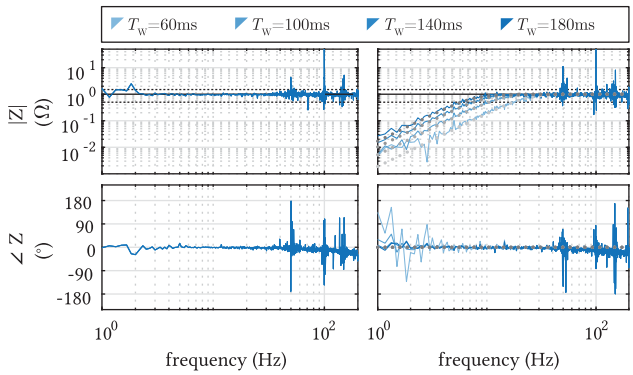

Fig. 11. IpDFT-based IE for different window sizes T_{W}, in dotted line: $1 - G_{\mathrm{IpDFT}}^{\mathrm{MODEL}}$.

antialiasing filter, leading to an effective sampling frequency of 1 MHz. Memory size allows a maximum recording time of 8 s.

V. Impedance Estimation Using IpDFT

The IpDFT-based grid angle estimation method presented in Fig. 3 is compared to the offline PLL method presented in the previous section using the standard parameters defined in Table III. To be comparable, the IpDFT and the PLL methods use the same sampling frequency (100 kHz) and the IpDFT uses a window time equivalent to the PLL settling time (100 ms). A 1-kHz PRBS signal of 2-A magnitude is injected in the grid by the AFE. The methods are then compared for different emulated grid impedances.

A. Frequency and Angle Tracking for PLL and IpDFT Methods

The PLL and IpDFT grid angle estimation tracking performance is presented in this section. As described in Section II, when a perturbation occurs in the q-axis of the voltage, the grid angle estimation is also perturbed. To illustrate the equivalent performance of the PLL and IpDFT in their function, the angles tracked by a PLL and by an IpDFT are drawn in Fig. 10. What can be noticed first is the large ripples in the frequency estimation of the PLL (up to 100 mHz), whereas the IpDFT-based technique is much more stable but has a small bias (around 70 mHz). When, at 0.5 s, a 2-V 1-kHz perturbation is injected in the q-axis grid voltage, the frequency estimation is visibly disturbed by the perturbation with a grid frequency perturbed up to 20 mHz. However, the resulting perturbation in the grid angle is not very visible, and both the PLL and the IpDFT-based techniques ensure good overall grid angle tracking.

To conclude, the PLL and the IpDFT seem to perform their grid angle estimation similarly with some small differences in terms of ripple and oscillation magnitudes. To evaluate the impact of those in the IE, in the following section, an impedance is estimated using the IpDFT-based technique.

B. Effect of the IpDFT Parameters on the IE

The parameters of the IpDFT modify the response of the GAE as described in Section III-C and, hence, impact the IE. Two IpDFT parameters are to be investigated: T_{W}, because it acts on the IpDFT response, and f_{S}, because it affects the time resolution. Since the grid frequency is stable, the update time does not have any direct impact on the IE, and the value defined in Table II is used (1 ms). To evaluate the impact of the parameters, a purely resistive grid impedance of 1 Ω is emulated by the grid emulator and a 1-kHz 2-A PRBS signal is injected in the grid.

As observed in Figs. 11 and 12, the grid IE in Z_{qq} is distorted following the same tendency as the PLL (−20 dB/dec below a

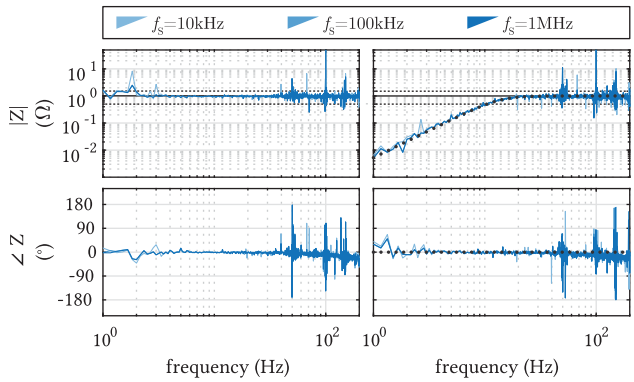

Fig. 12. IpDFT-based IE for different sampling frequencies f_S, in dotted line: $1 - G_{\text{IpDFT}}^{\text{MODEL}}$.

minimum frequency f_{min}) for the magnitude but it has no impact on the phase (the PLL, on the other hand, dephases the angle by 90°). This is well predicted by the estimated IpDFT transfer function derived in Section III-C and drawn in the figure. The effect of the sampling frequency is also investigated in Fig. 12 and it can be seen that above 100 kHz, it has a very minor impact in the grid IE.

C. GAE Effect Compensation

As the impact of the GAE on $Z_{\text{qq}}^{\text{est}}$ can be well predicted and modeled, it can also be compensated following

$$Z_{\text{qq}}^{\text{est,comp}}(j\omega) = (1 - G_{\text{GAE}}(j\omega))^{-1} \cdot Z_{\text{qq}}^{\text{est}}(j\omega). \tag{20}$$

The compensated 1 Ω impedance is compared to the noncompensated impedance in Fig. 13 using both a PLL or an IpDFT as a GAE. The compensation algorithm corrects accurately the impedance for both GAE techniques with a Z_{qq} now contained around 1 Ω even at low frequencies. However, one can notice the small ripple at low frequency (1–5 Hz). To evaluate this noise, two indicators are used: 1) the maximum magnitude error and 2) the impedance variance. Both of those indicators are evaluated on $|Z_{\text{qq}}|$ in the [2 Ω, 10 Ω] frequency range for different window times. In Fig. 14, the results for a pure resistive grid impedance of 1 Ω are plotted. Above 400 mHz, both indicators show better results when the IpDFT-based GAE is used. For instance, using a window time or a settling time of 800 ms, the maximum error on the impedance is of 225 mΩ for the PLL and 194 mΩ for the IpDFT (-13%) and the impedance variance is of 3.3 mΩ and 2.4 mΩ (−27%).

To confirm this tendency for the IpDFT-based GAE to perform better in the low frequency range, the variance indicator is applied to other grid impedances.

D. Performance With Different Grid Impedances

The IE has been performed on various passive grid impedances, with different low-frequency and high-frequency impedance characteristics. First, different resistance values for a pure resistive grid impedance have been emulated, ranging from 0.5 to 2 Ω. Resulting impedances are plotted in Fig. 15(b)

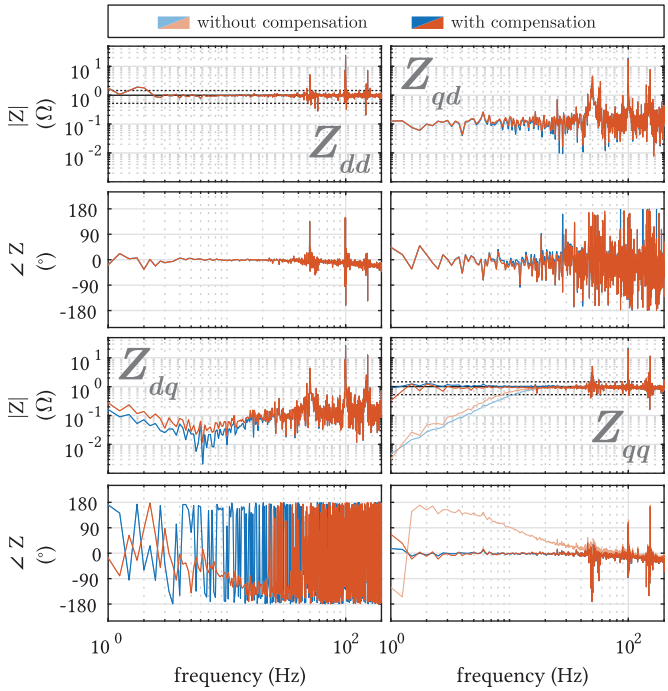

Fig. 13. IpDFT-based and PLL-based IE without and with compensation, $Z_g = R = 1\ \Omega$.

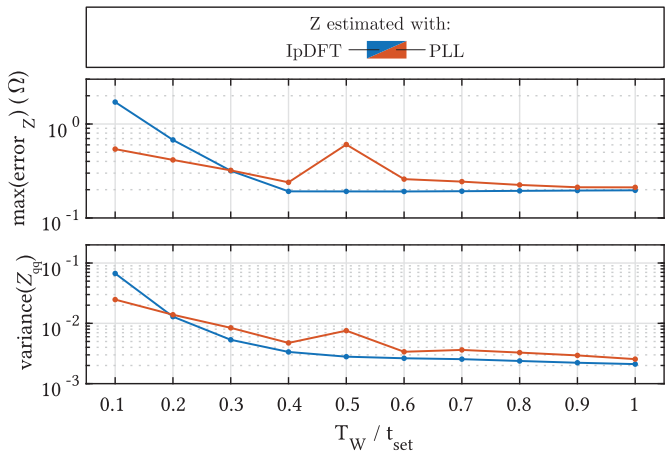

Fig. 14. Maximum error and variance on the impedance (from 2 to 100 Hz using a PLL-based GAE or an IpDFT-based GAE), $Z_g = R = 1\ \Omega$.

for a window time or a settling time of 400 mΩ. The impedance variance has been plotted in Fig. 15(a). As it can be seen, similar trends as what has been seen in Fig. 14, with a variance that decreases with the window time and that is generally larger for the PLL than for the IpDFT, beyond 200 ms and 400 ms. Using the IpDFT-based GAE, and comparing to the PLL, for the 0.5 Ω impedance, the estimation is up to 18% better (for a window time of 400 ms). For the 1 Ω impedance, the estimation is better by 20%–40% above 300 ms, and for the 2 Ω impedance, the estimation is better by 30%–300%.

An RL impedance is then emulated with the grid emulator and estimated in Fig. 16(b). With such impedance, the variance

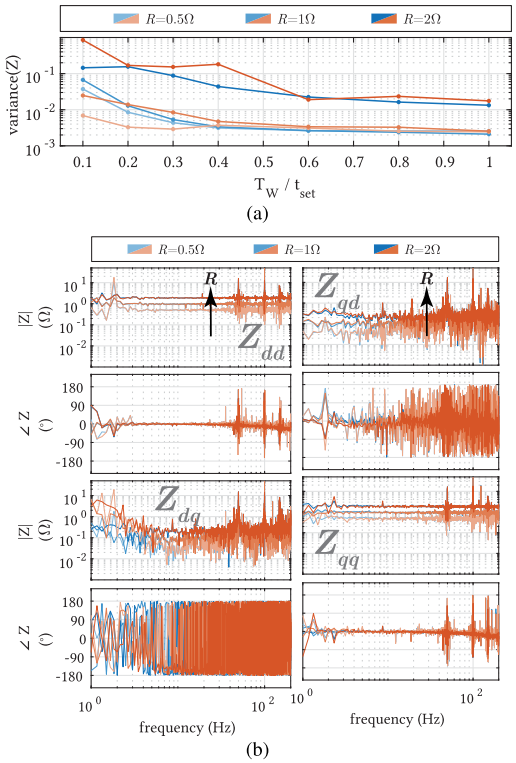

Fig. 15. PLL-based and IpDFT-based IE for different impedances $Z_g = R = \{0.5\,\Omega, 1\,\Omega, 2\,\Omega\}$. (a) Variance on the impedance. (b) Impedance for $T_W/t_{set} = 400$ ms.

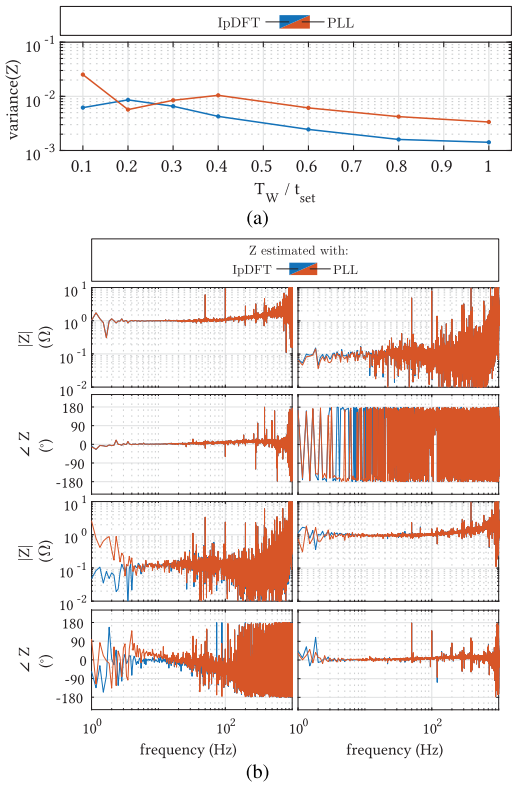

Fig. 16. PLL-based and IpDFT-based IE for an inductive impedance: $Z_g = R_g + j\omega_g L_g$. $R_g = 1\ \Omega$, $L_g = 300\ \mu$H. (a) Variance on the impedance. (b) Impedance for $T_W/t_{set} = 400$ ms.

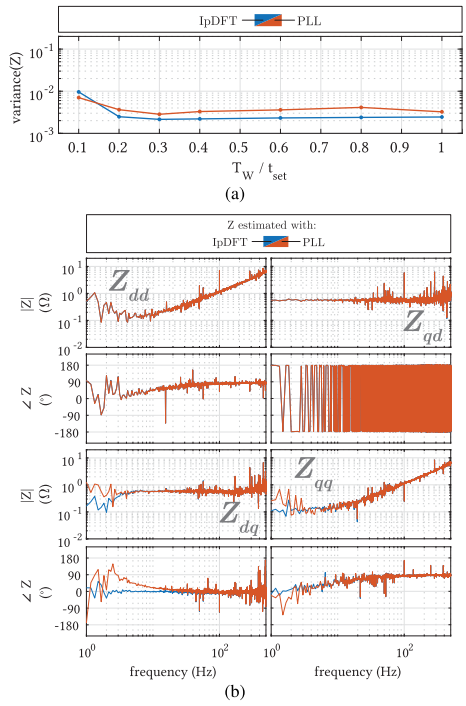

Fig. 17. PLL-based and IpDFT-based IE of an *LC* filter (EPCOS B84143V003R127). (a) Variance on the impedance. (b) Impedance for $T_W/t_{set} = 400$ ms.

is also much larger (from 130% and up to 160%) beyond 300 ms for the PLL-based estimated impedance, when compared to the IpDFT-based one.

Finally, to confirm results when using a grid emulator, a real grid impedance has been used. An *LC* filter from EPCOS has been inserted between the grid emulator and the IEU. In Fig. 17(b), the estimated *LC* filter impedance is plotted with a very low impedance at low frequencies (around 100 mΩ). As shown in Fig. 17(a), the variance is also larger when the PLL is used compared to when the IpDFT-based GAE is used. Using the IpDFT as a grid angle estimator, the variance on the impedance is reduced by 32%–72%.

Those results, using different impedances with different low frequency impedance values (ranging from 100 mΩ to 2 Ω), confirm that the IpDFT-based method shows better results in the low frequency range compared to the conventional PLL-based method.

VI. Conclusion

Self-synchronizing impedance measurement (grid frequency is tracked based on the acquired grid voltages) in the dq frame is unreliable at low frequencies due to the effect of the GAE, which causes distortion and large noise in Z_{qq} at low frequency, depending on its bandwidth. A tradeoff between fast grid angle tracking and good IE must, therefore, be found.

Conventionally, a PLL is used to track the grid angle; however, the impedance quality at low frequencies is not very good with relatively large noise levels, indicated by a large impedance variance.

The GAE proposed in this article uses an IpDFT technique, which computes the grid frequency based on an interpolation of bins of a Fourier transform around the fundamental frequency. This method shows similar transfer function properties as the PLL and can, hence, similarly be compensated. However, the resulting impedance shows a higher quality in the estimation, with lower variances, for all types of impedances estimated and different low-frequency impedance values. This method can, thus, serve as a good GAE for IE.

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