Improved Isolated Four-Switch Three-Level Soft-Switching Half-Bridge DC-DC Converter

José Luiz Saviel Geraldis, Claudinor Bitencourt Nascimento, *Member, IEEE*, and Eloi Agostini Jr., *Member, IEEE*

***Abstract*—This article proposes an improved isolated four-switch three-level half-bridge dc–dc converter suitable for high-input-voltage applications. The primary switches operate under zero voltage switching (ZVS) for a wide load range, which is accomplished by the inclusion of an auxiliary inductance in the circuit. In addition, the conditions necessary to ensure zero current switching (ZCS) for the output rectifiers are determined. A detailed mathematical analysis is carried out, allowing the proper design of the circuit. Output voltage control and input voltage balance are also investigated in detail. The analyses are validated by experimental tests performed with a 1 kW prototype, operating at 100 kHz, with an input voltage range of 700–800 V and output voltage of 400 V. Efficiency levels up to 96.13% and higher than 90% for the entire output power range of 20%–100% are demonstrated in laboratory.**

***Index Terms*—DC-DC converter, t-type, three-level (TL) converter, zero voltage switching (ZVS).**

I. Introduction

MEDIUM- and high-voltage direct-current (dc) systems are becoming a popular choice for efficient electrical energy distribution [1]. In this sense, dc–dc converters capable of operating at high input voltage are required to adjust voltage levels in order to meet the requirements of many end-user applications. However, high-voltage-rating semiconductor devices are known to have a poorer performance than their low-voltage counterparts, which imposes a challenge for designing efficient high-voltage power converters. This drawback has led to the proposal of several circuit configurations, in which the semiconductor devices are subjected to reduced voltage levels [2].

Three-level (TL) converters emerge as prominent solutions in the field, as most of them are capable of dividing the voltage on the semiconductors by half. The TL dc–dc converter was firstly introduced in [3] and [4], and was based on the neutral-point-clamping (NPC) cell. Other NPC-based alternatives were proposed by researchers worldwide. In [5], the TL-NPC dc–dc converter was adapted to operate under phase-shift modulation, and a further modification considering an additional active switch was proposed in [6] to improve the switching conditions and avoid the severe parasitic oscillations verified in the conventional configuration. The NPC cell was further investigated in resonant [7], full-bridge [8], [9], [10], and three-phase [11], [12] dc–dc converters.

An alternative to the TL-NPC was introduced in [13], known as the four-switch half-bridge three-level (HBTL) dc–dc converters. This solution also provides voltage division on the semiconductors but does not require two clamping diodes if compared with the TL-NPC, although an additional dc-blocking capacitor is necessary. Due its reduced number of components, this circuit served as the basis for deriving other topologies. In [14], the four-switch cell was used to generate an *LLC* resonant converter suited for wide-input-voltage range operation, while in [15] the concept was extended to a six-switch topology, in which the voltage stress on the semiconductors is further reduced to only a third of the input voltage. Other circuits are capable of providing TL operation, but without voltage division on all semiconductor devices. For instance, the T-type switching cell has been used to derive several dc–dc converters [16], [17], [18], but only two out of four switches are subjected to half the input voltage. As a result, these solutions are not adequate for high-input-voltage applications.

In most situations, input voltage is supplied as a single level V_{in} to the circuit. However, TL converters arranged as bridge configurations (e.g., half-bridge and full-bridge) require the input voltage to be divided by half before it is fed to the circuit, which is usually accomplished by a capacitive voltage divider [2]. Due to inevitable asymmetries occurring in practical implementations, such as duty cycle mismatch and distinct parasitic resistances of the devices, input voltage can be unevenly divided between the capacitors, thus leading to unbalance that can have a negative impact on the converter operation. A detailed explanation on the mechanism of unbalance generation is provided in [19], along with a control strategy for guaranteeing balanced operation. A modified pulsewidth modulation (PWM) strategy was also proposed in [20] to improve the voltage balance capability of the four-switch HBTL converter.

Extending the soft-switching operating range is also a concern in TL converters. In [21], two auxiliary switches were added to the four-switch HBTL converter to ensure soft-switching operation for a wide load range. Topologies containing two transformers were also proposed to address this issue, using a dual

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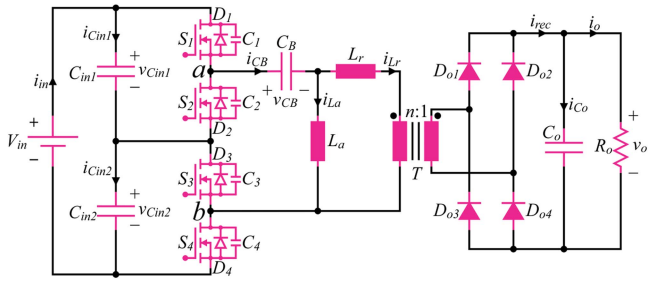

Fig. 1. Improved four-switch three-level soft-switching half-bridge DC–DC converter employing an auxiliary inductance, L_a, for wide soft-switching range operation.

half-bridge cascaded in [22] and a six-switch configuration in [23]. Also, challenges associated with soft-switching operation in a TL-NPC converter employing silicon carbide (SiC) devices and operating with an energy-recovery snubber were addressed in [24].

In this article, an improved four-switch TL soft-switching half-bridge converter is proposed, as depicted in Fig. 1. An auxiliary inductance L_a is used to ensure wide-zero voltage switching (ZVS)-range operation by providing a minimum switching current at light load conditions. The output rectifier is intended to be operated under the discontinuous conduction mode (DCM) to ensure zero current switching (ZCS) for the diodes D_{o1}–D_{o4} (called hereafter ZCS-Mode). In addition, having a capacitive output filter ensures that the blocking voltages of D_{o1}–D_{o4} are clamped to the output voltage and also prevents the use of any additional clamping circuit to limit voltage spikes on the diodes.

It is noteworthy that the structure composed of C_B, L_a, and L_r resembles the resonant tank contained in *CLL* converters [25]. However, the operation of *CLL* converters relies on the resonance between the components to process energy, while in the proposed converter C_B acts as a low-voltage-ripple dc-blocking capacitor and L_a does not affect the output transfer characteristic of the circuit. Another important observation is that a different approach to extend the ZVS range of the two-level full-bridge dc–dc converter was introduced in [26]. In this solution, two auxiliary inductors and four capacitors are required to implement the circuit, while in the proposed converter a single inductor (L_a) is necessary. It is important to observe that using a single inductor is only possible because the dc-blocking capacitor C_B also performs the task of blocking the dc component of the current on L_a.

II. Principle of Operation in Steady State

A PWM strategy is adopted for the operation of the proposed converter, in which S_1 is complementary to S_2 and S_3 to S_4. In addition, the PWM signals of the pairs S_1/S_2 and S_3/S_4 have the same duty cycle but are ideally phase-shifted by 180°. It is noteworthy that that a slight change in the phase shift can be applied to guarantee balanced input voltage distribution between $C_{\text{in}1}$ and $C_{\text{in}2}$, as detailed in Section III.

Twelve operating stages are observed in steady state when the proposed converter operates in the ZCS-Mode. However, describing only the first six stages is sufficient for the analysis because the pairs S_1/S_2 and S_3/S_4 work with equivalent duty cycles. The topological states of the converter within the first half of the switching period are shown in Fig. 2 and a brief description of these stages is provided next.

First Stage (t_0–t_1): Starts when D_1 becomes forward biased due to energy previously stored in L_a, which allows S_1 to be turned ON with ZVS. The current on L_r increases linearly and energy is provided to the output via T_r, D_{o1} and D_{o4}. At $t = t_1$, i_{Lr} becomes equal to -i_{La}, which forces the current on S_1 and S_4 to change its direction.

Second Stage (t_1–t_2): At $t = t_1$, S_1 and S_4 take over the current provided to C_B. During this stage, the current on L_a will change its direction and energy necessary for a future switching begins to be stored. As soon as S_1 is turned OFF, the second stage ends.

Third Stage (t_2–t_3): The blocking of S_1 gives rise to the charging/discharging process of the pair C_1/C_2. As can be seen in Fig. 2(c), both i_{La} and i_{Lr} are involved in the switching process, which facilitates the charging/discharging of the capacitors. Third stage is finished when C_2 becomes completely discharged.

Fourth Stage (t_3–t_4): After the switching process, D_2 becomes forward biased allowing S_2 to be turned ON with ZVS. Current starts flowing through the midpoint of the input capacitors, charging $C_{\text{in}1}$ and discharging $C_{\text{in}2}$. During the fourth stage, i_{Lr} decreases linearly and becomes null at $t = t_4$.

Fifth Stage (t_4–t_5): During this stage, there is no current on L_r, characterizing the discontinuous conductions of the output rectifier, which is key to guaranteeing ZCS operation for D_{o1} and D_{o2}. At $t = t_5$, S_4 is turned OFF thus finishing the fifth stage.

Sixth Stage (t_5–t_6): Another switching transition occurs after the blocking of S_4. However, differently from the third stage, there is no current flowing through L_r, and therefore L_a becomes solely responsible for the charging–discharging of the pair C_3/C_4. As it is going to be investigated in detail in Section II-C, this interval is critical to choosing an adequate value for L_a. Assuming that L_a is properly chosen, C_3 becomes completely discharged at $t = t_6$, which characterizes the end of the first half of the switching period.

It is evident from the operating stages that the simultaneous conduction of all four output diodes (D_{o1}–D_{o4}) does not occur, since the output filter is purely capacitive. As a result, the current flowing through the transformer always reaches the output, and therefore the proposed converter does not exhibit duty cycle loss as usually verified in soft-switching converters with an *LC* output filter.

The key theoretical waveforms regarding the operation of the proposed converter in the ZCS-mode are depicted in Fig. 3.

A. Mathematical Analysis

A complete understanding of the converter operation in the ZCS-Mode is only possible if a detailed mathematical analysis is carried out. In this article, this analysis is performed considering the following assumptions.

1) All semiconductors are ideal.
2) the voltages on capacitors $C_{\text{in}1}$, $C_{\text{in}2}$, C_B, and C_o are ripple free, and therefore they can be treated as constant voltage sources within a switching interval.
3) The magnetizing inductance of T_r is much larger than L_r and L_a.

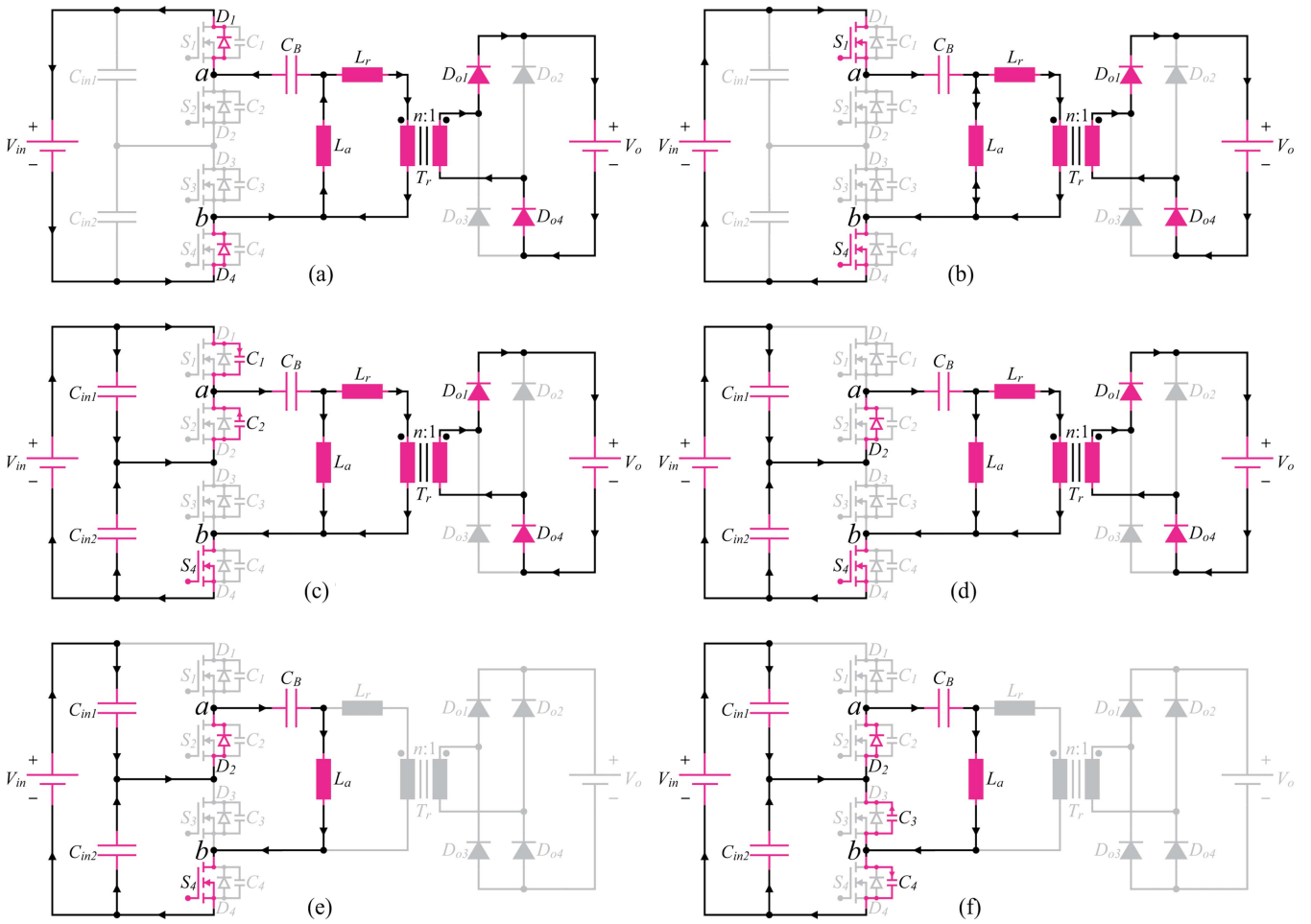

Fig. 2. Steady-state operating stages of the proposed converter in the ZCS-Mode. Due to symmetry, only the first six stages are necessary to perform the mathematical analysis. (a) First Stage. (b) Second Stage. (c) Third Stage. (d) Fourth Stage. (e) Fifth Stage. (f) Sixth Stage.

4) Due to symmetry, $v_{C\mathrm{in}1} = v_{C\mathrm{in}2} = v_{CB} = V_{\mathrm{in}}/2$. Inevitable asymmetries, such as duty cycle mismatch between the pairs S_1/S_2 and S_3/S_4 and distinct parasitic resistances of the devices, can generate unbalance between $v_{C\mathrm{in}1}$ and $v_{C\mathrm{in}2}$, but a control strategy is proposed to guarantee balanced operation as detailed in Section III.

From the analysis of the equivalent circuits of the operating stages depicted in Fig. 2, it is possible to determine the functions describing i_{Lr} and i_{La} that generate the piecewise linear waveforms depicted in Fig. 3. During the first stage, the currents on L_r and L_a are given by

$$i_{Lr}(t) = \frac{\left(V_{in}/2 - nV_o\right)}{L_r}(t - t_0) \tag{1}$$

$$i_{La}(t) = -I_{La,p} + \frac{V_{in}}{2L_a}(t - t_0). \tag{2}$$

At the end of the first stage, i_{Lr} and i_{La} are equal to I_1 and -I_1, respectively. Then

$$I_1 - \frac{\left(V_{in}/2 - nV_o\right)}{L_r}\Delta t_1 = 0 \tag{3}$$

$$I_{La,p} - I_1 - \frac{V_{in}}{2L_a}\Delta t_1 = 0. \tag{4}$$

As described in the qualitative analysis, the second stage begins when the current on D_{S1} becomes null. During this stage, i_{Lr} and i_{La} can be computed as

$$i_{Lr}(t) = I_1 + \frac{\left(V_{in}/2 - nV_o\right)}{L_r}(t - t_1) \tag{5}$$

$$i_{La}(t) = -I_1 + \frac{V_{in}}{2L_a}(t - t_1). \tag{6}$$

At $t = t_2$, i_{Lr} and i_{La} become, respectively, equal to $I_{Lr,p}$ and $I_{La,p}$, thus yielding

$$I_{Lr,p} - I_1 - \frac{\left(V_{\mathrm{in}}/2 - nV_o\right)}{L_r}\Delta t_2 = 0 \tag{7}$$

$$I_{La,p} + I_1 - \frac{V_{\mathrm{in}}}{2L_a}\Delta t_2 = 0. \tag{8}$$

Third and sixth stages correspond to switching processes, which are much briefer than the regular stages. Hence, their influence on the energy transfer of the converter can be neglected

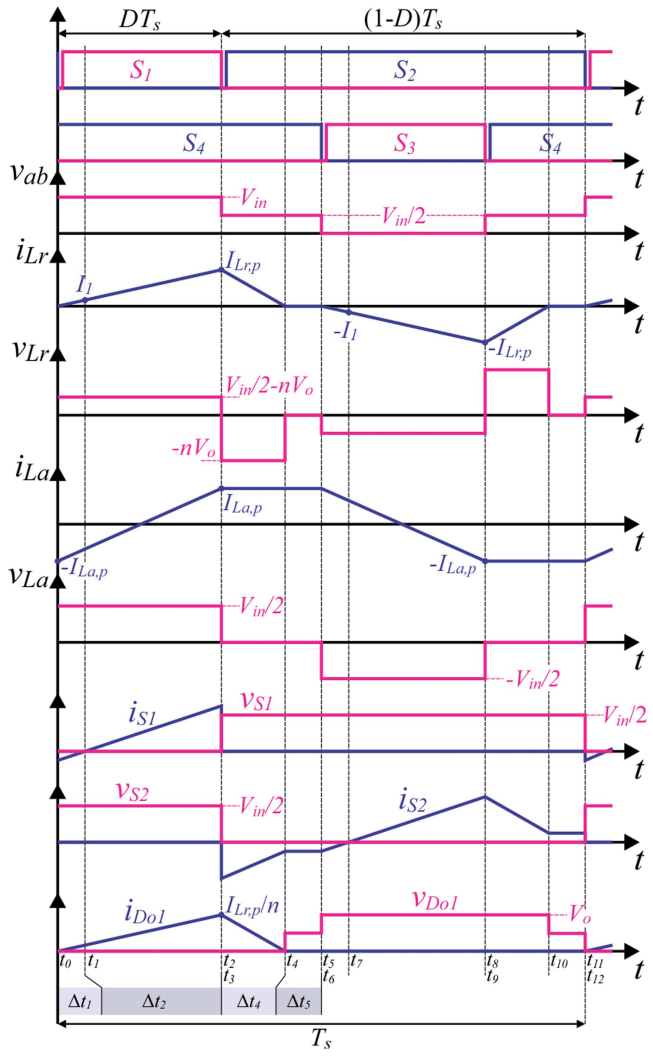

Fig. 3. Key theoretical waveforms for operation in the ZCS-Mode. The phase-shift angle between the PWM signals of the pairs S_1/S_2 and S_3/S_4 is considered to be 180°.

and the switching is analyzed in detail in Section II-C to determine the conditions necessary to guarantee ZVS operation. Consequently, only stages 4 and 5 remain to be addressed. During the fourth stage, the currents on L_r and L_a are given by

$$i_{Lr}(t) = I_{Lr,p} - \frac{nV_o}{L_r}(t - t_3) \tag{9}$$

$$i_{La}(t) = I_{La,p}. \tag{10}$$

Since the fourth stage ends when i_{Lr} becomes null, it follows that:

$$I_{Lr,p} - \frac{nV_o}{L_r}\Delta t_4 = 0. \tag{11}$$

Lastly, during the fifth stage, there is no current on L_r and the current on L_a remains constant, as given by

$$i_{Lr}(t) = 0 \tag{12}$$

$$i_{La}(t) = I_{La,p}. \tag{13}$$

From the equations derived so far, (3), (4), (7), (8), and (11) are of particular interest for the static analysis of the circuit, because they must be satisfied at the steady state operation of the converter. However, these equations alone do not provide the complete steady-state description of the circuit operation. The remaining equations can be derived based on the PWM pattern depicted in Fig. 3, from which it can be concluded that

$$\Delta t_1 + \Delta t_2 = DT_s \tag{14}$$

$$\Delta t_4 + \Delta t_5 = \frac{(1-2D)}{2}T_s. \tag{15}$$

By solving the system of (3), (4), (7), (8), (11), (14), and (15), it is possible to determine the normalized values of the unknowns defined for the analysis of the converter, as given by

$$\bar{I}_{Lr,p} = 2D(1-2q) \tag{16}$$

$$\bar{I}_{La,p} = D\lambda, \tag{17}$$

$$\bar{I}_1 = \frac{D\lambda(1-2q)}{\lambda+1-2q} \tag{18}$$

$$\Delta\bar{t}_1 = \frac{D\lambda}{2(\lambda+1-2q)} \tag{19}$$

$$\Delta\bar{t}_2 = \frac{D(\lambda+2-4q)}{2(\lambda+1-2q)} \tag{20}$$

$$\Delta\bar{t}_4 = \frac{D(1-2q)}{2q} \tag{21}$$

$$\Delta\bar{t}_5 = \frac{q-D}{2q}. \tag{22}$$

The normalization rules

$$q = \frac{nV_o}{V_{in}},\ \bar{I}_x = \frac{4f_sL_rI_x}{V_{in}},\ \Delta\bar{t}_y = \frac{\Delta t_y}{T_s},\ \lambda = \frac{L_r}{L_a} \tag{23}$$

are used to represent the results, where q corresponds to the static gain, $\bar{I}_x$ denotes the normalization of I_x, $\Delta\bar{t}_y$ denotes the normalization of Δt_y and λ is the inductance factor.

Due to symmetry, the average value of the output current is twice the average value of the current on D_{o1}. As a result, the average value of the output current

$$I_o = \frac{D^2(V_{\text{in}} - 2nV_o)V_{\text{in}}}{4f_sL_rV_o} \tag{24}$$

can be determined based on the waveform of i_{Do1} depicted in Fig. 3.

The output voltage can be computed from (24), as given by

$$V_o = \frac{D^2V_{\text{in}}^2}{4f_sL_rI_o + 2nD^2V_{\text{in}}}. \tag{25}$$

The static gain can now be determined using (23) and (25), resulting in

$$q = \frac{nV_o}{V_{\text{in}}} = \frac{D^2}{\bar{I}_o + 2D^2} \tag{26}$$

where

$$\bar{I}_o = \frac{4f_sL_rI_o}{nV_{\text{in}}}. \tag{27}$$

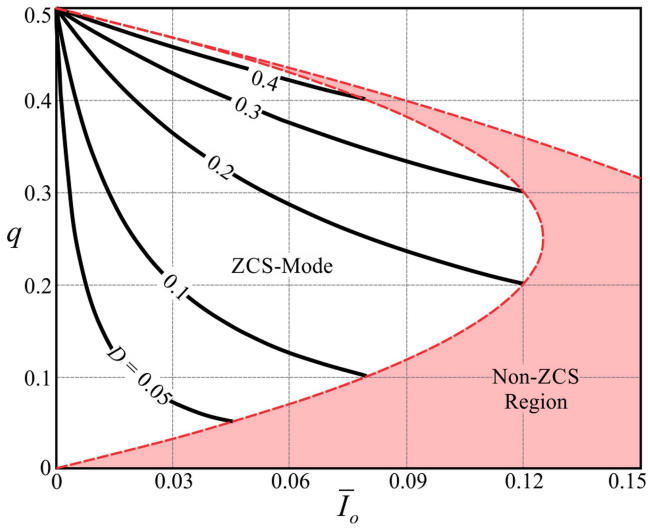

Fig. 4. Output characteristic of the proposed four-switch three-level half-bridge DC–DC converter.

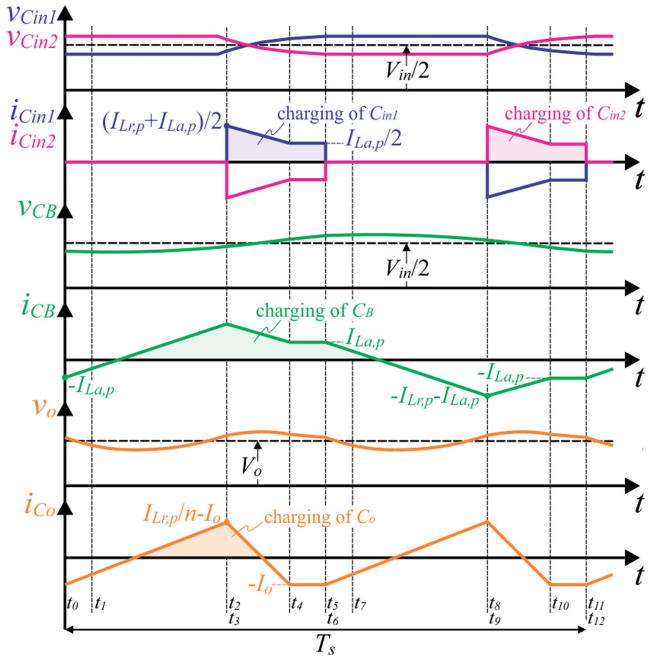

Fig. 5. Voltage and current waveforms on $C_{\text{in}1}$, $C_{\text{in}2}$, C_B, and C_o. The highlighted areas are proportional to the charge provided for the capacitors, and thus can be used to determine their respective voltage ripples.

As previously mentioned, ZCS-Mode occurs only if the output rectifier operates in DCM, which makes mandatory having an interval Δt_5 longer than zero. As a result, the restriction that must be met for ZCS operation can be computed from (22)

$$q > D. \tag{28}$$

Several curves generated from (26) are plotted in the graph depicted in Fig. 4 considering the region, in which the output diodes operate under ZCS. Based on (28), the boundary between the ZCS and non-ZCS regions, indicated by a dashed line, can be determined by substituting $D = q$ into (26)

$$\bar{I}_o < q\,(1-2q)\,. \tag{29}$$

It is important to observe that L_a does not affect the ideal static gain. Therefore, the proper choice of L_r is key to ensuring ZCS operation for the output diodes, given that this parameter is directly related to the normalized output current defined in (27). On the other hand, L_a plays a major role in guaranteeing ZVS operation for the converter's switches, as detailed in the switching analysis carried out in Section II-C.

B. Voltage Ripple on the Capacitors

Capacitances $C_{\text{in}1}$, $C_{\text{in}2}$, C_B, and C_o must be chosen based on voltage ripple requirements to ensure the proper operation of the converter. These ripples can be computed using the charging intervals highlighted in Fig. 5.

It must be noted that the currents on $C_{\text{in}1}$ and $C_{\text{in}2}$ are symmetric, and therefore the voltage ripple on these devices are equivalent and equal to $\Delta V_{C\text{in}}$ if $C_{\text{in}1} = C_{\text{in}2} = C_{\text{in}}$ is assumed. Using the waveform of $i_{C\text{in}1}$ (or $i_{C\text{in}2}$) provided in Fig. 5, it is possible to demonstrate that

$$\Delta V_{C\text{in}} = \Delta V_{C\text{in}1} = \frac{1}{C_{\text{in}}}\int_{t_3}^{t_5} i_{C\text{in}1}\,dt. \tag{30}$$

The integral contained in (30) yields the charging area of $C_{\text{in}1}$ indicated in Fig. 5, as given by

$$\int_{t_3}^{t_5} i_{C\text{in}1}\,dt = \left(\frac{I_{Lr,p}}{4} + \frac{I_{La,p}}{2}\right)\Delta t_4 + \frac{I_{La,p}}{2}\Delta t_5 \tag{31}$$

resulting in

$$\Delta V_{C\text{in}} = \frac{DV_{\text{in}}\left[D + \lambda q\,(1-2D) - 4Dq\,(1-q)\right]}{16 f_s^2 q L_r C_{\text{in}}}. \tag{32}$$

Proceeding similarly for C_B, the waveform of i_{CB} depicted in Fig. 5 allows computing

$$\Delta V_{CB} = \frac{DV_{\text{in}}}{8 f_s^2 L_r C_B\,(\lambda + 1 - 2q)\,q}\Big\{D(1-2q)^2 + q\lambda^2\,(1-D) + \lambda\left[(1-2D)\,q + D\right](1-2q)\Big\}. \tag{33}$$

Lastly, based on the waveform of i_{Co} depicted in Fig. 5, the voltage ripple on C_o can be calculated as

$$\Delta V_{Co} = \frac{nV_{\text{in}}D^2\,(1-2q)\,(D-2q)^2}{32 f_s^2 q^3 L_r C_o}. \tag{34}$$

C. Switching Analysis

A key feature of the proposed converter is the ZVS operation for S_1–S_4 and ZCS for the output diodes (D_{o1}–D_{o4}) for a wide load range. This is only possible due to the existence of an auxiliary inductance L_a, which guarantees a minimum current flow in the circuit to perform the charge/discharge processes of the capacitances C_1–C_4 even though the current on L_r is discontinuous. Hence, a detailed switching analysis is required to determine the conditions necessary to ensure soft-switching

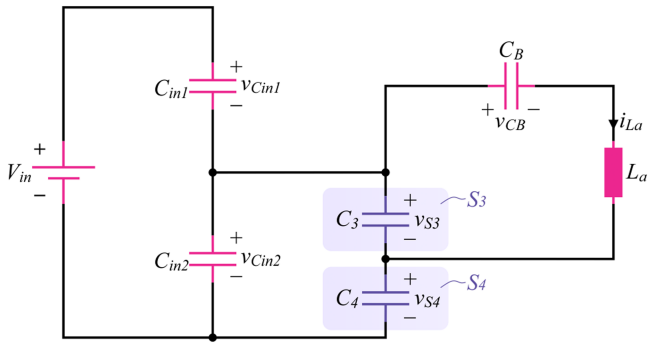

Fig. 6. Equivalent circuit for the analysis of the critical switching occurring during stage 6 [c.f., Fig. 2(f)]. Assuming balanced operation, voltages $v_{C\text{in}1}$, $v_{C\text{in}2}$, and v_{CB} are equal to $V_{\text{in}}/2$.

operation for a given load range, thus providing the basis for the proper choice of L_a.

From the six operating stages depicted in Fig. 2 two correspond to switching processes. In stage 3, S_1 is turned OFF and capacitances C_1 and C_2 are charged and discharged, respectively, prior to the conduction of D_2. Similarly, in stage 6, S_4 is turned OFF and the charging/discharging processes occur at C_3 and C_4 before D_3 becomes forward biased. However, the conditions of each switching interval are different because the currents involved are distinct. For instance, S_1 is turned OFF with a current level of $I_{Lr,p}+I_{La,p}$, while only $I_{La,p}$ is verified when S_4 blocks. As a result, guaranteeing the complete charge/discharge of the capacitances in stage 6 is harder than in stage 3, and therefore ensuring the conduction of D_3 to achieve ZVS in S_3 is a main concern for soft-switching operation.

Considering that the turn-OFF processes of S_2 and S_3 are similar to S_4 and S_1, respectively, one can conclude that the pair S_1/S_3 is critical, i.e., ZVS is lost in these devices first. Hence, a detailed analysis of stage 6 becomes mandatory to determine the conditions necessary to ensure the complete discharge/charge of C_3 and C_4, respectively.

Based on the topological state of stage 6 depicted in Fig. 2(f), one can determine the equivalent circuit regarding the critical switching, as given in Fig. 6. The analysis of this circuit yields the differential equation

$$\frac{d^2 v_{S3}}{dt^2} + \frac{v_{S3}}{2L_a C_S} = \frac{V_{\text{in}}}{4L_a C_S} \tag{35}$$

assuming that $C_1 = C_2 = C_3 = C_4 = C_S$ and $v_{C\text{in}1} = v_{C\text{in}2} = v_{CB} = V_{\text{in}}/2$.

At the beginning of stage 6, the voltage on C_3 is equal to $V_{\text{in}}/2$ and the current on L_a is $I_{La,p}$. For these particular initial conditions, the solution of (35) is

$$v_{S3}(t) = \frac{V_{\text{in}}}{2} - \sqrt{\frac{L_a}{2C_S}} I_{La,p} \sin(\omega_o t) \tag{36}$$

$$\omega_o = \frac{1}{\sqrt{2L_a C_S}}. \tag{37}$$

The complete discharge of C_3 is mandatory to achieve ZVS operation, which is only met if

$$C_S \leq \frac{2L_a I_{La,p}^2}{V_{\text{in}}^2}. \tag{38}$$

In addition, a minimum deadtime between the gate signals of the pair S_3/S_4 is necessary to guarantee that the switching process is over before S_3 is turned ON

$$\theta_{\text{min}} = \sqrt{2L_a C_S} \arcsin\left(\sqrt{\frac{C_S}{2L_a}} \frac{V_{\text{in}}}{I_{La,p}}\right). \tag{39}$$

It is evident from (39) that the minimum deadtime depends on the value of $I_{La,p}$, and therefore it varies as the operating condition is changed. An optimum choice for the deadtime is to set it to a quarter of the resonant period, so that the switch is turned ON at the valley of its voltage if ZVS is lost at light load conditions

$$\theta_{\text{opt}} = \frac{T_o}{4} = \frac{\pi}{2\omega_o} = \frac{\pi}{2}\sqrt{2L_a C_S}. \tag{40}$$

The results derived in this section allow the proper choice of L_a for a given ZVS range. For a particular choice of transistor, C_S becomes known and the designer can evaluate (38) using the value of $I_{La,p}$ given in (17). This yields the range of L_a in terms of the parameters of the converter

$$L_a \leq \frac{D^2}{8f_s^2 C_S}. \tag{41}$$

Equation (41) demonstrates that the choice of L_a depends on D, which in turn varies according to (26) in order to keep the output voltage (implicitly defined in q) regulated at some desired value. As a result, L_a can be determined based on the minimum value of D for a prespecified load range (or equivalently, range of output power)

$$L_a = \frac{D_{\text{min}}^2}{8f_s^2 C_S}. \tag{42}$$

It is noteworthy that choosing overly low values for L_a would result in high current stresses due to increased circulating current. However, in the proposed converter, the circulating current does not flow through the transformer, inductor L_r, and output diodes, thus not increasing the losses on these elements. It is also important to mention that, during the design of the converter, the value of L_a must be chosen taking into consideration the tradeoff between switching and conduction losses.

III. Output Voltage Control and Input Voltage Balance

Proper operation of the proposed converter requires that its output voltage is regulated and the distribution of the input voltage between $C_{\text{in}1}$ and $C_{\text{in}2}$ is balanced. In [19], a control strategy was proposed to guarantee balanced operation and also ensure that the voltage on the blocking capacitor is equal to $V_{\text{in}}/2$. This strategy requires the measurement of the voltage on the input capacitors and also on the blocking capacitor C_B. In [20], a modified strategy using an interleaved PWM scheme was

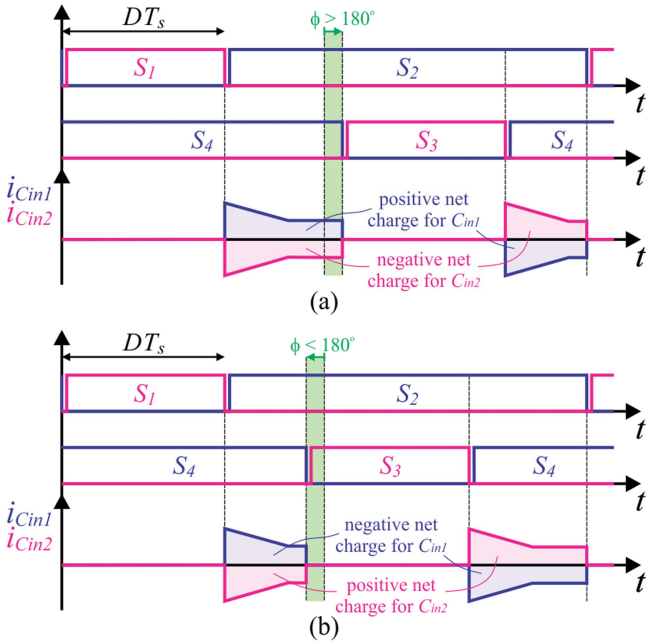

Fig. 7. Input voltage balance mechanism demonstrating unbalanced charging of $C_{\mathrm{in}1}$ and $C_{\mathrm{in}2}$ for $\varphi \neq 180°$: (a) $\varphi > 180°$ and (b) $\varphi < 180°$.

proposed and it was demonstrated that the deviation of v_{CB} from $V_{\mathrm{in}}/2$ is limited to the difference between the duty cycles of the pairs S_1/S_2 and S_3/S_4. Since even low-cost digital controllers are capable of generating accurate PWM signals, it can be concluded that the voltage on C_B remains close to $V_{\mathrm{in}}/2$ if balanced input voltage distribution is guaranteed, and therefore there is no need for measuring v_{CB}.

As discussed in [20], input voltage balance can be achieved by proper adjusting the phase shift between the PWM signals of the pairs S_1/S_2 and S_3/S_4. Ideally, a phase shift of 180° ($\varphi = 180°$) is required for balanced operation, but asymmetries that arise from a practical implementation make mandatory a slight correction of this parameter. The analysis of the converter unveils that increasing the phase shift results in more charge being transferred to $C_{\mathrm{in}1}$ than $C_{\mathrm{in}2}$, and consequently $v_{C\mathrm{in}1}$ is increased and $v_{C\mathrm{in}2}$ decreased. On the other hand, the opposite action can be performed by decreasing the phase shift. This behavior can be visualized in Fig. 7(a) and (b), which depicts the waveforms for φ higher and lower than 180°, respectively.

It is worth mentioning that, ideally, changing φ does not affect the output voltage in the case of balanced operation. This characteristic is interesting because input voltage balance and output voltage control can be performed independently by adjusting D and φ, respectively. Thus, for a complete control scheme to be proper defined, the response of the output voltage versus duty cycle variations must be determined.

In the case of balanced operation, voltages $v_{C\mathrm{in}1}$ and $v_{C\mathrm{in}2}$ are not affected by variations of D. In addition, since D defines the pulse width of both S_1 and S_3, it does not affect the average value of the current on i_{La} as well. As a result, it can be demonstrated that the proposed converter behaves as a single order nonlinear system.

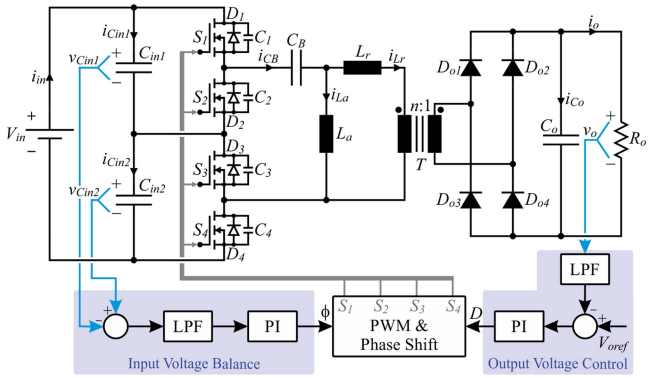

Fig. 8. Strategy for output voltage control and input voltage balance. Low-pass filters and PI compensators are used in the proposed scheme. An isolated voltage sensor is required for measuring v_o while the difference between $v_{C\mathrm{in}2}$ and $v_{C\mathrm{in}1}$ can be measured using a conventional nonisolated differential amplifier.

Equation (24) was derived by computing twice the average value of the current on D_{o1}, which in turn corresponds to the average value of i_{rec} defined in Fig. 1. Such result is only valid for steady-state operation, because the average value of i_{Co} is null in such condition. However, the quasi-instantaneous average value if i_{Co} is not zero during transient operation, thus requiring a specific analysis for determining the dynamic response of the output voltage. In this article, the dynamic analysis relies on the linearization of the mathematical model in the vicinity of a given quiescent point. Since (24) was derived directly from the waveform of i_{Do1}, it can be used to compute small perturbations on i_{rec} using the first-order Taylor series

$$\hat{i}_{\mathrm{rec}} = \frac{\partial I_o}{\partial V_o}\hat{v}_o + \frac{\partial I_o}{\partial D}\hat{d} \tag{43}$$

which yields

$$\hat{i}_{\mathrm{rec}} = -\frac{D^2 V_{\mathrm{in}}^2}{4 f_s L_r V_o^2}\hat{v}_o + \frac{D V_{\mathrm{in}}\left(V_{\mathrm{in}} - 2nV_o\right)}{2 f_s L_r V_o}\hat{d} \tag{44}$$

where $\hat{i}_{\mathrm{rec}}$, $\hat{v}_o$, and $\hat{d}$ correspond to small perturbations on i_{rec}, output voltage, and duty cycle, respectively.

The resulting model corresponds to the parallel association of C_o and R_o fed by a dependent current source $\hat{i}_{\mathrm{rec}}$, which can be described in the Laplace domain by the small-signal transfer function

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{2DR_oV_oV_{\mathrm{in}}\left(V_{\mathrm{in}} - 2nV_o\right)}{4f_sR_oL_rC_oV_o^2 s + R_oD^2V_{\mathrm{in}}^2 + 4f_sL_rV_o^2} \tag{45}$$

that can be used for proper control design, where $\hat{v}_o$ and $\hat{d}$ correspond to small perturbations on the output voltage and duty cycle, respectively.

A control strategy is proposed based on the results derived in this section, as depicted in Fig. 8. Since there is ideally no coupling between the output voltage and input voltage balance control loops, the design of the compensators can be carried out considering two separate single-input-single-output systems. In addition, voltages $v_{C\mathrm{in}1}$ and $v_{C\mathrm{in}2}$ can be measured by a simple differential amplifier, while the measurement of the output voltage v_o requires isolation. Differently from [20], balanced

TABLE I
PROTOTYPE SPECIFICATIONS

Parameter	Value
Output power (P_o)	1 kW
Input voltage (V_{in})	700–800 V
Output voltage (V_o)	400 V
Output current (I_o)	2.5 A
Switching frequency (f_s)	100 kHz
ZVS range	20–100% of P_o
Voltage ripple on C_{in1}, C_{in2} and C_B ($\Delta V_{Cin\%}$, $\Delta V_{CB\%}$)	< 10% of V_{in}/2
Voltage ripple on C_o ($\Delta V_{Co\%}$)	< 1% of V_o

TABLE II
PARAMETERS OF THE PROTOTYPE

Parameter	Value
S_1–S_4	IPW65R080CFD
D_{o1}–D_{o4}	STTH60L06
L_r	19.845 µH, ETD29, N87, 21 turns, 22/38 AWG (litz)
L_a	180 µH, E42/15, N87, 41 turns, 22/38 AWG (litz)
T_r	E55, N87, 19/24 turns, 22x38 AWG (litz)
C_{in1}, C_{in2}	2.2 µF, 630 V, polypropylene
C_B	2.2//2.2 µF, 630 V, polypropylene
C_o	220 µF, 450 V, electrolytic + 2.2//2.2 µF, 630 V, polypropylene

operation and output voltage regulation can be guaranteed using a simpler noninterleaved modulation strategy. In the proposed scheme, the input voltage balance control loop provides small adjustments around $\varphi = 180°$ to compensate for asymmetries, thus guaranteeing balanced operation.

IV. EXPERIMENTAL RESULTS

The feasibility of the proposed converter was verified in laboratory using a prototype designed considering the specifications given in Table I. In this design, the parameters $q = 0.46$ and $D = 0.45$ are chosen for full-load operation at $V_{\text{in}} = 700$ V, thus guaranteeing operation in ZCS-mode according to (28). The parameters of the prototype, given in Table II, can be determined using the several equations derived in the mathematical analysis. The proportional–integral (PI) compensator used in the output voltage control loop has a proportional gain of 0.005 and an integral gain of five, while the proportional and integral gains of the PI contained in the input voltage balance loop are 0.001 and 0.1, respectively. These parameters yield closed-loop bandwidths of 120 and 250 Hz for the output voltage and input voltage balance control loops, respectively. A picture of the 1 kW prototype is shown in Fig. 9.

Fig. 10 provides the main experimental results at minimum input voltage ($V_{\text{in}} = 700$ V). Voltages v_{CB}, $v_{C\text{in}1}$, and $v_{C\text{in}2}$, are depicted in Fig. 10(a), where it is evident that the distribution of the input voltage between $C_{\text{in}1}$ and $C_{\text{in}2}$ is balanced. Moreover, as predicted in the theoretical analysis, capacitor C_B is also subjected to half the input voltage, even though its voltage is not being directly controlled. Voltage v_{ab} and currents on L_r and L_a are shown in Fig. 10(b) and are in accordance with the theoretical waveforms depicted in Fig. 3. Drain-to-source and gate-to-source voltages on S_1 and S_2 are depicted in Fig. 10(c), showing the occurrence of ZVS for both switches at rated output power. Still regarding soft-switching, ZCS-Mode can be verified by the waveforms of the voltage and current on D_{o1} presented in Fig. 10(d), along with the output voltage. It is noteworthy that the waveforms for the remaining switches and diodes are not provided because they are similar to S_1/S_2 and D_{o1}, respectively. As demonstrated in Fig. 10(e), ZVS is still achieved at 20% of rated output power for both switches S_1 and S_2. Finally, control response under a 50%–100% load transient is shown in Fig. 10(f), where it is evident that the output voltage remains regulated at 400 V with very small perturbations during the disturbing event. It is worth mentioning that the load steps were carried out using the electronic load NHR 9430, the current of which contains a considerable ripple at a fundamental frequency of approximately 3 kHz.

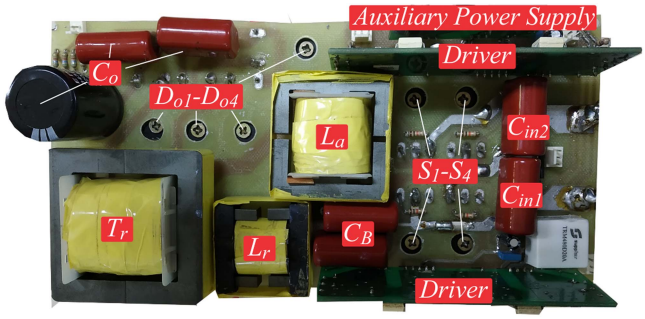

Fig. 9. Photograph of the 1 kW improved four-switch three-level DC–DC converter built for the experimental tests.

The condition of maximum input voltage ($V_{\text{in}} = 800$ V) was also investigated and the main results are depicted in Fig. 11. Measurements demonstrate that balanced operation is also guaranteed at the maximum input voltage condition, in addition to maintaining ZVS for the primary switches and ZCS for the output diodes. It is noteworthy that both switches keep ZVS operation at $P_o = 200$ W, which proves wide-ZVS-range operation since the condition of $V_{\text{in}} = 800$ V is the worst case in terms of soft-switching. Moreover, proper output voltage response for a 50%–100% load transient is also demonstrated at maximum input voltage.

The performance of the proposed converter in terms of input voltage balance and ZVS and ZCS operation during a 50%–100% load transient event was also investigated. The waveforms depicted in Fig. 12(a)–(f) demonstrate that input voltage balance is guaranteed even under transient for both conditions of input voltage. In addition, ZVS for the critical switches (only S_1 is shown) and ZCS for the output diodes (only D_{o1} is shown) are also achieved.

Efficiency measurements were taken using the YOKOGAWA WT500 precision power analyzer, as shown in Fig. 13. A maximum efficiency of 96.13% was verified at $P_o = 900$ W and $V_{\text{in}} = 700$ V. At rated output power, efficiency levels of 96.06% and 95.70% were measured for input voltage conditions of 700 and 800 V, respectively. An efficiency drop is observed at light load, mainly caused by the following:

1) fixed losses on the auxiliary power supply, MOSFET drivers and control circuitry;

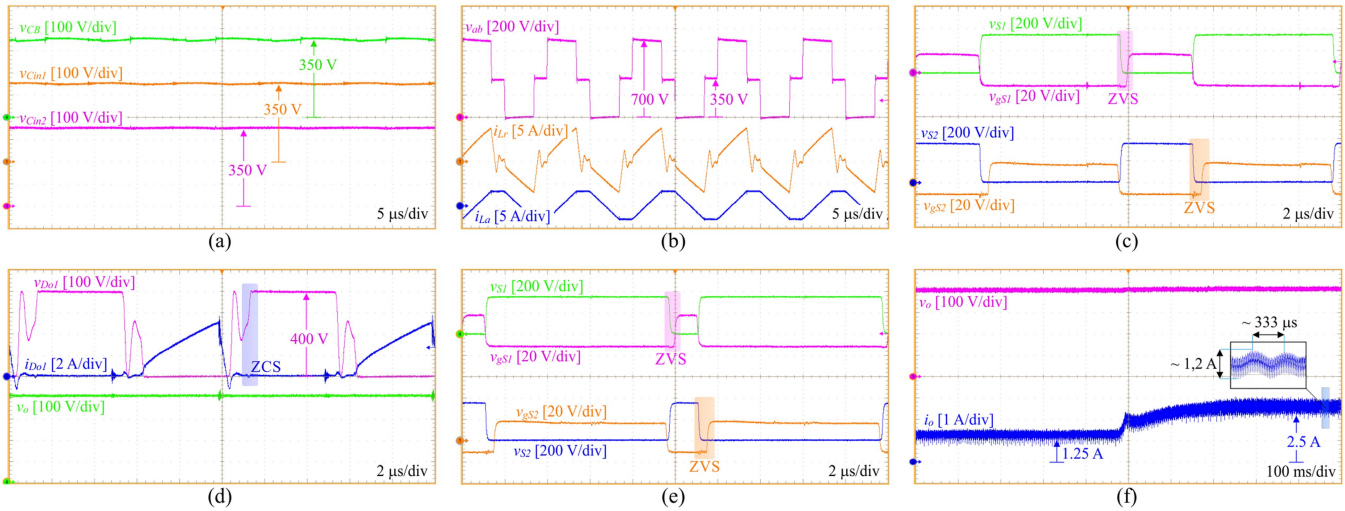

Fig. 10. Main experimental results for $V_{\rm in} = 700$ V: (a) voltages v_{CB}, $v_{C{\rm in}1}$, and v_{Cin2}; (b) voltage v_{ab} and currents i_{Lr} and i_{La}; (c) drain-to-source and gate-to-source voltages on S_1 and S_2; (d) voltage and current on D_{o1} and output voltage; (e) drain-to-source and gate-to-source voltages on S_1 and S_2 for $P_o = 200$ W; (f) output voltage and current during a 50%–100% load transient. All tests were performed at $P_o = 1$ kW, unless otherwise stated.

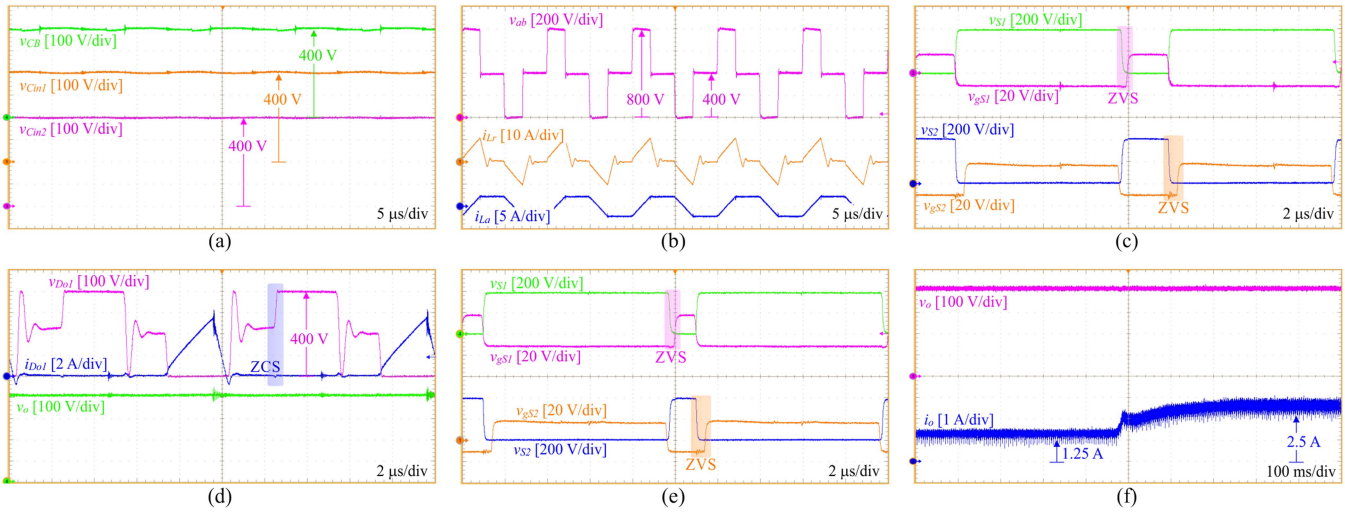

Fig. 11. Main experimental results for $V_{\rm in} = 800$ V: (a) voltages v_{CB}, $v_{C{\rm in}1}$, and v_{Cin2}; (b) voltage v_{ab} and currents i_{Lr} and i_{La}; (c) drain-to-source and gate-to-source voltages on S_1 and S_2; (d) voltage and current on D_{o1} and output voltage; (e) drain-to-source and gate-to-source voltages on S_1 and S_2 for $P_o = 200$ W; (f) output voltage and current during a 50%–100% load transient. All tests were performed at $P_o = 1$ kW, unless otherwise stated.

2) $C_{\rm oss}$ related losses on the MOSFETs, which can be significant in super junction devices [27];
3) circulating current due to the auxiliary inductor L_a;
4) magnetic losses on the transformer, which exhibit low dependency on the load conditions.

It is noteworthy that $C_{\rm oss}$ related losses could be reduced by using SiC or gallium nitride (GaN) devices [28], and the "other" losses could be minimized by optimizing the design of the auxiliary power supply, MOSFET drivers and control circuitry. In addition, choosing the highest possible value for L_a that meets restriction (41) is key to keeping reduced levels of circulating current and, consequently, minimized conduction losses. Nevertheless, the efficiency was higher than 90% for the entire 20%–100% output power range for both input voltage levels.

A loss distribution analysis was also carried out, as shown in Fig. 14. As demonstrated, most of the losses are concentrated on the semiconductor devices, which slightly increase for $V_{\rm in} = 800$ V because the rms currents are higher due to lower duty cycle operation. As predicted in the theoretical analysis, the current on L_a is lower for higher input voltage levels, thus resulting in lower losses on this element at $V_{\rm in} = 800$ V.

A. Comparison With Other TL Half-Bridge Converters

The proposed converter is compared with other isolated soft-switching TL half-bridge converters, as summarized in Table III. Only circuits capable of providing voltage division on the semiconductors are considered in the comparative analysis [4], [5], [7], [13], [14], [21], [22], [23], [24], [29], [30], [31], [32].

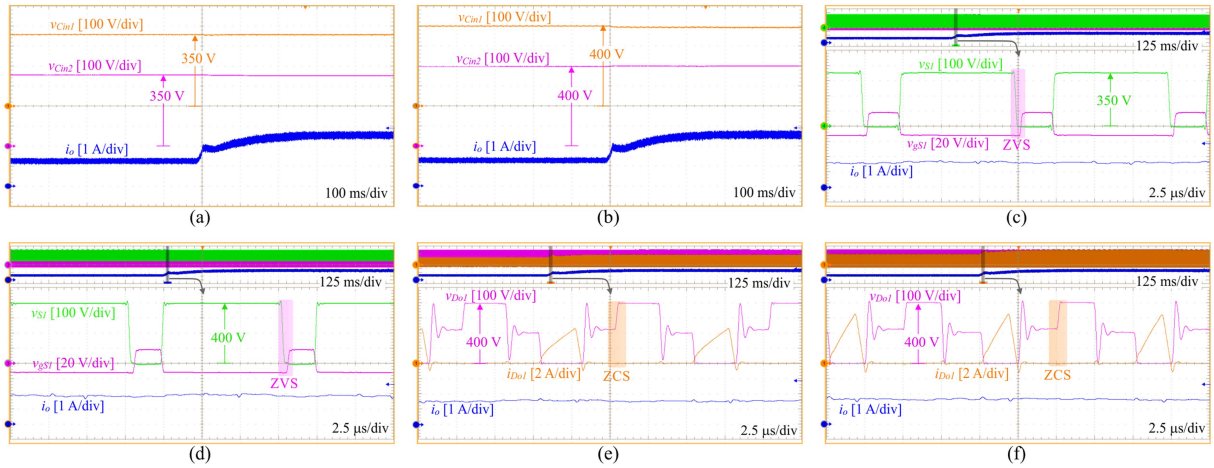

Fig. 12. Experimental results during a 50%–100% load transient: voltages v_{Cin1} and v_{Cin2} and output current for (a) $V_{in} = 700$ V and (b) $V_{in} = 800$ V; drain-to-source and gate-to-source voltages on S_1 and output current demonstrating ZVS operation for the critical switch during the transient event for (c) $V_{in} = 700$ V and (d) $V_{in} = 800$ V; voltage and current on D_{o1} and output current demonstrating ZCS operation during the transient event for (e) $V_{in} = 700$ V and (f) $V_{in} = 800$ V.

TABLE III
COMPARISON WITH OTHER ISOLATED SOFT-SWITCHING THREE-LEVEL HALF-BRIDGE CONVERTERS

Converter	Number of Components				Voltage Stress on the Output Diodes	ZCS on the Output Diodes?	Duty Cycle Loss?	Efficiency at Rated Output Power*
	Switches	Diodes	Capacitors	Magnetics				
Proposed	4	4	4	3	V_o	Yes	No	96.1% @ 1 kW, 100 kHz
[4]	4	6	3	3	$>V_o$	No	Yes	93.0% @ 1.5 kW, 100 kHz
[5]	4	4	4	3	$>2V_o$	No	Yes	92.7% @ 6 kW, 100 kHz
[7]	4	4	4	2	$2V_o$	Yes	No	92.9% @ 540 W, 88–150 kHz
[13]	4	2	4	3	$>2V_o$	No	Yes	93.6% @ 1.5 kW, 50 kHz
[14]	4	2	5	2	$2V_o$	Yes	No	94.4% @ 960 W, 35–50 kHz
[21]	6	4	4	3	$>V_o$	No	Yes	95.7% @ 1.1 kW, 100 kHz
[22]	4	4	7	3**	$>2V_o$	No	Yes	95.9% @ 750 W, 100 kHz
[23]	6	6	4	3**	$>2V_o$	No	Yes	94.1% @ 1 kW, 100 kHz
[24]	4	8	4	4	$>V_o$	No	Yes	92.7% @ 3 kW, 250 kHz
[29]	4	6	4	3	$>2V_o$	No	Yes	92.5% @ 540 W, 100 kHz
[30]	4	4	6	3	$>2V_o$	No	Yes	91.0% @ 1 kW, 100 kHz
[31]	4	6	4	3	$>2V_o$	No	Yes	94.3% @ 2.5 kW, 50 kHz
[32]	4	2	5	3	$2V_o$	Yes	No	95.5% @ 1 kW, 75–110 kHz

*At minimum input voltage
**May require two additional inductors if the leakage inductance of the transformer is not sufficiently large

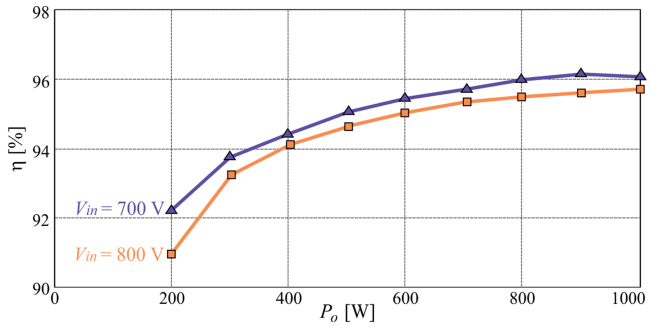

Fig. 13. Efficiency versus output power for $V_{in} = 700$ V and $V_{in} = 800$ V.

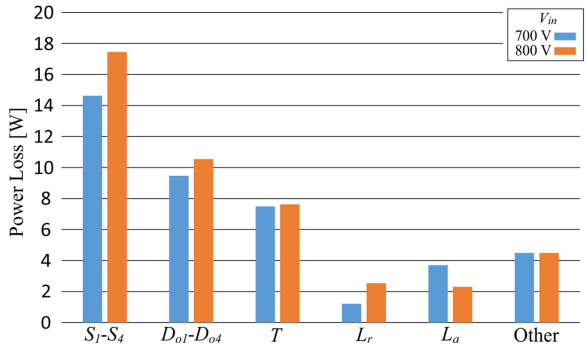

Fig. 14. Loss distribution for $V_{in} = 700$ V and $V_{in} = 800$ V at $P_o = 1$ kW. Losses on the auxiliary power supply, MOSFET drivers and control circuitry are approximately 4.5 W and computed as "other."

The converters proposed in [13] and [14] require the minimum component count to be implemented. Regarding the voltage stress on the output diodes, the circuit proposed in this work has its devices subjected to V_o. Another important feature is ZCS on the output diodes, which is verified in [7], [14], and [32], and also in the proposed converter. Duty cycle loss is another issue observed in several soft-switching converters. In this comparison, the circuits proposed in [4], [5], [13], [21], [22], [23], [24], [29], [30], and [31] suffer with this issue, which is not verified in the proposed solution. Finally, efficiency

measurements at rated output power and minimum input voltage are compared. It can be noted that the proposed converter exhibits the highest efficiency level among all the circuits considered in the analysis. The efficiency of the converter introduced in [22] is only slightly lower, but it contains two transformers and requires a higher number of components. It is important to have in mind that the solutions have very distinct design specifications and operating conditions, and therefore efficiency comparison must be performed with discretion.

V. Conclusion

An improved four-switch TL half-bridge dc–dc converter suitable for high-input-voltage applications was introduced in this article. The proposed circuit is capable of operating with ZVS on its primary switches and ZCS on the output diodes for a wide load range. A detailed mathematical analysis was carried out, providing the basis for the adequate design of the converter. The mechanism of input voltage unbalance was investigated in detail and a control strategy using a simple noninterleaved PWM strategy was discussed. In addition, a small-signal model for the proposed converter was derived, thus allowing the proper design of the output voltage control system. A 1 kW prototype, operating with $V_{\rm in} = 700$–800 V, $V_o = 400$ V, and $f_s = 100$ kHz was built and tested in laboratory to validate the theoretical analyses. Operation with efficiencies up to 96.13% and higher than 90% for a load range of 20%–100% indicates that the proposed circuit exhibits potential for high-voltage dc–dc conversion systems.

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