Comparative Study on High-Temperature Electrical Properties of 1.2 kV SiC MOSFET and JBS-Integrated MOSFET

Zhaoyuan Gu, Mingchao Yang, Yi Yang, Xihao Liu, Mingyang Gao, Jinwei Qi, Weihua Liu, *Associate Member, IEEE*, Chuanyu Han, *Member, IEEE*, Li Geng, *Senior Member, IEEE*, and Yue Hao, *Senior Member, IEEE*

***Abstract*—For 4H-SiC MOSFETs, the parasitic PiN body diode causes problems such as significant forward voltage drop of body diode and poor reverse recovery characteristics during high-temperature operation. A reasonable solution is a MOSFET with an integrated Schottky barrier diode to deactivate the PiN body diode. Since SiC MOSFETs can operate at extremely high temperatures, the characterization of electrical parameters at high temperatures and changing with the temperature are very important for high power applications and system reliability. However, there is a lack of comparison and analysis of the two devices on electrical properties at ultrahigh temperatures. In this article, a 1.2 kV conventional MOSFET and a MOSFET integrated with a junction barrier Schottky diode (JBSFET) were fabricated with a consistent process flow. In the temperature range from 300 to 575 K, analytical models of the temperature-dependent electrical parameters of these two devices were established and compared, which were successfully verified by the measurements. These models can provide guidance for ultrahigh temperature applications of JBSFETs. Temperature-related expressions can also be used for junction temperature monitoring of temperature-sensitive electrical parameters. Experimental results show that JBSFET has better third quadrant conduction characteristics and higher temperature stability below 450 K, but loses obvious performance advantages at 575 K. So, the recommended operating temperature range of JBSFET is from 300 to 450 K. Finally, the continuous operation performance of the body diodes in buck converters is analyzed. The higher efficiency of buck converter based on JBSFET's body diode indicates its great application potential in compact converters, especially in the recommended temperature range.**

***Index Terms*—4H-SiC, high-temperature, JBS-integrated MOSFET, MOSFET.**

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Zhaoyuan Gu, Mingchao Yang, Yi Yang, Xihao Liu, Mingyang Gao, Jinwei Qi, Weihua Liu, Chuanyu Han, and Li Geng are with the School of Microelectronics, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: guzhaoyuan@stu.xjtu.edu.cn; yangmingchao@mail.xjtu.edu.cn; 4121156013@stu.xjtu.edu.cn; liuxihao@stu.xjtu.edu.cn; gaomingyang@stu.xjtu.edu.cn; qijinwei@stu.xjtu.edu.cn; lwhua@mail.xjtu.edu.cn; hanchuanyu@mail.xjtu.edu.cn; gengli@xjtu.edu.cn).

Yue Hao is with the School of Microelectronics, Xidian University, Xi'an 710071, China (e-mail: yhao@xidian.edu.cn).

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I. Introduction

In many bridge circuits with hard switching, SiC Schottky barrier diode (SBD) has been widely used as freewheeling diode to increase conversion efficiency [1], [2], [3]. However, the external SBD and bonding wires introduce additional parasitic capacitance and inductance [4]. At the same time, studies show that the body diode of SiC MOSFET can be used as a freewheeling diode [5], but there are still two problems. One is that the long-time conduction of the p-i-n diode has a certain probability of causing bipolar degradation. Although 1.2 kV SiC MOSFETs show little degradation, this degradation still exists in higher voltage level SiC MOSFETs (>3.3 kV) [6], [7]. The other is that the switching losses during the reverse recovery would increase due to the bipolar action, especially at high temperatures [8], [9]. Integrating an SBD into SiC MOSFET may be a good solution. Based on the processes of commercial factories [10], SBD-integrated MOSFETs have been commercialized.

Most existing studies focus on optimizing the structural design of SBD-integrated MOSFETs. The electrical parameters are mainly analyzed at room temperature. The earliest SBD-integrated MOSFETs are extracellular integrated structures [11], [12]. In recent years, intracellular integrated structures have become more common. The planar SBD-integrated MOSFET is called JBSFET or JMOS, generally, it is divided into split-source structure [13], [14], [15], [16] and split-gate structure [17], [18], [19], [20], which integrate JBS between the split sources or split gates, respectively. The trench SBD-integrated MOSFETs were initially manufactured by Fuji Electric Co. and AIST in Japan [21], [22], which integrated SBD on the sidewall of the trench, and implanted a P+ region at the bottom of the trench to shield the high electric field, named SWICH-MOS. Based on these structures, other cell structures are derived. However, most of them are simulation studies [4], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41]. In addition, Han et al. [42], Agarwal et al. [43], [44], [45], and Agarwal and Baliga [46], [47] also made a series of designs on the devices, such as designing the cell shape, the gate oxide thicknesses, and channel types. Besides, some optimized layout designs are proposed to improve the performance [48], [49], [50]. Special packaging methods are also used to improve the

switching performance [51], short-circuit performance [52], and surge current capability [53] of Switch-MOS transistors.

Another part of the research focuses on the electrical properties of mature SBD-integrated MOSFET structures. Kanale et al. [54] compared the high-temperature switching performance at 150 °C, and the short-circuit performance at room temperature [55], [56] of JBSFETs with planar MOSFETs. Also, the avalanche robustness and gate leakage currents of JBSFETs are investigated [57], [58]. The avalanche failure mechanism of JMOS is investigated [59]. Okawa et al. [60], [61] characterized and analyzed the short-circuit withstand capability of SWICH-MOS and found that the short-circuit performance is directly related to the Schottky barrier height [62], similar conclusions were also obtained from the evaluation of the short-circuit stress of JBSFETs [63]. In addition, the team also conducted a comprehensive electrical performance evaluation and comparison of SWICH-MOS. For example, the electrical properties of SWICH-MOS and conventional trench MOSFETs are compared at 175 °C, such as switching performance [64], short-circuit withstand capability, UIS avalanche withstand capability [65], and reverse bias safe operating area [66]. At the same time, they also compared the specific ON-resistance and short-circuit safe operating area trade-OFF characteristics of SWICH-MOS and planar MOSFET at 175 °C [67]. Other teams also conducted a series of tests and analyses on JMOSs and MOSFETs, but high temperature features are not concerned [68], [69]. An equivalent circuit model of JBSFET body diode was established to analyze the ability of the integrated SBD to clamp the PiN at temperatures below 200 °C [70]. JBSFETs with different diode areas were fabricated, then their static [71], switching and robustness characteristics [72], and radiation influence [73] were tested and compared with those of MOSFETS [74].

In high switching frequency power conversion applications, in order to reduce the switching loss, an effective method is to use JBSFETs instead of MOSFETs, which has smaller reverse recovery effect at high temperatures [75]. Experiments found that the pairs based on JBSFETs can achieve higher efficiency and lower switching loss than the pairs based on MOSFETS [76] and conventional Si IGBT pairs with Si p-i-n diode [77]. The inverter using a JBSFET with the p-i-n diode deactivated can reduce the surge voltage at high temperature operation [78].

Power MOSFETs and JBSFETs often operate at high temperatures, such as the power converters in the down-hole oil and gas industry [79], aerospace electronic systems, and automotive and ON-engine electronics [80]. At those applications, MOSFETs need to work at a higher temperature range from 475 to 575 K. That puts forward strict requirements on the high temperature stability of the devices. However, the existing works lack a detailed analysis of the electrical characteristics of MOSFETs and JBSFETs in the high-temperature range, especially above 450 K [81]. Therefore, it is very meaningful and useful to establish the high temperature electrical characteristic model of MOSFETs and JBSFETs.

At present, there is a mature research basis for modeling the temperature characteristics of MOSFETs [82], [83], [84], [85], [86]. Most of these models simulate the static and dynamic waveforms at different temperatures, which is meaningful for circuit design. However, the models of JBSFET are few [87], especially the analysis of temperature-dependent electrical parameters at ultrahigher temperatures. Different from the abovementioned models, the temperature model established in this article is based on semiconductor physics and specially focuses on the direct dependence of key electrical parameters on temperature. By a small amount of calculation, the high-temperature features of devices can be provided or predicted, which is of great application significance.

It is shown that 31% of power electronic system breakdowns are caused by power semiconductor failure, and nearly 60% of the power semiconductor failures are thermally induced [88]. Therefore, online junction temperature monitoring is essential for reliability of power electronic systems. In recent years, various TSEPs have been used for temperature monitoring because of their accuracy and practicability advantages [88], [89]. The temperature-dependent equations of electrical parameters in this work provide a research basis for junction temperature monitoring by TSEPs of MOSFETs and JBSFETs, especially at extremely high power.

In this work, MOSFETs and JBSFETs are fabricated on the same wafer with a compatible process. Then, the temperature dependent electrical parameter models of MOSFETs and JBSFETs are established. Next, the parameters are extracted through static and dynamic measurements from 300 to 575 K. Furthermore, the parameters of the temperature model are determined. Finally, the continuous operation performance of the devices is verified based on a hard switching nonisolated buck converter.

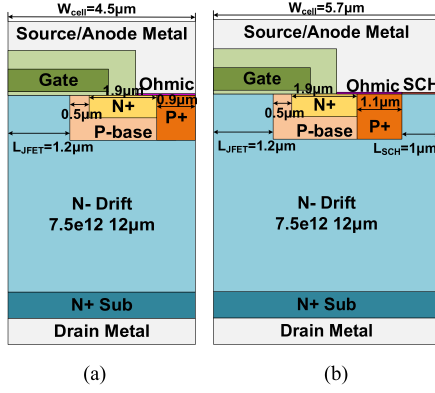
The temperature dependent electrical parameter models at ultrahigh temperatures (300 to 575 K) for JBSFETs, which are consistent with the device structural parameters and the process, are proposed and verified by measurements for the first time. The model is not a SPICE behavioral model. It based on semiconductor theory and directly describes the relationship between electrical parameters and temperature in a sufficiently concise expression.

In order to verify the continuous operation performance of the devices, a hard switching nonisolated buck converter (converting voltage from 600 to 200 V) is designed, which operates at continuous current mode.

The rest of this article is organized as follows. Section II presents the structures and equivalent circuit models of MOSFET and JBSFET. The temperature dependence of static characteristics, switching characteristics, and reverse recovery characteristics are analyzed in Sections III, IV, and V, respectively. The continuous operation performance of buck converter is analyzed in Section VI. Finally, Section VII concludes this article.

II. Device Structures and Equivalent Circuit Models

The cross-sectional views of JBSFET and conventional MOSFET are shown in Fig. 1. JBSFET in Fig. 1(b) embeds a Schottky junction on the right side of the P+ source region. The Schottky contact forms a JBS structure with the P+ regions on both sides. The P+ region shields the high electric field below the Schottky junction, which can effectively reduce the leakage current.



(a) (b)

Fig. 1. Schematic cross sections of (a) MOSFET and (b) JBSFET.

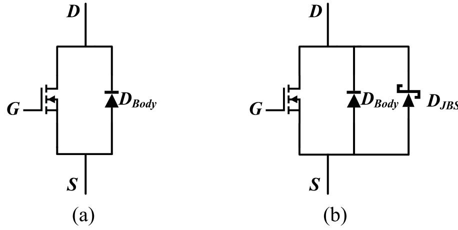


Fig. 2. Equivalent circuit models of (a) MOSFET and (b) JBSFET.

TABLE I
MEASURED STATIC CHARACTERISTICS OF MOSFET AND JBSFET

Parameters	MOSFET	JBSFET
Die Size	3.24 mm×2.76 mm	
$V_{(BR)DSS}$ / V (@V_{GS}=0 V, I_D=10 μA)	1640	1520
I_{DSS} / μA (@V_{GS}=0 V, V_{DS}=1200 V)	1	8.8
V_{th} / V (@V_{DS}=20 V, I_{DS}=5 mA)	2.6	2.6
$R_{DS\ (on)}$ / mΩ (@V_{GS}=20 V, I_{DS}=20 A)	71	74
V_{SD} / V (@V_{GS}=-5 V, I_{SD}=10 A)	4.9	3.1

With the help of TCAD, the parameters of the drift region are determined as 7.5×10^{15} cm^{-3} and 12 μm. The breakdown voltage of more than 1500 V can be achieved by selecting the appropriate junction termination structure. To be compatible with the original MOSFET process, we choose titanium as the Schottky contact metal with work function of 4.33 eV [63], [90].

The devices were fabricated on the same 4-in wafer with standard process flows, including high-temperature ion implantation, growth of gate oxide and polysilicon gate, fabrication of ohmic and Schottky contact electrodes, deposition of Metal, and passivation layers.

The equivalent circuit diagrams of MOSFET and JBSFET are shown in Fig. 2. MOSFET can be regarded as an antiparallel connection of a MOS transistor and a PiN body diode. JBSFET connects a JBS in parallel across the body diode. When JBSFETs operate in the third quadrant, the integrated JBS diodes turn ON before the p-i-n diodes.

The static parameters at room temperature are shown in Table I. Under the same active area, the reverse leakage current ($I_{\rm DSS}$) of JBSFET is 8.8 times as much as that of MOSFET, and the breakdown voltage ($V_{\rm (BR)DSS}$) is about 7% lower than that of MOSFET. The third quadrant voltage drop (V_{SD}) of JBSFET is about 36% lower than that of MOSFET. V_{SD} is related to the doping concentration of the N-region below SCH [17] and the $L_{\rm SCH}$ [91] in Fig. 1. The ON-resistance ($R_{\rm DS(ON)}$) of MOSFET is lower than that of JBSFET because of its larger conductive channel area.

Since the barrier height of the Schottky junction and the mobility of 4H-SiC are both affected by temperature, the effect of temperature on the electrical performance of JBSFETs should be carefully studied.

III. TEMPERATURE-DEPENDENCE MODELS OF STATIC PERFORMANCE

A high-temperature static performance characterization platform for power devices is built with the heating and temperature control unit and power device analyzer/curve tracer (Agilent B1505A). In this section, static performances of MOSFET and JBSFET are analyzed from 300 to 575 K.

A. Temperature Influence on Transfer Characteristics

The impact of the positive charge in the oxide on the threshold voltage can be given by

$$V_{th} = \frac{\sqrt{4\varepsilon_s N_A q \psi_B}}{C_{OX}} + 2\psi_B - \frac{Q_{OX}}{C_{OX}} \tag{1}$$

where ε_s is the dielectric constant of the semiconductor, N_A is the P-base doping concentration, q is the electron charge, C_{ox} is the characteristic capacitance of the oxide layer, Q_{OX} is the total effective charge in the oxide layer, and ψ_B is the semiconductor bulk potential. Q_{OX} mainly includes oxide movable ion charge (Q_{Na}), oxide trap charge (Q_T), oxide fixed charge (Q_F), and interface state trap charge (Q_{Dit}). Among them, ψ_B and Q_{Dit} are temperature-sensitive parameters. ψ_B is given by

$$\psi_B = \frac{kT}{q} \ln \frac{N_A}{n_i} \tag{2}$$

where k is Boltzmann's constant, T is the absolute temperature, and n_i is the intrinsic carrier concentration, given by [92]

$$n_i = 1.70 \times 10^{16} T^{3/2} \mathrm{e}^{-\left(2.08\times10^4\right)/T} \tag{3}$$

ψ_B of SiC MOSFET is large (about 1.6 V) and approximate linear descents with temperature [93].

If the temperature dependence of Q_{Dit} is considered, with the increase of temperature, fewer interface states are occupied. As a result, for a given gate voltage, the inversion charges is higher. Therefore, V_{th} decrease faster. The influence of interface state charge is more obvious at low temperatures [94]. The temperature dependence of V_{th} can be written as

$$V_{th} = a_1\sqrt{b_1 T + c_1 T \ln T + d_1} + 2\left(b_1 T + c_1 T \ln T + d_1\right) - e_1\left(\frac{T}{300}\right)^{f_1} + g_1 \tag{4}$$

where a_1, b_1, c_1, and d_1 are temperature-independent constant terms. The relationship between Q_{Dit} and temperature can be approximated in the form of an exponential by e_1 and f_1. It can also be approximated in the form of e-exponential for better

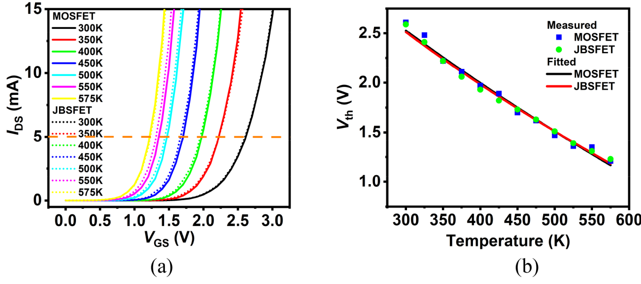


Fig. 3. (a) Measured transfer characteristics of MOSFET and JBSFET. (b) Measured and fitted V_{th} over a temperature range from 300 to 575 K.

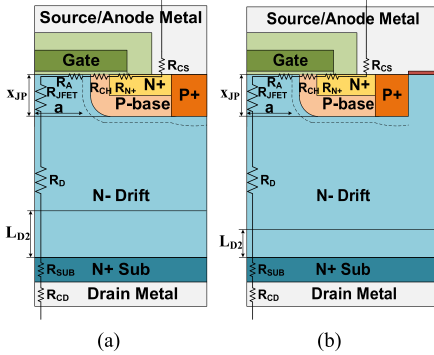


Fig. 4. Structures of (a) MOSFET and (b) JBSFET with internal resistances

continuity [95]. Some behavioral models describe V_{th} as a quadratic polynomial of temperature [85], [96].

The transfer characteristics of MOSFET/JBSFET in the temperature range from 300 to 575 K is shown in Fig. 3(a). The extracted and fitted V_{th} are shown in Fig. 3(b). Measured V_{th} of MOSFET/JBSFET drop from 2.61 V/2.59 V to 1.21 V/1.23 V, respectively. The fitted results are shown as the solid lines, which are in good agreement with the measurements.

B. Temperature Influence on On-Resistance

Fig. 4 shows the internal resistances of the MOSFET and JBSFET. Benefit from the mature ohmic contact process and the high doping concentration of the N+ source region and N+ substrate [97], only the effects of channel resistance (R_{CH}), JFET region resistance (R_{JFET}), and drift region resistance (R_D) on $R_{\text{DS(ON)}}$ are considered, which can be written as

$$R_{\text{DS(on)}} = R_{CH} + R_{\text{JFET}} + R_D \quad (5)$$

R_{CH} can be given by

$$R_{CH} = \frac{L_{CH}}{Z\mu_{ni}C_{ox}\left(V_{GS} - V_{th}\right)} \quad (6)$$

where L_{CH} and Z are the channel length and the channel width, respectively. μ_{ni} is the inversion layer mobility of electrons, V_{GS} is the gate voltage. Affected by the SiC-SiO$_2$ interface states, μ_{ni} has a nonmonotonic temperature coefficient. For low-temperature values, μ_{ni} exhibits a weak positive temperature coefficient, whereas a negative temperature coefficient takes place at high temperatures. It can be accurately described

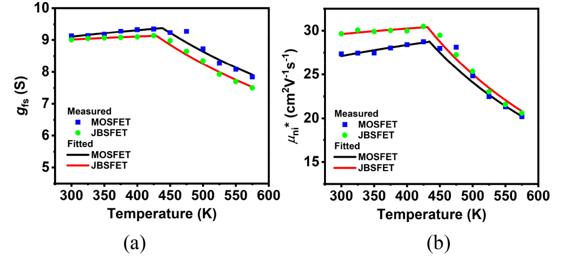


Fig. 5. Measured and fitted (a) g_{fs} and (b) μ^*_{ni} of MOSFET and JBSFET over a temperature range from 300 to 575 K with $V_{\text{DS}} = 20$ V.

through the power relationship [94], given by

$$\mu_{ni}\left(T\right) = \mu_{ni}\left(T_0\right)\left(\frac{T}{T_0}\right)^{-m(T)} \quad (7)$$

where exponent m is temperature-dependent. To simplify calculations, m can be considered as a temperature-independent negative value at low temperatures and a positive value at high temperatures.

The transconductance in the saturated current regime of operation is given by [92]

$$g_{\text{fs}} = \frac{dI_D}{dV_{GS}} = \frac{Z\mu_{ni}C_{OX}}{L_{\text{CH}}}\left(V_{GS} - V_{th}\right) \quad (8)$$

Here, I_D is the drain current. The temperature trend of g_{fs} is consistent with that of μ_{ni}. By extracting g_{fs} from transfer characteristics at different temperatures, the value of m in (7) can be obtained, as shown in Fig. 5. Since the depletion region below the channel is not accurately considered, the measurements of μ_{ni} are not accurate enough, denoted as μ^*_{ni}.

R_{JFET} and R_D can be given by

$$R_{\text{JFET}} = \frac{\rho_{\text{JFET}}x_{JP}}{Za} \quad (9)$$

$$R_D = \frac{\rho_D}{2Z}\ln\left(\frac{W_{\text{cell}}}{a}\right) + \frac{\rho_D}{ZW_{\text{cell}}}L_{D2} \quad (10)$$

where x_{JP} is the junction depth of the P-base, a is the width of the current flow in the JFET region, W_{cell} is the cell witch, L_{D2} is the length of the rectangular region in the current flow path of the drift region. ρ_{JFET} and ρ_D are the resistivities of the JFET region and the drift region, respectively, which are both affected by electron mobility. There is no additional implant in the JFET region, so ρ_{JFET} and ρ_D are equal, given by

$$\rho_{\text{JFET}} = \rho_D = \frac{1}{q\mu_{nD}N_D} \quad (11)$$

where μ_{nD} is electron mobility in the drift region and N_D is doping concentration of drift region. Considering the negative exponential relationship between μ_{nD} and temperature [92], the temperature dependence of $R_{\text{DS(ON)}}$ is expressed as

$$R_{\text{DS(on)}} = \frac{a_2\left(\frac{T}{300}\right)^{b_2}}{V_{GS} - V_{\text{th}}(T)} + d_2\left(\frac{T}{300}\right)^{e_2} \quad (300 \leq T < T_1)$$

$$R_{\text{DS(on)}} = \frac{a_2\left(\frac{T}{300}\right)^{c_2}}{V_{GS} - V_{\text{th}}(T)} + d_2\left(\frac{T}{300}\right)^{e_2} \quad (T_1 \leq T \leq 575) \quad (12)$$

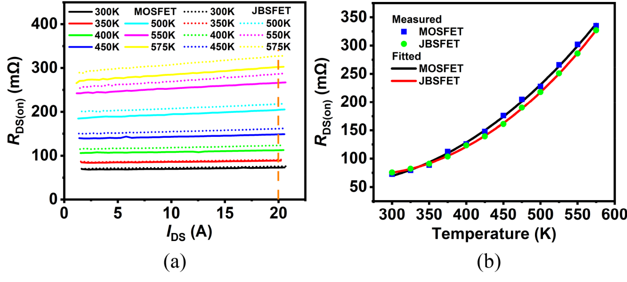


Fig. 6. (a) Measured $R_{\mathrm{DS(ON)}}$ of MOSFET and JBSFET with a gate bias voltage of 20 V. (b) Tested and fitted $R_{\mathrm{DS(ON)}}$ over a temperature range from 300 to 575 K.

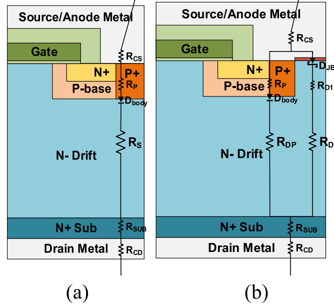


Fig. 7. Internal resistance of (a) MOSFET and (b) JBSFET in third quadrant.

where $V_{th}(T)$ needs to be substituted by (4), b_2 is a negative constant, and c_2 is a positive constant. When the temperature is less than T_1, μ_{ni} has a positive temperature coefficient, while it has a negative temperature coefficient when the temperature is greater than T_1. In some works, to simplify calculations, $R_{\mathrm{DS(ON)}}$ is written as a quadratic expression of temperature [83], [84].

The curves of $R_{\mathrm{DS(ON)}}$ and I_{DS} of MOSFET and JBSFET from 300 to 575 K are shown in Fig. 6(a). In Fig. 6(b), the $R_{\mathrm{DS(on)}}$ versus temperature curve at $I_{\mathrm{DS}} = 20$ A is draw with scatters. The tested $R_{\mathrm{DS(on)}}$ of the MOSFET/JBSFET increases from 73 mΩ/75.6 mΩ to 302 mΩ/327 mΩ, while the fitted results are plotted by solid lines, which are very closed to the measurement results.

C. Temperature Influence on Third Quadrant Characteristics

Fig. 7 shows the internal resistors of MOSFET and JBSFET when conducting in the third quadrant. When a sufficiently negative bias is applied between the gate and source, the channel can be completely turned OFF. At this situation, the third quadrant current is no longer affected by the gate voltage bias [98], [99].

For MOSFET, its body diode is a p-i-n diode, the junction voltage drop is given by

$$V_{PN} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right). \tag{13}$$

Since V_{PN} is affected by n_{i}, it is a negative temperature coefficient [100].

The PiN body diode works in high current mode after turning ON, so there is a significant voltage drop in the internal series resistance of the diode. Therefore, the voltage drop on the p-n junction is less than the bias voltage of the body diode (V_F)

$$V_F = V_{PN} + I_F \times R_S \tag{14}$$

where I_F is body diode current and R_S is drift region resistance [101], given by

$$R_S = \frac{2d}{ZW_{\mathrm{cell}} q\mu_n N_D + \frac{ZW_{\mathrm{cell}}(\mu_n+\mu_p)J_F\tau_{HL}}{2d}} \tag{15}$$

where d is half the length of drift region, μ_n is electron mobility, μ_p is hole mobility, J_F is body diode current density, and τ_{HL} is the high-level lifetime in the drift region. Since μ_n and μ_p can be described as negative exponential relationship with T [97], while τ_{HL} can be expressed as a positive exponential relationship with T [102], R_{S} decreases slightly with temperature [103]. V_{SD} is mainly affected by V_{PN}, which is manifested as a negative temperature coefficient, written by

$$V_{SD-\mathrm{PIN}} = a_3T + b_3 + c_3T\ln T + \frac{1}{d_3\left(\frac{T}{300}\right)^{e_3} + f_3\left(\frac{T}{300}\right)^{g_3}} \tag{16}$$

where ($a_3T + b_3$+$c_3T\ln T$) and the exponential term represent the temperature change of V_{PN} and R_{S}, respectively.

For JBSFET, the body diode is a parallel connection of a p-i-n diode and a JBS diode. At current trim levels, JBS turns on first. If the resistive voltage drop is ignored, the applied voltage is almost entirely devoted to the Schottky junction. The turn-ON voltage drop of the Schottky junction is a negative temperature coefficient, affected by the negative temperature characteristic of the Schottky barrier height Φ_{BN}, given by

$$V_{FS} = \Phi_{BN} + \frac{kT}{q}\ln\left(\frac{J_F}{AT^2}\right) \tag{17}$$

where A is the effective Richardson's constant.

At high current levels, the resistive voltage drop cannot be ignored. The main component is the voltage drop across the series resistors R_{D1} and R_{DJ} in the drift region, given by

$$V_F = V_{FS} + I_F \times R_{D1} + I_F \times R_{DJ} \tag{18}$$

where the JBSFET is in unipolar operation, so the temperature dependence of R_{D1} and R_{DJ} are similar to (8), which increase exponentially with temperature [104]. Assuming that Φ_{BN} approximates a linear relationship of temperature [105], the relation between V_{SD} and T of JBSFET in unipolar operation can be written as

$$V_{SD-\mathrm{JBS}} = \mathrm{a}_4T + b_4 + c_4T \times \ln\frac{1}{T^2} + d_4\left(\frac{T}{300}\right)^{e_4} \tag{19}$$

where (a_4T+b_4+c_4T × ln(1/T^2)) represents the temperature change of V_{FS}. The exponential term represents the temperature change of R_{D1} and R_{DJ}. In order to obtain good fitting results, V_{SD} in some previous works is directly defined as the e-exponential relationship of temperature [106], which may limit the accuracy.

When the current continues to increase, once the voltage drops across $\mathrm{D_{JBS}}$ and R_{D1} exceeds the turn-ON voltage drop of p-i-n diode, $\mathrm{D_{body}}$ is turned ON, so JBSFET enters the bipolar conduction mode. At this time, I_F is composed of two parts, one

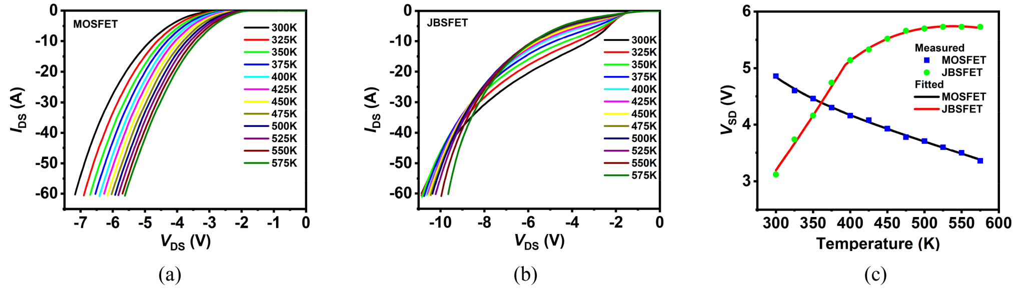


Fig. 8. Measured third quadrant characteristics of (a) MOSFET and (b) JBSFET with V_{GS} of -5 V. (c) Measured and fitted V_{SD} over a temperature range from 300 to 575 K.

part is the bipolar current I_{F1} flowing through PiN, the other part is the unipolar current I_{F2} flowing through JBS. V_F and I_F are written as

$$V_F = V_{FS} + I_{F2} \times (R_{D1} + R_{DJ}) = V_{PN} + I_{F1} \times R_{DP}$$
$$I_F = I_{F1} + I_{F2} \tag{20}$$

where R_{DP} is the series resistance of PiN body diode, and the expression is similar to (15). Therefore, the relation between V_{SD} and T of JBSFET in bipolar operation can be written as

$$V_{SD-\mathrm{JBS}} = \frac{V_{PN}(T) + \mathrm{a}_5\left(\frac{T}{300}\right)^{b_5} + V_{FS}(T)c_5\left(\frac{T}{300}\right)^{d_5}}{1 + c_5\left(\frac{T}{300}\right)^{d_5}} \tag{21}$$

where V_{PN}(T) and V_{FS}(T) substitute the first three terms of (16) and (19), respectively. The exponential term with a_5 and b_5 represents R_{DP}. The other exponential term with c_5 and d_5 represents (R_{DP}/(R_{D1}+R_{DJ})).

The third quadrant characteristics of MOSFET and JBSFET in the temperature range from 300 to 575 K are shown in Fig. 8(a) and (b). The corresponding V_{SD} when I_{DS} is -10 A is extracted shown in Fig. 8(c) along with the fitted curves. It shows that V_{SD} of MOSFET decreases from 4.85 to 3.36 V, while V_{SD} of JBSFET increases from 3.19 to 5.71 V. From the fitted curve of Fig. 8(c), it can be deduced that the p-i-n diode of JBSFET has been activated above 400 K.

It is worth noting that when the bias voltage between source and drain increases to 3 V for the JBSFET, the slope of the third quadrant I-V curve decreases, and an additional "inflection point" occurs. The inflection point is caused by the forward current saturation phenomenon of JBS. The saturation current is related to the saturation drift velocity, the length of the Schottky junction, the doping concentration below the Schottky junction, and the temperature.

It can be seen that V_{SD} of the JBSFET is small at room temperature and has a positive temperature coefficient in the range from 300 to 475 K, which can effectively avoid the local overheating of the device resulting in current concentration. Therefore, JBSFET has better third quadrant conduction characteristics than those of MOSFET in this temperature range.

D. Temperature Influence on Blocking Characteristics

When the devices are in blocking state, the body diodes are reverse biased and suffer from high drain-source voltages. The SBD integrated into the JBSFET provides an additional leakage current path, so the leakage current of the MOSFET and JBSFET exhibit different temperature trends.

For MOSFET, the leakage current before avalanche breakdown is related to the diffusion current I_{dff}, generating and recombining current I_{gen} generated in the barrier region, and surface leakage I_{SL}, given by

$$I_{R-\mathrm{MOS}} = I_{dff} + I_{gen} + I_{SL}. \tag{22}$$

Since n_{i} of 4H-SiC is minimal, the I_{dff} and I_{gen} can be ignored, so surface leakage is the main leakage mechanism, given by [107], [108]

$$I_{R-\mathrm{MOS}} \approx I_{SL} \propto \exp\left(-E_A/kT\right) \tag{23}$$

where the E_A is the activation energy. The leakage current increases significantly at high temperatures, be written as

$$I_{R-\mathrm{MOS}} = a_6 \exp\left(-b_6/kT\right) \tag{24}$$

where a_6 is a temperature-independent constant term and b_6 represents the activation energy. Some paper only considers the impact of I_{gen}, expressed as related to n_{i} [94].

For JBSFET, the possible reverse leakage current mechanisms are 1) thermionic emission, 2) thermionic field emission and field emission, 3) generation and recombination in the depletion region, 4) diffusion, and 5) surface leakage and defect-related leakage [109]. In this article, 3), 4), and 5) can be ignored, while 1) and 2) are mainly considered [109], [110], [111].

Thermionic emission current I_{SCH} is determined by the Schottky barrier height Φ_{BN}, which is given by

$$I_{\mathrm{SCH}} = -AA_J^* T^2 \exp\left(-\frac{q\Phi_{BN}}{kT}\right) \tag{25}$$

where A_{J}^* is cross-sectional area of JBS. Due to the negative temperature coefficient of Φ_{BN}, I_{SCH} increase significantly at high temperatures. At the same time, affected by the image force, the Schottky barrier height also decreases with the increase of the maximum electric field at the metal-semiconductor interface, which is related to the reverse bias voltage. Equation (25) does not show the image force barrier height lowering because it is independent of temperature.

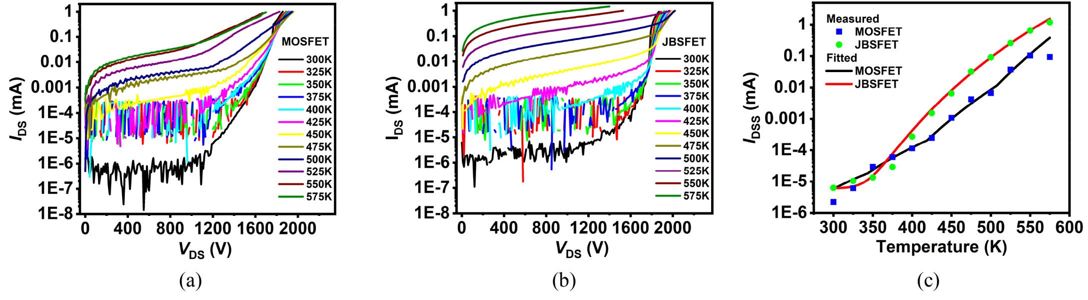


Fig. 9. Measured blocking characteristics of (a) MOSFET and (b) JBSFET with gate bias voltage of 0 V. (c) Tested and fitted I_{DSS} over a temperature range from 300 to 575 K.

Thermionic field emission and field emission are usually described as F-N tunneling current, highly related to the electric field and Schottky barrier, which is given by

$$I_T = -A_J^* \frac{A.T \cdot E_S^2}{q\Phi_{BN}} \exp\left(-\frac{B.T \cdot (q\Phi_{BN})^{3/2}}{E_S}\right) \qquad (26)$$

where $A.T$ and $B.T$ are considered as constants related to effective mass, which are independent of temperature. E_{S} is the electric field at Schottky contact in volts per centimeter [114]. The F-N tunneling current is strongly related to the electric field and weakly affected by temperature. It can be speculated that the leakage current of JBSFET is mainly thermionic emission current under low electric field. However, under high electric field, the leakage current of JBSFET is tunneling current.

If the effect of temperature on tunneling current is neglected at low electric field, the relation between leakage current of JBSFET and T can be given by

$$I_{R-\mathrm{JBS}} = a_7 T^2 \exp\left(-\frac{\Phi_{BN}(T)}{T}\right) + b_7 \qquad (27)$$

where a_7 and b_7 are temperature-independent constant terms, Φ_{BN} (T) represents the linear relationship between Φ_{BN} and T, and b_7 represents correction for leakage current at room temperature.

The blocking characteristics of MOSFET and JBSFET are shown in Fig. 9(a) and (b). When V_{DS} is 1200 V, I_{DS} is extracted as the reverse leakage current I_{DSS}, as shown in Fig. 9(c), the response fitted results are also included. In Fig. 9(b), I_{DS} of JBSFET shows a more obvious temperature dependence at low electric field, where thermal emission current is dominant. At high electric field, the temperature dependence is weakened, and tunneling current becomes dominant. In Fig. 9(c), MOSFET's I_{DSS} is fitted with different activation energies, corresponding to different slopes in exponential coordinates. It indicates that the position of trap energy level changes at different temperatures. JBSFET has larger leakage current than MOSFET at high temperatures. I_{DSS} of JBSFET can reach 100 μA when temperature exceeds 500 K.

E. Junction Capacitance

The structural capacitances, including the input capacitance C_{iss}, output capacitance C_{oss}, and reverse transfer capacitance C_{rss} were measured by Agilent 1505 and N1272A Device Capacitance Selector. The full curves of C_{iss}/C_{oss}/C_{rss} are shown in Fig. 10. The test conditions are $V_{GS} = 0$ V, $V_{\mathrm{DS}} = 1000$ V, $f = 1$ MHz, and $V_{\mathrm{ac}} = 25$ mV, which are consistent with the test conditions in the datasheets of commercial SiC MOSFETs at the same voltage level.

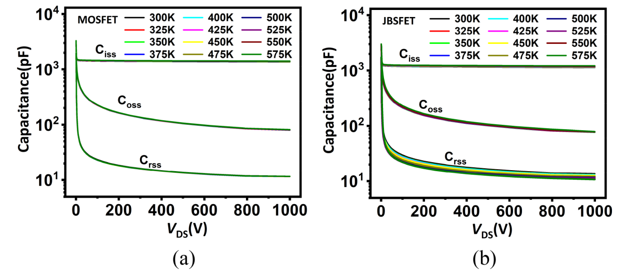


Fig. 10. Measured temperature dependence of C_{iss}, C_{oss}, and C_{rss} of (a) MOSFET and (b) JBSFET over a temperature range from 300 to 575 K.

In Fig. 10(a), the structural capacitance of MOSFET hardly changes with temperature. However, the reverse transfer capacitance C_{rss} of JBSFET decreases slightly as temperature increases. This may be because at high temperatures the integrated Schottky junction is in a reverse-biased state. The hot electron emission current extracts electrons from the drift region, making the thickness of the depletion region under the oxide layer larger, thereby reducing the capacitance of the depletion layer.

In general, the structural capacitance of MOSFET and JBSFET does not change significantly with temperature. Only C_{rss} of JBSFET changes by about 18% at 575 K.

IV. Temperature-Dependence Models of Switching Performance

A. Analytical Modeling of Switching Parameters

The switching performance of power MOSFETs is usually tested through a double pulse test (DPT). Rise/fall times (T_{r}/T_{f}), turn-ON/turn-OFF delay times ($T_{d\mathrm{ON}}$/$T_{d\mathrm{OFF}}$), and switching-ON/switching-OFF/total switching energy losses (E_{ON}/E_{OFF}/E_{sw}) can be extracted to evaluate the switching performance. During switching, the parasitic body diodes of the switched devices (MOSFETs/ JBSFETs) have no effect on the switching process. So, their switching performance parameters exhibit consistent temperature dependence.

When the device is turned ON, the decreasing process of $V_{\rm DS}$ is the process of charging the Miller capacitance C_{GD} by the gate current. During turn-ON and turn-OFF periods, $dV_{\rm DS}/dt$ can be written as [112]

$$dV_{\rm DS}/dt = -\frac{V_{CC} - V_{GP}}{R_g C_{GD(V_{\rm DS})}} \tag{28}$$

$$dV_{\rm DS}/dt = \frac{V_{GP} - V_{EE}}{R_g C_{GD(V_{\rm DS})}} \tag{29}$$

where V_{CC} is the high level of the gate-source voltage V_{GS}, V_{EE} is the low level of V_{GS}, V_{GP} is Miller plateau voltage, $R_{\rm g}$ is gate resistance. In the transient state, C_{GD} can take the mean value of the transient process, then $dV_{\rm DS}/dt$ can be seen as a fixed value related to V_{GP}, which can be written as

$$V_{GP} = V_{th} + \sqrt{\frac{I_{\rm load} L_{CH}}{\mu_{ni} C_{ox} Z}} \tag{30}$$

where $I_{\rm load}$ is load current. V_{GP} is affected by temperature because of the temperature dependence of $V_{\rm th}$ and μ_{ni}.

The temperature dependence of $T_{\rm r}$ and $T_{\rm f}$ can be given by

$$T_r = \frac{a_8}{V_{CC} - V_{th}(T) - \frac{b_8}{\sqrt{\mu_{ni}(T)}}} + c_8 \tag{31}$$

$$T_f = \frac{a_8}{V_{th}(T) + \frac{b_8}{\sqrt{\mu_{ni}(T)}} - V_{EE}} + c_9 \tag{32}$$

where $V_{\rm th}(T)$ is determined by (4), and $\mu_{ni}(T)$ is substituted from (7). a_8 and b_8 are temperature-independent constant terms, c_8 and c_9 represent the temperature-independent correction term in the measurement process.

$T_{\rm dON}$ is the time interval from the moment V_{GS} starts to rise to the moment $V_{\rm DS}$ starts to fall, which can be given by

$$T_{\rm don} = R_g \left(C_{GS} + C_{GD-HV}\right) \ln\left(\frac{V_{CC} - V_{EE}}{V_{CC} - V_{GP}}\right) \tag{33}$$

where C_{GS} is gate-source capacitance and C_{GD_HV} is the gate-drain capacitance with high $V_{\rm DS}$.

$T_{\rm dOFF}$ is the time interval from the moment V_{GS} starts to fall to the moment $V_{\rm DS}$ starts to rise [112], which can be given by

$$T_{\rm doff} = R_g \left(C_{GS} + C_{GD-LV}\right) \ln\left(\frac{V_{CC} - V_{EE}}{V_{GP} - V_{EE}}\right) \tag{34}$$

where C_{GD_HV} is the gate-drain capacitance with low $V_{\rm DS}$.

Considering the temperature dependence of V_{GP}, the relationship between $T_{\rm dON}$ / $T_{\rm dOFF}$ and T can be given by

$$T_{\rm don} = a_{10} \ln\left[\frac{V_{CC} - V_{EE}}{V_{CC} - \frac{b_{10}}{\sqrt{\mu_{ni}(T)}} - V_{th}(T)}\right] + c_{10} \tag{35}$$

$$T_{\rm doff} = a_{11} \ln\left[\frac{V_{CC} - V_{EE}}{V_{th}(T) + \frac{b_{10}}{\sqrt{\mu_{ni}(T)}} - V_{EE}}\right] + c_{11} \tag{36}$$

where a_{10}, b_{10}, and a_{11} are temperature-independent constant terms, c_{10} and c_{11} represent the temperature-independent correction terms in the measurement process.

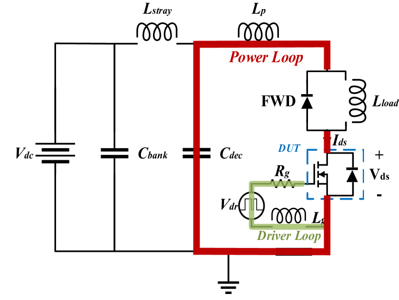


Fig. 11. Schematic diagram of double pulse test circuit.

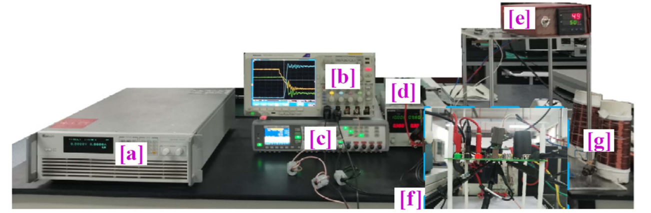


Fig. 12. High-temperature characterization hardware.

In summary, the temperature dependence of $T_{\rm r}$ / $T_{\rm f}$ / $T_{\rm dON}$ / $T_{\rm dOFF}$ depends on V_{GP}. Similar expressions are used in other analytical models [86], [96].

Based on theoretical expressions and measurements, the switching parameters are described as equations that only depend on temperature. The whole work and the established equations can provide valuable guidance for high temperature operations of MOSFETs and JBSFETs.

The switching loss of devices is defined as the time integral of the product of voltage and current over the turn-ON and turn-OFF intervals. Obviously, due to the shorter turn-ON time and longer turn-OFF time, if the reverse recovery and forward recovery of the FWD can be neglected, $E_{\rm ON}$ decreases and $E_{\rm OFF}$ increases with the increase of temperature.

B. Double Pulse Test Circuit for Switching Test

The schematic diagram of DPT circuit is shown in Fig. 11. The test platform of high-temperature DPT is shown in Fig. 12.

In Fig. 11, the device under test (DUT) forms a drive loop with the gate drive power supply and the drive board. The power loop includes DUT, power load inductor, and freewheeling diode. The gate resistance ($R_{\rm g}$), the bus voltage ($V_{\rm dc}$), the load inductance ($L_{\rm load}$), and the capacitance of the dc bus ($C_{\rm bank}$) have significant impacts on the test results.

In Fig. 12, the DUT, the high-temperature test fixture, and the double-pulse test circuit are marked with blue frame lines. Other equipment includes programmable dc power supply [a], digital phosphor oscilloscope [b], pulse function arbitrary generator [c], auxiliary power supply [d], temperature controller [e], and load inductance [g]. The DUT is separately connected to a temperature control unit, heated by MCH alumina ceramic. In this way, the other components of the test circuit are kept at room temperature during the high temperature test.

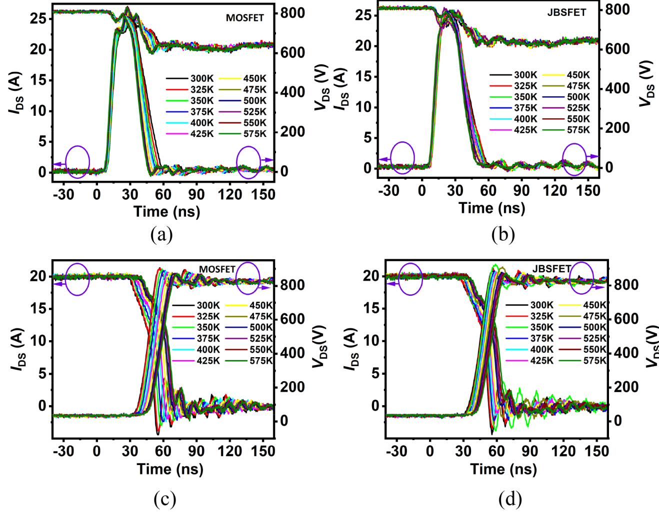


Fig. 13. Measured turn-ON transient waveforms of (a) MOSFET and (b) JBSFET, and turn-OFF transient waveforms of (c) MOSFET and (d) JBSFET with temperature increase from 300 to 575 K. Measurement conditions: $V_{\mathrm{dc}} =$ 800 V, $I_{\mathrm{load}} = 20$ A, and $R_{\mathrm{g}} = 6.66\ \Omega$.

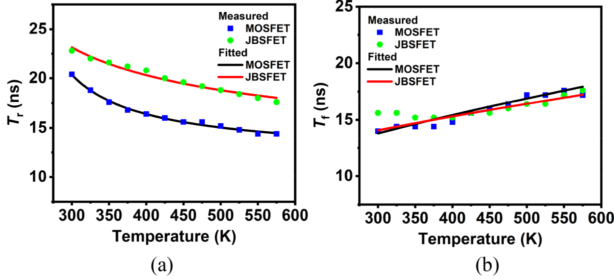


Fig. 14. (a) Extracted and fitted T_{r} and (b) T_{f} of two DUTs with a temperature range from 300 to 575 K.

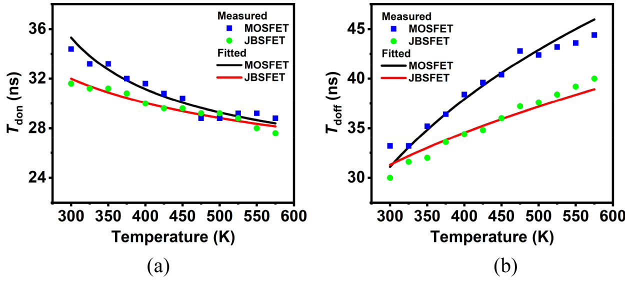


Fig. 15. (a) Extracted and fitted $T_{d\mathrm{ON}}$ and (b) $T_{d\mathrm{OFF}}$ of two DUTs with a temperature range from 300 to 575 K.

C. Temperature Influence on Switching Parameters

The switching waveforms at different temperatures of MOSFET and JBSFET are shown in Fig. 13. The freewheeling diode is C4D20120A.

The switching time ($T_{\mathrm{r}}/T_{\mathrm{f}}$), switching delay time ($T_{d\mathrm{ON}}/T_{d\mathrm{OFF}}$) of MOSFET and JBSFET at different temperatures are extracted and represented as scatter points, and the corresponding model fitted results are represented as solid lines in Figs. 14 and 15.

In Fig. 14, when the temperature increases from 300 to 575 K, T_{r} of the MOSFET (JBSFET) decrease and T_f increase. The T_r and T_f of MOSFET are smaller than JBSFET because the

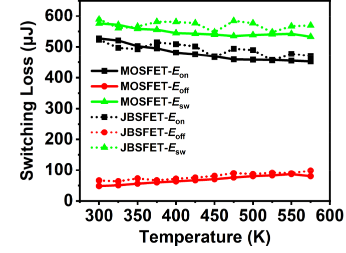


Fig. 16. Extracted $E_{\mathrm{ON}}/E_{\mathrm{OFF}}/E_{\mathrm{sw}}$ of two DUTs with a temperature range from 300 to 575 K.

Miller capacitance is smaller. The fitted results of Tr are in good agreement with the measured results, while the fitted results of T_f deviate slightly from the measured results. This may be due to the introduction of some deviations in the measurement and the limitation of the sampling accuracy of the test equipment (for example, the minimum sampling interval of the digital phosphor oscilloscope is 0.4 ns).

In Fig. 15, $T_{d\mathrm{ON}}$ of the MOSFET (JBSFET) decreases while $T_{d\mathrm{OFF}}$ increases with the increase of temperature. $T_{d\mathrm{ON}}$ of MOSFET is larger than that of JBSFET because the measured C_{GS} is larger. Although there is a little deviation, the trend of the fitted $T_{d\mathrm{ON}}/T_{d\mathrm{OFF}}$ is in good agreement with the measurements. Therefore, the fitted results of the analytical model can predict the unmeasured temperature points.

According to the test waveforms, the switching loss is calculated, as shown in Fig. 16.

As previously inferred, E_{ON} of the MOSFET/JBSFET is reduced from 527.4 μJ / 523.2 μJ to 452.6 μJ / 470.5 μJ, and E_{OFF} increase from 48.3 μJ / 66.2 μJ to 80.3 μJ / 98.7 μJ, E_{sw} does not change much, only drops from 575.7 μJ / 589.4 μJ to 533 μJ / 569.2 μJ.

V. Temperature-Dependence Models of Reverse Recovery Performance

A. Analytical Model of Reverse Recovery Parameters

The reverse recovery performance is mainly related to the performance of body diode. The peak reverse recovery current I_{rm}, and the reverse recovery charge Q_{rr} are extracted to evaluate the reverse recovery performance.

For MOSFET, the parasitic PiN body diode is a bipolar device, so one part of its reverse recovery current comes from the charging current of the diode junction capacitance $I_{Coss(\mathrm{t})}$, and the other part is used to sweep excess carriers in the drift region $I_{D(t)}$ [113], which can be written as

$$I_{\mathrm{DUT}(t)} = I_{C_{oss}(t)} + I_{D(t)} \tag{37}$$

where $I_{Coss(\mathrm{t})}$ is related to the junction capacitance C_F and the rate of change of the diode voltage V_F, which has no apparent temperature dependence. The diffusion current density at the boundary of the p-n junction is related to the carrier concentration gradient, described as

$$J_F = 2qD_a(dn/dx)_{x=-d} \tag{38}$$

where D_a is the ambipolar diffusion coefficient, $(dn/dx)_{x=-d}$ is carrier concentration gradient at the boundary of the p-n junction. Combined with the exponential relationship between minority carrier lifetime and temperature, the relationship between I_{rm} and temperature of MOSFET can be expressed as

$$I_{rm-\text{MOS}} = I_{rmT_0-\text{MOS}}\left(\frac{T}{300}\right)^{a_{11}} + b_{11} \tag{39}$$

where $I_{rmT0\text{-MOS}}$ is I_{rm} of MOSFET at 300 K, the exponential term represents the relationship between the minority carrier lifetime and temperature, b_{11} represents the temperature-independent measurement correction term for $I_{rm\text{-MOS}}$. Similar exponential relationships between I_{rm} and T have also been used in other work [95].

For JBSFET, in the unipolar mode, its reverse recovery current is mainly caused by the charging of the diode capacitance. Correspondingly, the minority carrier current introduced by the built-in SBD can be ignored. Since the body-diode junction capacitance hardly changes with the temperature, the JBSFET exhibits weak temperature dependence. Once the p-i-n diode is turned on, similar to the MOSFET, the JBSFET needs to sweep additional minority carriers during the reverse recovery. Assuming that when the temperature exceeds T_1, the JBSFET starts to work in bipolar mode, then the relationship between I_{rm} and temperature of JBSFET can be expressed as

$$I_{rm-\text{JBS}} = I_{rmT_0-\text{JBS}} + b_{12} \text{ (unipolar mode)}$$
$$I_{rm-\text{JBS}} = I_{rmT_1-\text{JBS}}\left(\frac{T}{T_1}\right)^{a_{12}} + b_{12} \text{ (bipolar mode)} \tag{40}$$

where $I_{rmT0\text{-JBS}}$ is I_{rm} of JBSFET at 300 K, $I_{rmT1\text{-JBS}}$ is I_{rm} of JBSFET at T_1, b_{12} represents the temperature-independent measurement correction term for $I_{rm\text{-JBS}}$.

Similarly, Q_{rr} is introduced by junction capacitance charging and extracting excess carriers in the drift region. The relationship between Q_{rr} and temperature can be written as

$$Q_{rr-\text{MOS}} = Q_{rrT_0-\text{MOS}}\left(\frac{T}{300}\right)^{a_{13}} + b_{13} \tag{41}$$

$$Q_{rr-\text{JBS}} = Q_{rrT_0-\text{JBS}} + b_{14} \text{ (unipolar state)}$$
$$Q_{rr-\text{JBS}} = Q_{rrT_1-\text{JBS}}\left(\frac{T}{T_1}\right)^{a_{14}} + b_{14} \text{ (bipolar state)} \tag{42}$$

where $Q_{rrT0\text{-MOS}}$ is Q_{rr} of MOSFET at 300 K, $Q_{rrT0\text{-JBS}}$ is Q_{rr} of JBSFET at 300 K, $Q_{rrT1\text{-JBS}}$ is I_{rm} of JBSFET at T_1, the exponential term represents the relationship between lifetime and temperature, b_{13} and b_{14} represent the temperature-independent measurement correction term. Q_{rr} is described as a linear relationship with temperature in [86], but the narrow temperature range is not suitable for the discussion of this work.

B. Temperature Influence on Reverse Recovery Parameters

Reverse recovery test for MOSFET and JBSFET from 300 to 575 K is performed with DPT circuit. The reverse recovery performance of DUT can be extracted from the turn-ON waveform of the auxiliary MOSFET. When the DUT is heated

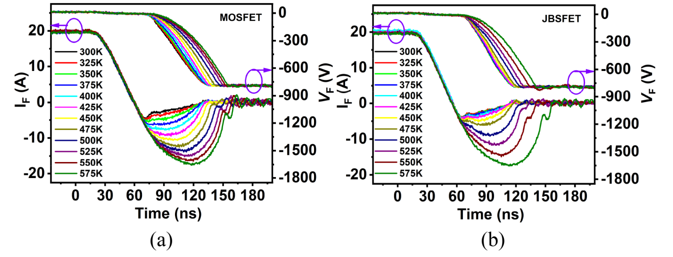


Fig. 17. Measured reverse recovery waveforms of (a) MOSFET and (b) JBSFET. Measurement conditions: $V_{\text{dc}} = 800$ V, $I_{\text{load}} = 20$ A, $R_g = 33\ \Omega$, $di/dt = 556$ A/μs.

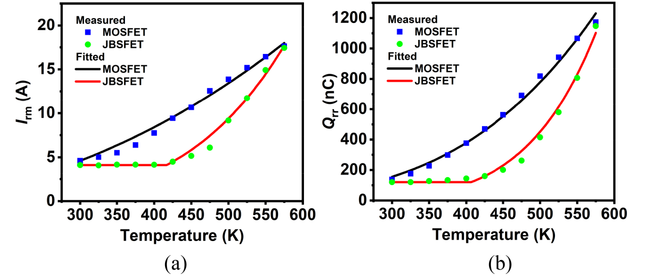


Fig. 18. Extracted and fitted temperature dependence of (a) I_{rm} and (b) Q_{rr} of two DUTs with a temperature range from 300 to 575 K.

to high temperatures, other devices in the circuit remain at room temperature.

In the reverse recovery test, C2M0080120D is selected as the auxiliary MOSFET. By comparing the measured waveforms under different conditions, larger V_{dc} increases Q_{rr} but has little effect on I_{rm}. Too small R_g results in inaccurate measurements. Larger I_{load} reduces I_{rm} and Q_{rr} of JBSFET, however, it has little effect on MOSFET. The test conditions of $V_{\text{dc}} = 800$ V, $I_{\text{load}} = 20$ A, and $R_g = 33\ \Omega$ are selected.

The measured reverse recovery waveforms are shown in Fig. 17. From Fig. 17(a), the reverse recovery current of MOSFET has significantly increased as temperature increases. In contrast, the reverse recovery waveforms of JBSFET almost does not change below 450 K. Although the reverse recovery waveforms of JBSFET deteriorate when the temperature is higher than 450 K, they are still better than MOSFET, as shown in Fig. 17(b).

In Fig. 18, I_{rm} and Q_{rr} of the MOSFET and JBSFET are represented by the scatter points, and the fitted results are represented by solid lines. In Fig. 18(a), the measured I_{rm} of MOSFET increases by 4.6 times while I_{rm} of JBSFET does not change much when the temperature changes from 300 to 450 K. Especially, in temperature range from 475 to 575 K, I_{rm} of JBSFET starts to increase highly. It is 17.42 A at 575 K, 4.23 times as much as that at 300 K, approximately equal to MOSFET. The body diode of JBSFET starts to work in bipolar mode at a temperature between 400 and 425 K, which is close to the speculation in Fig. 8.

The same conclusion can also be drawn from Fig. 18(b). Over the temperature range from 300 to 575 K, Q_{rr} of the MOSFET increases from 138 nC (@300 K) to 1173 nC (@575 K) by about 8.5 times. In contrast, Q_{rr} of JBSFET varies very little over the temperature range from 300 to 450 K, increasing only from

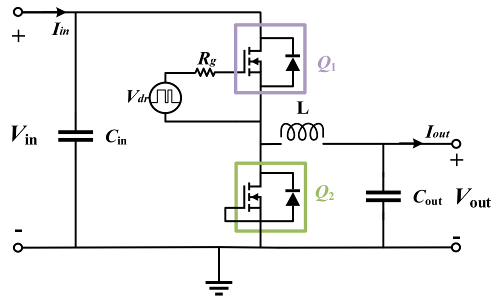


Fig. 19. Schematic of hard switching nonisolated buck converter.

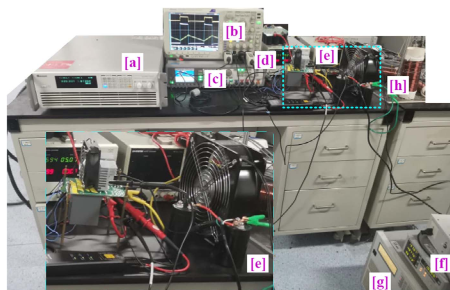


Fig. 20. Test setup of buck converter.

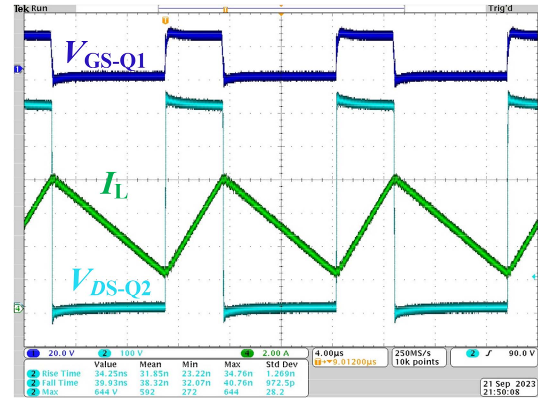


Fig. 21. Measured waveform of buck converter with taking body diode of JBSFET as freewheel diode. Test conditions are $V_{\text{in}} = 600$ V, $P_{\text{out}} = 1$ kW, and $f_{\text{sw}} = 75$ kHz.

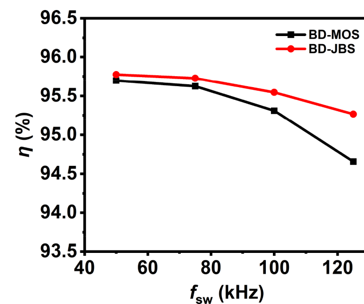


Fig. 22. Comparison of conversion efficiency variation over switching frequency scale.

120 nC (@300 K) to 200 nC (@ 450 K). Q_{rr} of the JBSFET starts to increase significantly when the temperature is higher than 450 K. It is 1171 nC at 575 K, 9.76 times as much as that at 300 K, close to those of MOSFET. In this case, JBSFET has lost its advantage in reverse recovery performance.

To sum up, for the temperature stability of the reverse recovery performance, we recommend that the operating temperature of JBSFET is from 300 to 450 K.

VI. Continuous Operation Performance of Body Diodes

A. Hard Switching DC–DC Buck Converter

In order to evaluate the continuous operation performance of the body diodes of MOSFETs and JBSFETs, a hard-switching nonisolated dc–dc buck converter is designed in this section shown in Fig. 19. It includes a switching MOSFET Q_1, a freewheeling diode Q_2, a R_g of 20 Ω for Q_1, an input capacitor of 42.3 μF, an output capacitor of 1 mF, and a power inductor of 334 μH. The input voltage of the converter s 600 V with 33.3% duty ratio.

The buck converter test setup is shown in Fig. 20, which includes a programmable dc power supply [a], a digital phosphor oscilloscope [b], a pulse function arbitrary generator [c], an auxiliary power supply [d], a buck converter and cooling facilities [e], a digital power meter [f], a programmable electronic load [g], and a load inductance [h].

The measured waveforms of buck converter in 75 kHz are shown in Fig. 21. Including the gate-source voltage of Q_1 ($V_{GS\text{-}\mathrm{Q1}}$), the drain-source voltage of Q_2 ($V_{\text{DS-Q2}}$), and the inductor current (I_{L}). The smooth waveforms show that the buck converter can work stably under this condition. The rise/fall time of $V_{\text{DS-Q2}}$ is 34.25 ns/39.93 ns, the effective value of output current is 4.91 A and the output power is 970.6 W.

B. Analysis of Converter Efficiency

The power loss of the buck converter can be written as [8]

$$P_{\text{loss}} = P_{Mcon} + P_{Msw} + P_{Dcon} + P_{Drec} + P_{\text{passive}} \quad (43)$$

where P_{Mcon} and P_{Msw} are MOSFET conduction loss and switching loss, P_{Dcon} and P_{Drec} are diode conduction loss and reverse recovery loss, and P_{passive} is passive devices loss. Since the other components in the circuit are identical except for the diode, the difference in P_{loss} of buck converter based on body diode of MOSFET/JBSFET (BD-MOS/BD-JBS) is determined by P_{Dcon} and P_{Drec}.

The real-time input power is displayed by the high-voltage dc power supply, and the output power is measured by the power meter. The conversion efficiency of the buck converter is the ratio of output power to input power. In the frequency range from 50 to 125 kHz, the conversion efficiency η of buck converter is shown in the Fig. 22.

The conversion efficiency η of BD-JBS based buck is higher than that of BD-MOS based buck in this frequency range, especially under high frequency conditions. Monitored by an infrared thermal camera, the steady-state junction temperature is from 377 to 427 K.

According to the previous analysis in Section III, V_{SD} of JBSFET has no obvious advantage compared with that of MOSFET in this temperature range. Therefore, the higher efficiency of BD-JBS based buck converter can be regarded as benefit from the lower reverse recovery loss of BD-JBS.

VII. Conclusion

Two kinds of 1.2 kV power devices, i.e., a conventional MOSFET and a junction barrier Schottky diode integrated MOSFET (JBSFET) are fabricated on the same wafer in this work. Analytical models for the temperature sensitive electrical parameters of devices in the temperature range from 300 to 575 K were established, and verified by the test results. In general, the forward operating characteristics of MOSFET and JBSFET, such as $V_{\rm th}$, $R_{\rm DS(ON)}$, and switching performance, have the same temperature trend. In contrast, the temperature trends of their reverse operational aspects such as V_{SD}, $V_{\rm (BR)DSS}$, $I_{\rm DSS}$, and the reverse recovery performance are different. Based on this, we provide a guidance for the application temperature range of JBSFETs, which is from 300 to 450 K. In addition, the obtained temperature equations of electrical parameters provide a basic principle and guidance for junction temperature monitoring and protection. Finally, the continuous operation performance of MOSFETs and JBSFETs are evaluated and quantified based on hard-switched nonisolated buck converter. Conversion efficiency can be improved by using JBSFET as freewheeling diode due to its lower reverse recovery loss, especially at high frequency.

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Zhaoyuan Gu received the B.Sc. degree in communication engineering and the M.Sc. degree in integrated circuit engineering from Zhengzhou University, Zhengzhou, China, in 2015 and 2018, respectively. She is currently working toward the Ph.D. degree in electronic science and technology with the Xi'an Jiaotong University, Xi'an, China.

Her current research interests include silicon carbide power device modeling and electrical performance analysis under ultrawide temperature scales.

Mingchao Yang received the B.S. and M.S. degrees in engineering from Xi'an University of Technology, Xi'an, China, in 2009 and 2012, respectively.

From 2012 to 2015, he was with Jingjing Optoelectronic Technology Company Ltd. Since 2016, he has been a member with the School of Microelectronic, Xi'an Jiaotong University. His main research interest includes wide band gap devices.

Yi Yang received the B.S. degree in microelectronics science and engineering from Jilin University, Changchun, China, in 2021. He is currently working toward the Ph.D. degree in electronic science and technology with the School of Microelectronics, Xi'an Jiaotong University, Shanxi, China.

His research interests include silicon carbide power electronic devices and reliability of power devices.

Xihao Liu received the B.Sc. degree in microelectronics in 2020 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree in electronic science and technology with the School of Microelectronics, Xian Jiaotong University, Xian, China.

His research interests include power management circuit and system design, efficient SiC-based power converters, and system–level packaging or integration of wide bandgap power devices.

Mingyang Gao received the B.Sc. degree in microelectronics science and engineering and the M.Sc. degree in microelectronics and solid-state electronics from Xi'an Jiaotong University, Xi'an, China, in 2019 and 2022, respectively.

His current research interests include the design, modeling, and characterization of the SiC-based power MOSFET.

Jinwei Qi received the B.S. degree in microelectronics and solid-state electronics and the Ph.D. degree in electronic science and technology from Xi'an Jiaotong University, Xi'an, China, in 2015 and 2021, respectively.

He was a Visiting Ph.D. with the Electrical Engineering Division, University of Cambridge, U.K., from 2019 to 2020. His current research interests include wide band gap device modeling and reliability analysis under ultrawide temperature scales.

Weihua Liu (Associate Member, IEEE) received the B.Sc., M.Sc., and the Ph.D. degrees in electronic science and technology from Xi'an Jiaotong University, Jiaotong, China, in 1998, 2001, and 2005 respectively.

From 2009 to 2010, he was a visiting researcher in Prof. W. Zhonglin's research team with the Georgia Institute of Technology. He is currently a Professor with the School of Microelectronics, Xi'an Jiaotong University, Xi'an, China. His current research interests include micronano sensors, carbon-based electronics, and power semiconductor devices and processes.

Chuanyu Han (Member, IEEE) received the B.Sc. degree in applied physics from Shandong University of Science and Technology, Qingdao, China, in 2008, the M.Sc. degree in microelectronics from Graduate University of Chinese Academy of Sciences, Beijing, China, in 2011, and the Ph.D. degree in microelectronics from The University of Hong Kong, Hong Kong, in 2015.

From 2017 to 2018, he was a Visiting Scholar with the Department of Electrical Engineering, Columbia University, New York, NY, USA. He is currently an Associate Professor with the School of Microelectronics, Xi'an Jiaotong University, Xi'an, China. His current research interests include neuromorphic devices and their systems, pulsed neural networks and their hardware implementations, memristors, thin-film transistors, and power semiconductor devices.

Li Geng (Senior Member, IEEE) received the B.Sc. degree in physics and the M.Sc. and Ph.D. degrees in electrical engineering from the Xi'an University of Technology, Xi'an, China, in 1990, 1998, and 2001, respectively.

She was a Visiting Scholar with the Department of Electrical Engineering, Ilmenau University of Technology, Ilmenau, Germany, from 1999 to 2000. From 2007 to 2008, she was a Visiting Professor with the Department of Electrical Engineering, Stanford University, Stanford, CA, USA. She is currently a Professor with the School of Microelectronics, Xi'an Jiaotong University, Xi'an, China. Her research interests include power management integrated circuits, low-voltage low-power analog- and mixed-signal integrated circuits, RF-integrated circuits, and bioimplant systems.

Yue Hao (Senior Member, IEEE) received the Ph.D. degree in computational mathematics from Xi'an Jiaotong University, Xi'an, China, in 1991.

He is currently the Executive Director with the Chinese Association of Electronics and the Chairperson of the Executive Councils of the Shaanxi Provincial Association of Electronics, the Trade Association of Integrated Circuits, and the Shaanxi Provincial Semiconductor Illumination Association. He is the Leader of the Experts Group for the implementation of the major sci-tech items of "core electronic devices, high-end universal chips, and basic software products" in the medium-to-long term program. He is the Leader of the Microelectronic Technology Experts Group, General Armament Department, People's Liberation Army of China, China. He is the Vice Chairperson with the National Steering Committee of the Specialty of Electronic Information Science and Engineering. His current research interests include wide forbidden band semiconductor materials and devices.

Dr. Hao is a member of the Ninth and Tenth Chinese People's Political Consultative Conference and the Deputy to the 11 National People's Congress of the People's Republic of China. He is the Vice President with the State Key Discipline Laboratory of Wide Bandgap Semiconductor Technology, School of Microelectronics, Xidian University, Xi'an, China.