Bipolar Current-Fed DC–DC Converter With Automatic Voltage Balance and Full Range ZVS for Bipolar DC System

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***Abstract*—The bipolar dc microgrid is attracting attention for its high efficiency and reliability, but the bipolar dc bus is susceptible to unbalanced power. This article proposes a bipolar current-fed dc–dc converter with automatic voltage balance under phase-shift plus pulsewidth control. Combined with the current-fed dual active bridge converter and voltage balancer, the circuit structure is streamlined and fewer devices are required. The proper magnetizing inductance allows the converter to achieve automatic bipolar voltage balancing even under extreme load imbalance, and achieve full-range zero-voltage switching (ZVS) over a wide voltage range. In addition, the coupled inductor is utilized to further reduce the number of magnetic components. Finally, based on the accurate ZVS analysis considering parasitic capacitance, the parameters of the converter are designed, and an experimental prototype is constructed to verify the feasibility of the proposed scheme.**

***Index Terms*—Bipolar voltage balance, current-fed dual-active-bridge converter, zero-voltage switching.**

I. Introduction

RENEWABLE energy sources and distributed energy supply technologies have become a research hotspot in recent years due to the advantages of clean, efficient, and grid operation improvement. However, distributed power sources such as photovoltaic are susceptible to environmental influences and are volatile, so they are usually connected to dc microgrids with energy storage systems (ESSs). Compared to the ac bus, the dc bus can reduce the number of power conversions [1] and the input of reactive power compensation equipment, as well as avoid harmonic pollution and voltage intermittency [2].

According to the structure of the dc bus, dc systems can be divided into unipolar dc systems and bipolar dc systems [3]. Although the unipolar dc system is simple to implement, it can only provide one voltage level. In contrast, the bipolar dc system can generate three voltage levels on a three-wire configuration, including symmetrical positive and negative polarity voltages, to meet the voltage needs of different loads and distributed power sources, and are more flexible to use. In addition, bipolar dc systems offer higher efficiency, reliability, and security [4], [5], [6]. Therefore, it can be widely used in bipolar dc-bus-fed fast charging stations [7], data centers, and residential complexes [8]. However, there is a challenge in the bipolar dc system, namely bipolar voltage imbalance [9], because there are loads with different characteristics connected to the bipolar dc bus, absorbing or injecting different levels of power flow into it, resulting in an imbalance between positive and negative voltages, which in turn affects the normal operation of the equipment.

Therefore, a series of voltage balancers have been proposed to alleviate the bipolar voltage imbalance problem [9], [10], [11], [12]. For example, a simple buck/boost-type voltage balancer is proposed in [10], but its topology has a risk of shoot-through. Thus, in the literature [11], a dual-buck half-bridge voltage balancer is presented to avoid the problem of shoot-through of the bridge arms in the converter. In addition, a three-level voltage balancer is proposed to reduce the voltage stress of switches [12]. In [9], based on the existing voltage balancers, a general topology principle for voltage balancers is derived and several new voltage balancers are proposed.

In addition, considering the safety of the dc bus system, more and more scholars are focusing on the integration of conventional voltage balancers with isolated dc–dc converters in solid-state transformers to provide electrical isolation and voltage balancing capability [13]. Enhancements are proposed for different optimization objectives such as achieving soft switching [8], reducing the number of switches [14], decoupling the bipolar control [15], and so on.

For the above studies [13], [14], [15], the voltage gain range of the converter is narrow, which would limit the application used for ESSs connected to the bipolar dc bus system. To increase the

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voltage regulation range, some modified topologies are studied, which could be roughly divided into nonisolated solutions with a wide voltage range [16], [17] and isolated solutions with a wide voltage range [18], [19], [20], [21].

For nonisolated solutions with a wide voltage range, Prabhakaran and Agarwal [16] proposed a converter that can feed power into the bipolar dc bus to mitigate voltage imbalance. A four-port converter is proposed in [17], which can integrate photovoltaic (PV) systems and ESSs into a bipolar dc system, but it suffers from hard switching and high component count. Prabhakaran and Agarwal [16] and Tian et al. [17] do not have galvanic isolation, which makes it difficult to eliminate high floating voltages and leakage currents [22], and the system safety is low. In addition, most nonisolated boost converters face the contradiction of high voltage gain and low component count [23].

Compared with nonisolated solutions, the isolated solutions offer higher reliability and security. Tian et al. [18] proposed a family of bipolar converters based on the voltage multiplier technique, and Tian et al. [19] used a switched-capacitor circuit on the secondary side of the converter. Tian et al. [18] and [19] belong to the voltage-fed dual-active-bridge (VF-DAB) converters, but they can provide higher voltage gains and automatic bipolar voltage balancing compared to conventional VF-DAB converters. However, VF-DAB converters are not suitable for energy storage systems [24] that are sensitive to current ripple. Therefore, bipolar CF-DAB converters [20], [21] are proposed, which not only have the advantage of low input current ripples [24] but also make it easier to construct multiport structures [25]. Tian et al. [20] deduce a series of isolated converters with bipolar outputs and illustrates characteristics of a typical topology (full-bridge interleaved buck/boost structure on the primary side and center-tap semiactive rectifier on the secondary side), including the soft switching range. Tian et al. [21] integrated the rectifier and the buck–boost voltage balancer into the secondary side of the converter, thus providing the advantages of bipolar voltage balancing and single-stage power conversion. However, Tian et al. [20] and [21] suffered from the difficulty of achieving ZVS at light loads and extremely unbalanced loads, which may cause problems such as high switching losses, high voltage spikes, and severe electromagnetic interference to the converter [26]. In [27], it is mentioned that using the magnetizing inductor can improve the ZVS range, but the dead time factor is ignored. In summary, existing bipolar converters mostly face challenges such as the need for bulky balancing inductors [13], [14], a large number of components, and difficulties in achieving ZVS under extremely unbalanced loads [18], [19], [20], [21].

In this article, a modified CF-DAB converter with balanced bipolar voltage is proposed. Compared with the existing bipolar converters, such as literature [20] and [21], the advantages of the proposed converter are shown as follows.

1) Only two active switches and two capacitors are required for the bipolar ports. By utilizing the magnetizing inductance of the transformer to offer the possibility to balance the bipolar voltage under unbalanced load conditions, the need for the additional dc inductor is eliminated. Consequently, the component number can be much reduced.

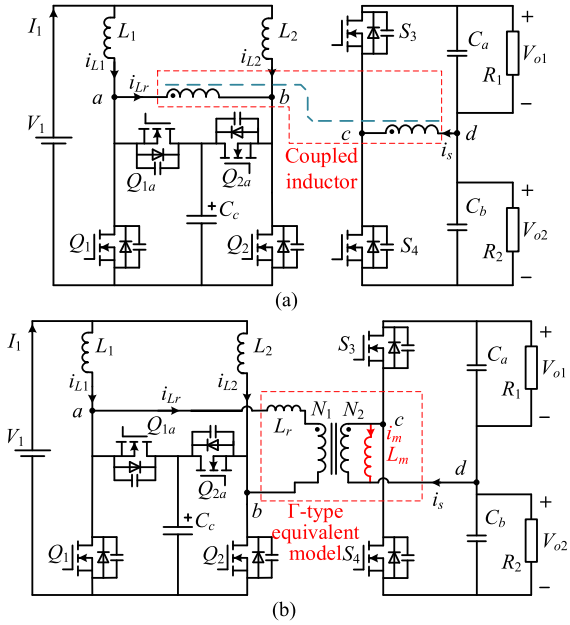

Fig. 1. Proposed bipolar CF-DAB converter. (a) Circuit topology. (b) Equivalent circuit.

2) Full load range ZVS of the proposed converter can be realized under a wide voltage range, and even under extreme load conditions, without the need for complex control and auxiliary components. In addition, precise ZVS analysis is used, which takes into account junction capacitors and dead time, and reveals the impact of ZVS implementation on bipolar voltage deviations.
3) To further reduce the magnetic component, a coupled inductor is utilized, which integrates the external leakage inductance, magnetizing inductance, and transformer into an EE core.

The rest of this article is organized as follows. The topology and modulation scheme of the proposed converter are described in Section II. Section III focuses on the converter voltage balancing mechanism under unbalanced power and the bipolar voltage deviation that may be generated in a practical case. After that, the influence of unbalanced power on the ZVS performance of the converter is investigated in Section IV, combined with the consideration of different magnetizing inductances. The related parameter optimization design is given in Section V, including the coupled inductor design. Based on this, Section VI provides experimental results to test the validity of the theory. Finally, Section VII concludes this article.

II. Basic Operation Principle

A. Circuit Topology

Fig. 1 illustrates the topology of the proposed current-fed dc–dc converter with bipolar ports. In order to streamline the circuit structure to the extent possible, a coupled inductor is utilized in the proposed converter, as shown in Fig. 1(a). To facilitate the subsequent analysis of the principles and characteristics, Fig. 1(b) shows the Γ-type equivalent model of the

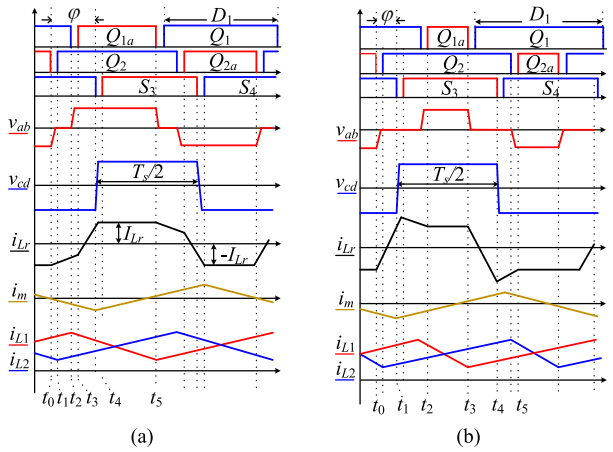

Fig. 2. Working waveforms of the converter in the forward under balanced load. (a) Mode I. (b) Mode II.

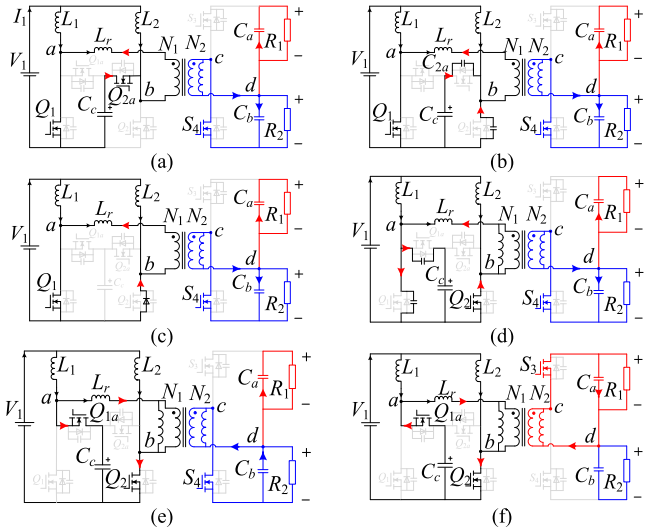

Fig. 3. Operation modes in the boost mode I. (a) Before t_0. (b) t_0-t_1. (c) t_1-t_2. (d) t_2-t_3. (e) t_3-t_4. (f) t_4-t_5.

coupled inductor, which can be considered as a combination of leakage inductance L_r, magnetizing inductance L_m, and ideal transformer. On the primary side of the converter, an interleaved double boost structure is formed by two dc boost inductors L_1/L_2 and switches Q_1/Q_2/Q_{1a}/Q_{2a}, and clamping capacitor C_c is added. On the secondary side, S_3, S_4, C_a, and C_b form a half-bridge circuit with bipolar output capability, and combined with the magnetizing inductance L_m, it is equivalent to a conventional buck–boost voltage balancer, which can automatically balance pole voltage regardless of load conditions.

B. Modulation Scheme and Basic Operation Principles

The operating waveforms of the proposed converter in the boost mode (energy flows from the low-voltage side to the high-voltage side) under the balanced load are shown in Fig. 2. v_{ab} and v_{cd} are the primary and secondary side voltages of the coupled inductor of the proposed converter in Fig. 1(a), respectively. The signals of switches Q_1, Q_2, and S_3 are complementary to the signals of Q_{1a}, Q_{2a}, and S_4, respectively, and the interval time between the rising edges of the driving signals of switches Q_1 and Q_2 differs by half a switching cycle. The power flow can be controlled by regulating the phase shift angle φ between the primary and secondary sides of the converter, and the duty cycle D_1 of the primary side switch Q_1 is adjusted to achieve voltage amplitude matching when the input voltage changes. As shown in Fig. 2, the current ripples of the two dc inductors can partially offset each other, and therefore, the current ripples embodied in the ports are small.

Taking boost mode I under balanced loads as an example, due to the symmetry of the topology and working process, only half of the switching cycle is analyzed next, and the circuit operating modes at different times are shown in Fig. 3.

Stage 1 *(Before t_0):* Q_1, Q_{2a}, and S_4 conduct. The converter is in the power transfer stage (power flows from the low-voltage side to the high-voltage side) and $i_{Lr} = -I_{Lr}(0)$.

Stage 2 *(t_0-t_1):* Q_{2a} is turned OFF at t_0. L_r, C_2, and C_{2a} begin to resonate.

Stage 3 *(t_1-t_2):* D_2 conduct at t_1. The voltage of C_{2a} is clamped at V_{Cc}. Q_2 can be turned ON under zero voltage. During this stage, the current of the leakage inductance can be expressed as

$$i_{Lr} = -I(0) + \frac{N_1 V_o}{2N_2 L_r} \cdot t. \tag{1}$$

Stage 4 *(t_2-t_3):* Q_1 is turned OFF at t_2. L_r, C_1, and C_{1a} begin to resonate.

Stage 5 *(t_3-t_4):* At t_3, Q_{1a} is turned ON under zero voltage. During this stage, the leakage inductance current rises to a positive value

$$i_{Lr} = -I(0) + \frac{N_1 V_o (2D_1 - 1)\pi}{2N_2 \omega L_r} + \frac{N_1 V_o [2t - (2D_1 - 1)T_s]}{2N_2 L_r}. \tag{2}$$

Stage 6 *(t_4-t_5):* S_3 conducts at t_4, and S_3 can achieve ZVS. Similar to Stage 1, the converter is in the power transfer stage, and $i_{Lr} = I_{Lr}(0)$.

Under the balanced power, the magnetizing current has no dc offset, and the circuit working modes are like those of conventional CF-DAB converters under pulse-width plus phase shift (PPS) control. However, under the unbalanced power, the working principle of the secondary side of the converter is somewhat different from that of the conventional CF-DAB converter, which will be described in detail in the following section.

III. Bipolar Voltage Balance Principle Under Unbalanced Load

A. Ideal Bipolar Voltage Balance

Usually, when analyzing the operation principle of bipolar output converters under unbalanced loads, the parasitic parameters of the switches are ignored, i.e., the ideal case. When the unbalanced loads are connected to the bipolar ports, the bipolar

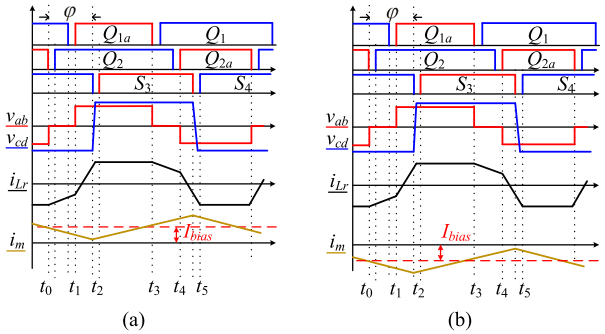

Fig. 4. Steady-state waveforms of the converter under unbalanced load. (a) $P_{\text{out1}}<P_{\text{out2}}$. (b) $P_{\text{out1}}>P_{\text{out2}}$.

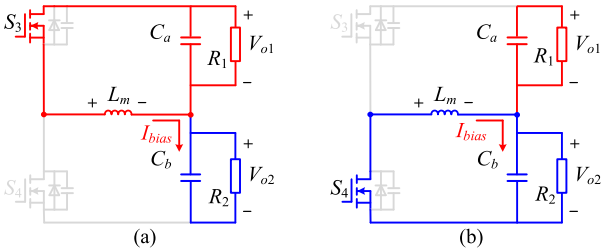

Fig. 5. Equivalent circuits on the secondary side for voltage balance ($P_{\text{out1}}<P_{\text{out2}}$). (a) When S_3 is ON. (b) When S_4 is ON.

ports of the proposed converter can automatically maintain a balanced voltage between the two dc buses regardless of the load. Fig. 4 demonstrates the working waveforms of the proposed converter under two unbalanced load conditions.

As shown in Fig. 4, when the V_{o2} side needs more power, i.e., $P_{\text{out1}}<P_{\text{out2}}$, a positive dc bias current is generated on the magnetizing inductance, and vice versa for $P_{\text{out1}}>P_{\text{out2}}$, a negative dc bias value. The waveform of the leakage inductance current on the primary side will not be affected by the unbalanced loads. Fig. 5 shows the principle of voltage balancing achieved by the proposed converter under unbalanced loads with $P_{\text{out1}}<P_{\text{out2}}$ as an example. Since the load $R_1>R_2$ makes the bipolar voltage $V_{o1}>V_{o2}$ at the beginning, then the bipolar voltage difference generates a dc bias current on the magnetizing inductance to compensate for the power on the V_{o2} port, and the bipolar port can supply a symmetrical voltage.

Based on Figs. 4, 5, and the volt-second balance principle of the magnetizing inductance L_m, the following formula can be listed

$$\int_0^{T_s} v_{Lm}(t)dt = V_{o1}D_2T_s - V_{o2}(1-D_2)T_s = 0 \tag{3}$$

$$\frac{V_{o1}}{V_{o2}} = \frac{1-D_2}{D_2} \tag{4}$$

where D_2 is the duty cycle of the secondary side switch S_3. After simplifying (3), formula (4) can be obtained, and it can be known that as long as the secondary side switches conduct complementarily with a duty cycle D_2 of 0.5, bipolar voltage balance can automatically be achieved.

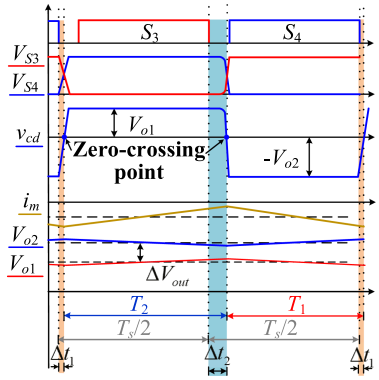

Fig. 6. Generation of pole voltage deviation ($P_{\text{out1}}>P_{\text{out2}}$).

B. Practical Bipolar Voltage Balance

However, as verified by the experimental section, the partial loss of ZVS under unbalanced loads leads to an imperfectly balanced bipolar voltage, which is closely related to the parasitic capacitance of switches. Therefore, an analysis of the voltage equalization case taking into account the parasitic capacitance and the dead time will follow. Taking the unbalanced loads $R_1<R_2$ as an example, the specific mechanism of voltage deviation generation is shown in Fig. 6.

Considering the actual waveform of the high-frequency voltage v_{cd} of the transformer secondary winding, the volt-second product of the magnetizing inductance should be re-expressed as

$$\int_0^{T_s} v_{Lm}(t)dt = V_{o1}\cdot T_2 - V_{o2}T_1 = 0 \tag{5}$$

$$\frac{V_{o1}}{V_{o2}} = \frac{T_1}{T_2} = \frac{T_s/2-(\Delta t_2-\Delta t_1)}{T_s/2+\Delta t_2-\Delta t_1} \tag{6}$$

where Δt_1 and Δt_2 are the times for the voltage v_{cd} to rise and drop to 0, respectively, and are also times for the voltage of the junction capacitance of switches S_3 and S_4 to discharge to half of the total output voltage, respectively. It can be seen from (6) that V_{o1} and V_{o2} are no longer strictly equal under the unbalanced loads because the parasitic parameters make the charging and discharging times of the balancing inductor unequal, while the inductors need to satisfy the conservation principles of flux linkages.

As illustrated in Fig. 6, the unbalanced load ($P_{\text{out1}}>P_{\text{out2}}$) makes it easier for the switch voltage V_{s3} to discharge faster, and Δt_1 is very short. However, S_4 cannot achieve soft switching, and V_{s4} drops slowly before the turn-ON signal of S_4 comes, so Δt_2 is longer than Δt_1, almost equal to the secondary side dead time T_d. According to formula (6), when $P_{\text{out1}}>P_{\text{out2}}$, V_{o1} is less than V_{o2}. The degree of bipolar voltage deviation is represented by ε

$$\varepsilon = \frac{|V_o/2-V_{o1}|}{V_o/2} = \frac{2\,|\Delta t_2-\Delta t_1|}{T_s}\times 100\%. \tag{7}$$

To further illustrate the practical pole voltage deviation case, the following parameters are used as an example: $V_o = 400$ V,

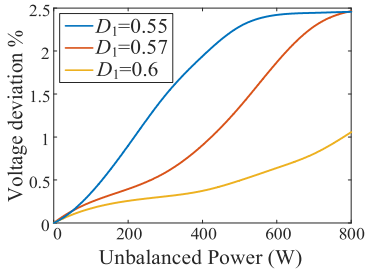

Fig. 7. Voltage deviation curves under unbalanced loads ($T_d = 150$ ns, $C_3 = C_4 = 176$ pF, $L_m = 800$ μH).

$T_s = 10$ μs, $C_3 = C_4 = 176$ pF, $T_d = 150$ ns, $L_m = 800$ μH, and Fig. 7 plots the pole voltage deviation curves under different unbalanced powers. The three lines from left to right in Fig. 7 represent the pole voltage deviations when the duty cycle D_1 is 0.55, 0.57, and 0.6, respectively. As seen in Fig. 7, the higher unbalanced power will result in a relatively large bipolar voltage deviation. Therefore, in the following section, the effect of unbalanced power on the converter performance is discussed in detail, taking into account the junction capacitance of switches, and the impact of the magnetizing inductance is analyzed to improve the performance.

IV. ZVS Performance of Converter Under Unbalanced Load

As mentioned above, unbalanced power reduces the voltage-sharing performance of the converter, which is caused by an asymmetrical soft-switching range of the secondary side switches. Furthermore, the ZVS performance of the converter has an important impact on turn-ON loss and EMI noise. Therefore, it is necessary to analyze the ZVS region in detail and investigate design methods to achieve a full load range ZVS.

A. ZVS Model Considering Parasitic Capacitance

For the ZVS range of the primary-side switches, the unbalanced load will not affect the current on the primary side and the ZVS range of the primary-side switches due to the isolation function of the converter. The soft switching of the primary-side switches can be easily realized with the proper design of the dc inductances. Therefore, this section will focus on the ZVS analysis of the secondary-side switches of the converter under unbalanced loads and consider the junction capacitance, dead-time effect, and magnetizing inductance to obtain a more accurate ZVS range.

Taking the converter operating in boost mode I and unbalanced power condition ($P_{\text{out1}} > P_{\text{out2}}$) as an example to analyze the ZVS range of the secondary-side switches and the steady-state waveforms of the bipolar CF-DAB converter with different magnetizing inductances are illustrated in Fig. 8.

For the convenience of analyzing the ZVS situations of the secondary side switches considering the junction capacitance, Fig. 9 plots the resonant equivalent circuits before the turn-ON signal of switches S_3 and S_4 comes.

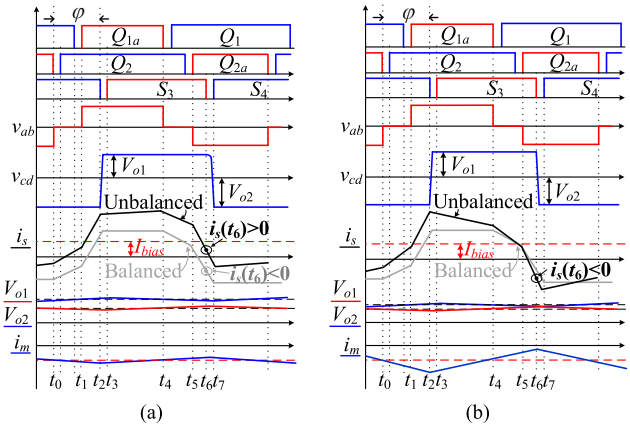

Fig. 8. Steady-state waveforms of the converter with different magnetizing inductances L_m under unbalanced loads ($P_{\text{out1}} > P_{\text{out2}}$). (a) $L_m = 800$ μH. (b) $L_m = 300$ μH.

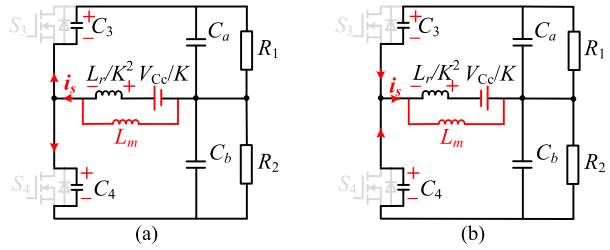

Fig. 9. Resonant equivalent circuits on the secondary side. (a) t_2-t_3. (b) t_6-t_7.

Taking Fig. 9(a) as an example, the dynamic equations can be expressed

$$\begin{cases} \frac{L_r}{K^2}\frac{dKi_{Lr}(t)}{dt} - \frac{V_{Cc}}{K} = u_{C3}(t) - V_{o1} \\ i_s(t) = Ki_{Lr}(t) - i_m(t) = -2C_3\frac{du_{C3}(t)}{dt} \end{cases} \tag{8}$$

where V_{Cc} is the clamping voltage, K is the turn ratio, L_r is the primary-side leakage inductance, $u_{C3}(t)$ is the voltage of junction capacitor C_3, $i_{Lr}(t)$ is the primary-side leakage inductance current, $i_s(t)$ is the secondary-side current, and $i_m(t)$ is the magnetizing current.

After the Laplace transform and simplification of formula (8), the voltage equation for parasitic capacitor C_3 follows:

$$u_{C3}(t) = \left(\frac{V_{Cc}}{K} + V_{o2}\right)\cos\omega_3 t - \sqrt{\frac{L_r}{2C_3}}I_s \sin\omega_3 t - \frac{V_{Cc}}{K} + V_{o1} \tag{9}$$

where $\omega_3 = K/(2L_rC_3)^{1/2}$, and I_s is the secondary side current at t_2.

The voltage on the parasitic capacitor C_3 should be discharged to 0 within the dead time (t_2-t_3) to realize soft switching, so the ZVS condition is

$$i_s(t_2) = KI_{Lr\_t0} + I_{\text{bias}} + \frac{V_oT_s}{8L_m} + \frac{(V_{Cc} + KV_{o2})\varphi - V_{Cc}(2D_1 - 1)\pi}{2\pi L_r/K} \cdot T_s > 0 \tag{10}$$

$$\arccos \frac{V_{Cc}/K - V_{o1}}{\sqrt{\left(V_{Cc}/K + V_{o1}\right)^2 + L_r I_s^2/\left(2C_3\right)}} - \arcsin \frac{\sqrt{V_{Cc}/K}\cdot I_s}{\sqrt{\left(V_{Cc}/K + V_{o1}\right)^2 + L_r I_s^2/\left(2C_3\right)}} \le \omega_3 T_d \tag{11}$$

where I_{Lr_t0} is the primary-side leakage inductance current at t_0, I_{bias} is the dc bias current, and T_d is the dead time of switches. (10) is a necessary and insufficient condition for the achievement of ZVS, and ZVS can be preliminarily judged by the direction of the switching current in (10), but a sufficient switching current is also required to make the junction capacitance discharge time less than the dead time, i.e., formula (11) should be satisfied.

Similarly, the condition that the switch S_4 needs to meet to realize ZVS can also be obtained.

B. ZVS Range With Different Magnetizing Inductances

From Fig. 8(a) and formulas (10), when $P_{\text{out1}}>P_{\text{out2}}$, switch S_3 is easier to achieve ZVS than under the balanced load conditions, while it is more difficult for switch S_4 to realize ZVS because dc bias current at this unbalanced case is greater than 0. If $P_{\text{out1}}<P_{\text{out2}}$, the ZVS situations are opposite. Therefore, taking $P_{\text{out1}}>P_{\text{out2}}$ as an example, i.e., V_{o2} side with no-load and V_{o1} side with a load. The ZVS ranges of the secondary-side switch regarding unbalanced power for different magnetizing inductances are demonstrated in Fig. 10(a) and (c). Fig. 10(b) and (d) illustrates the ZVS range of switch S_3/S_4 with different magnetizing inductances under the balanced load, where P^* is the normalized value of the total transmission power.

As seen in Fig. 10(b), the ZVS boundaries of the two switches ON the secondary side are the same under balanced loads, and the converter has difficulty in achieving ZVS under light load when D_1 is close to 0.5. By comparing Fig. 10(a) and (b), it is obvious that the ZVS ranges of switches S_3 and S_4 become different due to the bipolar unbalanced load. Although the ZVS range of S_3 is extended, the ZVS range of S_4 is greatly reduced, and even zero-voltage conduction cannot be achieved under any unbalanced load when $D_1<0.53$. Therefore, the ZVS performance of the bipolar converter with an unsuitable magnetizing inductance will degrade at unbalanced loads.

However, by comparing Fig. 10(a) and (c), as well as Fig. 10(b) and (d), respectively, it can be seen that the introduction of a suitable magnetizing inductance can effectively extend the ZVS range of switches S_3 and S_4, regardless of whether the load is balanced or not, and enhance the ZVS performance of the bipolar converter under light load. It can also be known from the waveform analysis in Fig. 8 that the introduction of a smaller magnetizing inductance can make the switching current less than 0 when the switch S_3 is turned OFF, i.e., $i_s(t_6)<0$, while the switching current $i_s(t_6)$ of the converter with an 800 μH magnetizing inductance is greater than 0, and switching current less than 0 is beneficial for the ZVS implementation of S_4. Similarly, when $P_{\text{out1}}<P_{\text{out2}}$, the ZVS ranges for different magnetizing inductances are shown in Fig. 10(e) and (f), and the ZVS situations are exactly opposite to Fig. 10(a) and (c)($P_{\text{out1}}>P_{\text{out2}}$).

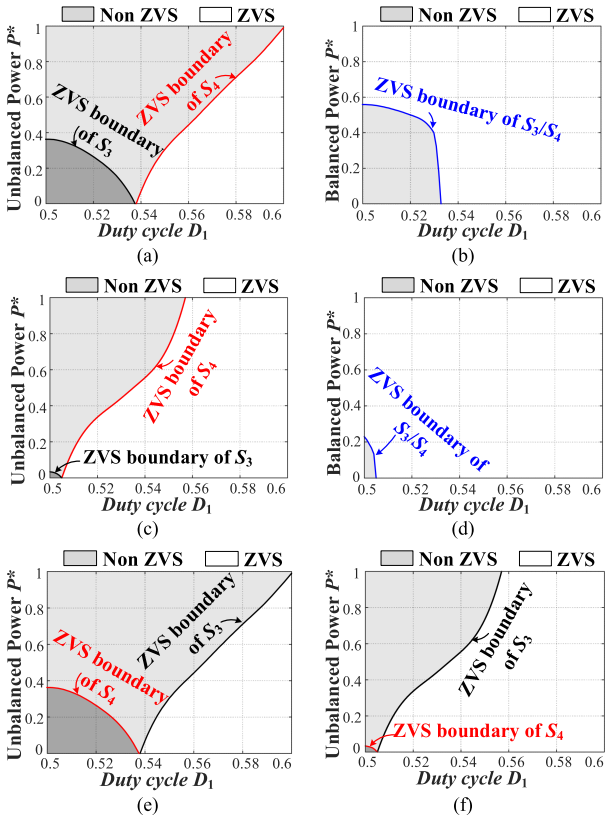

Fig. 10. ZVS region of the secondary-side switches with different magnetizing inductances. (T_d = 150 ns, C_3 = 176 pF) (a) L_m = 800 μH, $P_{\text{out1}}>P_{\text{out2}}$. (b) L_m = 800 μH, $P_{\text{out1}}=P_{\text{out2}}$. (c) L_m = 300 μH, $P_{\text{out1}}>P_{\text{out2}}$. (d) L_m = 300 μH, $P_{\text{out1}}=P_{\text{out2}}$. (e) L_m = 800 μH, $P_{\text{out1}}<P_{\text{out2}}$. (f) L_m = 300 μH, $P_{\text{out1}}<P_{\text{out2}}$.

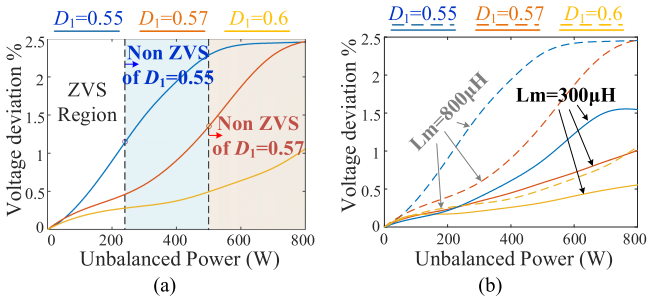

Fig. 11. Voltage deviation curves under unbalanced loads (T_d = 150 ns, C_3 = C_4 = 176 pF). (a) L_m = 800 μH with the non ZVS region. (b) Comparison between L_m = 800 μH and L_m = 300 μH.

C. Effect of ZVS on Voltage Equalization Performance

In addition, the problem of asymmetric realization of ZVS for different switches on the secondary side of the transformer can be improved due to a proper design of the magnetizing inductance so that the bipolar voltage steady-state error can be reduced in part. Taking the dead time T_d = 150 ns and junction capacitance $C_3 = C_4$ = 176 pF for example, Fig. 11(a)

demonstrates the voltage deviation curves of the converter with an 800 μH magnetizing inductance under different unbalanced powers, the curve gradually shifts downward as the duty cycle of the primary side switches increases, and the voltage deviation is high in the non-ZVS region. Fig. 11(b) compares the pole voltage deviation of the converter with different magnetizing inductances at different unbalanced loads, which are represented by dotted and solid lines. The pole voltage deviation of the converter with a 300 μH magnetizing inductance is always lower than that of the converter with an 800 μH magnetizing inductance at the same duty cycle.

Therefore, a suitable design of the magnetizing inductance not only can realize the full range ZVS of the converter under any load condition but also relieves the problem of bipolar voltage deviation under unbalanced loads. The specific design method will be explained in Section V with the parameters of the prototype.

V. Design Considerations

The proposed converter is taken as an example with the following basic parameters: switching frequency $f_s = 100$ kHz, input voltage $V_1 = 32$–53 V, output voltage $V_o = 400$ V, and rated power $P_N = 750$ W.

A. Turn Ratio

To reduce the circulating loss, the proposed converter adjusts the duty cycle D_1 to realize voltage amplitude matching on two sides of the converter, and the transformer ratio K should satisfy

$$K = \frac{2V_1}{(1-D_1)V_o}. \tag{12}$$

With the premise of duty cycle $D_1 \geq 0.5$ (to facilitate ZVS implementation), the turn ratio K is finally set to be 1:1.86.

B. Leakage Inductance

Leakage inductor L_r plays the role of energy transfer in the converter, so L_r should be taken to ensure the maximum power transmission of the bipolar converter, and can be expressed as

$$L_r < \frac{\pi K^2 V_o^2 \left(-8D_1^2 + 8D_1 - 1\right)}{16\omega P_N}. \tag{13}$$

where $\omega = 2\pi f_s$, $\varphi = 0.5\pi$, $D_1 = 0.72$. Considering the high rms value of leakage inductance current because of too small leakage inductance and according to (13), a leakage inductance of 7.5 μH is chosen.

C. Magnetizing Inductance

To achieve the full range ZVS, the most difficult ZVS realization situation is considered to design the magnetizing inductance. From the above analysis, it is clear that the unbalanced load will reduce the ZVS range, especially when one port is unloaded and one port is loaded. However, one port unloaded and one port fully loaded is not the most difficult situation to realize ZVS. Take the ZVS analysis of switch S_4 under $P_{\text{out1}} > P_{\text{out2}}$ as an example, as it is more challenging to achieve soft switching

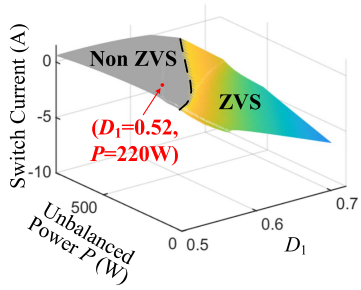

Fig. 12. Switching currents under different duty cycles and unbalanced power ($C_3 = C_4 = 176$ pF, $T_d = 160$ ns).

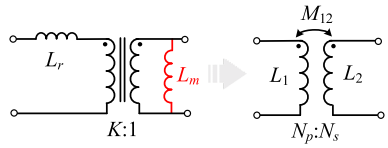

Fig. 13. Coupled inductor equivalent model.

of S_4 in that case. Although the dc bias current increases the switching current when switch S_3 is turned OFF under full load, the negative value of its secondary side current is also large, so the switching current flowing through S_4 is not necessarily the maximum. Therefore, Fig. 12 plots the switching currents of switch S_4 for different duty cycles and unbalanced power.

According to Fig. 12, ZVS is most difficult to achieve when the duty cycle D_1 is 0.52 and the unbalanced power is 220 W. Therefore, the ZVS condition to be satisfied by the introduced magnetizing inductance is shown below

$$KI_{Lr} + I_{\text{bias}} - \left(\frac{V_o T_s}{8L_m} - \frac{V_o T_d}{2L_m}\right) < 0 \tag{14}$$

where I_{Lr} is the leakage inductance current when S_3 is turned OFF. Based on formula (14) and keeping a certain margin, it is advisable to design a larger magnetizing inductance due to a low circulating current while meeting the ZVS requirement. Finally, a 260 μH magnetizing inductance is designed.

D. Coupled Inductor Design

Conventional CF-DAB converters usually add an external leakage inductor in series with the transformer. Meanwhile, conventional voltage balancers also require dc inductors, which increases the number of magnetic components. Therefore, the proposed bipolar CF-DAB converter integrates the leakage inductor, transformer, and magnetizing inductor into a coupled inductor, making the structure more compact. The winding structure is different from conventional transformers. The equivalent model of the coupled inductor and its circuit model can be seen in Fig. 13, where L_1, L_2, and M_{12} are the primary-side self-inductance, the secondary-side self-inductance, and the mutual inductance of the coupled inductor, respectively. Based on

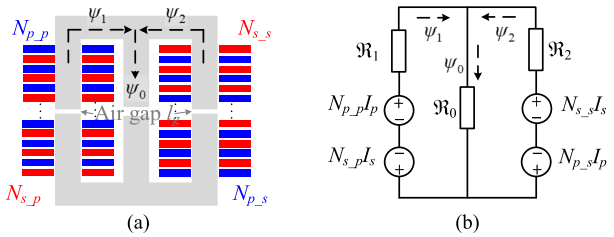

Fig. 14. Coupled inductor. (a) Winding structure. (b) Reluctance model.

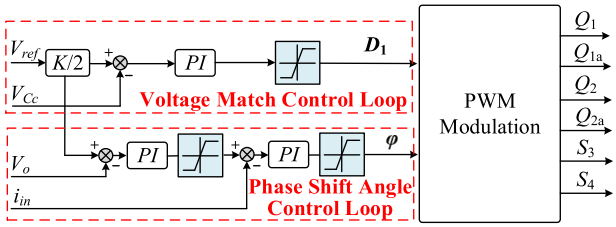

Fig. 15. Control scheme for the proposed bipolar CF-DAB converter.

TABLE I
SPECIFIC PARAMETER OF THE COUPLED INDUCTOR

Parameters	Design
Core model	EE42/20
Magnetic flux density change	ΔB=180 mT
Air gap of out legs	0.477 mm
Air gap of center legs	0.816 mm
Turn ratio N_p:N_s	22:41
N_{p_p}:N_{p_s}	17:5
N_{s_s}:N_{s_p}	20:21

Fig. 13, the expressions of L_1, L_2, and M_{12} are derived from

$$\begin{cases} L_1 = L_r + K^2 L_m \\ L_2 = L_m \\ M_{12} = K \cdot L_m \end{cases} . \tag{15}$$

Substitute $L_r = 7.5\ \mu$H, $L_m = 260\ \mu$H, $K = 1/1.86$ into (15) to get $L_1 = 82.65\ \mu$H, $L_2 = 260\ \mu$H, $M_{12} = -139.78\ \mu$H, and then the coupling coefficient $k = M_{12}/(L_1L_2)^{1/2} = 0.95$ for the coupled inductor is obtained. Because of the relatively high coupling coefficient k, the proposed converter uses winding interleaving of the primary and secondary side windings, which enhances coupling to reduce inductance losses compared to the conventional non-interleaved winding [28]. The winding structure of the coupled inductor can be seen in Fig. 14(a), and the corresponding reluctance model in Fig. 14(b) can be deducted from Fig. 14(a), where $\Re_0$, $\Re_1$, $\Re_2$ are the reluctance on the three magnetic circuits and are mainly affected by the air gap, N_{p_p} is the number of turns to be wound on the primary side for the primary winding, and N_{s_p} is the number of turns to be wound on the primary side for the secondary winding. In the same way, the definitions of N_{s_s} and N_{p_s} can be obtained, and $N_{p\_p} + N_{p\_s} = N_p$, $N_{s\_s} + N_{s\_p} = N_s$.

Based on Fig. 14(b) and using the superposition theorem, the relationship between each reluctance and self-inductance L_1, L_2, mutual inductance M_{12}, and $N_{p\_p}/N_{p\_s}/N_{s\_s}/N_{s\_p}$ can be obtained to calculate the required air gap length [28]. Finally, the specific design parameters of the coupled inductor can be found in Table I. In addition, the magnetic flux density under extremely unbalanced load conditions will not exceed the saturation magnetic flux density, with a certain margin.

E. Control Scheme

Fig. 15 illustrates the control strategy diagram of the proposed converter, which mainly adopts decoupled primary-side duty cycle closed-loop and phase shift angle closed-loop control to achieve voltage matching control and power control, respectively. In the phase shift angle closed-loop control, the bandwidth of the current loop should be higher than that of the voltage loop as much as possible to ensure the fast response of the inner loop. Although the duty ratio D_2 of the secondary-side switch can also be fine-tuned to further reduce the bipolar voltage deviation (For example, when V_{o1} is lower than V_{o2}, D_2 of S_3 and S_4 is controlled to be smaller than 50%), the proposed converter still uses PPS control to simplify the control, which is enough to keep the bipolar voltage deviation within 1.5%.

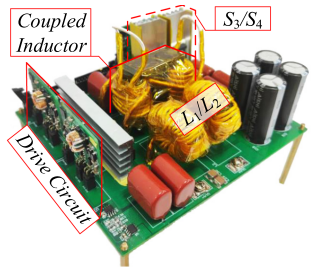

Fig. 16. Laboratory prototype of the proposed bipolar CF-DAB converter.

TABLE II
SPECIFICATIONS OF THE LABORATORY PROTOTYPE

Parameters	Value
Input voltage (V_1)	32–53 V
Output voltage (V_o)	400 V (2×200 V)
Nominal power (P_N)	750 W
Switching frequency (f_s)	100 kHz
Turn ratio (K)	1:1.86
Equivalent leakage inductance (L_r)	7.5 μH
Dc inductance (L_1/L_2)	25 μH

VI. EXPERIMENTAL RESULTS AND DISCUSSIONS

As shown in Fig. 16, a 750 W prototype was built to validate the feasibility of the proposed bipolar converter, where the corresponding experimental parameters can be seen in Table II. The experimental parameters can be modified according to the specific application in accordance with the design recommendations in Section V.

Fig. 17 shows the steady-state operating waveforms of the proposed bipolar CF-DAB converter under different loads, where Fig. 17(a) and (b) represents the steady-state waveforms under light and medium loads, respectively, when the balanced power condition is met. Fig. 17(c) and (d) illustrates the operating

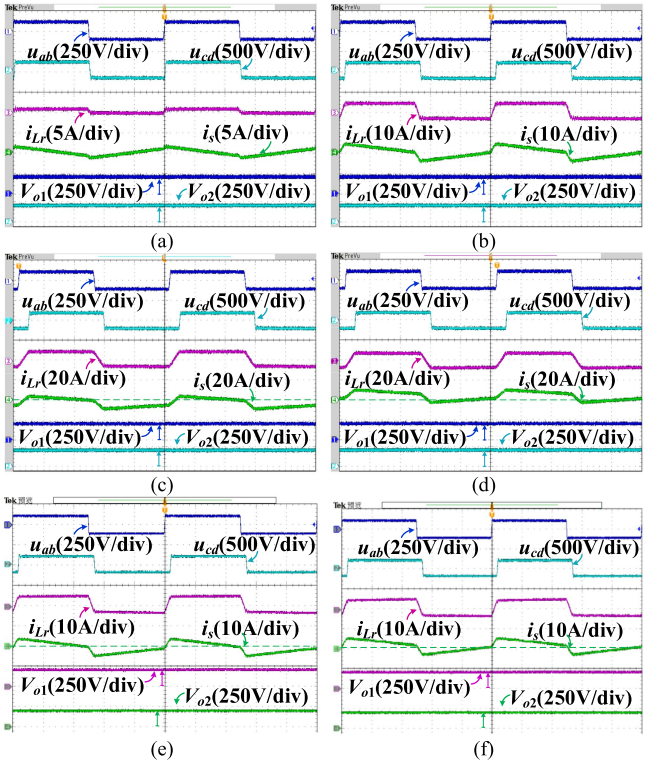

Fig. 17. Steady-state operating waveforms under different loads ($V_1 = 53$ V). (a) $P_{\text{out}1} = P_{\text{out}2} = 25$ W. (b) $P_{\text{out}1} = P_{\text{out}2} = 187.5$ W. (c) $P_{\text{out}1} = 0$ W, $P_{\text{out}2} = 750$ W. (d) $P_{\text{out}1} = 750$ W, $P_{\text{out}2} = 0$ W. (e) $P_{\text{out}1} = 100$ W, $P_{\text{out}2} = 300$ W. (f) $P_{\text{out}1} = 300$ W, $P_{\text{out}2} = 100$ W.

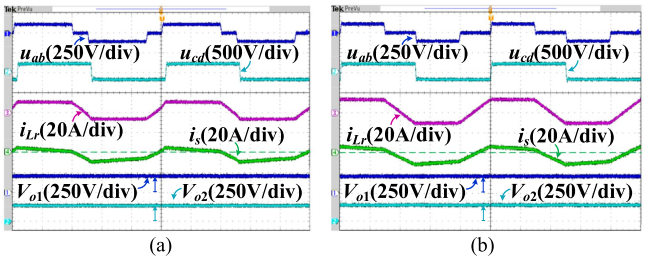

Fig. 18. Steady-state operating waveforms under different input voltages ($P_{\text{out}1} = 0$ W, $P_{\text{out}2} = 750$ W). (a) $V_1 = 43$ V. (b) $V_1 = 32$ V.

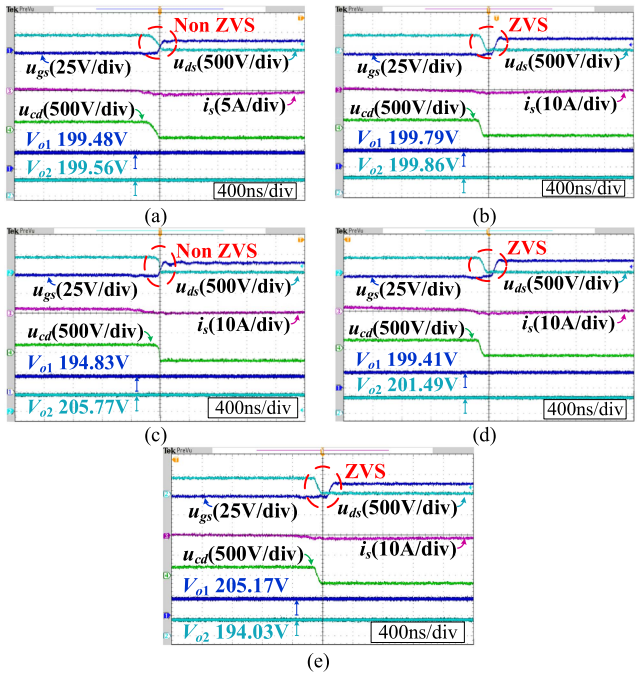

Fig. 19. Experimental ZVS waveforms of switch S_4 with different magnetizing inductances ($V_1 = 53$ V). (a) $L_m = 678$ μH ($P_{\text{out}1} = P_{\text{out}2} = 0$ W). (b) $L_m = 260$ μH ($P_{\text{out}1} = P_{\text{out}2} = 0$ W). (c) $L_m = 678$ μH ($P_{\text{out}1} = 200$ W, $P_{\text{out}2} = 0$ W). (d) $L_m = 260$ μH ($P_{\text{out}1} = 200$ W, $P_{\text{out}2} = 0$ W). (e) $L_m = 678$ μH ($P_{\text{out}1} = 0$ W, $P_{\text{out}2} = 200$ W).

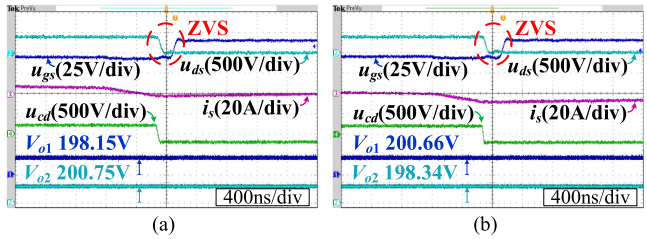

Fig. 20. Experimental ZVS waveforms of switch S_4 of the proposed converter ($V_1 = 53$ V). (a) $P_{\text{out}1} = 750$ W, $P_{\text{out}2} = 0$ W. (b) $P_{\text{out}1} = 0$ W, $P_{\text{out}2} = 750$ W.

waveforms under extremely unbalanced power conditions, i.e., $P_{\text{out}1} = 0, P_{\text{out}2} = P_N$, and $P_{\text{out}1} = P_N, P_{\text{out}2} = 0$, respectively. Fig. 17(e) and (f) illustrates the operating waveforms under unbalanced power conditions with $P_{\text{out}1}$ and $P_{\text{out}2}$ more than zero, i.e., $P_{\text{out}1} = 100$ W, $P_{\text{out}2} = 300$ W, and $P_{\text{out}1} = 300$ W, $P_{\text{out}2} = 100$ W, respectively. As shown in Fig. 17, the port voltage V_{o1} is stable at around 200 V regardless of the load condition. Similarly, bipolar voltage balancing for different input voltages can still be achieved, taking the unbalanced power $P_{\text{out}1} < P_{\text{out}2}$ as an example, as shown in Fig. 18.

Compared with the conventional converter with a narrow ZVS range under the unbalanced load, the proposed converter utilizes the magnetizing current to assist in achieving the full range ZVS. To verify the impact of different magnetizing inductances on the ZVS performance of the converter, Fig. 19 compares the ZVS waveforms with different magnetizing inductances under unloaded and unbalanced loads, considering the most difficult input voltage situation for achieving ZVS on the secondary-side switches ($V_1 = 53$ V, $D_1 = 0.5$). As shown in Fig. 19(a) and (c), the conventional converter with a large magnetizing inductance has difficulty achieving ZVS at both no-load and unbalanced load conditions. Furthermore, the conventional converter has a bipolar voltage deviation of 2.9% under unbalanced loads, which is much higher than the proposed method under the same load conditions with a voltage deviation of only 0.7%. Combined with the observation of Fig. 19(c) and (e), when $P_{\text{out}1} > P_{\text{out}2}$, a positive dc bias value is generated on the magnetizing current, making it more difficult for switch S_4 to achieve ZVS; conversely, when $P_{\text{out}1} < P_{\text{out}2}$, S_4 can conduct at zero voltage, implying an asymmetrical ZVS range for the secondary side switches at unbalanced loads.

TABLE III
COMPARISON WITH SIMILAR BIPOLAR CONVERTER

		[8]	[21]	[20]	[27]	[18]	[19]	Proposed
Topology type		CF-DAB	CF-DAB	CF-DAB	VF-DAB	VF-DAB	VF-DAB	CF-DAB
Number of components	MOSFET	8	6	6	8	6	6	6
	Diode	0	2	4	0	2	4	0
	Capacitor	3	4	4	3	5	4	3
	Magnetic components	1T+3L	1T+4L	1T+2L	1T+1L	1T+1L	1T+1L	1T+2L
Modulation scheme		PSM	PSM	PSM	PSM	PSM	PSM	PPS
Voltage gain		n	$\frac{n}{1-D}$	$\frac{n}{1-D}$	n	$2G_{VF\text{-}DAB}$	$2G_{VF\text{-}DAB}$	$\frac{2n}{1-D}$
Input voltage range		380 V	40 V	40 V	380 V	80-120 V	90-120 V	32-53 V
Output voltage		2×190 V	2×60 V	2×60 V	2×190 V	2×190 V	2×120 V	2×200 V
Soft switching		ZVS	ZVS+ ZCS	ZVS+ ZCS	ZVS	Wide range ZVS	Wide range ZVS+ZCS	Full range ZVS
Peak efficiency		96.7%	96.4%	95.6%	97.7%	97.9%	97.9%	97%

*Magnetic components includes the transformer (T) and inductors (L); $G_{VF\text{-}DAB}$ is the voltage gain of traditional VF-DAB converters; $n = 1/K = N_2{:}N_1$.

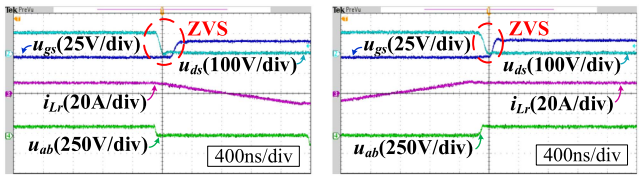

Fig. 21. Experimental ZVS waveforms of the primary-side switches of the proposed converter ($V_1 = 32$ V, $P_{\text{out1}} = 750$ W, $P_{\text{out2}} = 0$ W). (a) Q_1. (b) Q_{1a}.

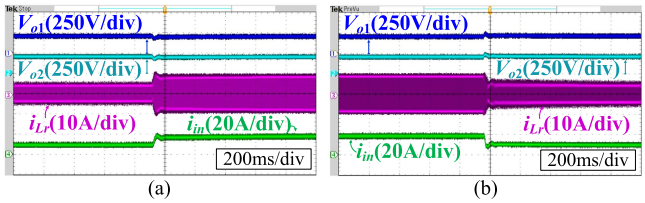

Fig. 22. Experimental transient waveforms of load variation at P_{out1} when P_{out2} is full-load. (a) P_{out1} from 0 W to 375 W. (b) P_{out1} from 375 W to 0 W.

Except for Fig. 19(b) and (d), Fig. 20 also provides the ZVS waveforms of switch S_4 of the proposed bipolar converter under two extremely unbalanced load conditions, i.e., no load at one port and full load at the other. In addition, Fig. 21 illustrates the ZVS waveforms of the primary-side switches of the proposed converter under an input voltage of 32 V and an unbalanced power of 750 W, as this operating condition is more difficult to realize ZVS compared to other operating conditions. Following Figs. 20 and 21, the proposed converter switches can realize ZVS under extreme loads, and the degree of bipolar voltage deviation does not exceed 1.5% at extreme load unbalance.

Fig. 22 illustrates the experimental transient waveforms of the proposed converter when P_{out2} is fixed at full load and P_{out1} undergoes load variation, where P_{out1} in Fig. 22(a) steps from 0 to 375 W, and P_{out1} in Fig. 22(b) switches from 375 to 0 W. It can be seen from Fig. 22 that voltages of bipolar ports can remain stable at 200 V and the leakage inductance current can be changed smoothly. The transition waveforms between unbalanced and balanced load conditions show that the proposed converter can effectively achieve automatic bipolar voltage balance.

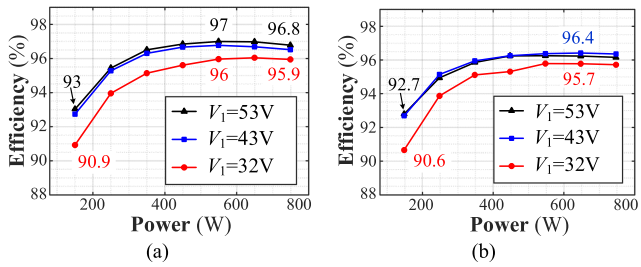

Fig. 23. Efficiency of the proposed bipolar CF-DAB converter at different input voltages. (a) Under balanced loads. (b) Under unbalanced loads.

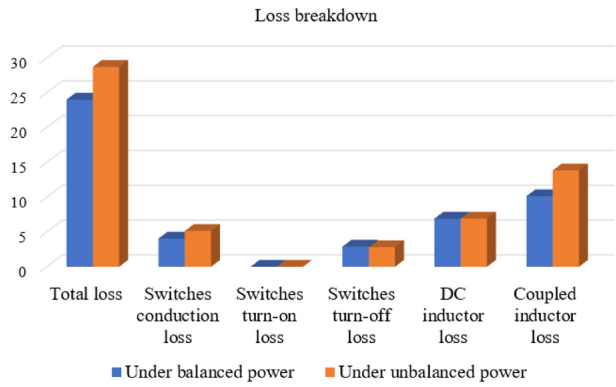

Fig. 24. Loss breakdown comparisons between balanced power and unbalanced power. ($V_1 = 53$ V, $P_N = 750$ W).

Fig. 23(a) and (b) illustrates the efficiency curves of the proposed bipolar CF-DAB converter under balanced power and unbalanced power, respectively, where three curves in each figure represent different input voltages. Under balanced power, the highest efficiency of the converter can be up to 97%, but the efficiency of the converter is slightly lower under unbalanced power than under balanced power conditions. Fig. 24 shows the converter loss breakdown for balanced and unbalanced loads with the same input voltage and total operating power, which

reveals that the increased loss under unbalanced load mainly comes from the switch conduction loss and coupled inductance loss. Because under the unbalanced load condition, in order to achieve bipolar voltage automatic balance, the secondary side of the converter generates a dc bias current to compensate for the unbalanced voltage, which leads to changes in the secondary side currents and an increase in loss. However, even if the efficiency of extreme unbalanced loads is compared with the efficiency of balanced loads, the efficiency difference does not exceed 1% under the same input voltage and total operating power.

Furthermore, Table III compares the performance of the proposed converter with similar bipolar converters. It can be seen that the proposed converter has fewer component counts and a wider input voltage range. It can provide higher voltage gain due to the CF-DAB-based topology structure. Compared with similar CF-DAB-based converters [8], [20], [21], the proposed converter has a relatively higher efficiency. The efficiency of the proposed converter is slightly lower than that of the VF-DAB-based converters [18], [19], [27] because the proposed converter is often used in low-voltage high-current applications. Lee et al. [8], and Tian et al. [20], [21] can achieve ZVS at a fixed voltage gain, but it will be difficult to achieve ZVS if the input voltage is varied or when under extremely unbalanced load conditions. The proposed converter can achieve soft switching under any operating conditions.

VII. Conclusion

In this article, a bipolar current-fed dual-active-bridge converter with automatic voltage balancing is presented. The proposed converter has only two switches at the bipolar ports, eliminating the need for cascading extra voltage balancers and utilizing a coupled inductor to make the structure more compact. Then, it is revealed that unbalanced power in practical operation makes ZVS lost, leading to high voltage deviation problems. To increase the converter efficiency and to improve the bipolar voltage equalization performance, this article proposes to integrate the magnetizing inductor into a conventional structure. Its design is analyzed in detail so that the converter can accomplish full-range ZVS, thus providing the benefits of low losses, low EMI noise, and low voltage deviation. Because of the PPS control and primary-side interleaved double boost structure, the converter has a wide voltage range and low current ripple, which is suitable for the connection to the bipolar dc system and energy storage system. Finally, the effectiveness and advantages of the proposed converter are verified by a 750 W prototype.

References

[1] P. A. Madduri, J. Poon, J. Rosa, M. Podolsky, E. A. Brewer, and S. R. Sanders, "Scalable DC microgrids for rural electrification in emerging regions," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1195–1205, Dec. 2016.

[2] C. Zhang, D. Jiang, H. Zheng, and L. Ye, "A Bi-directional buck/boost voltage balancer for DC distribution system," in *Proc. 4th Int. Conf. Digit. Manuf. Automat.*, 2013, pp. 9–13.

[3] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids—Part II: A review of power architectures, applications, and standardization issues," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3528–3549, May 2016.

[4] H. Kakigano, Y. Miura, and T. Ise, "Low-voltage bipolar-type DC microgrid for super high quality distribution," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3066–3075, Dec. 2010.

[5] S. Rivera, R. Lizana F., S. Kouro, T. Dragičević, and B. Wu, "Bipolar DC power conversion: State-of-the-art and emerging technologies," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1192–1204, Apr. 2021.

[6] J. Ma, M. Zhu, Y. Li, and X. Cai, "Monopolar fault reconfiguration of bipolar half bridge converter for reliable load supply in DC distribution system," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 11305–11318, Sep. 2022.

[7] S. Kim, H. Cha, and H.-G. Kim, "High-efficiency voltage balancer having DC–DC converter function for EV charging station," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 812–821, Feb. 2021.

[8] J.-Y. Lee, H.-S. Kim, and J.-H. Jung, "Enhanced dual-active-bridge DC–DC converter for balancing bipolar voltage level of DC distribution system," *IEEE Trans. Ind. Electron.*, vol. 67, no. 12, pp. 10399–10409, Dec. 2020.

[9] F. Wang, Z. Lei, X. Xu, and X. Shu, "Topology deduction and analysis of voltage balancers for DC microgrid," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 672–680, Jun. 2017.

[10] H. Kakigano, Y. Miura, T. Ise, and R. Uchida, "DC voltage control of the DC micro-grid for super high quality distribution," in *Proc. Power Convers. Conf.*, 2007, pp. 518–525.

[11] X. Zhang and C. Gong, "Dual-buck half-bridge voltage balancer," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3157–3164, Aug. 2013.

[12] X. Zhang, C. Gong, and Z. Yao, "Three-level DC converter for balancing DC 800-V voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3499–3507, Jul. 2015.

[13] B. Li et al., "DC/DC converter for bipolar LVdc system with integrated voltage balance capability," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5415–5424, May 2021.

[14] K. Kim and H. Cha, "Dual-active-half-bridge converter with output voltage balancing scheme for bipolar DC distribution system," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6850–6858, Jul. 2022.

[15] J.-Y. Lee and J.-H. Jung, "Modified three-port DAB converter employing voltage balancing capability for bipolar DC distribution system," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6710–6721, Jul. 2022.

[16] P. Prabhakaran and V. Agarwal, "Novel boost-SEPIC type interleaved DC–DC converter for mitigation of voltage imbalance in a low-voltage bipolar DC microgrid," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6494–6504, Aug. 2020.

[17] Q. Tian, G. Zhou, M. Leng, G. Xu, and X. Fan, "A nonisolated symmetric bipolar output four-port converter interfacing PV-battery system," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 11731–11744, Nov. 2020.

[18] Q. Tian, X. Zhang, G. Zhou, X. Wang, B. Guo, and H. Ma, "A family of symmetrical bipolar output converters based on voltage-multiplying rectifiers for interfacing renewable energy with bipolar DC microgrid," *IEEE Trans. Power Electron.*, vol. 38, no. 7, pp. 9157–9172, Jul. 2023.

[19] Q. Tian, X. Zhang, G. Zhou, H. Li, and H. Ma, "Improved dual active bridge DC–DC converter with symmetric bipolar output by utilizing a switched-capacitor circuit for bipolar DC distribution system," *IEEE Trans. Ind. Electron.*, vol. 71, no. 1, pp. 524–536, Jan. 2024.

[20] Q. Tian, G. Zhou, H. Li, Y. Yang, and D. Zhou, "Symmetrical bipolar output isolated four-port converters based on center-tapped winding for bipolar DC bus applications," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 2338–2351, Feb. 2022.

[21] Q. Tian, G. Zhou, L. Wang, Q. Bi, and M. Leng, "Symmetric bipolar output full-bridge four-port converter with phase-shift modulated buck–boost voltage balancer," *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 8040–8054, Aug. 2022.

[22] C. Verdugo, J. I. Candela, F. Blaabjerg, and P. Rodriguez, "Three-phase isolated multimodular converter in renewable energy distribution systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 854–865, Mar. 2020.

[23] V. F. Pires, A. Cordeiro, D. Foito, and J. F. A. Silva, "Dual output and high voltage gain DC-DC converter for PV and fuel cell generators connected to DC bipolar microgrids," *IEEE Access*, vol. 9, pp. 157124–157133, 2021.

[24] P. Gunawardena, D. Nayanasiri, N. Hou, and Y. Li, "A soft-switched current-fed dual-input isolated DC–DC converter topology," *IEEE Trans. Ind. Electron.*, vol. 70, no. 5, pp. 4842–4853, May 2023.

[25] S. Kurm and V. Agarwal, "Characterization of ZVS behavior and optimum control point determination for three-port current-fed dual active bridge converter," *IEEE Trans. Ind. Appl.*, vol. 58, no. 4, pp. 4816–4824, Jul./Aug. 2022.

[26] L. Li, G. Xu, W. Xiong, D. Liu, and M. Su, "An optimized DPS control for dual active bridge converters to secure full load range ZVS with low current stress," *IEEE Trans. Transp. Electrific.*, vol. 8, no. 1, pp. 1389–1400, Mar. 2022, doi: 10.1109/TTE.2021.3106130.
[27] M. Lee, D. Choi, J. Chae, S. Cheon, and G.-W. Moon, "Voltage-balancing dual-active-bridge (VB-DAB) converter for bipolar DC distribution system," *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2461–2471, Mar. 2023.
[28] M. Fu, C. Fei, Y. Yang, Q. Li, and F. C. Lee, "Optimal design of planar magnetic components for a two-stage GaN-based DC–DC converter," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3329–3338, Apr. 2019.

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