A Half-Bridge Gate Driver With Self-Adjusting and Tunable Dead-Time Modes for Efficient Switched-Mode Power Systems

Mostafa Amer, Ahmed Abuelnasr, Ahmad Hassan, *Member, IEEE*, Ahmed Ragab, Mohamad Sawan, *Fellow, IEEE*, and Yvon Savaria, *Fellow, IEEE*

***Abstract*—The design of high-voltage (HV) switched-mode power systems (SMPSys) poses multiple challenges, such as minimizing the switching losses and preventing possible shoot-through currents, to achieve efficient and reliable operation. This article introduces a reconfigurable half-bridge gate driver (GD) for SMPSys, with an open-drain output configuration, electrostatic discharge self-protection, and two dead-time management modes to address these challenges. The first mode is an externally tunable fixed dead-time generator (FDTG) capable of achieving a wide dead-time range from 5 to 200 ns. The second mode is a self-adjusting dead-time generator (SDTG), designed to adapt to delay mismatches between the GD's channels, regardless of process, voltage, and temperature (PVT) variations, while minimizing dead-time and preventing cross-conduction. The GD was fabricated in an HV 0.18-μm silicon-on-insulator CMOS process technology, supporting a high-side floating bias voltage rail up to 100 V and occupying a core area of 0.285 mm^2. It was tested in a buck converter system using a gallium nitride (GaN)-based half-bridge with a switching frequency of 0.5 to 1 MHz. It achieves a total propagation delay of 11.4 ns and a minimum dead-time of 3.6 ns (3$\times$ smaller than state-of-the-art) using its SDTG mode. The system achieved a peak efficiency of 90.5% at an output load of 8 W. Notably, the SDTG mode improves the overall efficiency by up to 20% over the FDTG mode, specifically at higher switching frequencies, showing its effectiveness in enhancing the performance of SMPSys.**

***Index Terms*—DC–DC converter, dead-time management, dual-channel gate driver (GD), open-drain output, process, voltage, and temperature (PVT) variations, shoot-through currents, switched-mode systems, synchronous switching.**

Manuscript received 5 July 2023; revised 28 October 2023; accepted 7 December 2023. Date of publication 12 December 2023; date of current version 16 February 2024. This work was supported in part by the Natural Sciences and Engineering Research Council of Canada (NSERC) and in part by the Mathematics of Information Technology and Complex Systems (MITACS). Recommended for publication by Associate Editor H. H.-C. Iu. *(Corresponding author: Mostafa Amer.)*

Mostafa Amer, Ahmed Abuelnasr, Ahmad Hassan, Mohamad Sawan, and Yvon Savaria are with the Department of Electrical Engineering, Polytechnique Montréal, Montreal, QC H3T 1J4, Canada (e-mail: mostafa.amer@polymtl.ca).

Ahmed Ragab is with CanmetENERGY, Varennes, QC J3X 1P7, Canada, also with the Department of Mathematics and Industrial Engineering, Polytechnique Montréal, Montreal, QC H3T 1J4, Canada, and also with the Faculty of Electronic Engineering, Menoufia University, Menouf 32952, Egypt.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3341691.

Digital Object Identifier 10.1109/TPEL.2023.3341691

I. Introduction

SWITCHED-MODE power systems (SMPSys), including dc–dc converters and power amplifiers (PAs), are widely used in various applications such as renewable energy systems, electric vehicles, and avionics [1], [2], [3]. However, achieving high efficiency and reliability in these systems, particularly in high-frequency (few MHz range) and high-voltage (HV) (100 V range) domains, poses significant challenges [1], [4]. A key approach to addressing these challenges is the utilization of efficient and integrated gate drivers (GDs), ensuring safe and rapid switching of power transistors [5]. Although SMPSys can theoretically reach 100% efficiency, there exist three sources of power losses in practice that degrade their performance, namely conduction losses (P_{cond}), GD losses (P_{gate}), and switching losses (P_{sw}). P_{cond} is mainly due to the finite ON-resistance (R_{ON}) of the power switches, whereas P_{gate} and P_{sw} stem from the charge transfer during the switching activity of the power transistors and the simultaneous presence of high voltages and high currents for short time periods, respectively [6], [7].

Recently, SMPSys have shifted from asynchronous designs, which use freewheeling diodes as rectifier switches causing large ON-state losses, to synchronous half-bridge (HB) designs [7], [8]. While transistor switches in synchronous designs offer lower voltage drops and lower R_{ON}, boosting efficiency [9], they risk cross-conduction, which leads to shoot-through currents that degrade overall efficiency and can potentially damage the HB [5]. This issue stems from the propagation delay mismatch (DM) between the high-side GD channel (HSGD) and the low-side GD channel (LSGD) control signals, which can activate both switches simultaneously, as shown in Fig. 1(a). Many factors internal to the GD chip can cause this DM, such as the delay of the level-up shifter (LUS) block in the HSGD, and the delay dependencies of the different blocks on process, voltage, and temperature (PVT) variations. In addition, external factors, such as the type of the HB switches and the output load variations of the SMPSys, can also increase the DM value [10]. Addressing these issues requires advanced GD circuitry with a robust and effective dead-time generator (DTG).

A DTG prevents the simultaneous conduction of the HB switches to eliminate shoot-through currents. This is achieved by introducing a dead-time (DT) interval between the HSGD and LSGD control signals, as shown in Fig. 1(b). In this interval,

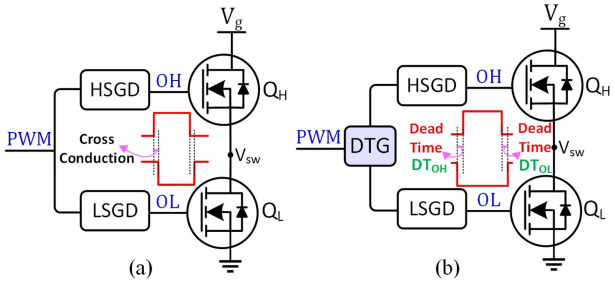


Fig. 1. Simplified GD diagram interfacing an HB. (a) Without a DTG. (b) With a DTG.

both switches are OFF, which puts the low-side (LS) transistor in a reverse-conduction state. This causes a source-drain voltage drop equal to the transistor's body-diode potential, elevating P_{cond} [11], [12]. Therefore, it is essential to minimize DTs to reduce body-diode losses, prevent heating up of the power switches, and avoid output signal's distortion in applications such as audio PAs [2], [13]. As a solution to eliminate the body-diode losses and reduce both P_{sw} and P_{gate}, resonant GDs have been introduced, offering soft-switching and energy recovery techniques [14], [15], [16]. However, they require complex DT control, in addition to resonant tanks, which comprise off-chip capacitors and inductors, to achieve soft switching [17]. Also, with the increase in switching frequency (F_{sw}), there is a notable rise in P_{gate}, thus requiring a careful tradeoff between the two quantities, which limits the maximum F_{sw} below the MHz range.

Prior research has explored many approaches to dynamically adjust the DT and generate optimal values that prevent shoot-through currents [18]. Some designs employed digital-based circuits, such as the work in [19], which uses a senseFET, passive components, a flip-flop, and a finite-state machine. In [20], a DTG is integrated with a digital feedback controller to produce an optimal DT value. Other designs, such as the one in [12], use senseFETs for body-diode conduction detection at the switching node (V_{sw}), followed by comparators and digital circuits for DT adjustment. The research works presented in [18] and [19] utilize circuit blocks including current sources, switched capacitors, comparators, and digitally-controlled delay cells. However, some of these reported designs are susceptible to noise due to their reliance on passive devices and analog components. Others necessitate complex additional circuits for DT calculations or calibration to avoid unwanted variations. In addition, certain designs realized in low-voltage (LV) processes may require scaling and adaptation for proper operation in HV domains. A high-resolution DT controller was presented in [8], which scales down V_{sw} and compares it to a fixed window. However, the scaling coefficient and the window's width largely affect the DT accuracy. The impact of PVT variations on the DM and DT generation was considered in [5], [10], [16], and [21]. However, they either considered external calibration of the DTG or accounted for the variations by corner simulations before fabrication. A recent DTG architecture, based on a few digital gates and level-down shifters (LDSs), was proposed in [22] and validated in [2], This approach aims to minimize the applied DT while accounting for DMs in the GD.

The performance of many controllers in SMPSys is directly affected by time delays in the control loop, often stemming from blocks such as the GD [23], [24]. Surpassing a certain threshold for the control signals' propagation delay in the GD may lead to control performance diversion, causing system instability. This delay also sets an upper limit on F_{sw}. Thus, GDs with lower propagation delays are favored and more suitable for closed-loop systems and high-frequency applications. The individual delay of each component in the GD contributes to its total delay. For instance, most LUSs have increased delays in HV operation [25]. Also, the conventional two-phase clock DTG adds a delay equal to twice the applied DT to the total GD delay [2]. The following sections will further explain these aspects and propose solutions to improve performance.

Addressing the limitations and needs discussed above, this article proposes a fully integrated GD for HB-based SMPSys featuring a dual-mode DTG. The first mode is a self-adjusting DTG (SDTG) adopted from [2], which can adapt to the DM variations between the HSGD and LSGD by self-adjusting the generated DTs without external intervention or manual adjustment. The second mode is a tunable fixed DTG (FDTG), which can be externally adjusted to generate a wide range of DTs accommodating various types of applications, such as motor drives and zero voltage switching (ZVS) topologies [24], [26]. The proposed GD's performance is experimentally validated by interfacing it with a synchronous dc–dc buck converter. The system's efficiency is measured across different power loads and operating frequencies for both DT operating modes to validate the significance of the DTG circuits developed and the overall functionality of the GD. The key contributions of this article can be summarized as follows.

1) A reconfigurable fast HB GD supporting the following two DT management modes:
   a) FDTG;
   b) SDTG.
2) The FDTG mode employs a novel delay circuit for voltage-based external adjustment of applied symmetric DTs between 5 and 200 ns.
3) The SDTG mode lowers the GD's total propagation delay significantly, in addition, it achieves the minimum DT possible without manual adjustment to prevent shoot-through currents regardless of the effects of PVT variations on the DM between the HSGD and LSGD.
4) The GD has a floating HS channel with a voltage clamp for safe operation and with a high *dv*/*dt* immunity of 120 V/ns, which is verified using post-layout simulations.
5) The GD features an open-drain output configuration for both its HS and LS channels, in addition to an electrostatic discharge (ESD) self-protection in the output stage of the HS buffer.

The rest of this article is organized as follows. In Section II, we illustrate the importance of having a DTG circuit and present a comparative analysis between the different DT operating modes. Section III presents a detailed overview of the structure of the proposed GD and the implementation of the different circuit blocks including the enable/disable protection logic, the FDTG circuit, the level shifters, and the HV pads for the open-drain

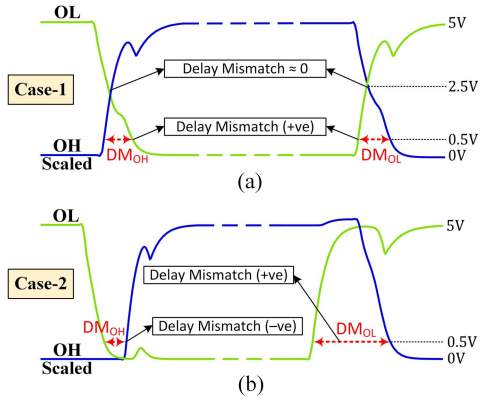


Fig. 2. Illustration of the propagation DM between OH and OL with (a) matched HSGD and LSGD, and (b) unmatched HSGD and LSGD.

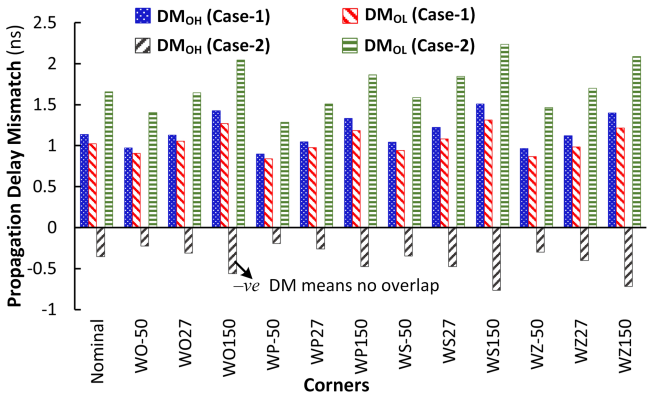


Fig. 3. Simulations of the propagation DM between OH and OL at different process corners and temperatures for the two cases in Fig. 2.

outputs. Section IV shows the experimental results of the fabricated GD prototype, as well as the measured performance of a proposed dc–dc buck converter system based on our GD. In addition, a comparison to state-of-the-art similar works is presented. Finally, Section V concludes this article.

II. Comparative Analysis of Dead-Time Generators

In this section, the need for a DTG circuit in a dual-channel GD is illustrated by performing corner simulations on the DM between the HSGD and the LSGD. In addition, a comparative analysis between the employed DT modes is presented to show their advantages and disadvantages.

In a GD without a DTG circuit, as depicted in Fig. 1(a), the driving output signals, OH and OL, will switch simultaneously if the HSGD and LSGD exhibit matched propagation delays, as demonstrated in Fig. 2(a). However, if a positive (+ve) DM exists between the HSGD and LSGD, OH and OL will switch at different times, resulting in an overlap period where both signals remain high, as demonstrated in Fig. 2(b). In both cases, cross-conduction is likely to happen, causing shoot-through currents as the power transistors, Q_H and Q_L, will be either partially or fully turned ON at the same time. The partial turn-ON can occur if one of the power transistors, such as Q_H, starts to turn ON whereas the other Q_L is turning OFF at the same time and vice versa, as illustrated in Fig. 2(a), where +ve DM exists if the switching threshold is considered at 0.5 V. To address this cross-conduction issue, a DTG circuit is necessary, as shown in Fig. 1(b). An effective DTG should apply two DTs to eliminate any overlap, by converting any +ve DM to negative (–ve) DM, like DM_{OH} shown in Fig. 2(b), and ensuring that the OH and OL signals switch sequentially to prevent any potential cross-conduction. In this context, DM_{OH} is defined as the DM between OL's falling edge and OH's rising edge, whereas DM_{OL} refers to the DM between OH's falling edge and OL's rising edge. In this article, we employed a DTG with two modes of operation that can either function separately or combined. The first is the externally tunable FDTG mode, and the second is the SDTG mode. The DTG generates two DTs, DT_{OH} and DT_{OL}, as illustrated in Fig. 1(b), which counteract DM_{OH} and DM_{OL}, at the rising events of OH and OL, respectively.

The FDTG mode generates symmetric and fixed DT_{OH} and DT_{OL}, where the values of the applied DTs need to be higher than the highest +ve value between DM_{OH} and DM_{OL} to eliminate any potential overlap at the switching events. Even though post-layout and corner simulations can give an estimate of the DM between the HSGD and LSGD, as shown in Fig. 3, there are external post-fabrication factors that are specific to each application, such as the output load, input supply, and power transistors, that can affect the DM value [10]. Hence, using the FDTG mode requires the generation of DTs sufficiently larger than the largest DM for safe and reliable operation, which can consequently cause large body-diode losses. Conversely, the SDTG mode generates adaptive DT_{OH} and DT_{OL} according to the propagation delays encountered in the HSGD and the LSGD, respectively, as will be explained in Section III. This mode is expected to handle the DM variations as well as the external factors because it guarantees a sequential turn-OFF and turn-ON of Q_H and Q_L.

To demonstrate how the DM can change considerably with the process variations, corner simulations are performed to examine the GD performance when interfacing with an HB, whose power transistors each have a maximum input capacitance of 288 pF. The process corners considered include worst zero, where slow NMOS and fast PMOS are used, worst one, where fast NMOS and slow PMOS are used, worst speed (WS), where both NMOS and PMOS are slow, and worst power (WP), where transistor parameters are set to consume the most power [27]. Also, three temperatures (–50, 27, and 150 °C), including the two extremes tolerated by the process, are considered. Fig. 3 reports the simulated DM_{OH} and DM_{OL} at the different corners and temperatures for matched HSGD and LSGD [see Case 1, Fig. 2(a)] and unmatched HSGD and LSGD [see Case 2, Fig. 2(b)], where DM is measured at 10% (0.5 V) level of the signals to consider partial turn-ON. It is worth noting that Case 2 is realized by removing the LUS block from the LSGD, hence, OH is delayed in comparison to OL. The notations on the *x*-axis denote the nominal corner in addition to the 12 different combinations of corners and temperatures that were simulated. For instance, "WP-50" represents the WP corner at a temperature of –50°C. For Case 1, both DM_{OH} and DM_{OL} are +ve with maximum values of 1.51 ns and 1.31 ns, respectively,

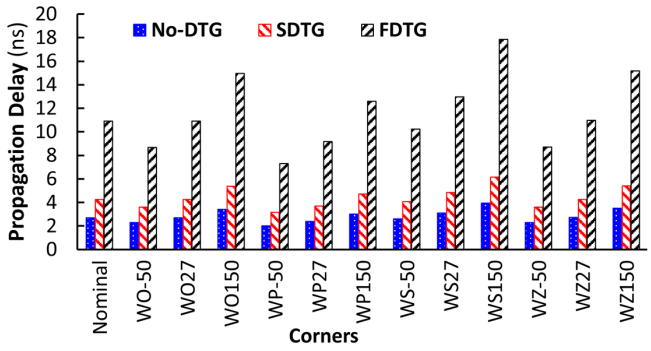


Fig. 4. Simulations of the average total propagation delay of the GD from the input PWM signal to OH/OL once for each DT mode (SDTG and FDTG) and once without using any DTG at different process corners and temperatures.

at "WS150," which translates to a WS corner at 150°C. After post-layout simulation, DM_{OH} and DM_{OL} get worse and jump to 1.83 ns and 1.82 ns, respectively. For Case 2, DM_{OH} is always –ve indicating no overlap between OL and OH, whereas DM_{OL} is +ve with a maximum value of 2.24 ns at "WS150." After post-layout simulation, DM_{OL} gets worse and jumps to 2.52 ns. These observations stress the need for a DTG to handle any +ve DM in the GD whether a LUS is used in the LSGD or not.

Whether the FDTG mode or the SDTG mode is used to generate the DTs or no DTG is used at all, the input pulsewidth modulated (PWM) signal traversing the GD experiences a propagation delay until OH and OL are generated. Fig. 4 shows the simulated total propagation delay across the GD for the different DTG modes and the different process corners and temperatures. It is quite notable that, in the worst-case corner "WS150," the smallest delay (4 ns) occurs when no DT is applied (no-DTG). On the other hand, the SDTG mode increases the propagation delay slightly to be 1.6× that of the no-DTG scenario, whereas the FDTG mode increases the propagation delay significantly to be 4.5× that of the no-DTG scenario. This is a significant improvement offered by the SDTG mode over the FDTG mode, where in some applications, small propagation delays are critical for high-frequency closed-loop control stability. In addition, the SDTG mode helps to reduce the body-diode drop by minimizing the generated DTs as will be explained in the following section.

III. Proposed Gate Driver: Design and Implementation

In this section, we present a detailed design procedure for the proposed GD and elaborate on the implementation of its various circuit blocks in the HV 0.18-μm silicon-on-insulator (SOI) process technology. Fig. 5 depicts the block diagram of the GD while interfacing with a synchronously switching buck power-stage. The GD's operation starts with a PWM signal passing through an enable/disable protection logic, resulting in two complementary signals, H and L. Subsequently, H and L can either be channeled to the FDTG block to introduce a symmetric DT interval between them or bypass the FDTG to be directed to the HS and LS channels with the SDTG enabled by the SEL signal. Regardless of the path taken, the HS signal undergoes level-shifting from (0V–VDD) to (VSSH–VDDH), which generates the OH signal to drive the power switch Q_H via the HS buffer chain. Simultaneously, the LS signal passes through an identical LUS block, maintaining the (0V–VDD) level, to minimize any DM between the two GD channels and to produce the OL signal to drive the power switch Q_L through the LS buffer chain. The following sections provide a comprehensive description of each block in the GD.

A. Enable/Disable Protection Logic

The input PWM signal is first fed to a Schmitt trigger, as shown in Fig. 6(a), to produce a clean signal mitigating input noise with fast edges. Otherwise, slow and noisy edges might cause oscillations and excessive current consumption if they repeatedly cross the switching threshold. The Schmitt trigger circuit, depicted in Fig. 6(c), acts as an inverter with hysteresis whose high (V_{SH}) and low (V_{SL}) switching thresholds are designed to be 3 V and 2 V according to [28], respectively. The sizing of transistors is based on the hysteresis amount (1 V), determined by the design equations given as follows [29]:

$$\frac{W_{N1}L_{N1}}{W_{N3}L_{N3}} = \left[\frac{VDD - V_{SH}}{V_{SH} - V_{THN}}\right]^2 \quad (1)$$

$$\frac{W_{P1}L_{P1}}{W_{P3}L_{P3}} = \left[\frac{V_{SL}}{VDD - V_{SL} - |V_{THP}|}\right]^2 \quad (2)$$

where V_{THN} and V_{THP} are the threshold voltages of the NMOS and PMOS transistors, respectively, whereas $W_{N,P}$ and $L_{N,P}$ are the transistor's width and length, and VDD is equal to 5 V.

The enable/disable protection logic block, depicted in Fig. 6(a), allows the external control of the GD operation using the En signal. When En is high, the signal polarity of H (DT_H) and L (DT_L) follows the PWM and its complement, respectively, as illustrated in the truth table in Fig. 6(b). Conversely, when En is low, both H and L become high, causing the GD to operate in one of two modes (OFF mode or debug mode) based on the DT_Mode signal polarity, as shown in the truth table in Fig. 5. If DT_Mode is low, both PWMH and PWML signals remain low, effectively disabling the HS and LS channels (OFF mode). However, if DT_Mode is high, both PWMH and PWML will be high, mirroring H and L, which enables the debug mode by controlling the HS and LS channels through the IN_H and IN_L signals (when SEL is high). In addition, external driving control signals can be supplied to both channels when the debug mode is active. If both En and DT_Mode are high, and SEL is low, the SDTG mode will be active and in control of OH and OL.

B. Tunable Fixed Dead-Time Generator

In certain applications, FDTG can be advantageous when the DT needs to be externally fine-tuned while maintaining predictability. The FDTG circuit is implemented using a nonoverlapping two-phase clock generator, as depicted in Fig. 7(a). By incorporating a voltage-controlled delay element (Delay) in both the upper and lower paths, the DT between the two output signals (DT_H and DT_L) becomes externally adjustable. Fig. 7(c) presents the proposed circuit diagram and transistor sizing of this delay element, which relies on the modulation of transistor resistance to control the propagation delay of its input signal In

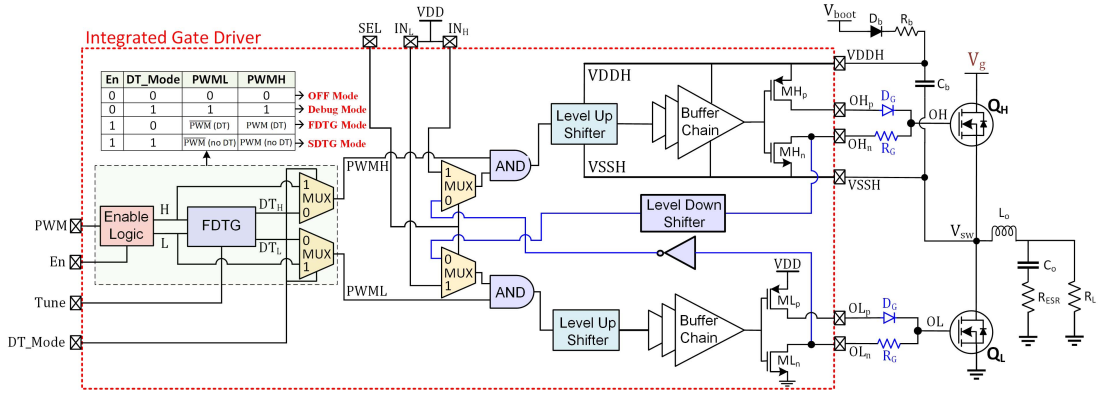
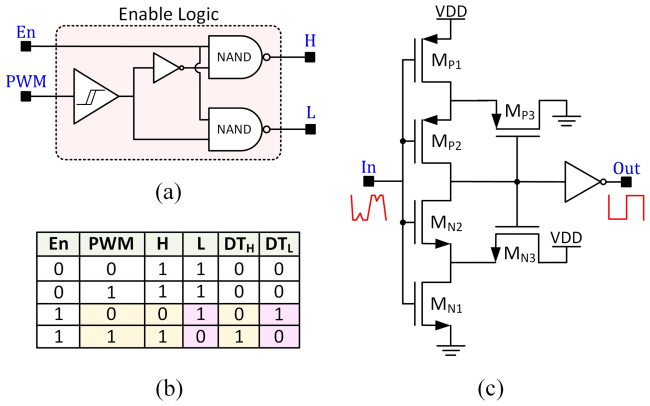


Fig. 5. Block diagram of the proposed GD while interfacing an off-chip dc–dc buck power-stage. A table summarizing the DTG operation modes (OFF, debug, FDTG, and SDTG) is shown in the top left corner of the figure.



En	PWM	H	L	DT_H	DT_L
0	0	1	1	0	0
0	1	1	1	0	0
1	0	0	1	0	1
1	1	1	0	1	0

Fig. 6. (a) Enable protection logic circuit diagram. (b) Schmitt trigger circuit diagram. (c) Truth table of the enable protection logic.

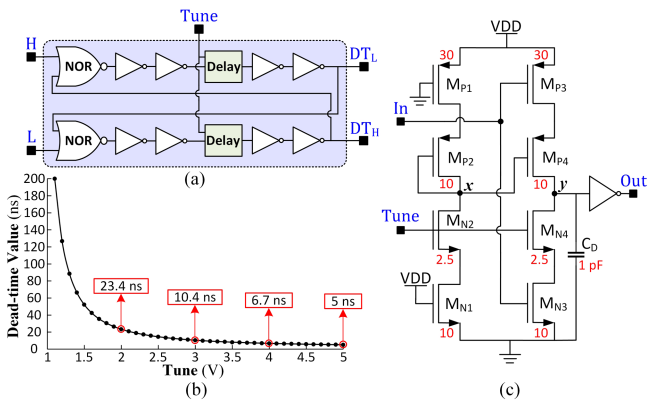


Fig. 7. (a) Circuit diagram of the FDTG block. (b) Post-layout simulated DT value achieved by the FDTG as a function of the Tune signal value. (c) Circuit diagram of the voltage-controlled delay element (Delay).

using the external analog signal Tune. The circuit operation is described as follows. When Tune is set close to VDD, M_{N2} is fully active, effectively pulling node x toward GND. This fully activates either M_{P4} or M_{N4} based on In's polarity, turning the M_{P3}–M_{N3} transistor pair into a strong inverter, which drives the capacitor C_D to produce a fast output. As Tune decreases, M_{N2} becomes less conductive, resulting in node x being pulled up gradually by M_{P2} and M_{P1}. This leads to increased resistance in

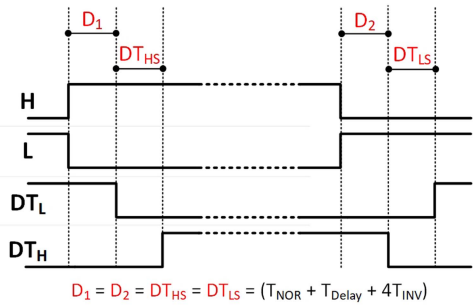


Fig. 8. Waveforms of the input and output signals of the FDTG block illustrating the DTs and propagation delays.

M_{P4} and M_{N4}, making the M_{P3}–M_{N3} inverter weaker and, thus, increasing the propagation delay. This configuration achieves highly symmetric DTs between DT_L and DT_H, ranging from 5 ns to 200 ns when Tune varies from 5 to 1.1 V, as illustrated in the post-layout simulation in Fig. 7(b). The minimum DT value (5 ns) is designed to be slightly higher than twice the worst +ve DM (1.83 ns) in both the HSGD and LSGD to ensure safe operation in case the FDTG mode is activated without the SDTG mode.

In the event where we can match the rising and falling delays (which cannot always be guaranteed), Fig. 8 shows waveforms of the input (H and L) and output (DT_H and DT_L) signals of the FDTG block while analyzing the different propagation delays. The achieved DT between $DT_{L(rise)}$ and $DT_{H(fall)}$ is denoted by DT_{LS} and expressed in (3), whereas the achieved DT between $DT_{H(rise)}$ and $DT_{L(fall)}$ is denoted by DT_{HS} and also expressed by (3):

$$DT_{LS} = DT_{HS} = T_{NOR} + T_{Delay} + 4T_{INV} \quad (3)$$

where T_{NOR}, T_{Delay}, and T_{INV} are the propagation delays through the NOR gate, Delay block, and inverter gate, respectively, that constitute the FDTG circuit [see Fig. 7(a)]. It is notable here that the FDTG block adds an additional delay to the output signals which is represented by D_1 and D_2, as illustrated in Fig. 8. Thus, the propagation delay (T_{FDTG}) of $DT_{L(rise)}$ and $DT_{H(rise)}$ with respect to L_{rise} and H_{rise}, respectively, will be approximately twice the DT value (~10 ns at Tune = 5 V)

as expressed by (4). This will significantly increase the total propagation delay of the whole GD since both the HS and LS channels add more delays from the LUS and buffer chain blocks.

$$T_{\mathrm{FDTG}} = \mathrm{D}_1 + \mathrm{D}T_{\mathrm{HS}} = \mathrm{D}_2 + \mathrm{D}T_{\mathrm{LS}} = 2\left(T_{\mathrm{NOR}} + T_{\mathrm{Delay}} + 4T_{\mathrm{INV}}\right). \quad (4)$$

C. Level-Up Shifter

Utilizing an HB with an HS n-type power transistor offers many advantages, such as faster switching speeds and reduced P_{gate} and P_{sw} [8]. However, this configuration requires an external bootstrapping circuit, as depicted in Fig. 5, to maintain a proper driving operation. Furthermore, the HSGD must incorporate an LUS capable of preserving the output OH state and ensuring immunity to the fast slew rates of the floating supply VSSH connected to the switching node (V_{sw}).

The level-shifter design process involves tradeoffs between achieving high slew-rate immunity, low propagation delay, less complexity, and low power consumption [11]. Therefore, we decided to employ the LUS proposed in [30], whose sized circuit diagram is shown in Fig. 9(a), as it offers an excellent balance between latency (<1 ns), power consumption (111 μW, at VSSH = 50 V), and layout area (0.011 mm^2). Moreover, this LUS features pull-up and pull-down current mirrors to cancel injected common-mode coupling currents, achieving slew-rate immunity of 120 V/ns, as shown in the post-layout simulation in Fig. 10, where the output latch nodes (N1 and N2) maintain their state regardless of the switching activity of VSSH. HV transistors, with a maximum rating of 125 V, are used to implement the LUS as shown in Fig. 9(a). This allows the GD to operate at up to 100 V safely. The current mirrors, output latch, and HV transistors are implemented in HV p-type wells and surrounded by deep trench isolation (DTI) to handle high common-mode voltage with respect to the substrate potential.

Furthermore, the LUS achieves falling (T_{F}) and rising (T_{R}) propagation delays of less than 1 ns across most of the VSSH signal range, as shown from the post-layout simulations in Fig. 11. Also, the used pulse-triggered input mechanism contributes to reducing the LUS power consumption remarkably (111 μW, at VSSH = 50 V). Finally, as depicted in Fig. 5, the LUS is employed for both the HSGD and LSGD to match the signal propagation delay and minimize any discrepancy between the two channels for optimum operation of the FDTG mode.

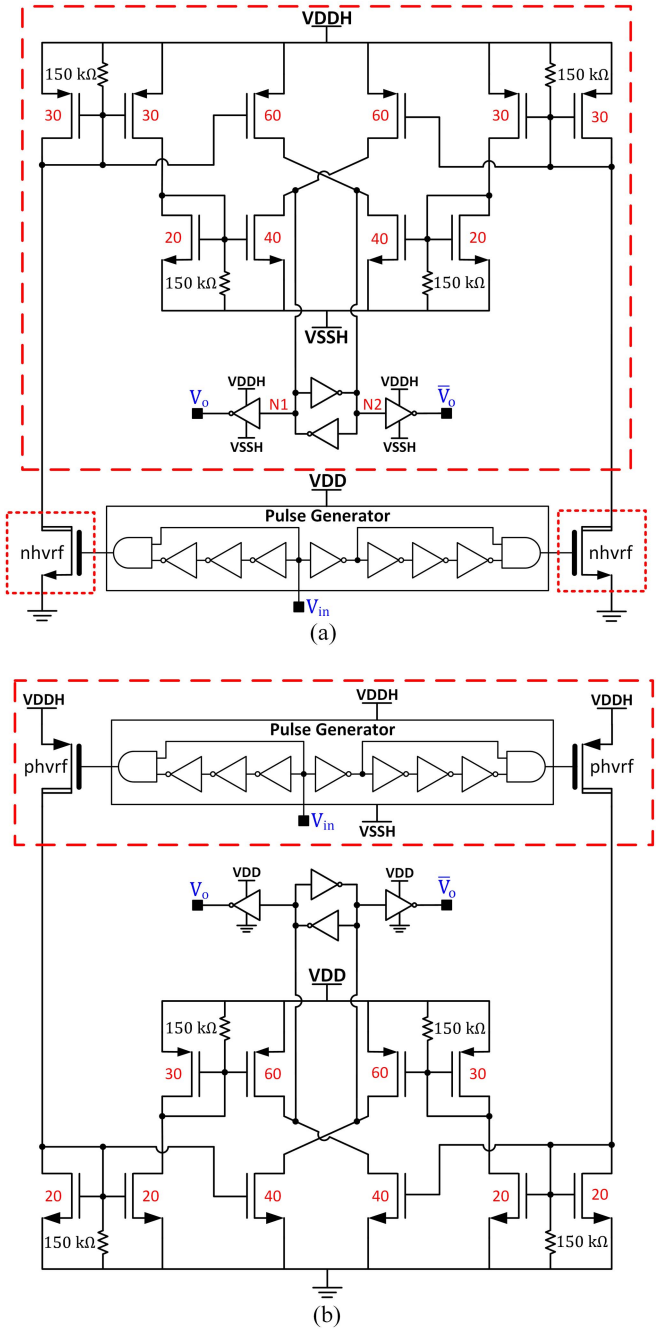


Fig. 9. Circuit diagrams of the implemented: (a) LUS (adapted from [30]) and (b) LDS. Red dashed boxes are HV p-type wells surrounded by DTI.

D. Self-Adjusting Dead-Time Generator

Efforts have been made to construct the GD architecture and optimize its layout to minimize DM between the HSGD and LSGD. However, as explained in Fig. 3, +ve mismatch still exists. This can be due to the PVT variations, as well as the fact that the LUS used does not exhibit a constant propagation delay across the full voltage range of the VSSH signal, as shown in Fig. 11. By using the FDTG mode, a fixed DT value is achieved, which in turn converts the DM into a –ve value, thus, preventing the possible cross-conduction and shoot-through currents. However, the total propagation delay through the GD increases to a minimum of 18 ns (when Tune = 5 V) and even more (when Tune < 5 V) for higher DT values, as shown in Fig. 4, limiting the maximum operating frequency of the SMPSys. Moreover, unpredictable DMs that exceed the applied fixed DT value may occur as a consequence of changing the power load for the switching dc–dc converter or replacing the HB power transistors with different types [10]. The applied fixed DT could also be much higher than the DT required to cancel the DM, consequently, large body-diode losses caused by the reverse recovery current can occur [12]. For these reasons, we recommend employing the SDTG mode, which can be activated by setting the SEL signal (see Fig. 5) to low.

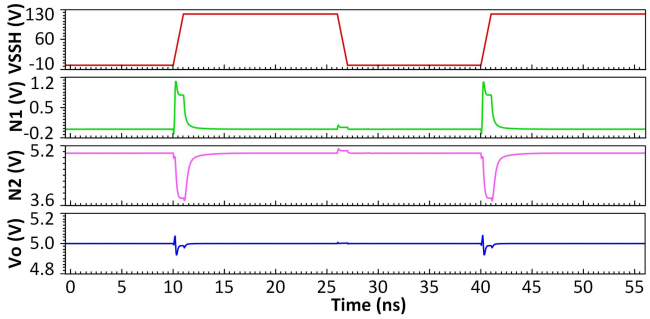


Fig. 10. Post-layout simulation of the LUS signals when VSSH experience slew rate of 120 V/ns.

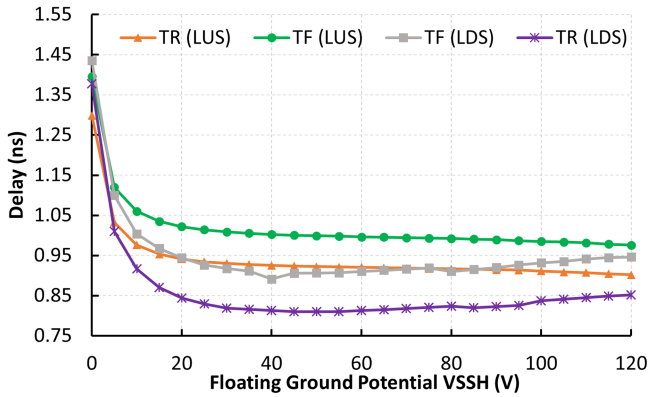


Fig. 11. Post-layout simulated rising (T_{R}) and falling (T_{F}) propagation delays of the LUS and the LDS.

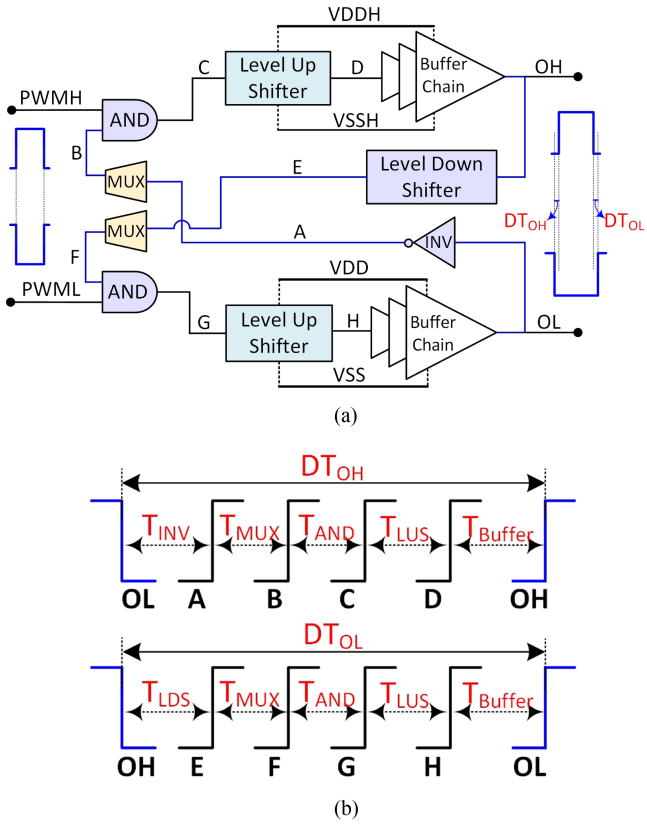


Fig. 12. (a) Simplified diagram of the GD with SDTG mode activated. (b) Waveforms of the various propagating signals forming the DTs ($\mathrm{DT_{OH}}$ and $\mathrm{DT_{OL}}$).

The SDTG operation is explained here through the simplified diagram of the GD, with the SDTG mode activated, as shown in Fig. 12(a). The rising edge of each of the two complementary input signals (PWMH and PWML) does not propagate to the HS and LS channels, unless signal B and signal F turns high, respectively. Signal B (and A) represents the inverted version of OL, whereas signal F (and E) represents the inverted and level-down shifted version of OH. This configuration ensures the sequential turn-OFF and turn-ON of the HB power transistors, thereby theoretically preventing any shoot-through current. Furthermore, the DT between $\mathrm{OH_{rise}}$ and $\mathrm{OL_{fall}}$ ($\mathrm{DT_{OH}}$) accounts for the propagation delay through the HS channel, as illustrated in Fig. 12(b). Similarly, the DT between $\mathrm{OL_{rise}}$ and $\mathrm{OH_{fall}}$ ($\mathrm{DT_{OL}}$) accounts for the propagation delay through the LS channel, as illustrated in Fig. 12(b). So, $\mathrm{DT_{OH}}$ and $\mathrm{DT_{OL}}$ constitute their DT value based on the delay of the two GD channels as expressed by the following equations, respectively, without adding an additional propagation delay to the GD as in the case of the FDTG mode:

$$\mathrm{DT_{OH}} = T_{\mathrm{Buffer}} + T_{\mathrm{LUS}} + T_{\mathrm{AND}} + T_{\mathrm{MUX}} + T_{\mathrm{INV}} \quad (5)$$

$$\mathrm{DT_{OL}} = T_{\mathrm{Buffer}} + T_{\mathrm{LUS}} + T_{\mathrm{AND}} + T_{\mathrm{MUX}} + T_{\mathrm{LDS}} \quad (6)$$

where T_{Buffer}, T_{LUS}, T_{AND}, T_{MUX}, T_{INV}, and T_{LDS} represent the propagation delays through the buffer chain, LUS, AND gate, multiplexer, inverter gate, and LDS blocks used in the GD, respectively. Hence, the proposed SDTG can adapt to any DM variations between the HS and LS channels while applying the minimum DT possible to prevent cross-conduction. In addition, it can adapt to external modifications in the power-stage that affect the required minimum DT value, such as varying the load impedance or altering the power transistors (changing C_{load}) that affects T_{Buffer}.

As explained above, an LDS block is essential for the proper operation of the SDTG mode to invert and level-shift the OH signal to the LV domain in HB GDs. The LDS circuit, depicted in Fig. 9(b), is implemented by applying the concept of duality to the LUS circuit [see Fig. 9(a)]. This approach involves reversing the role (pulling down or pulling up) and the type (NMOS or PMOS) of each component except for the pulse-triggered input part [25]. In the LDS design, the pulse-triggered input, along with the HV transistors, are integrated into HV p-type wells as they interface with the floating rails, unlike their role in the LUS. Similar to the LUS performance, the LDS achieves T_{F} and T_{R} values of less than 1 ns across most of the VSSH signal range. This is shown in the post-layout simulation results presented in Fig. 11.

E. Buffer Chains and Open-Drain Outputs

A buffer chain is used at the end of both the HS and LS channels, as shown in Fig. 5, to amplify the propagating signal power. It minimizes the signal propagation delay by efficiently driving the large input capacitance of the power switches in the HB. The buffer block is designed with a tapered configuration,

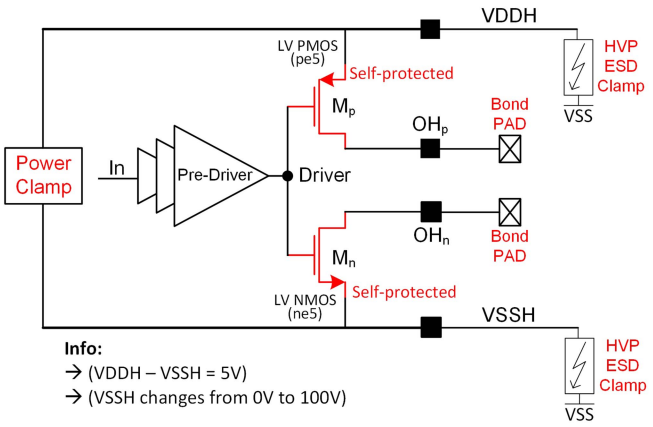


Fig. 13. Structure of the HS buffer with the open-drain configuration.

comprising a chain of N inverters, each stage being k times larger than the preceding one. The total propagation delay of a tapered buffer driving a capacitive load (C_{load}) with a minimum size inverter as the first stage, featuring input capacitance ($C_{\rm in}$) and delay (T_0), can be calculated using the following equation [29]:

$$T_{\rm buffer} = T_0 \frac{k}{\ln(k)} \ln(y) \tag{7}$$

where $y = C_{\rm load}/C_{\rm in}$ and $k = y^{1/N}$ represents the tapering factor. In our GD, the tapered buffer consists of six stages. The first stage is an inverter whose PMOS transistor has 0.5 μm length and 30 μm width and its NMOS transistor has 0.5 μm length and 15 μm width. The tapering factor is selected to be 3, enabling the buffer to provide source and sink currents up to 1.75 A. Consequently, this allows switching GaN transistors such as the EPC2019 device ($C_{\rm load} = 288$ pF) in less than 3 ns.

The open-drain (or split-output) configuration is adopted in both the HS and LS buffers, as it provides flexibility to interface with different types of power transistors. In addition, this configuration facilitates the use of an external gate diode (D_G) in the push path and an external gate resistor (R_G) in the pull path, as illustrated in Fig. 5. The R_G resistor helps in damping oscillations and ringing caused by parasitic capacitances and inductances within the gate drive loop, which is crucial for reliable operation and minimizing switching losses. On the other hand, the D_G diode enables fast turn-ON and reduces the reverse leakage current through the push path [31]. To realize the open-drain configuration, the push-pull (final) stage of the tapered buffer incorporates ESD self-protected transistors, whose drains are directly connected to bond pads for external access, as depicted in Fig. 13. In addition, an isolated power ESD clamp is installed between the floating rails, VSSH and VDDH, to internally clamp the voltage difference at 5 V for safety. Following the recommendations of ESD specialists, each rail is connected to an HV pad (HVP) with PMOS-based ESD clamps for external access, as shown in Fig. 13.

The self-protected PMOS transistor (M_p) is implemented using 60 instances of the circuit configuration shown in Fig. 14(a), each of which being equivalent to a PMOS with a 120 μm width and a drain resistance (rd_p) of 3.5 Ω, yielding a total width of 7.2 mm. The self-protected NMOS transistor (M_n)

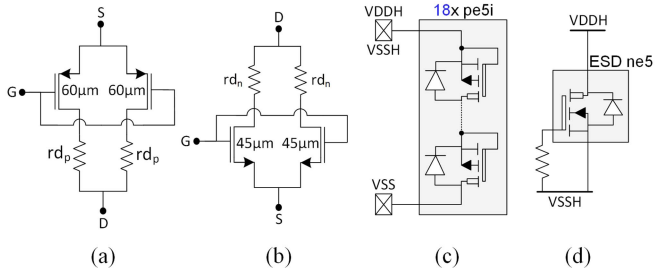


Fig. 14. Circuit configurations illustrating the composition of the HS buffer. (a) PMOS unit of the self-protected transistor M_p. (b) NMOS unit of the self-protected transistor M_n. (c) Trench-isolated PMOS stack representing the HVP with ESD clamp. (d) Isolated power ESD clamp.

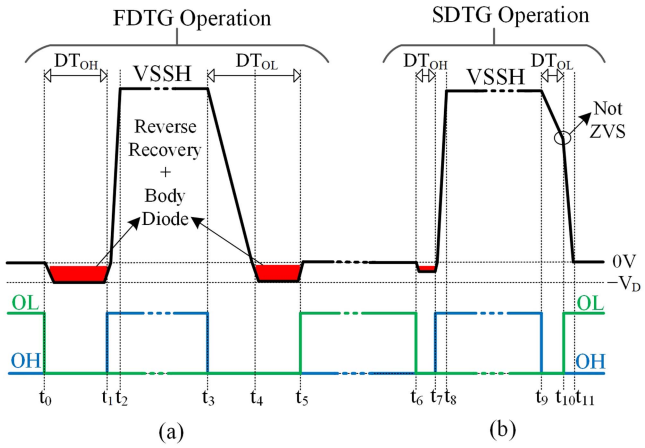


Fig. 15. Switching states of the DT modes. (a) FDTG. (b) SDTG.

is implemented using 40 instances of the circuit configuration shown in Fig. 14(b), each of which being equivalent to an NMOS with a 90 μm width and a drain resistance (rd_n) of 4.2 Ω, yielding a total width of 3.6 mm. The HVPs support up to 120-V operation and are implemented using a trench-isolated PMOS stack of 18 transistors, as shown in Fig. 14(c), where each transistor has a total width of 800 μm. Finally, the power clamp used consists of an ESD NMOS transistor that has a total width of 480 μm, as shown in Fig. 14(d). The structure of the open-drain LS buffer chain is like that of the HS (see Fig. 13), but the HVP clamps are replaced with LV analog pads in which the power clamp is not used.

F. Further Analysis and Simulation Results

The operation of both the FDTG and SDTG modes is further illustrated by the switching state diagram of a buck power-stage, as shown in Fig. 15, with the assumption of +ve inductor current (I_L) throughout the switching period. Since the FDTG mode does not consider the DM between the HSGD and LSGD, in addition to its lack of information on the state of Q_H and Q_L, large DT_{OH} and DT_{OL} are required to prevent cross-conduction. This results in time intervals, t_1–t_0 and t_5–t_4, during DT_{OH} and DT_{OL}, respectively, where Q_L's body-diode becomes active, as shown in Fig. 15(a), causing significant conduction and reverse recovery losses (P_{BD}) expressed by (8):

$$P_{\rm BD} = V_D\, F_{\rm sw}\, (I_o t_c + I_{\rm rr} t_{\rm rr}) \tag{8}$$

where V_D is the voltage across the body diode, I_o is the average output current, t_c is the diode's conduction period, I_{rr} is the reverse recovery current, and t_{rr} is the reverse recovery time [32]. It is notable that P_{BD} rises as the DT period and F_{sw} increase degrading the system efficiency. In addition, for certain power switches, such as GaNFETs, V_D can reach values as high as 2.5 V [33], worsening the performance even more. On the other hand, the SDTG mode generates DTs as short as the propagation delay of the GD's channels, as given by (5) and (6), accounting for DMs and ensuring safe switching by sequential turn-ON of Q_H and Q_L. This reduces P_{BD} significantly on the DT_{OH} side by minimizing t_c (t_7–t_6) and not fully activating the body diode, and eliminates P_{BD} totally on the DT_{OL} side, as shown in Fig. 15(b). It is important to note that the SDTG mode does not support a complete ZVS operation, but only partial ZVS during the high-to-low transition of V_{sw}, resulting in some switching losses ($P_{not\text{-}ZVS}$). These losses occur as a result of Q_L turning ON at t_{10}, whereas V_{sw} is still +ve, requiring the discharge of the parasitic capacitance (C_{sw}) at the V_{sw} node as expressed by (9) [8]. However, with power switches like GaNFETs that have minimal parasitic capacitances, both C_{sw} and $P_{not\text{-}ZVS}$ are reduced. If ZVS is required, we recommend combining both the SDTG and FDTG modes to set longer DT_{OH} and DT_{OL} while preventing simultaneous turn-ON. Further analysis and modeling of power losses in the HBs during different switching scenarios can be found in [7] and [8].

$$P_{not-ZVS} = \frac{1}{2} C_{sw} V_{sw}^2 (t_{10}) F_{sw}. \tag{9}$$

Based on Fig. 12, the SDTG mode depends on using OH and OL in its operation. However, both signals are only available off-chip given that the open-drain configuration separates each into two different signals on-chip, (OH_p, OH_n) and (OL_p, OL_n), as shown in Fig. 5. Hence, for compatibility with the open-drain configuration and correct operation, the SDTG mode uses the on-chip signals, OH_n and OL_n, which correspond to the pull down output signals of the HSGD and LSGD, respectively. Indeed, OH_n and OL_n can capture the falling events of OH and OL. To verify such a technique and show the adaptability of the SDTG mode to any variations that can affect the DM between the HSGD and LSGD, we fixed Q_L to type EPC2019 ($C_{load} = 288$ pF) and simulated the GD operation within a buck converter; first for Q_H of the same type as Q_L and second for Q_H of type EPC2010C ($C_{load} = 580$ pF), as shown in Fig. 16. The results show that Q_H has lower switching speed in the second scenario reflected in the increased rise and fall times of OH and detected by signal E (level-shifted inverted version of OH_n). However, the SDTG self-adjusted the value of DT_{OH} from 2.8 to 3.06 ns as it considers T_{buffer} of the HSGD according to (5). Meanwhile, the value of DT_{OL} is kept the same at 3.6 ns with OL's rising event shifted in time as much as OH has been delayed preventing any cross-conduction by the SDTG mode. Another simulation is performed to show the adaptability of the SDTG mode to variations in the input voltage (V_g) of the buck power-stage at a fixed I_o. The results shown in Fig. 17 depict the generated DT_{OH} and DT_{OL}. The SDTG self-adjusts DT_{OH}

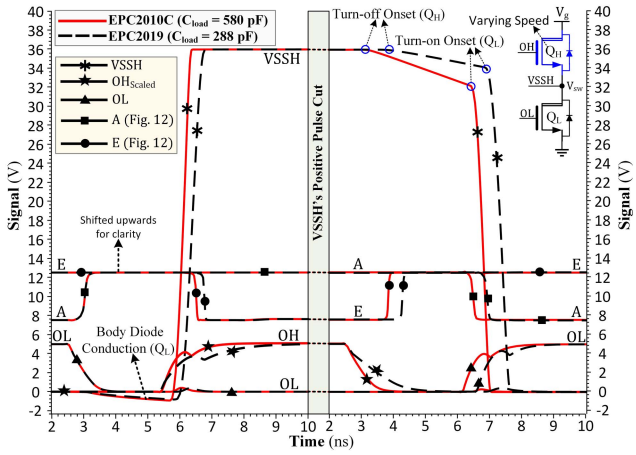


Fig. 16. Simulated waveforms of the GD showing SDTG mode adaptability to variations in the switching speed of the HS power switch (Q_H).

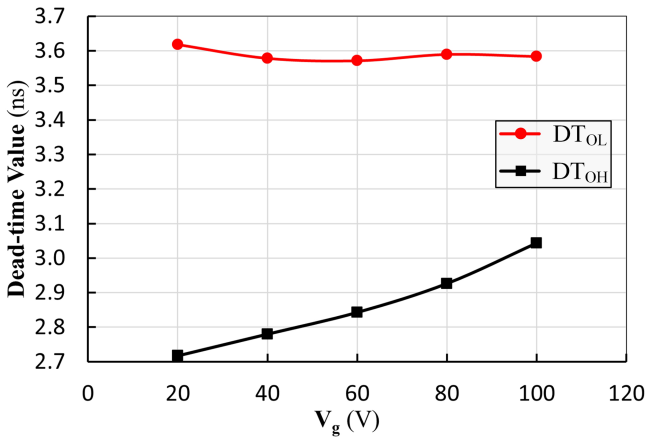


Fig. 17. Simulated DT_{OH} and DT_{OL} using SDTG mode while varying V_g.

TABLE I
BUCK CONVERTER PARAMETERS

Parameter	Value	Parameter	Value
V_g, V_o	36 V,18 V	F_{sw}	0.5–1 MHz
L_o	24 μH	r_L	37 mΩ
C_o	33 μF	r_C	2.7 mΩ
R_{ON}	42 mΩ	R_L	40–900 Ω

from 2.72 to 3.05 ns as V_g increases from 20 to 100 V, as Q_H takes more time to fully turn-ON and charge C_{sw} to a higher V_g. Conversely, DT_{OL} is fixed at 3.6 ns as both Q_L and I_L help discharge C_{sw} quickly without added delays for all V_g values.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed GD was fabricated using an HV SOI 0.18-μm technology. The micrograph and layout of the integrated chip are shown in Fig. 18, where different blocks of the GD are highlighted, along with their respective dimensions. The total chip area, including the input/output (IO) pads, is 2 mm^2, whereas the proposed GD circuit occupies only a core area of 0.285 mm^2. The GD is set up to drive a dc–dc buck converter power-stage whose parameters are summarized in Table I. The output filter comprises a 24 μH inductor (L_o) with a dc

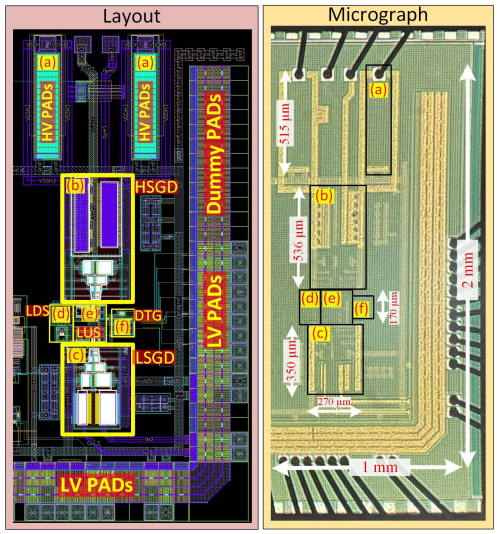


Fig. 18. Micrograph (right) and layout (left) of the fabricated 1 × 2 mm^2 die of the GD comprising (a) modified HVPs, (b) HS buffer, (c) LS buffer, (d) level-down shifter, (e) LUSs, and (f) fixed DTG and enable logic.

resistance value ($r_{\rm L}$) of 37 mΩ, and a 33 μF capacitor ($C_{\rm o}$) with an equivalent series resistance value ($r_{\rm C}$) of 2.7 mΩ. The power-stage HB comprises two EPC2019 power transistors ($Q_{\rm H}$ and $Q_{\rm L}$), each of which has $R_{\rm ON}$ of 42 mΩ. In the target application [3], the input voltage (V_g) is set at 36 V, and the nominal output voltage ($V_{\rm o}$) is 18 V. Finally, the desired load resistance (R_L) ranges from 40 to 900 Ω, whereas the system switching frequency ($F_{\rm sw}$) ranges from 0.5 to 1 MHz.

The experimental setup, used to test and characterize the performance of the fabricated prototype chip, is shown in Fig. 19. The chip die is mounted on a pin grid array package, that was assembled on a custom-designed printed circuit board (PCB). This PCB houses the buck power-stage which consists of the GaN-based HB and the low-pass filter described above. As suggested in [34], we selected BAV21 as the bootstrapping diode ($D_{\rm b}$) and a bootstrapping capacitor ($C_{\rm b}$) of 0.22 μF. $R_{\rm G}$ is selected to be 1 Ω and $D_{\rm G}$ is of type BAS40LP-7. The N5771A Agilent dc source supplies the desired V_g. The EL34243A DC electronic load is used to obtain the desired R_L for the various experiments performed. Two different supplies externally feed the GD supply (VDD = 5 V), the bootstrap supply ($V_{\rm boot}$ = 6.2 V), and Tune signal (1.1–5 V). The measured performance of the fabricated GD when driving the GaN-based HB, including aspects such as the total propagation delay and the achieved DTs, is detailed in the following subsection. Afterward, in the second subsection, the buck system performance is characterized when utilizing the GD under its various DT modes.

A. Measured Performance of Proposed Gate Driver

Table II summarizes the measured and post-layout-simulated propagation delay of the GD's channels, along with the generated DTs for both the FDTG (at Tune = 5 V, 4 V, and 3 V) and the SDTG modes. Specifically, the table details the total rising and falling propagation delays for the output OL and OH

TABLE II
SUMMARY OF MEASURED AND SIMULATED DELAYS AND DEAD-TIMES

	Propagation delays [a]				Dead-times [a]	
	OL_{rise} (ns)	OL_{fall} (ns)	OH_{rise} (ns)	OH_{fall} (ns)	DT_{OH} (ns)	DT_{OL} (ns)
FDTG[(b)] (*Tune* = 5V)	**20**	13.8	**18.4**	13.8	4.6	6.2
FDTG[(c)] (*Tune* = 5V)	14.3	9.3	14.2	9.2	4.9	5.2
FDTG[(b)] (*Tune* = 4V)	**22.4**	14.4	**20.4**	14.6	6	7.8
FDTG[(c)] (*Tune* = 4V)	16.6	10	16.7	9.8	6.7	6.8
FDTG[(b)] (*Tune* = 3V)	**28.4**	17	**28.2**	17.2	11.2	11.2
FDTG[(c)] (*Tune* = 3V)	23.1	12.7	23	12.6	10.3	10.5
SDTG [b]	**13.6**	8.2	**11.8**	8.4	**3.6**	**5.2**
SDTG [c]	7.2	3.2	6.2	3.2	3	4

[(a)] All propagation delays and dead-times were measured at 50% level of the propagating signals at V_g = 5V. [(b)] Measured values. [(c)] Post-layout simulation values.
Bold entities either signify the values where our design is better (superior) than the literature, or they represent the comparison points.

signals, referenced from the input PWM signal, and displays the achieved DTs ($DT_{\rm OL}$ and $DT_{\rm OH}$). The measured results closely align with the post-layout simulation results. However, the simulated delays are generally lower than the measured ones. This can be explained by several factors not accounted for in simulations, such as the PCB and package parasitics, or the fabrication process variations. Fig. 20 visually complements the measured data recorded in Table II. It shows the GD waveforms for the FDTG mode with a Tune voltage of 4 V in Fig. 20(a) and (b) and for the SDTG mode in Fig. 20(c) and (d). As the Tune voltage decreases, $DT_{\rm OL}$ and $DT_{\rm OH}$ increase, leading to a corresponding rise in the total propagation delay, which can reach 28.4 ns and even 400 ns (as shown later in Fig. 22), when Tune is set to 3 V and 1.1 V, respectively. This significant rise in total propagation delay with higher DTs not only limits the maximum $F_{\rm sw}$ value of the system but can also degrade the feedback control performance of closed-loop systems, leading them to the point of instability. On the other hand, the SDTG mode achieves propagation delays at least 32% lower compared to the lowest propagation delay achieved by the FDTG mode (20 ns at Tune of 5 V), showing the advantage of the self-adjusting approach. In addition, the SDTG mode achieves the lowest DT possible (3.6 ns), as illustrated in Fig. 20(c), while preventing cross-conduction, thus reducing the reverse recovery losses and body-diode losses compared to the FDTG mode [5].

While Table II provides specific data points of the FDTG mode for clarity, Fig. 21 presents the further characterization of the DTs generated by the FDTG mode as a function of the Tune voltage. From this figure, it is apparent that $DT_{\rm OL}$ and $DT_{\rm OH}$ remain nearly symmetric across the full range of the Tune signal. However, small differences ($\Delta DT < 3$ns) exist between $DT_{\rm OL}$ and $DT_{\rm OH}$, particularly in the Tune range from 1.5 to 5 V. These differences can be attributed to the DM between the HSGD and LSGD. The PCB and package parasitics in the driving path can also cause additional delays and add noise to the driving signals, which sometimes impact the measurement accuracy. On the other hand, in the lower range of Tune (1.1–1.5 V), ΔDT becomes more pronounced, reaching up to 20 ns as shown in Fig. 21. This can be due to the increased sensitivity of the generated DTs to any noise in the Tune signal, which significantly affects the measurement results. Notably, for a Tune

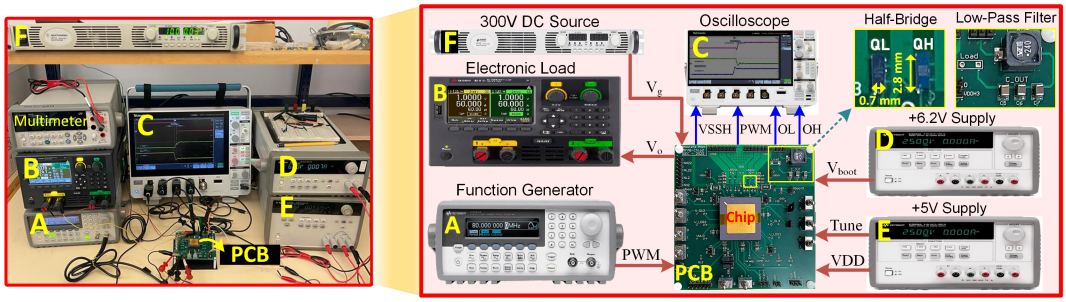


Fig. 19. Experimental setup to characterize the proposed GD chip and test its performance within a DC–DC buck converter system. The figure highlights the test PCB comprising the driver chip, and the equipment used to perform the reported measurements.

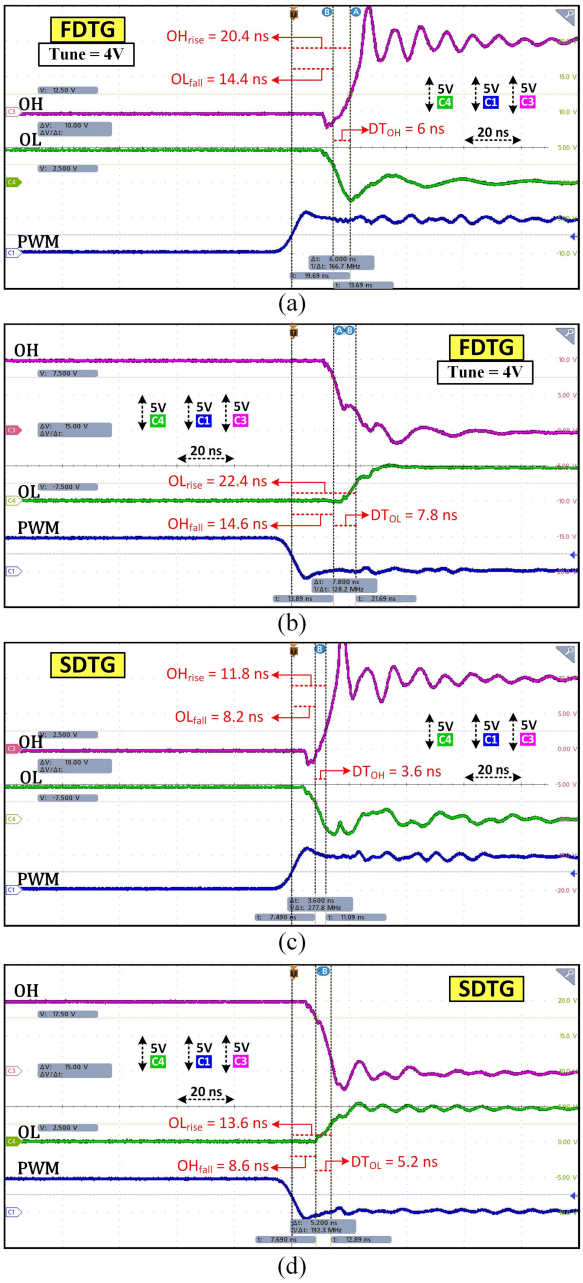


Fig. 20. Measured waveforms of the input and output driving signals for (a) and (b) FDTG mode operating at Tune = 4 V and (c) and (d) SDTG mode.

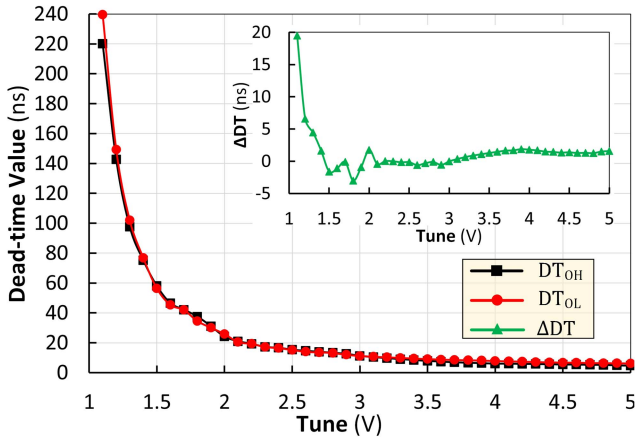


Fig. 21. Measured DT_{OH} and DT_{OL} generated by the FDTG mode versus the Tune signal voltage with the GaN-based HB as a load to the GD.

voltage ranging between 1.3 and 1.1 V, there is a difference of ∼100 ns in the generated DT, indicating a sensitivity rate of 500 ns/V. Hence, we advise maintaining the Tune signal at values larger than 1.5 V to limit the sensitivity rate, while maintaining more accurate DTs and lower propagation delays. The measured GD waveforms obtained with Tune set to 1.1 and 1.3 V are presented in Fig. 22(a) and (b), respectively, to highlight the highest DT achieved by the FDTG mode.

Table III compares our proposed GD's performance with various commercially available solutions recommended by EPC to drive their GaN-based HBs [35]. Our design, developed using the 0.18-μm SOI process, shows clear advantages. With minimum rising and falling propagation delays of 11.8 and 8.4 ns using the SDTG mode, respectively, our GD is faster than all the commercially available drivers considered. It offers an adjustable DT ranging from 5 to 200 ns, which is not present in many commercially available solutions. Moreover, the minimum DM between the GD's channels is 0.6 ns, highlighting its precision. This mismatch has been measured by applying the same PWM signal to IN_H and IN_L in the debug mode, as shown in Fig. 5, and observing the delay between OH and OL. Other features, such as the bootstrap voltage clamp and split outputs (open-drain configuration), align with what the commercial drivers offer, confirming that our design is an advantageous and practical solution. It is worth noting that the die temperature of our GD

TABLE III
PERFORMANCE COMPARISON BETWEEN THE PROPOSED GD AND COMMERCIALLY AVAILABLE SOLUTIONS

Reference[a]	LM5113-Q1	LMG1205	ADuM4221-1	NCP51810	uP1966E	MPQ1918	**This Work**
Technology	Texas Instruments	Texas Instruments	Analog Devices	On Semi	UPI Semi	MPS	0.18-μm SOI
Driver configuration	Dual-channel	Dual-channel	Dual-channel	Dual-channel	Dual-channel	Dual-channel	Dual-channel
Galvanic isolation	No	No	Yes	No	No	No	No
Power switch	GaNFET, MOSFET	GaNFET, MOSFET	IGBT, MOSFET	GaNFET	GaNFET	GaNFET, MOSFET	GaNFET, MOSFET
Input supply voltage (V)	4.5 - 5.5	4.5 - 5.5	2.5 - 6.5 [b]	9 - 17	4.5 - 5.5	3.7 - 5.5	4.5 - 5.5
Quiescent current (mA)	0.15	0.1	7.2	0.1	0.12	0.11	2.11[c]
Peak output current (A)	1.2	1.2	4	1	Not Available	1.6	1.75
Floating bus voltage (V)	100	90	35	150	80	100	100
Rising propagation delay (ns)	28	35	25	25	20	20	**11.8**[d]
Falling propagation delay (ns)	26.5	33.5	30	25	20	20	**8.4**[d]
Bootstrap voltage clamp	Yes	Yes	No	No	Yes	Yes	Yes
Split outputs	Yes	Yes	No	No	Yes	Yes	Yes
Slew rate immunity (V/ns)	50	50	Not Available	200	Not Available	Not Available	120[e]
Adjustable dead-time (ns)	No	No	62 - 2320	30 - 200	No	No	**5 - 200**
Minimum delay mismatch (ns)	1.5	1.5	1.5	5	1.5	1.5	**0.6**

[a] Typical performance values are reported. [b] Isolated output supply is between 4.5V and 35V. [c] Half the measured value is reported as our chip carries two identical GDs. [d] Measured value when SDTG mode is operating as reported in Table II. [e] Post-layout simulation result.
Bold entities either signify the values where our design is better (superior) than the literature, or they represent the comparison points.

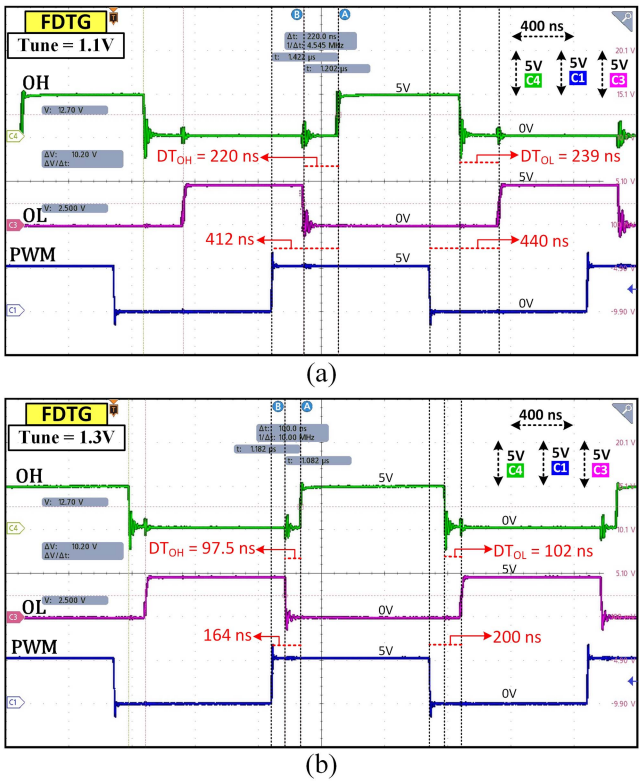


Fig. 22. Measured waveforms of the input and output driving signals with the FDTG mode operating at (a) Tune = 1.1 V and (b) Tune = 1.3 V.

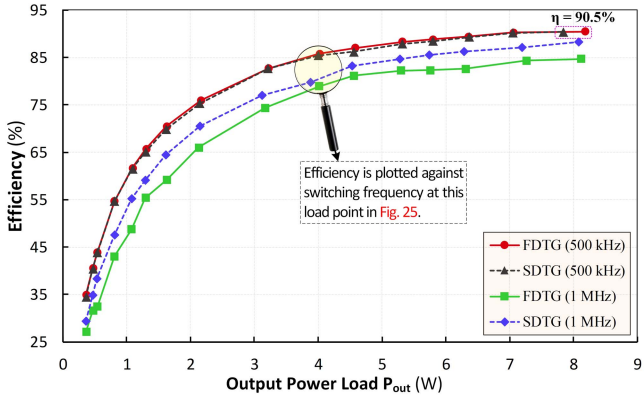


Fig. 23. Measured efficiency versus output power load ($P_{\rm out}$) of the buck converter at two different $F_{\rm sw}$ (500 kHz, 1 MHz) for the two DT modes: FDTG (at Tune = 4 V) and SDTG.

never exceeded 25.4°C (measured with an infrared thermometer applied on an open-lid package) while driving the GaN HB.

B. Measured Performance of the Buck Converter System

The measured efficiency of the buck converter system as a function of the output power load ($P_{\rm out}$) is plotted in Fig. 23. This figure presents a comparison between the FDTG and SDTG modes at two different $F_{\rm sw}$ (500 kHz, 1 MHz). At $F_{\rm sw}$ of 500 kHz, the efficiency curves for both modes are nearly identical across the entire $P_{\rm out}$ range. This observation suggests that the power losses are balanced between the two modes at this specific $F_{\rm sw}$ and that the DTs generated by the FDTG mode are sufficient to prevent cross-conduction, resulting in comparable efficiency. However, at the higher $F_{\rm sw}$ of 1 MHz, the efficiency curve for the FDTG mode is consistently lower than that of the SDTG mode by an average of 4% on the efficiency scale across the $P_{\rm out}$ range. This disparity between the two modes at the higher $F_{\rm sw}$ can be attributed to the inability of the FDTG mode to self-adjust $\rm DT_{OH}$ and $\rm DT_{OL}$ in response to propagation delay variations in the GD channels, unlike the SDTG mode. Moreover, the frequency-dependent losses using the FDTG mode are higher than the losses using the SDTG mode as clarified in Fig. 15.

The waveforms of the buck power-stage are measured while SDTG mode is active at ($R_L = 300\,\Omega, F_{\rm sw} = 1$ MHz), as shown in Fig. 24(a), and while FDTG mode is active at ($R_L = 100\,\Omega$, $F_{\rm sw}$ = 500 kHz), as shown in Fig. 24(b). As the achieved $\rm DT_{OH}$ and

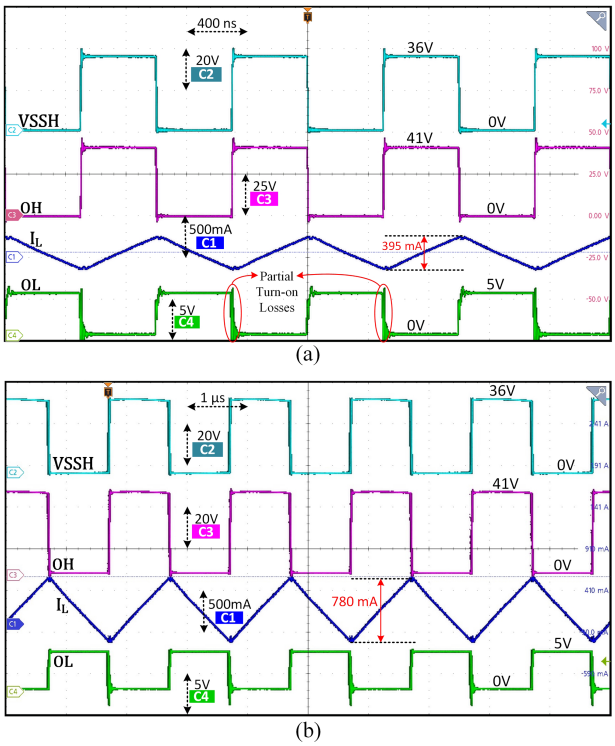


Fig. 24. Measured waveforms of the buck power-stage driven by the fabricated GD circuit with (a) SDTG mode activated at $R_{\mathrm{L}} = 300\ \Omega$ and $F_{\mathrm{sw}} = 1$ MHz and (b) FDTG mode activated at $R_{\mathrm{L}} = 100\ \Omega$ and $F_{\mathrm{sw}} = 500$ kHz.

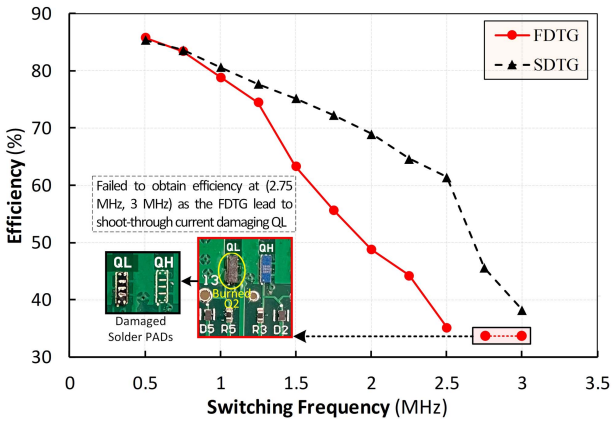


Fig. 25. Measured efficiency versus switching frequency of the buck converter at P_{out} of 4 W ($R_{\mathrm{L}} = 80\ \Omega$) for the two DT modes, SDTG (Tune = 4 V), and FDTG.

$\mathrm{DT_{OL}}$ are very small (~3.6 ns), they are difficult to observe given the comparably large time scale of the graph (> 400 ns). We can observe in Fig. 24 the unintended (or partial) turn-ON issue of $\mathrm{Q_L}$ at the rising-edge of OH. This issue primarily stems from the high slew rate (dv/dt) of the V_{sw} node, which induces peak currents into $\mathrm{Q_L}$'s gate by Miller coupling through the gate-drain capacitance (C_{gd}), causing a rise in OL which can partially or fully turn-ON $\mathrm{Q_L}$ [36]. This leads to shoot-through currents and consequent power losses severely degrading the efficiency as F_{sw} increases, as shown in Fig. 25. Quantifying such losses is challenging due to its dependence on several factors, including PCB parasitics, V_g value, slew rate of V_{sw}, in addition to $\mathrm{Q_L}$'s threshold voltage, speed, and its C_{gd} value. A possible solution is to replace the unipolar driving scheme with bipolar or three-level gate driving architectures [37], [38].

Fig. 25 presents the measured efficiency of the buck converter system versus F_{sw} (ranging from 0.5 to 3 MHz) at P_{out} of 4 W ($R_{\mathrm{L}} = 80\ \Omega$). The figure has two curves, each corresponding to one of the two modes, FDTG and SDTG. As F_{sw} increases, the overall system's efficiency decreases, mainly due to the impact of P_{sw} including the partial turn-ON losses explained above. At F_{sw} smaller than 0.75 MHz, both modes achieved almost similar efficiencies. However, as F_{sw} rises above 1 MHz, the efficiency curve for the FDTG mode deteriorates more rapidly and significantly compared to the SDTG curve. This divergence between the two curves is attributed to the increased susceptibility of the FDTG mode to cross-conduction and higher P_{sw}. The SDTG mode improved the efficiency by 5% at F_{sw} of 1 MHz and by 20% at F_{sw} of 2 MHz compared to the FDTG mode. Notably, measurements of the system's efficiency in the higher frequency range (>2.5 MHz) were unsuccessful for the FDTG mode, as $\mathrm{Q_L}$ in the HB suffered damage, as highlighted in the left bottom corner of Fig. 25. This damage may be due to the fixed DT realized by the FDTG mode, which becomes increasingly inadequate as F_{sw} increases. On the other hand, the SDTG mode demonstrates a more robust performance at higher frequencies, as it can adapt its DT to account for varying propagation delays and it can minimize the risk of cross-conduction.

Table IV summarizes the measured performance of the buck converter operated using the fabricated GD and compares it to the performance of similar state-of-the-art works. The buck system achieves a peak power efficiency of 90.5%, at F_{sw} of 500 kHz and P_{out} of 8 W ($R_{\mathrm{L}} = 40\ \Omega$), which is comparable to previously reported results. Notably, the proposed GD occupies the smallest area (0.285 $\mathrm{mm^2}$) which is two times smaller than the smallest GD's area reported among prior designs in [2]. In addition, when operating in the SDTG mode, the GD achieves the shortest DT value of 3.6 ns, which is three times lower compared to the lowest value in considered prior works (10.8 ns). The figure-of-merit, $\mathrm{FOM_1}$, proposed in [2] and expressed by (10), is adopted for comparison with other works. A lower $\mathrm{FOM_1}$ value indicates the attainment of shorter DT and higher efficiency. Our system outperforms other works by achieving $\mathrm{FOM_1}$ of 0.04, which is one order of magnitude lower than the lowest previously reported value. In addition, the proposed SDTG can adapt to PVT variations, device mismatches, and load and supply changes, all while providing the shortest possible DT. As a result, this enhances the efficiency and reliability of the entire system. A second figure of merit, $\mathrm{FOM_2}$, which combines the area of the DTG circuit with the shortest DT value achieved as expressed in (11), is proposed to quantify the complexity of the implemented DTG among the different works. As shown in Table IV, our design achieves the lowest $\mathrm{FOM_2}$, lower by an order of magnitude when compared to other works. This reflects the simplicity of our implementation without the need for complex detection circuits or additional passive components such as in [7] and [5]. Note that the feature size of the process node is included in the denominator of $\mathrm{FOM_2}$ to normalize the

TABLE IV
SWITCHED-MODE POWER SYSTEM PERFORMANCE SUMMARY AND COMPARISON

Reference	JSSC 2015 [7]	JSSC 2015 [39]	TPEL 2016 [5]	TCAS-I 2022 [10]	TCAS-I 2023 [2]	**This work**
Topology	Class-D	Buck	Buck	Buck	Class-D	Buck
Process	SOI 0.14 μm	CMOS 0.5 μm	CMOS 0.35 μm	CMOS 0.35 μm	CMOS 0.35 μm	SOI 0.18 μm
Half-bridge (Power Transistors)	On-chip (MOSFET)	On-chip (MOSFET)	Off- chip (GaN)	Off- chip (GaN)	On- chip (MOSFET)	Off- chip (GaN)
Power Supply (V)	80	40	45	45	24	36
Frequency (MHz)	0.15 – 0.55	0.5	0.1	1	0.5	0.5 - 1
Load	12 Ω	60 Ω	3.33 Ω - 40 Ω	100 Ω	100 mH + 342.5 Ω	40 Ω - 900 Ω
DTG Area (mm^2)	0.55[a]	0.332[a]	0.22	0.0126	0.066	0.046[b]
GD Area (mm^2)	1.286[a]	1.15	1.5	Off-Chip (LM5113)	0.401	0.285
Half-bridge C_{load} (pF)	2000[a]	500	240	140	17	288
Peak efficiency (η)	91% @P_{out} = 45 W @I_o = 1.95 A	94.9% @P_{out} = 6 W @I_o = 250 mA	95% @P_{out} = 13 W @I_o = 1.2 A	82% @P_{out} = 4.41 W @I_o = 210 mA	95.1% @P_{out} = 1.2 W @I_o = 60 mA	90.5% @P_{out} = 8 W @I_o = 450 mA
Shortest dead-time (ns)	100	25	15	35	10.8	3.6
FOM_1[c] (ns/%)	1.1	0.263	0.158	0.427	0.114	**0.04**
FOM_2[c] ($\frac{ns * mm^2}{\mu m}$)	393	16.6	9.429	1.26	2.037	**0.56**[d]
FOM_3[c] ($\frac{ns}{\% * MHz * nF}$)	1	1.054	6.58	3.05	13.36	**0.276**

[a] Estimated Value, [b] DTG area (0.046) = 0.018 (FDTG) + 0.028 (SDTG), [c] FOM_1, FOM_2, and FOM_3 are in (10-12) [d] Area of SDTG (0.028 mm^2) is used in the calculation.
Bold entities either signify the values where our design is better (superior) than the literature, or they represent the comparison points.

comparison between integrated areas in different technologies. Finally, a third figure of merit, FOM_3, is proposed in (12) for a more reasonable and fairer efficiency-based comparison to other works. This FOM_3 modifies FOM_1 by incorporating other metrics (F_{sw} and C_{load}) that influence the switching power and body-diode losses, consequently impacting the efficiency calculation, as explained in [7] and [10]. Our buck converter system achieves the lowest FOM_3 in comparison to all considered other works in the literature. It is also notable from the trend in Fig. 23 that our system's efficiency is expected to be higher for higher output power loads.

$$\mathrm{FOM}_1\left(\frac{\mathrm{ns}}{\%}\right) = \frac{\text{Shortest Deadtime (ns)}}{\text{Efficiency (\%)}} \tag{10}$$

$$\mathrm{FOM}_2\left(\frac{\mathrm{ns}*\mathrm{mm}^2}{\mu\mathrm{m}}\right) = \frac{\text{Shortest Deadtime (ns)} * \text{DTG Area } \left(\mathrm{mm}^2\right)}{\text{Process Node } (\mu\mathrm{m})} \tag{11}$$

$$\mathrm{FOM}_3\left(\frac{\mathrm{ns}}{\%*\mathrm{MHz}*\mathrm{nF}}\right) = \frac{\text{Shortest Deadtime (ns)}}{\text{Efficiency (\%)} * \mathrm{F_{sw}\,(MHz)} * \mathrm{C_{load}\,(nF)}}. \tag{12}$$

V. CONCLUSION

In conclusion, this article presented a half-bridge (HB) gate driver (GD) for switched-mode power systems (SMPSys) featuring two distinct dead-time (DT) control modes and open-drain outputs with electrostatic discharge (ESD) self-protection. The first mode was an externally tunable fixed dead-time generator (FDTG) offering a wide range of DTs from 5 to 200 ns. The second mode was a self-adjusting dead-time generator (SDTG) featuring adaptive capabilities against propagation delay mismatches (DMs) and protection against shoot-through currents. Detailed timing analysis and design procedures were presented for each block of the proposed GD. The GD circuit was implemented in high-voltage (HV) 0.18-μm silicon-on-insulator (SOI) technology characterized by a compact size with a core area of 0.285 mm^2. Its performance was evaluated experimentally by employing it in a synchronously switching buck converter system with an HB composed of two e-GaN power transistors. The buck system achieved a peak efficiency of 90.5% at an output power load of 8 W. Measurement results validated the advantages of the SDTG mode in terms of reduced propagation delays (< 13.6 ns) and minimized DTs (< 5.2 ns), contributing to an overall system efficiency improved by up to 20% compared to using the FDTG mode. In addition, the SDTG mode showed robust performance at higher frequencies, adapting to PVT variations, as well as device mismatches, and load/line changes, preventing cross-conduction and enhancing the efficiency and reliability of the entire system. Moreover, our system's performance surpassed all the considered similar works in the literature, excelling across various figures of merit, thereby establishing the proposed GD as a highly compelling solution for high-performance SMPSys. Finally, future work could explore the integration of bipolar or three-level gate-driving architectures to further enhance the system's efficiency and robustness, particularly at higher switching frequencies. In addition, we can modify the delay circuit in the FDTG block to generate more accurate DTs.

ACKNOWLEDGMENT

The authors would like to acknowledge the access to CAD tools and fabrication technologies provided by the Canadian Microelectronics Corporation (CMC) Microsystems. The authors would also like to acknowledge the valuable comments received from Prof. Benoit Gosselin (ULaval) to enhance this article.

REFERENCES

[1] M. Ali et al., "A versatile SoC /SiP sensor interface for industrial applications : Implementation challenges," *IEEE Access*, vol. 10, pp. 24540–24555, 2022, doi: 10.1109/ACCESS.2022.3152379.

[2] A. Abuelnasr et al., "Delay mismatch insensitive dead time generator for high-voltage switched-mode power amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 4, pp. 1555–1565, Apr. 2023, doi: 10.1109/TCSI.2022.3232074.

[3] M. Amer et al., "Fully integrated dual-channel gate driver and area efficient PID compensator for surge tolerant power sensor interface," in *Proc. IEEE 18th Int. New Circuits Syst. Conf.*, 2020, pp. 166–169, doi: 10.1109/NEWCAS49341.2020.9159789.

[4] RTCA, Inc., "Environmental conditions and test procedures for airborne equipment," RTCA, Inc., Washington, DC, USA, RTCA/DO-160F, 2007.
[5] R. Grezaud, F. Ayel, N. Rouger, and J. C. Crebier, "A gate driver with integrated deadtime controller," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8409–8421, Dec. 2016, doi: 10.1109/TPEL.2016.2517679.
[6] A. Lidow, M. de Rooij, J. Strydom, D. Reusch, and J. Glaser, *GaN Transistors for Efficient Power Conversion*. Hoboken, NJ, USA: Wiley, 2019.
[7] H. Ma, R. Van Der Zee, and B. Nauta, "A high-voltage class-D power amplifier with switching frequency regulation for improved high-efficiency output power range," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1451–1462, Jun. 2015, doi: 10.1109/JSSC.2015.2421994.
[8] J. Wittmann, A. Barner, T. Rosahl, and B. Wicht, "An 18 V input 10 MHz buck converter with 125 ps mixed-signal dead time control," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1705–1715, Jul. 2016, doi: 10.1109/JSSC.2016.2550498.
[9] D. C. Mode, "Modelling of SEPIC, cuk and zeta converters in discontinuous conduction mode and performance evaluation," *MDPI Sensors*, vol. 21, 2021, Art. no. 7434.
[10] M. Karimi, M. Ali, A. Hassan, M. Sawan, and B. Gosselin, "An active dead-time control circuit with timing elements for a 45-V input 1-MHz half-bridge converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 1, pp. 30–41, Jan. 2022, doi: 10.1109/TCSI.2021.3096522.
[11] D. Liu, S. J. Hollis, and B. H. Stark, "A new design technique for sub-nanosecond delay and 200 V/ns power supply slew-tolerant floating voltage level shifters for GaN SMPS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 3, pp. 1280–1290, Mar. 2019, doi: 10.1109/TCSI.2018.2878668.
[12] A. Niwa et al., "A dead-time-controlled gate driver using current-sense FET integrated in SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3258–3267, Apr. 2018, doi: 10.1109/TPEL.2017.2704620.
[13] M. Berkhout and L. Dooper, "Class-D audio amplifiers in mobile applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 5, pp. 992–1002, May 2010, doi: 10.1109/TCSI.2010.2046200.
[14] T. Lopez, G. Sauerlaender, T. Duerbaum, and T. Tolle, "A detailed analysis of a resonant gate driver for PWM applications," in *Proc. 18th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2003, pp. 873–878, doi: 10.1109/APEC.2003.1179319.
[15] L.-F. Shi, F.-B. Liu, H.-S. He, X.-Y. Mao, and X.-Q. Lai, "Design of adaptive dead-time control circuit for resonant half-bridge driver," *Int. J. Electron.*, vol. 100, no. 10, pp. 1317–1331, 2013, doi: 10.1080/00207217.2012.743084.
[16] L. Cong, J. Xue, and H. Lee, "A 100V reconfigurable synchronous gate driver with comparator-based dynamic dead-time control for high-voltage high-frequency DC-DC converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 2007–2010, doi: 10.1109/APEC.2015.7104623.
[17] J. Xue, K. D. T. Ngo, and H. Lee, "A 99%-efficiency 1-MHz 1.6-kW zero-voltage-switching boost converter using normally-off GaN power transistors and adaptive dead-time controlled gate drivers," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits*, 2013, pp. 31–32.
[18] X. Mu, S. Member, G. Zhao, and S. Member, "Floating-domain integrated GaN driver techniques for DC–DC converters : A review," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 70, no. 9, pp. 3790–3805, Sep. 2023, doi: 10.1109/TCSI.2023.3288871.
[19] W. Yan, C. Pi, W. Li, and R. Liu, "Dynamic dead-time controller for synchronous buck DC-DC converters," *Electron. Lett.*, vol. 46, no. 2, pp. 164–165, 2010, doi: 10.1049/el.2010.2651.
[20] B. T. Yeh, C. H. Yang, K. C. Juang, and C. H. Tsai, "Sensorless dead-time exploration for digitally controlled switching converters," in *Proc. IEEE Int. Symp. VLSI Des., Autom., Test*, 2013, pp. 4–7, doi: 10.1109/VLDI–DAT.2013.6533802.
[21] M. Karimi et al., "A versatile non-overlapping signal generator for efficient power-converters operation," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2020, pp. 1–5, doi: 10.1109/ISCAS45731.2020.9180718.
[22] A. Abuelnasr et al., "Self-adjusting deadtime generator for high-efficiency high-voltage switched-mode power amplifiers," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2020, pp. 2–6, doi: 10.1109/iscas45731.2020.9181166.
[23] M. C. W. Høyerby, M. A. E. Andersen, and P. Andreani, "A 0.35μm 50V CMOS sliding-mode control IC for buck converters," in *Proc. IEEE 33rd Eur. Solid-State Circuits Conf.*, 2007, pp. 182–185, doi: 10.1109/ESSCIRC.2007.4430275.
[24] X. Zhang and Z. Zhao, "Model predictive control for PMSM drives with variable dead-zone time," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 10514–10525, Sep. 2021, doi: 10.1109/TPEL.2021.3066636.
[25] Y. Moghe, T. Lehmann, and T. Piessens, "Nanosecond delay floating high voltage level shifters in a 0.35 μm HV-CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 485–497, Feb. 2011, doi: 10.1109/JSSC.2010.2091322.
[26] S. Havanur, "Optimizing dead time selection in ZVS topologies," *Power Electron. Technol.*, vol. 38, no. 6, pp. 22–25, 2012.
[27] S. Dongaonkar, S. P. Mudanai, and M. D. Giles, "From process corners to statistical circuit design methodology: Opportunities and challenges," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 19–27, Jan. 2019, doi: 10.1109/TED.2018.2860929.
[28] C. Cockrill, "Understanding Schmitt triggers," Texas Instruments Incorporated, Dallas, TX, USA, Appl. Rep. SCEA046, 2011. [Online]. Available: www.ti.com, Accessed: Apr. 8, 2019.
[29] R. Jacob Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd ed. Hoboken, NJ, USA: Wiley, 2010.
[30] D. Liu, S. J. Hollis, H. C. P. Dymond, N. McNeill, and B. H. Stark, "Design of 370-ps delay floating-voltage level shifters with 30-V/ns power supply slew tolerance," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 63, no. 7, pp. 688–692, Jul. 2016, doi: 10.1109/TCSII.2016.2530902.
[31] J. Strydom, D. Reusch, S. Colino, and A. Nakata, "Using enhancement mode GaN-on-silicon power FETs," *Proc. Int. Soc. Magn. Reson. Med.*, vol. 22, 2017, Art. no. 926.
[32] A. I. Colli-Menchi and S. Sánchez-Sinencio, "A high-efficiency self-oscillating class-d amplifier for piezoelectric speakers," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5125–5135, Sep. 2015, doi: 10.1109/TPEL.2014.2363406.
[33] J. Strydom and D. Reusch, "Dead-time optimization for maximum efficiency," EPC – Power Convers. Technol. Leader, White Paper WP012, 2013. [Online]. Available: www.epc-co.com
[34] Efficient Power Conversion Corporation (EPC), "Development Board EPC9014 Quick Start Guide: 200V Half Bridge With Gate Drive, Using EPC2019," Efficient Power Convers. Corporation, 2014.
[35] J. Strydom and D. Reusch, "Gallium nitride (GaN) FET drivers and controllers," Efficient Power Convers. Corporation, 2023. [Online]. Available: https://epc-co.com/epc/products/gan-drivers-and-controllers, Accessed: Oct. 28, 2023.
[36] H. Ma, R. van der Zee, and B. Nauta, "Design and analysis of a high-efficiency high-voltage class-D power output stage," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1514–1524, Jul. 2014, doi: 10.1109/JSSC.2014.2317780.
[37] A. Seidel and B. Wicht, "Integrated gate drivers based on high-voltage energy storing for GaN transistors," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3446–3454, Dec. 2018, doi: 10.1109/JSSC.2018.2866948.
[38] D. Luo, Y. Gao, and P. K. T. Mok, "A GaN driver for a bidirectional buck/boost converter with three-level VGS protection and optimal-point tracking dead-time control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 5, pp. 2212–2224, May 2022, doi: 10.1109/TCSI.2022.3146190.
[39] Z. Liu, L. Cong, and H. Lee, "Design of on-chip gate drivers with power-efficient high-speed level shifting and dynamic timing control for high-voltage synchronous switching power converters," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1463–1477, Jun. 2015, doi: 10.1109/JSSC.2015.2422075.

Mostafa Amer received the B.Sc. degree in nanotechnology and nanoelectronics engineering from the University of Science and Technology at Zewail City, Giza, Egypt, in 2018. He is currently working toward the Ph.D. degree with the Electrical Engineering Department, Polytechnique Montréal, Montreal, QC, Canada.

His Ph.D. research focuses on the design and optimization of controllers and gate drivers for efficient high-voltage dc–dc converters. His research interests include high-voltage mixed-signal analog integrated circuits, switching dc–dc converters, controller design, device modeling, artificial intelligence–based generative design, and simulation-based optimization.

Ahmed Abuelnasr received the B.Sc. degree in nanotechnology and nanoelectronics engineering from the University of Science and Technology at Zewail City, Giza, Egypt, in 2018. He is currently working toward the Ph.D. degree with the Electrical Engineering Department, Polytechnique Montréal, Montreal, QC, Canada.

His Ph.D. research focuses on the design of efficient high-voltage power amplifiers and developing advanced artificial intelligence-based tools for accelerating circuit design. His research interests include high-voltage mixed-signal analog integrated circuits, power amplifiers, dc–dc converters, deep learning, reinforcement learning, simulation-based optimization, and causality analysis.

Ahmad Hassan (Member, IEEE) received the Ph.D. degree in electrical engineering from Polytechnique Montréal, Montreal, QC, Canada, in 2019.

From 2019 to 2021, he was a Postdoctoral Fellow with the Polystim Neurotechnologies Laboratory, Department of Electrical Engineering, Polytechnique Montréal. From 2021 to 2022, he was a Postdoctoral Fellow with the Integrated Systems Laboratory, Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada. In 2023, he joined the Electrical Engineering Department, Polytechnique Montréal as an Assistant Professor. During his research, he contributed to various research and industrial projects and has authored more than 45 research papers in international journals and symposiums. His research focuses on emerging technologies, including integrated circuits for harsh environments and photonic computing. Dr. Hassan was a recipient of FRQNT Postdoctoral Research Scholarship.

Ahmed Ragab received the Ph.D. degree in industrial engineering from Polytechnique Montréal, Montreal, QC, Canada, in 2014.

He is currently a Scientist in artificial intelligence (AI) with Natural Resources Canada (NRCan), Ottawa, ON Canada. He is also an Adjunct Professor with the Department of Mathematics and Industrial Engineering, Polytechnique Montréal. His research interests include AI, machine learning, pattern recognition, image processing, data and decision fusion, causality analysis, reliability modeling, operations research, discrete event systems, and process mining. At NRCan, he has worked on strategic projects funded by the Government of Canada, including forest value chain optimization and carbon capture, utilization, and storage. His main thematic activities focus on the practical challenges of Big Data and AI in several industrial applications, including abnormal events diagnosis and prognosis, predictive maintenance, supervisory control, real-time optimization, production scheduling, and systems design. He has a bunch of experience in developing advanced AI algorithms and tools in the manufacturing industry, aiming at reducing energy consumption, greenhouse gas emissions, and operational and maintenance costs while improving operation's performance. He also teaches industrial engineering courses at graduate levels and supervises M.Sc. and Ph.D. students.

Mohamad Sawan (Fellow, IEEE) received the Ph.D. degree in electrical engineering from Sherbrooke University Sherbrooke, QC, Canada, in 1990.

From 1991 to 2019, he led the Microsystems Strategic Alliance of Quebec. He is currently the Chair Professor, Founder, and Director of the Center for Biomedical Research and Innovation (CenBRAIN), Westlake University, Hangzhou, China. He is also an Emeritus Professor in microelectronics and biomedical engineering and the Founder and Director of the Polystim Neurotech Laboratory, Polytechnique Montréal, Montreal, QC, Canada. He supervised the thesis of more than 120 master's and 60 Ph.D. students. He authored or coauthored more than 800 peer-reviewed papers. He holds 12 patents, and his 11 other patents are pending.

Dr. Sawan is a Fellow of the Canadian Academy of Engineering, a Fellow of the Engineering Institute of Canada, and an Officer of Quebec's National Order. Since 2019, he has been the Vice-President of Publications of the IEEE CAS Society. He is the Founder of the IEEE Interregional NEWCAS Conference. From 2016 to 2019, he was the Co-Founder and Editor-in-Chief of IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS. He was the recipient of several awards, including the Queen Elizabeth II Golden Jubilee Medal, the Shanghai International Collaboration Award, the Bombardier Award for Technology Transfer, the Jacques-Rousseau Award, the Medal of Merit from the President of Lebanon, and the Barbara Turnbull Award for Spinal Cord Research in Canada.

Yvon Savaria (Life Fellow, IEEE) received the B.Ing. and MASc. degrees in electrical engineering from École Polytechnique Montréal, Montreal, QC, Canada, in 1980 and 1982, respectively, and the Ph.D. degree in electrical engineering from McGill University, Montreal, QC, Canada, in 1985.

Since 1985, he has been with Polytechnique Montréal, Montreal, QC, Canada, where he is currently a Professor with the Department of Electrical Engineering. He has carried out work in several areas related to microelectronic circuits and microsystems, such as testing, verification, validation, clocking methods, defect and fault tolerance, effects of radiation on electronics, high-speed interconnects, and circuit design techniques, CAD methods, reconfigurable computing and applications of microelectronics to telecommunications, aerospace, image processing, video processing, radar signal processing, and the acceleration of digital signal processing. He is currently involved in several projects related to embedded systems in aircraft, wireless sensor networks, virtual networks, software-defined networks, machine learning (ML), embedded ML, computational efficiency, and application-specific architecture design. He holds 16 patents, has authored or coauthored 205 journal papers and 490 conference papers, and has been the thesis advisor of 190 graduate students who completed their studies.

Dr. Savaria is a Fellow of the Canadian Academy of Engineering. He was the Program Co-Chairman of NEWCAS 2018 and the General Chairman of NEWCAS 2020. He was a consultant or sponsored for carrying out research with Bombardier, Buspass, CNRC, Design Workshop, Dolphin, DREO, Ericsson, Genesis, Gennum, Huawei, Hyperchip, Intel, ISR, Kaloom, LTRIM, Miranda, MiroTech, Nortel, Octasic, PMC-Sierra, Space Codesign, Technocap, Thales, Tundra, and Wavelite. He is the Codirector of the Regroupement Stratégique en Microélectronique du Québec and a member of the Ordre des Ingénieurs du Québec. In 2001, he was awarded a Tier 1 Canada Research Chair (www.chairs.gc.ca) on the design and architecture of advanced microelectronic systems that he held until June 2015. He was also the recipient of the Synergy Award from the Natural Sciences and Engineering Research Council of Canada in 2006. Since June 2019, he has been the NSERC-Kaloom-Intel-Noviflow Chair professor.