A Fast-Transient Radiation-Tolerant LDO-cum-Latching Current Limiter

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***Abstract*—The low-dropout regulator (LDO) and the latching current limiter (LCL) are two important constituent components of the power management system in satellites, including for the impending 6G satellite communications. In this article, we present a fast-transient radiation-tolerant LDO-cum-LCL realized in CMOS (vis-à-vis III/V or BiCMOS exotic processes). The LCL therein detects load current anomalies, thereby protecting the load against current anomalies (when the load suffers from single-event-latch-up, a radiation effect). The fast-transient response is realized by our proposed triple-feedforward-path technique that is efficacious over wide range of load currents (up to 3A) and off-chip capacitors (100 to 880 μF). The LDO-cum-LCL is monolithically realized in a 130 nm CMOS process. The dropout voltage is 210 mV at the full load, and the overshoot and undershoot are 14.2 and 11.8 mV, respectively, at fast 3A load transitions. The load regulation is 0.15 mV/A while the power supply rejection is −52.3 dB@100 kHz. These parameters of the LDO-cum-LCL are very competitive when benchmarked against reported LDOs, albeit the reported LDOs not featuring radiation tolerance.**

***Index Terms*—Fast transient, feedforward compensation, latching current limiter (LCL), load current anomalies protection, loop stability, low-dropout regulator (LDO), radiation-tolerance.**

I. Introduction

With the integration of satellite communications with terrestrial communication networks in the impending next-generation 6G communications [1], advanced commercially-off-the-shelf CMOS-based ICs [e.g., field programmable gate arrays (FPGAs) and system-on-chips (SoCs)] are increasingly applied in satellites. This is congruous with the evolution from "Traditional Space" to the present "New Space" [2].

Generally, state-of-the-art FPGAs and SoCs demand increasingly "more robust" power supplies. For example, the Xilinx radiation-tolerant Kintex UltraScale FPGA specify the tolerance of 2% for its integrated high-speed serial transceiver's supply voltage [3]. Furthermore, with the trend of the multiprocessor integration [4], [5], the ensuing high load current (large load current variations of >1A) and complex in-situ functionalities present challenges to the power management circuit. In the case of an application in satellites, the power management circuit would need to be at least tolerant to radiation effects, i.e., featuring radiation-tolerance, particularly against microsingle-event-latch-ups (μ-SELs) and SELs [6], [7].

The power management circuit includes the switching regulator and linear regulator, e.g., the low-dropout regulator (LDO). Although (buck) switching regulators are generally more power efficient particularly when the ratio of V_{IN}/V_{OUT} is large, they require large inductors resulting in a large form factor and heavy weight, both of which may not be acceptable. They also suffer from significant output ripples that would degrade the performance of ripple-sensitive analog and RF blocks in FPGAs or SoCs [4], [8], [9]. In contrast, the LDO could provide a "clean" power supply without ripples and respond quickly to load changes. Meanwhile, due to the relatively simple structure of the LDO, the corresponding smaller die area reduces the probability of being affected by radiation effects [10].

To provide a "clean" power supply to accommodate large load current variations, an LDO with a large off-chip capacitor is more appropriate than its capless counterpart. This is because an off-chip capacitor can sink or source sudden transient currents [5], [11], [12]. Furthermore, a large capacitor would also enhance radiation tolerance [12], [13]. Nevertheless, given that our target FPGAs or SoCs feature high load current (>1A), the necessary extremely large off-chip capacitors (up to 220 μF) would pose stability challenges, especially over wide load current range, e.g., 3A in this design. Meanwhile, the typically limited unity gain bandwidth (UGB) would negatively affect its power supply rejection.

A plethora of LDOs with off-chip capacitors that feature fast-transient response has been reported. For example, a reported design [8] implemented multiple dynamic feedback loops while another [14] introduced a left-half-plane zero through the feedforward path to accelerate the transient response. However, the load currents in these designs are small – only 100s of milliamperes which is insufficient for many advanced contemporary FPGAs and SoCs. Although several reported LDOs [4], [5] can supply load current exceeding 1A, their overshoot/undershoot for large load current variations (e.g., 3A) do not meet the 2% overshoot/undershoot specifications of contemporary FPGAs

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and SoCs. Furthermore, all these reported LDOs do not feature radiation tolerance.

Put simply, there is a need for an LDO (with a large off-chip capacitor) that is both radiation tolerant and accommodates the fast-transient stringent requirements of contemporary FPGAs and SoCs.

In addition, the LDO needs to be radiation tolerant, particularly against μ-SELs and SELs occurring in the load [7]. An SEL is an event where when an ionizing particle strikes a semiconductor, the semiconductor draws an abnormally high current, often rendering the semiconductor device nonfunctional, and in some cases, the ensuing damage is permanent. The μ-SEL, on the other hand, is a more localized version of the SEL and the abnormal current is typically lower. μ-SELs and SELs typically compromise the operating lifetime of the semiconductor.

The commonly adopted protection circuit against the current anomalies in the load connected to the LDO is the latching current limiter (LCL). The modus operandi of the LCL is to simply clamp the load current to a "safe" value when anomalies are sensed [15], [16]. In addition to the usual modus operandi of the LCL, the European standards [17] recommends that a trip-off timer that counts the anomaly time and a restart trigger that resets the complete system be augmented as part of the protection mechanism. To date, this recommendation is yet to be realized in any radiation-tolerant LCL.

In this article, we propose a full-CMOS fast-transient radiation-tolerant LDO-cum-LCL designed for contemporary FPGAs and SoCs and embodying the European standards – this integration of the LDO and LCL is beneficial to protect load circuits in space electronic payloads from radiation effects, yet with small IC area and potentially lower cost due to the integration. Its fast-transient response is realized with an off-chip 220 μF tantalum polymer capacitor and from the implementation of our proposed triple-feedforward-path (TFF) technique. This proposed technique is effective over the entire load current range, i.e., from 0 to 3A, hence applicable to the impending 6G communications. The protection against loading radiation effects is obtained by a module-level radiation-hardened-by-design (RHBD) technique [18].

The proposed LDO-cum-LCL is monolithically realized in a commercial 130 nm CMOS process. To realize radiation-tolerance, particularly to ensure self-robustness against μ-SELs and SELs, the LDO is designed with wide guard rings and with deep N-wells. The minimum output is 0.8 V, designed for the internal supply voltage of an FPGA, and the dropout voltage is 210 mV. When 3A load variation occurs with 400 ns rising/falling times, the overshoot and undershoot are 14.2 mV and 11.8 mV, respectively, thereby satisfying the stringent 2% requirement of contemporary FPGAs and SoCs. The load regulation is 0.15 mV/A, the power supply rejection at 100 kHz is -52.3 dB while the maximum current efficiency is 99.5%. When the load current anomalies are emulated at the load, the LCL functionality of the LDO-cum-LCL is effective to protect the load from in-rush current damage, and it can reset the load system when the anomaly is recognized as a permanent error. The LCL also embodies European standards.

The rest of this article is organized as follows. Sections II and III elaborate the design details of our proposed LDO-cum-LCL. The measurement results are presented in Section IV to demonstrate the merits of our design and are benchmarked against reported designs. Of particular note, our design is not only highly competitive but also radiation-tolerant while the reported designs are not. Finally, Section V draws the conclusion.

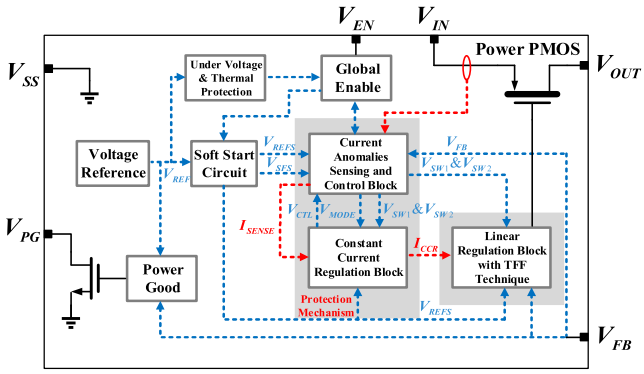

Fig. 1. Block diagram of the proposed fast-transient LDO-cum-LCL with load current anomalies protection.

II. System Overview

The block diagram of the proposed fast-transient LDO-cum-LCL is illustrated in Fig. 1. The power PMOS transistor is controlled by the linear regulation block where our proposed TFF technique is employed to enhance the transient response. The proposed protection mechanism by the embodied LCL protects the load from the current anomalies by continuously monitoring the load current. It consists of a current anomalies sensing and control block and a constant current regulation block.

As the power PMOS is realized by the 20 V laterally diffused MOSFET (LDMOS), it can accommodate the various power and voltage requirements in the satellite, e.g., V_{IN} >12 V. The minimum V_{IN} is 2.4 V, which is determined by the constant-transconductance biasing circuit in the system, to ensure the correct working condition of inner functional blocks. The output voltage (V_{OUT}) is normally 0.8 V to power the internal processors in the FPGA while the reference voltage (V_{REF}) generated by the on-chip voltage reference is 0.6 V [19]. The LDO can operate in the low dropout region with the dropout voltage of 210 mV at a load current of 3A.

III. Circuit Design and Analysis

A. Linear Regulation Block With TFF Technique

Fig. 2 depicts the schematic of our proposed LDO regulated by the linear regulation block. For convenience of analysis, the power PMOS (*MPP*), and the fundamental off-chip components, including the resistive feedback divider (R_{F1} and R_{F2}), loading capacitor (C_L) and the satellite load, are included where a complete feedback loop is constructed. The high precision off-chip resistors, R_{F1} and R_{F2}, not only provide flexibility for defining V_{OUT} during testing, but also slightly reduce on-chip heat dissipation. A simple linear voltage regulator (grey shaded box in the middle of the top of Fig. 2) is adopted to

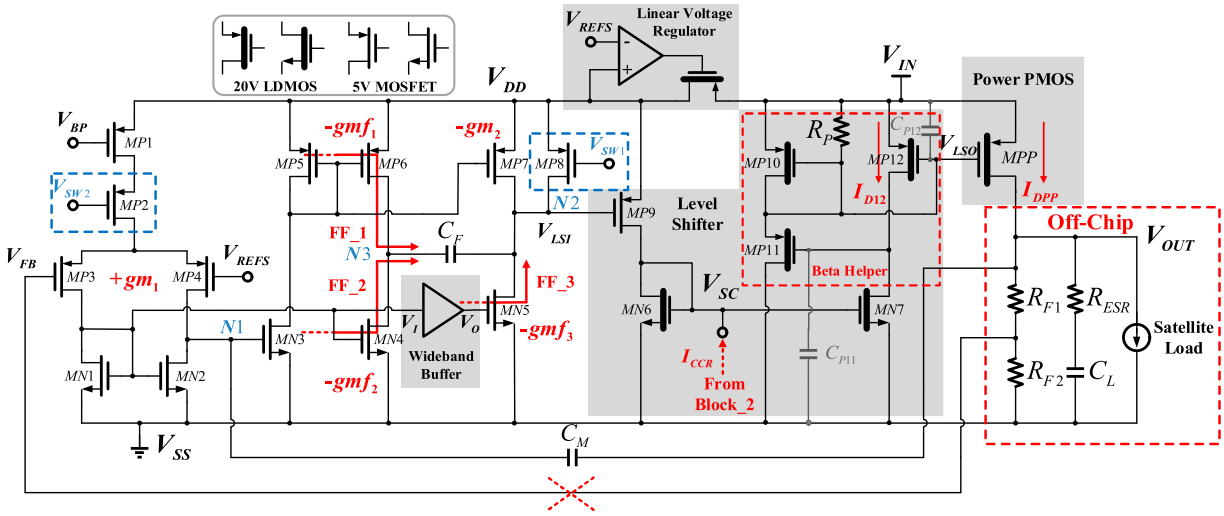

Fig. 2. Schematic of the proposed fast-transient LDO-cum-LCL regulated by the linear regulation block.

power the core control circuit with a constant supply voltage, i.e., V_{DD}, from V_{IN}. This is beneficial to enhance the power supply rejection (PSR) of our proposed LDO and to reduce the risk of damage to V_{DD} from the potential high voltage spike at V_{IN}.

The proposed TFF technique is applied to the core control circuit (the linear regulation block) where *MP*6, *MN*4, and *MN*5 serve as three high-gain transconductors. The transconductors provide three feedforward paths, denoted as FF_1 to FF_3 in Fig. 2. When an output variation happens due to the load changes or the current anomalies due to radiation, these paths will respond to generate substantial transient current to charge or discharge the input of the level shifter (V_{LSI}). Amongst the three feedforward paths, the FF_1 and FF_2 traverse an ac-coupling capacitor, C_F. Hence, only the high-frequency gain will be augmented that is beneficial for the UGB extension without sacrificing the loop stability [20]. A high-gain wideband buffer is inserted into the FF_3 to further extend the UGB by the augmentation of an additional left-half-plane zero.

With respect to large signal performance, the proposed TFF technique enhances the slew rate at V_{LSI} due to the double push-and-pull structure (*MP*6, *MN*4, *MP*7, and *MN*5).

In short, both the wide UGB and high slew rate are two dominant factors that facilitate the fast-transient response and small-scale variations at the LDO output [8], [21], [22].

*MP*2 and *MP*8 serve as the switches that work in cooperation with the protection mechanism and are responsible for the power PMOS control switching – see Section III-B. In default, the LDO is under the linear regulation with *MP*2 and *MP*8 ON and OFF, respectively.

1) Wideband Level Shifter With Beta Helper Implementation: To bridge the core control circuit and the *MPP* from two distinctive power domains, we design a level shifter constructed by 20 V LDMOS in Fig. 2. For current mirrors, the aspect ratio (*W*/*L*) of *MN*7 is 3× of *MN*6 while the *W*/*L* of *MP*10 is 2× of *MP*12. For high power efficiency, the size proportion between *MPP* and *MP*12 (K_P) is defined to be 640, so the power efficiency is 99.5% at the full load condition; this is comparable to prevalent LDOs [5], [12], [13], [23].

One major issue of this level shifter is the potential instability caused by the low-frequency pole at V_{LSO} that originates from *MPP*'s large parasitic capacitance. To mitigate this, we construct a beta helper structure into the level shifter. This configuration of the beta helper [24] was initially utilized to reduce the systematic error in the bipolar transistor circuits but can also be effective to extend the bandwidth in CMOS circuits [25]. In Fig. 2, negative feedback is established by *MP*10 to *MP*12 and R_P. We ascertained that the ensuing small-signal current gain ($A_i(s)$) from the drain current of *MP*12 (I_{D12}) to that of *MPP* (I_{DPP}) is

$$A_i(s) \approx \frac{K_P(gm_{11}ro_{12}gm_{12}R)}{s^2C_{P11}C_{P12}ro_{12}R+sC_{P11}ro_{12}(1+gm_{11}R)+gm_{11}ro_{12}gm_{12}R} \quad (1)$$

where gm_i, ro_i, and C_{Pi} are the transconductance, the drain resistance, and the lumped gate parasitic capacitance of *MPi*, respectively, and $R = R_P/(1+gm_{10}R_P)$.

It can be inferred that the low frequency pole is improved by a gain that is equal to $\sqrt{gm_{11}C_{P12}/gm_{12}C_{P11}}$. In order to ensure adequate gain, gm_{11}/gm_{12} must be high enough under all load current circumstances. When the load current is high, *MP*11 and *MP*12 operate in the saturation region, and gm_{11}/gm_{12} is proportional to $\sqrt{K_D(W/L)_{11}/(W/L)_{12}}$ where K_D is the current ratio between *MP*10 and *MP*12 and is equal to 2. Since $(W/L)_{11}/(W/L)_{12}$ is designed to be 16, gm_{11}/gm_{12} is equal to ∼5.7. However, when the load current descends below 20 mA, *MP*11 and *MP*12 will enter the subthreshold region and the ensuing gm_{11}/gm_{12} will degrade to K_D which is impertinent of the size ratio. Hence, to ascertain a minimum biasing current to *MP*11, we add R_P in parallel with *MP*10. This ensures a sufficiently high gm_{11} at the no load condition. Note that R_P can be ignored when the LDO drives heavy load. This is because of the somewhat high gm_{10}. Furthermore, R_P provides the flexibility to ascertain the damping factor in (1) to circumvent complex poles.

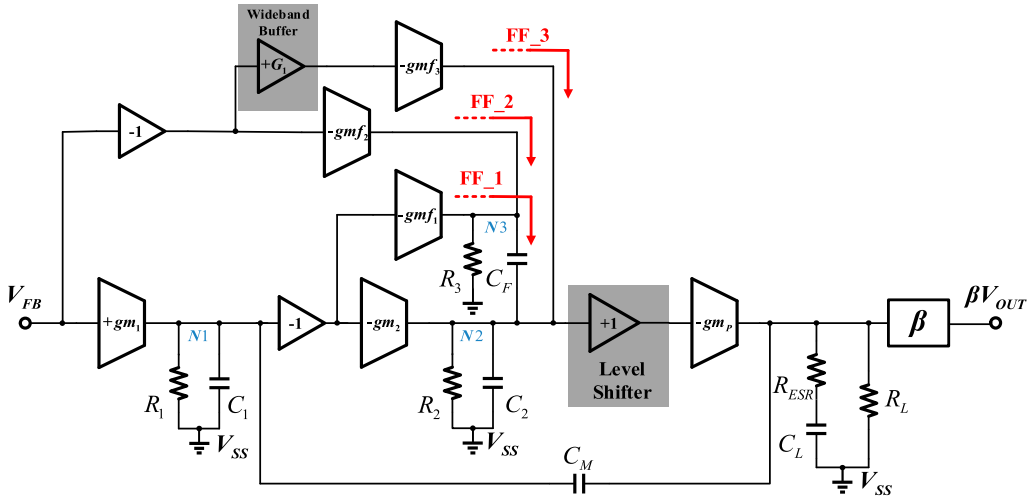

Fig. 3. Small-signal model of the proposed LDO-cum-LCL regulated by the linear regulation block.

From simulations, with the beta helper, we ascertain that the 3-dB bandwidth of the level shifter is advantageously extended from 5.1 to 67.9 MHz at full load condition while from 10.1 to 406.0 kHz at no load condition. The respective bandwidth improvements are 22.5 and 32.1 dB. The added ∼10 dB gain at the no load condition is largely attributed to the deployment of R_P. This added gain is advantageous because degradation of the bandwidth under this condition would seriously jeopardize the stability of the overall LDO.

2) Stability Analysis: We depict in Fig. 3, the equivalent small-signal model of the proposed LDO which is regulated by the linear regulation block. The broken node is at the feedback path from the resistive divider (the feedback factor is β) which is marked as a red-cross in the bottom of Fig. 2.

Since the bandwidth of the level shifter is effectively widened by the proposed beta helper, it is modeled as a simple unity-gain buffer that drives the power PMOS directly. In Fig. 3, gm_1, gm_2, and gm_P represent the transconductances of two gain stages and power PMOS in the main loop, respectively. gmf_1 to gmf_3 represent the transconductances of three feedforward paths. G_1 is a high-gain wideband buffer in the FF_3 to further enhance the transient performance of the LDO. R_i and C_i represent the equivalent resistance and lumped capacitance at the node of N_i annotated in both Figs. 2 and 3, respectively. C_F and C_M are the ac-coupling capacitor and Miller capacitor, respectively. R_{ESR} and R_L emulate the equivalent series resistance of the practical tantalum polymer capacitor, C_L, and the satellite load.

The detailed schematic of G_1 is depicted in Fig. 4. Two identical channel-length-insensitive small-gain structures [14], [26] are implemented therein to provide high gain without introducing low-frequency poles below the UGB. *MP*17 and *MP*18 biased by V_{REFS} (same to V_{REF} from the soft start circuit) guarantee the same dc level of V_I and V_O. Hence, $G_1 = k^2$ where k is the biasing current ratio and designed to be 3 in order to avoid complex poles [26]. From simulations, the 3-dB bandwidth is ascertained to be 75.5 MHz, with G_1 equal to 18.8 dB. This means that its application will not complicate the loop stability analysis.

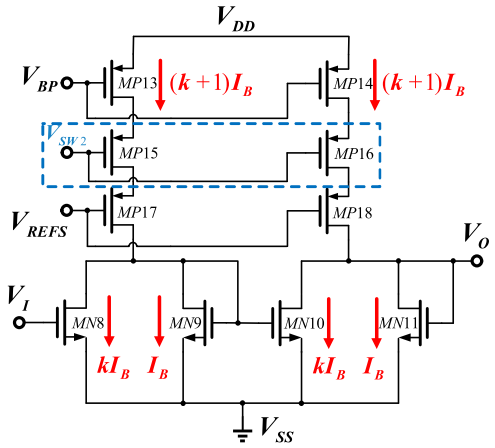

Fig. 4. Schematic of the wideband buffer in the feedforward path FF_3.

In the small-signal model in Fig. 3, we note the following.

a) Capacitance relationship: $C_L \gg C_M > C_F > C_2 \gg C_1$.
b) Resistance relationship: $R_1 = R_2 = 3R_3$.
c) Transconductance relationship: $gm_2 \approx gmf_3$, $gmf_1 \approx gmf_2$.
d) The dc gain of each stage is $\gg 1$.

With the aforesaid, we derive the overall loop transfer function expressed in (2) with the dc loop gain of A_{dc}.

$$T(s) = \frac{\beta V_{OUT}}{V_{FB}} = -\frac{A_{dc}\left(1+sC_LR_{ESR}\right)\left(1+a_1s+a_2s^2+a_3s^3\right)}{\left(1+b_1s+b_2s^2+b_3s^3+b_4s^4\right)} \tag{2}$$

where

$$A_{dc} = (gm_1R_1gm_2 + G_1gmf_3)R_2gm_PR_L\beta \tag{3}$$

$$a_1 = C_F(gm_2 + gmf_1)R_3/gm_2 \tag{4}$$

$$a_2 = C_MC_F(G_1gmf_3 + gmf_2)R_3/gm_1gm_2 \tag{5}$$

TABLE I
POLES AND ZEROS LOCATIONS OF THE LDO IN HEAVY AND LIGHT LOADS

Poles / zeros	Heavy load	Light load
p_{3dB}	$-1/C_M R_1 gm_2 R_2 gm_P R_L$	$-1/C_L R_L$
p_{n1}	$-1/[R_{ESR}C_L + C_F R_3(1+gmf_1/gm_2)]$	$-1/(C_F R_2 + C_F R_3 + C_M R_1)$
p_{n2}	$-gm_2/C_F(gm_2+gmf_1)R_3 - 1/R_{ESR}C_L$	$-1/C_M R_1 - 1/C_F(R_2+R_3)$
p_{n3}	$-R_{ESR}(gm_2+gmf_1)gm_P/C_2$	$-(R_2+R_3)/C_2 R_2 R_3$
z_1	$-1/R_{ESR}C_L$	
z_2	$-gm_2/C_F(gm_2+gmf_1)R_3$	
z_3	$-(gm_1/C_M)[(gm_2+gmf_1)/(G_1 gmf_3+gmf_2)]$	
z_4	$+(G_1 gmf_3+gmf_2)gm_P/C_2 gm_1$	

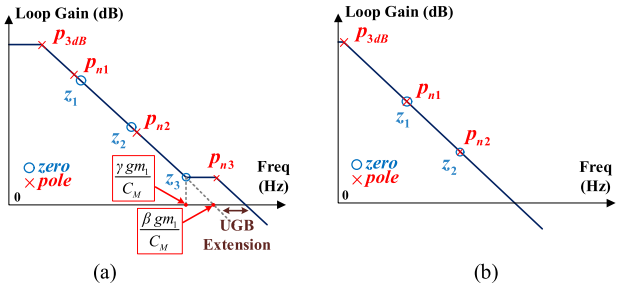

Fig. 5. $T(s)$ frequency response of the proposed LDO when driving (a) heavy load and (b) light load.

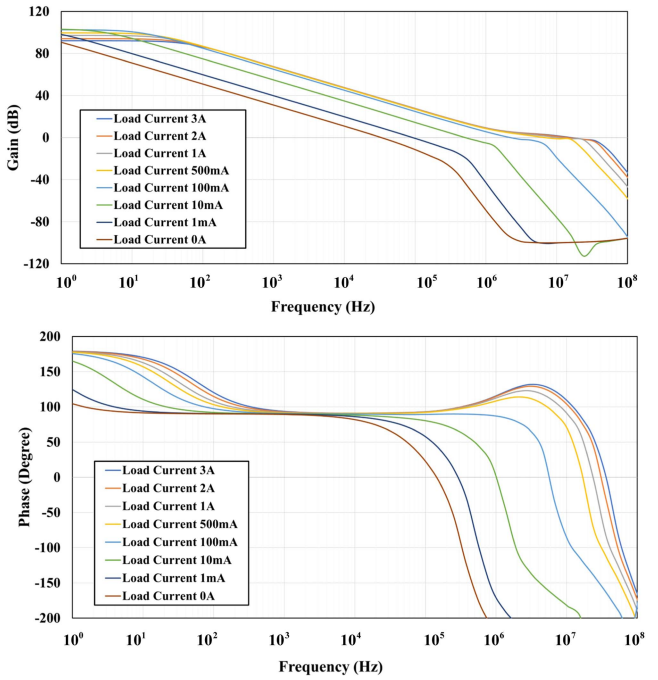

Fig. 6. Simulated $T(s)$ frequency responses (gain and phase) with the load current from 0 to 3A at the typical process and temperature corner.

$$a_3 = -C_M C_F C_2 R_3 / gm_2 gm_P \tag{6}$$

$$b_1 = C_M R_1 gm_2 R_2 gm_P R_L + C_L R_L \tag{7}$$

$$b_2 = C_L R_{ESR} C_M R_1 gm_2 R_2 gm_P R_L + C_M R_1 C_F R_2 (gm_2 + gmf_1) R_3 gm_P R_L + C_L R_L (C_F R_2 + C_F R_3 + C_M R_1) \tag{8}$$

$$b_3 = C_L R_{ESR} C_M R_1 C_F R_2 (gm_2 + gmf_1) R_3 gm_P R_L + C_L R_L C_M R_1 (C_F R_2 + C_F R_3) \tag{9}$$

$$b_4 = C_L R_L C_M R_1 C_2 R_2 C_F R_3. \tag{10}$$

It can be observed that many polynomial coefficients are dependent on gm_P and/or R_L. As our proposed LDO features wide loading range up to 3A, gm_P and R_L will significantly vary from the light load to the heavy load on the premise of the constant V_{OUT}, e.g., 0.8 V. To this end, we will classify and discuss the light load and heavy load scenarios in turn in the following analyses. The load current demarcation between the heavy and light loads is 10 mA at which the LDO has the lowest phase margin – see Fig. 7.

Consider first when the LDO drives the heavy load. gm_P is large while R_L is conversely somewhat small. The corresponding poles and zeros locations are summarized in the left column in Table I, and the pertinent frequency response of $T(s)$ is depicted in Fig. 5(a). p_{3dB} is the dominant pole while p_{ni} and z_i represent the ith nondominant pole and zero, respectively. Given that $C_L R_{ESR} gm_2 / A_H$ is significantly larger than C_F where $A_H = (gm_2 + gmf_1)R_3$ that is defined as the high frequency gain contributed by the TFF technique, the two pairs of pole and zero, p_{n1} & z_1 and p_{n2} & z_2, to a first order cancel.

FF_2 and FF_3 introduce z_3 to the overall loop that is located at $\gamma(gm_1/C_M)$ where $\gamma = (gm_2+gmf_1)/(G_1 gmf_3+gmf_2)$. With the choice of a moderate $G_1 gmf_3$, γ will be smaller than β, which leads to z_3 being located before the original UGB, i.e., $\beta(gm_1/C_M)$. Hence, the ensuing UGB is substantially extended, which is beneficial for the fast-transient response. Since $G_1 gmf_3$ also improves A_{dc} of the loop as expressed in (3), the dc performance is also enhanced. However, an A_{dc} that is excessively high may degrade the loop stability, a proper value of gmf_2 is necessary to balance this trade-off. After comprehensive simulations, we judiciously select gmf_2 to be 3× of gmf_3, and the resultant γ is 0.32 while A_{dc} is enhanced by ∼3dB. Although z_4 is a right-half-plane zero, it can be ignored in the stability analysis due to the very large gm_P and G_1. For example, under the 100mA load condition with simulated dc parameters and extracted parasitics, z_4 is calculated to be 746GHz. z_4 is hence far beyond the final LDO's UGB – see Fig. 6.

Consider now when the LDO drives the light load or no load. gm_P decreases by two orders of magnitude while R_L increases significantly. The dominant term in expressions (7)–(9) is now the most right term. The poles under the light load condition are summarized in the right column of Table I. The zeros' positions remain relatively the same.

The Miller multiplication now becomes less effective due to the somewhat small gm_P and the LDO is converted to a simple single-pole system where p_{3dB} depends on C_L. To maintain an adequate phase margin for stability, it is desirable that p_{n1} and p_{n2} are canceled by z_1 and z_2, respectively. $p_{n2} \approx z_2$ when $C_M = nC_F$ and $n \gg 1$. In this design, with n setting to 8, we

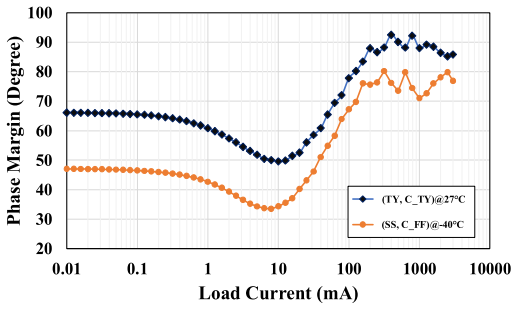

Fig. 7. Simulated phase margins for different load currents at different corners.

derive the C_F as expressed in (11) by equalizing the expressions of p_{n1} and z_1.

$$C_F = \frac{R_{ESR}C_L}{(4+3n)R_3}. \tag{11}$$

From simulations, we finally set C_F and C_M to 6.3pF and 50pF, respectively. The consequential frequency response $T(s)$ is depicted in Fig. 5(b). As p_{3dB} is very close to the origin under the light load condition, the rest of the poles and zeros are far away from the UGB, hence they have negligible influence on the system stability.

It can be inferred that the stability under the heavy load condition is largely independent of C_L while the stability under the light load condition sets a lower limit to selection of C_L. Hence, our proposed LDO can accommodate various large value commercial capacitors – this is beneficial for its radiation-tolerance and accommodating current anomalies. From simulations, we ascertained that our proposed LDO operates stably when loaded with C_L from 100 to 880 μF.

The postlayout simulated frequency response of the loop transfer function at the typical process and temperature corner, i.e., the typical transistors (TY), typical metal-oxide-metal capacitors (C_TY), and room temperature (27 °C), with C_L = 220 μF, is depicted in Fig. 6. Different load current conditions are considered, ranging from no load to the full load (3A). From the plots, the UGB at 3A load is up to 16.3 MHz while the associated dc loop gain is high (92.1 dB). The corresponding phase margins at different loads are plotted in Fig. 7. All conditions can be guaranteed to be stable, where in the worst case (10 mA), the phase margin is 49.44°.

The stability of our proposed LDO has also been verified by simulations across different process, voltage, and temperature corners (−40 °C to 125 °C). Among them, the worst-stability corner is (SS, C_FF) at −40 °C where SS represents the slowest electrical performance of transistors, e.g., the slowest carrier mobility, and C_FF represents the smallest capacitance due to process variations. The phase margins at different loads at this corner are also plotted in Fig. 7 for comparison. Specifically, the phase margin at 10 mA is 34.35° and our proposed LDO remains stable.

B. Current Anomalies Protection Mechanism

Consider now the LCL of the proposed LDO-cum-LCL. In terms of the current anomaly definition, we are addressing the SEL problem. An SEL [27] is defined as "a condition which causes loss of device functionality due to a single event induced high current state. An SEL may or may not cause permanent device damage, but requires power strobing of the device to resume normal device operations." Specifically, when an SEL occurs, the operating current of the affected IC exceeds 4×−5× of its maximum operating current [28]. As delineated earlier, the modus operandi of the LCL to simply clamp the load current to a "safe" value when anomalies are sensed [15], [16]. Also, as delineated earlier, we will also realize the European standards [17].

Our proposed LCL comprises two blocks – the current anomalies sensing and control block and the constant current regulation block ("Block_1" and "Block_2," respectively).

1) Current Anomalies Sensing and Control Block: Fig. 8(a) depicts the simplified schematic of the Block_1, and it can be divided to two sub-blocks: the anomalies sensing circuit and anomalies control logic. In the former sub-block, the load current flowing through the power transistor *MPP* is sensed by *MP*1 with a large current ratio K_S of 25600. A self-biased structure, comprising *MP*2, *MP*3, *MN*2, and *MN*3, is employed to mitigate the channel length modulation effect between *MPP* and *MP*1 and improves the sensing accuracy [5], [29]. This structure features high speed but with a small die area cost. The sensed load current is mirrored to both the Block_2 and the anomalies control logic by *MN*1 and *MN*4, respectively.

The latter sub-block is constructed by two memory latches (*L*1 and *L*2), two timer blocks (*T*1 and *T*2), two unilateral hysteresis comparators (*CMP*1 and *CMP*2), two unilateral delay inverters (*D*1 and *D*2) and other logics. Its modus operandi is summarized in the flow chart in Fig. 9. We will now delineate the steps using sophisticated timing diagrams in Fig. 10 based on the schematic in Fig. 8(a). Specifically, the responses to two load anomaly conditions of interest, namely the recoverable and permanent anomalies will be described in detail.

When the LDO is first powered by V_{IN} with the global switches disabled ($V_{EN} = 0$ and $V_{SFS} = 0$), the LDO is in the OFF state. Hence, *L*1 and *L*2 along with timer blocks are reset, and ready for the load protection from load current anomalies. When V_{EN} is switched to "1," the LDO enters the startup state. The soft start circuit is activated and V_{SFS} is switched to "1" after the completion of the startup state (the soft start process). Then, the LDO enters the linear regulation delineated earlier. To avoid the false triggering of the protection mechanism in the Block_1 due to the undefined state transition, *D*1 is applied after V_{SFS}. The schematic of *D*1 (and *D*2) is depicted in Fig. 8(b). It can be observed that they feature the unilateral delay at the rising edge of the input, and the delay time constant is defined by a preset current source (*MP*6) and a small size on-chip capacitor (C_D). The delay time is designed to be tens of microseconds which is longer than the stabilization time required for the state transition. After Delay_A introduced by *D*1 as depicted in Fig. 10, switch *MP*4 is open and the Block_1 begins to continuously sense the anomalies through the sensing resistor, R_S. The corresponding converted voltage (V_{SEN}) is

$$V_{SEN} = V_{DD} - \frac{I_L R_S}{K_S} \tag{12}$$

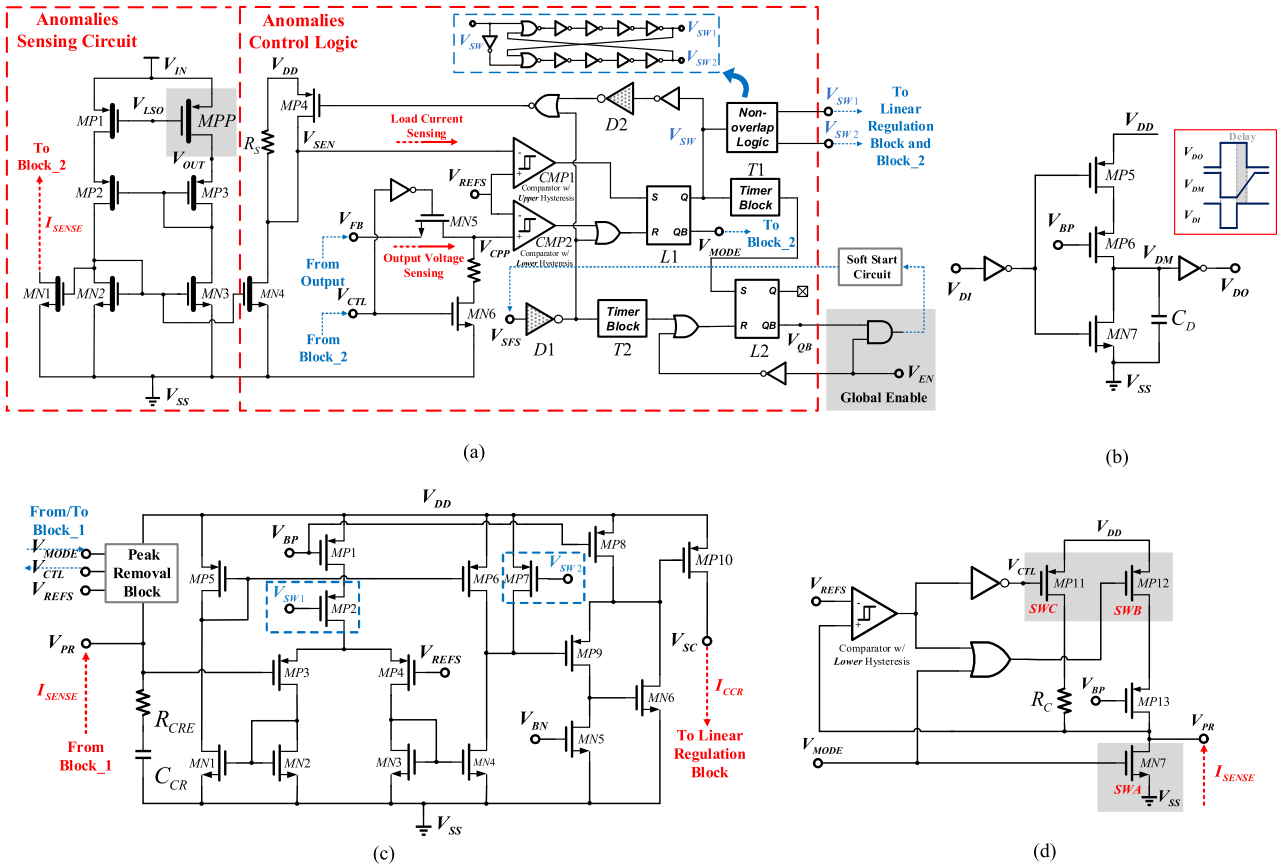

Fig. 8. Simplified schematics of the proposed LCL including (a) proposed current anomalies sensing and control block (Block_1), (b) proposed unilateral delay inverter, (c) proposed constant current regulation block (Block_2), and (d) proposed peak removal block.

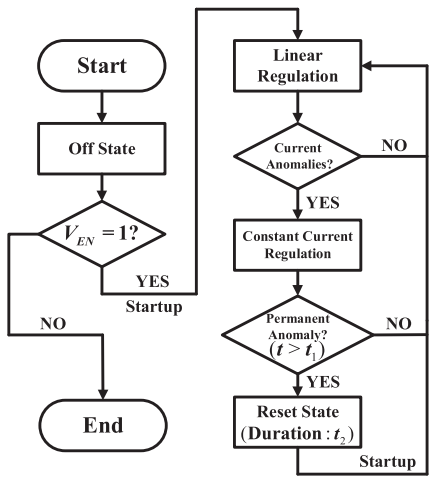

Fig. 9. Flow chart on the working process of the anomalies control logic.

where I_L is the load current flowing through *MPP*.

If an anomaly occurs, i.e., $I_L > I_{TH}$, where I_{TH} is the current threshold defined by R_S, *L*1 will receive an indication from *CMP*1, and switch the *MPP* control from the linear regulation block to the Block_2 by toggling V_{SW} and V_{MODE}. The ensuing load current is clamped to the preset constant value, I_{CONS} – see Section III-B2, which is designed to be the same as I_{TH}. Nonoverlap logic [15] is adopted to avoid the condition where both regulation blocks are activated which would cause massive in-rush current flowing in *MPP*. Meanwhile, *MP*4 is closed to short R_S for avoiding the erroneous trigger to *L*1 during the control handover, and *T*1 is triggered to count and its timing time is set as t_1.

During t_1, V_{CTL} from the Block_2 will open *MN*6 and close *MN*5 after Delay_C introduced by the proposed peak removal block – see Section III-B2, so that $V_{CPP} = V_{FB}$ and the stable output voltage will be monitored instead of the load current through *CMP*2. Since I_{CONS} is constant, if V_{OUT} rises up to V_{REFS}/β within t_1, it means the load has restored to the normal working condition spontaneously, thereby the *MPP* control returns back to the default linear regulation by resetting *L*1 through *CMP*2 – denoted as a recoverable anomaly. *T*1 is reset at the same time. V_{SW} is restored to "0" and the falling edge triggers *D*2 to introduce Delay_B to delay the current sensing reactivation, i.e., opening switch *MP*4, which helps circumvent the false triggering of the Block_1 due to the transition uncertainties.

If the anomaly lasts over t_1, a "permanent anomaly" signal will be asserted by *T*1 and passed to *L*2, so V_{QB} falls to "0" and the LDO enters the reset state. The reset state will last the time period of t_2 that is defined by *T*2. In this state, the soft start circuit is shut down, and the whole LDO system along with the loaded circuits are powered OFF. It is a direct but efficacious method to resolve most load current anomalies. t_2 is normally long enough for the substrate and/or well to discharge the cumulative charge

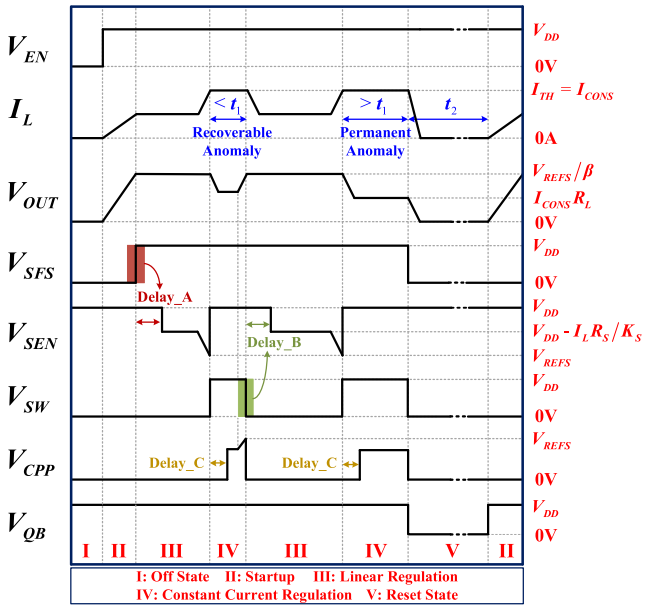

Fig. 10. Timing diagrams at the occurrence of the recoverable and permanent current anomalies.

carriers resulting from an anomaly due to SEL in the load device. After t_2, $L2$ will be reset by $T2$ and the proposed LDO will restart.

The control chain realized in the Block_1, as depicted in Fig. 9, is a closed loop with a self-correction property against the logical errors in digital logics caused by the radiation single events, specifically the single-event-upset (SEU). Consider the case when an SEU occurs and the state of the latches ($L1$ or $L2$) is inadvertently corrupted. Although the LDO may inadvertently enter into constant current regulation, it will nevertheless be spontaneously restored to the default linear regulation because of the closed loop, thereby resetting the corrupted logics to the correct states. Note that even if the LDO inadvertently enters into the reset state, it will automatically restart (power cycle) without the need for an external signal.

2) Constant Current Regulation Block: The constant current regulation block (Block_2) sets an upper limit to the load current (I_{CONS}) so as to protect the load from load current anomalies. The schematic of our proposed Block_2 is depicted in Fig. 8(c). It consists of a high-gain error amplifier and a wideband super source follower [15], [29]. Switches *MP*2 and *MP*7 function the same as switches *MP*2 and *MP*8 in Fig. 2. They ensure that *MPP* is controlled by either the linear regulation block or the Block_2 based on the commands sent by the Block_1 (V_{SW1} and V_{SW2}). Power saving is also realized.

Together with the level shifter in Fig. 2, a negative feedback loop is constructed. The frequency compensation network comprising C_{CR} and R_{CRE} ensures stable operation within the entire load current range. We derive the relationship between I_{SENSE} and I_{CCR} [in Fig. 8(c)] in (13) while I_{CONS} is given in (14) that is defined by R_C. Note that during the transition from linear regulation to constant current regulation, if only R_C is connected between V_{PR} and V_{DD}, V_{OUT} would suffer a large voltage peak. This is because when the system enters the constant

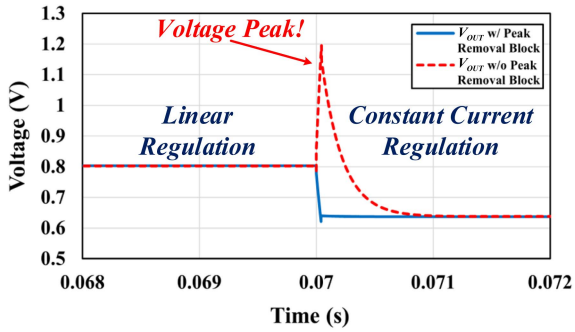

Fig. 11. Simulated outputs when the Block_2 is with and without the peak removal block.

current regulation in response to a load anomaly, V_{PR} is unable to track the changes of I_{SENSE} due to the large C_{CR}, 100 nF. Consequently, the positive voltage difference from V_{REFS} will pull down the gate of *MPP* and the ensuing large transient current will lead to a large voltage peak. To accommodate this, we propose a peak removal block depicted in Fig. 8(d).

$$\frac{I_{SENSE}}{I_{CCR}} = \frac{K_P}{K_S} \tag{13}$$

$$I_{CONS} = K_S \frac{V_{DD} - V_{REFS}}{R_C}. \tag{14}$$

Three switches, namely *SWA*, *SWB*, and *SWC*, manipulate the working process. In the default state when the LDO is regulated by the linear regulation block ($V_{MODE} = 1$), *SWA* is always ON to fully discharge C_{CR} ($V_{PR} = 0$). *SWB* and *SWC* are both OFF by the logics, which is advantage in power saving. Once the transition to the Block_2 happens, V_{MODE} is changed to 0, and *SWA* is then switched OFF while *SWB* is switched ON. The biasing current (*MP*13) starts to charge C_{CR}.

SWC is not turned ON until V_{PR} approaches V_{REFS} and the output of the comparator switches from low to high. At the same time, *SWB* is turned OFF to cut off the charging path, and the feedback loop established by the Block_2 becomes effective to regulate the constant load current. With this proposed circuit application, the voltage difference between V_{PR} and V_{REFS} will be small when the feedback loop is established. This voltage difference is determined by the input offset voltage, V_{OS}, of the comparator where $V_{OS} = V_{PR}$ - V_{REFS}. This means that only when V_{PR} is charged up to $V_{REFS} + V_{OS}$, the output of the comparator switches from low to high, and the control of *MPP* is handed over to Block_2. From 200-point Monte Carlo simulations, the mean value (μ) of this difference is -1.55 mV while the standard deviation (σ) is 5.55 mV. For completeness, from Monte Carlo simulations, the V_{OS} is expected to range from -18.2 to 15.1 mV (3σ range) – it is much smaller than the counterpart without our peak removal block implementation as discussed earlier. Put simply, the large voltage peak is mitigated or possibly eliminated. The whole block will be reset to the default state whenever V_{MODE} returns to 1.

Fig. 11 demonstrates the validity of the proposed peak removal block by comparing the simulated V_{OUT} obtained with and without this block. The simulation conditions are V_{OUT}

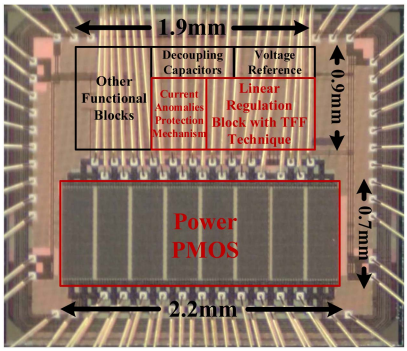

Fig. 12. Microphotograph of the proposed LDO-cum-LCL.

$= 0.8$V, $I_{TH} = I_{CONS} = 3$A, the normal I_L is 2A while the anomaly is emulated by an 4A overcurrent. It can be observed the large voltage peak is successfully removed which confirms the efficacy of our proposed peak removal block as well as the Block_2.

IV. Measurement Results

The proposed fast-transient radiation-tolerant LDO-cum-LCL is fabricated in 130 nm bulk silicon CMOS process, and its microphotograph is depicted in Fig. 12. Wide guard rings (1.5–2 μm width) and deep N-wells are extensively applied in the proximity to the active regions, i.e., $<10\mu$m, to realize its radiation-tolerance feature to eliminate μ-SELs and SELs [11], [30]. The active area is $\sim$3.25 mm^2 where the power PMOS accounts for almost the area of the other functional blocks. The large power transistor area is designed for 3A current capacity. R_{F1} and R_{F2} in the resistive feedback divider are realized by a chip resistor (1.8 kΩ) and a variable resistor, respectively, to ease our measurements and troubleshooting during testing. The output capacitor is a 220 μF tantalum polymer capacitor (model number: T530D227M010ATE006) which features low R_{ESR}($\sim$6 mΩ) and high radiation resistance [12], [13]. The default V_{IN} and V_{OUT} are 2.8 V and 0.8 V, respectively.

The measured quiescent current (I_q), current efficiency, and power efficiency are summarized in Fig. 13(a). When the LDO is operating at heavy load, the I_q and current efficiency increases with the load current. For example, at full load of 3A, the peak current efficiency is high – 99.5%, with an I_q of 15.2 mA. Even at the medium load (10 mA), the efficiency remains high – 89.4%. The relatively high current efficiencies are attributed to the large K_P.

In contrast, when the LDO is operating at light load ($<$10 mA) with $V_{IN} = 2.8$ V and $V_{OUT} = 0.8$ V, the current efficiency is compromised, e.g., the quiescent current is approximately 1.1 mA, which is mostly consumed by the core control, resistive voltage divider and our proposed R_P in the level shifter. Note that we deliberately designed the quiescent current at the light load to a relatively high value (1.1 mA). This is to enhance the radiation tolerance of our proposed LDO against the single-event-transients (SETs) and SELs. This is because the relatively high quiescent current can ensure extensive low impedance nodes in circuits [7]. For completeness, note that

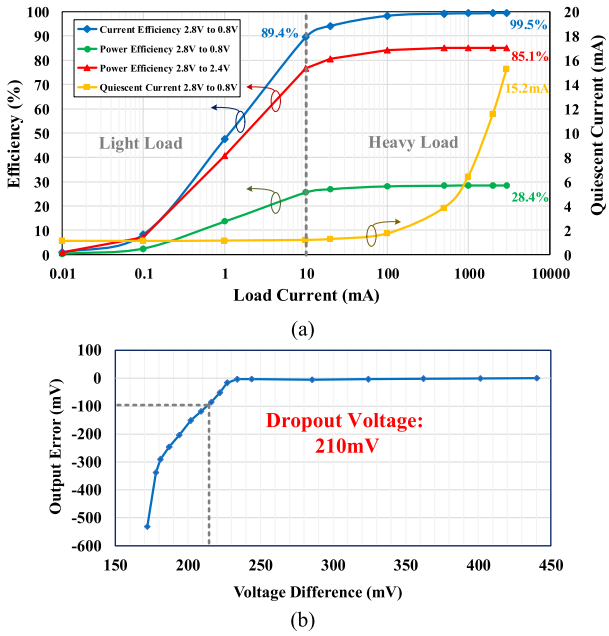

Fig. 13. (a) Measured quiescent current, current efficiency, and power efficiency and (b) measured static output error versus the voltage difference.

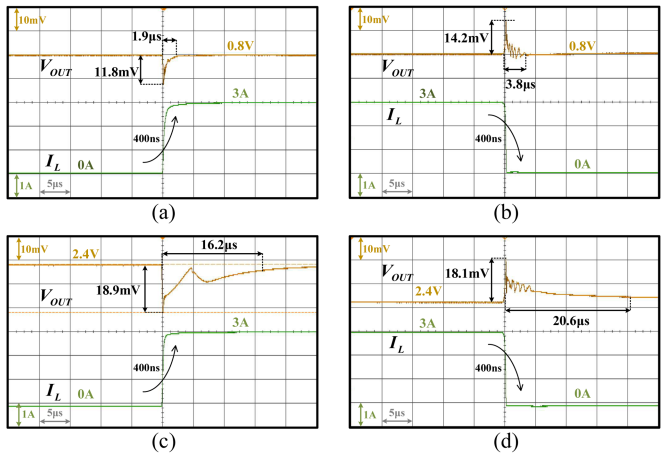

Fig. 14. Measured output transient response under 3A load transient with 400 ns rising and falling time. (a) Rising edge and (b) falling edge of the load transient when $V_{OUT} = 0.8$ V. (c) Rising edge and (d) falling edge of the load transient when $V_{OUT} = 2.4$ V.

this relatively high quiescent current at light loads is commonly practiced in commercial radiation-hardened ICs [12], [13].

The LDO's power efficiency is, as expected, low – it is an inherent (and common) drawback of LDOs in comparison to switching power converters. At full load (3A) when $V_{IN} = 2.8$ V and $V_{OUT} = 0.8$V, the power efficiency is only 28.4%. However, when the LDO works in the dropout region, e.g., at 2.4 V V_{OUT}, the power efficiency is high – 85.1% – as shown in Fig. 13(a) but traded-off with slightly degraded transient performance depicted in Fig. 14. This specific operating efficiency is comparable to most state-of-the-art LDO designs [5], [8], [23], [31].

The dropout voltage and line regulation measured at the load of 3A can be inferred from Fig. 13(b). Specifically, Fig. 13(b)

TABLE II
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART LDOS

	This work	2017 [12]	2017 [13]	2017 [8]	2020 [5]	2020 [23]	2021 [11]	2022 [31]
Process	**130 nm CMOS**	Proprietary process	600 nm BiCMOS	130 nm CMOS	130 nm CMOS	180 nm CMOS	600 nm BiCMOS	180 nm CMOS
Dropout voltage	**210 mV**	210 mV	225 mV	29.7 mV	200 mV	200 mV	300 mV	200 mV
Maximum load current	**3 A**	3 A	3 A	0.3 A	1 A	0.15 A	6 A	0.2 A
Input Voltage	**2.4 – 12 V**	1.5 – 7 V	2.2 – 6 V	1.05 – 2 V	2 V	1.4 – 1.8 V	2.8 – 5.5 V	1.8 – 2.2 V
Minimum output voltage	**0.8 V**	0.8 V	0.52 V	0.7 V	1.8 V	1.19 V	2.5 V	1.6 V
Output capacitor	**100 – 880 µF**	22 – 220 µF	47 – 220 µF	1 µF	1 µF	4.7 µF	100 µF	1 µF
Load regulation	**0.15 mV/A**	0.64 mV/A*	0.27 mV/A*	6 mV/A	0.6 mV/A	75 mV/A	2.16 mV/A	211 mV/A
Overshoot/ undershoot	**14.2 mV/ 11.8 mV**	22.4 mV/24 mV*	50 mV/80 mV*	24 mV/56 mV	12 mV/11 mV	17 mV/20 mV	45 mV/45 mV	25.3 mV/50.7 mV*
PSR@100kHz	**–52.3 dB**	–25 dB	–30 dB	–28 dB	–51 dB	–29 dB*	N.A.	–27 dB*
Quiescent current	**1.1 mA–15.2 mA**	7 mA	13 mA–18 mA	14 µA–120 µA	35 µA–1 mA	13.5 µA	150µA	48 µA
Maximum current efficiency	**99.50%**	99.77%*	99.60%*	99.96%	99.90%	>99.00%	99.998%*	99.98%
FoM	**5.7 ns**	31.8 ns*	41.3 ns*	59.3 ps*	11.9 ps*	104.3 ps	37.5 ps*	91.2 ps
Load current Anomalies protection	**Yes**	Yes	Yes	No	No	No	No	No

* The parameter is derived from the information provided in this article or datasheet.

depicts the measured static output error (the deviation from the normal V_{OUT}) versus the voltage difference (V_{IN} - V_{OUT}). According to an industry definition [32], the dropout voltage is inferred to be 210 mV. The line regulation is calculated as 0.4 mV/V. These highly competitive (see Table II) static characteristics are attributed to the high dc gain (92dB) of the feedback loop, arising from our proposed TFF technique.

Fig. 14 depicts the output transient response of our proposed LDO regulated by the linear regulation block. The load variation is between 0 and 3A with the fast transition of 400ns rising and falling time. The equivalent load transition speed is 7.5 A/μs, which is one of the fastest in comparison to that of many reported state-of-the-art LDO designs [5], [8], [23], [31]. Two conditions are measured: V_{OUT} = 0.8 V [Fig. 14(a) and (b)] and V_{OUT} = 2.4 V [Fig. 14(c) and (d)]. The former condition features the minimum output voltage, while the latter one reflects the performance of the LDO working close to the dropout region. It can be observed that for V_{OUT} = 0.8 V, the undershoot and overshoot are 11.8 mV and 14.2 mV with the settling times of 1.9 μs and 3.8 μs, respectively. The longer overshoot settling time is due to the narrower UGB under the no load condition as depicted in Fig. 6. When V_{OUT} is elevated to 2.4 V, the undershoot and overshoot are increased to 18.9 mV and 18.1 mV, respectively, while the corresponding settling times are increased to 16.2 μs and 20.6 μs, respectively. These increments result from the degraded UGB caused by the reduced β and the power PMOS entering the triode region.

There is an obvious ~2MHz oscillation during the settling time in Fig. 14(b) and (d), but not in Fig. 14(a) and (c). This is not a consequence of insufficient phase margin, but by the considerable ringing on V_{IN} as depicted in Fig. 15. This originates from the LC-oscillation due to the nonideal components in the test instruments connections, e.g., the parasitic inductance and resistance from short wire leads. Specifically, when the load transitions from heavy to light, from 3 to 0A, the quickly cut-off power transistor is effectively an open circuit, and the tank circuit comprising the series parasitic resistance, inductance, and input decoupling ceramic capacitors resonates accordingly. Conversely, when the load transitions from light to heavy, from

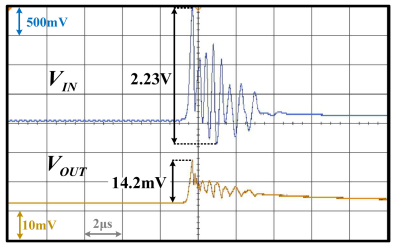

Fig. 15. V_{OUT} oscillation results from the ringing on V_{IN}.

0 to 3A, the power transistor will be quickly turned ON and enter the low impedance mode after a short response time due to our proposed TFF technique. The low impedance greatly damps the LC-oscillation – explaining why there is negligible impact in Fig. 14(a) and (c). Nevertheless, the oscillation in Fig. 15 has little impact on the magnitude of the measured output variations due to the high PSR – see Fig. 17.

Put simply, the small output variations under both conditions are much smaller than 2% of the output voltage, which confirms that our proposed LDO meets the stringent requirements of the state-of-the-art FPGAs [3] and SoCs. In short, our proposed TFF technique is efficacious.

The load regulation can also be inferred from the measured output transient response by setting different heavy loads (30 mA to 3A). It is 0.15 mV/A that is much smaller than most reported fast-transient LDOs [5], [8], [11], [23], [31].

To verify the effectiveness of the proposed protection mechanism, the Richtek load transient tool (RD0004) is utilized to emulate current anomalies at the load. For our specific application to protect an advanced FPGA (e.g., the programmable logics and memories) whose maximum nominal current into a specific power pin is around 425 mA, we define a current anomaly when the operating current exceeds 4× of the maximum nominal current, ≥1.7A [28]. When duration of the current anomaly exceeds 32 ms, the LDO-cum-LCL power cycles that specific power pin, and the SEL is circumvented. In short, the measurement conditions are: V_{OUT} = 0.8 V, I_{TH} = I_{CONS} = 1A, t_1 = 32 ms,

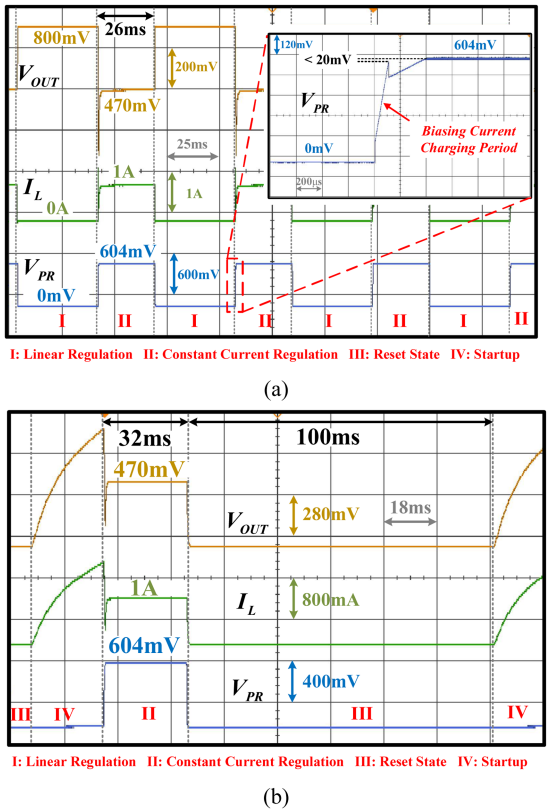

Fig. 16. Measured output transient waveforms in response to (a) the recoverable and (b) the permanent current anomalies.

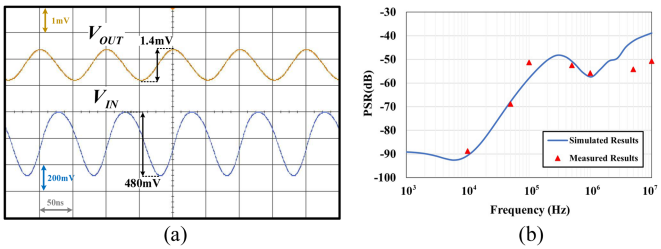

Fig. 17. (a) Measured PSR at 10MHz for $I_L = 3$ A when the LDO works in the dropout region and (b) corresponding PSR trend with frequency.

$t_2 = 100$ ms and the current anomaly is represented by 0.47 Ω (1.7 A).

Fig. 16(a) and (b) depict the measured results in response to the recoverable (26 ms) and permanent anomalies (>32 ms), respectively. Whenever a load anomaly is sensed, the LDO enters the constant current regulation, and V_{OUT} is clamped to 470 mV. If this anomaly extends over t_1, the LDO is shut down and restart automatically after t_2. The measured results are congruous with the working process delineated in Section III-B.

The zoom-in view of the rising edge of V_{PR} is shown in Fig. 16(a). The constant current charging period can be clearly observed, depicting that the proposed peak removal block works properly during the *MPP* control transition from the linear regulation block to the Block_2. The high voltage peak at V_{OUT} is hence avoided. In short, our proposed LCL mechanism in our LDO-cum-LCL is effective to protect the load, e.g., the FPGA or SoC, against current anomalies when the load suffers from an SEL.

Fig. 17(a) shows the measured PSR at 10MHz when the LDO works close to the dropout region with I_L of 3A. It can be calculated that the PSR is −50.7 dB at this frequency. The Picotest J2120A line injector is used to supply the ac testing signal at V_{IN} [29]. In the same approach, the trend of PSR with frequency is plotted in Fig. 17(b). The simulated PSR values are depicted for comparison. The PSR of the proposed LDO is very competitive (highest among the benchmarked LDOs in Table II), i.e., −52.3 dB@100 kHz, is in part contributed by the simple linear voltage regulator depicted in Fig. 2. By means of simulations, we ascertained that our proposed LDO achieves >30 dB PSR improvement at high frequencies (1 kHz to 10 MHz) by the implementation of this linear regulator.

We have conducted the laser testing to verify the radiation tolerance of our proposed LDO-cum-LCL. The integrated laser detection system (SEMICAPS 1100) was used for the testing. From measurement results, our proposed LDO-cum-LCL is immune to the μ-SELs and SELs even after prolonged exposure to the highest energy laser which is set to 4.2nJ (to avoid potential physical damage). Moreover, the SET-induced output voltage variations are less than 30 mV.

Table II benchmarks our proposed LDO-cum-LCL against several state-of-the-art LDOs with high load current capacity. We make the following comments. One, our LDO-cum-LCL is the only RHBD device and realized in CMOS to date. Three reported designs are radiation-hardened-by-process requiring exotic processes [11], [12], [13] while the rest are not radiation-tolerant/hardened designs [5], [8], [23], [31].

Two, from the table, although the overshoot and undershoot in [5] are smaller than others, the pertinent load variation is low – 1A, which is one-third of our 3A load variation. In view of this, our proposed LDO would feature the smallest overshoot and undershoot for a 3A load variation. We attribute this to our proposed TFF technique.

Three, for the same reason, the load regulation of our design is the best when compared to the state-of-the-art.

Four, further to three, also for the same reason, PSR performance of our design is the highest.

Five, our proposed LDO can accommodate the largest off-chip capacitor. It is a worthy attribute with respect to the radiation hardness, in addition to our RHBD implementation.

Six, although our power transistor is PMOS vis-à-vis NMOS [5], [8], its dropout voltage is, as expected, not the smallest. Nevertheless, the 210 mV dropout voltage is still very competitive considering the high current (3 A) capacity.

Seven, for a fair comparison, a common figure-of-merit (FoM) [8] that reflects the overall performance of the LDO is given as follows:

$$\text{FoM} = \frac{C_L \Delta V_{OUT} I_q}{I_{L\_MAX}^2} \tag{15}$$

where C_L, ΔV_{OUT}, and $I_{L\cdot MAX}$ are the output capacitor, the peak-to-peak output voltage change due to overshoots and undershoots, and the maximum load current, respectively. The average value of the I_q is taken into calculation to ensure

fairness [31]. Since the LDOs reported in [5], [8], [23], and [31] target nonradiation-hardened applications. As the high current efficiency is prioritized, e.g., the much lower quiescent current, I_q, it is not unexpected that their FoMs are lower (better) than radiation-hardened LDOs (including our proposed LDO) where their I_q is significantly higher. Nevertheless, our proposed LDO achieves the smallest (best) FoM among the radiation-hardened LDOs [12], [13].

Eight, our design and two commercial products [12], [13] are able to protect the load against anomalous load currents. However, in comparison with [12] and [13], our proposed module-level protection mechanism features a unique capability. Specifically, it assists the LDO to distinguish the recoverable or permanent current anomaly that occur in the load and treat them differently as delineated in Section III-B.

Nine, our design is the only design that embodies the European standards [17].

In summary, our proposed fast-transient LDO-cum-LCL is highly competitive compared to the state-of-the-art, albeit the reported LDOs not featuring radiation tolerance or requiring exotic fabrication processes.

V. Conclusion

We have delineated a fast-transient radiation-tolerant LDO-cum-LCL (with protection for load current anomalies) monolithically realized in 130 nm CMOS. The innovations include the proposed TFF technique implemented in the main control circuit, and the proposed module-level current anomalies protection mechanism. With these innovations, the proposed LDO features very competitive attributes when benchmarked against reported LDOs (albeit the reported LDOs not featuring radiation tolerance or requiring exotic fabrication processes), including small overshoot and undershoot (14.2 mV/11.8 mV at 3A load variation), load regulation (0.15 mV/A), PSR (−52.3 dB@100 kHz).

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