A Drain Current Extraction Technique Using Source Parasitic Resistance and Inductance in SiC Power MOSFETs

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***Abstract*—In order to monitor the operating status of silicon carbide power MOSFETs, an in-circuit real-time drain current extraction technique based on packaging parasitic parameters is proposed. The connection between the Kelvin source and the power source is modeled as a resistor (R_{SS}) and inductor (L_{SS}) in series. By integrating and sampling the voltage across the series combination of R_{SS} and L_{SS} as the drain current ramps up, a quadratic function can be obtained. An field programmable gate array (FPGA) is used to calculate the values of the parasitic parameters (R_{SS} and L_{SS}) and the initial drain current (I_{DS0}) in real time. Double pulse tests under different temperatures are used to verify the accuracy of the proposed technique. The test results show that the extraction accuracy of R_{SS} and L_{SS} is greater than 90% and 89%, respectively. The extraction accuracy of I_{DS0} is greater than 90% over a current range of 2.5–20 A from 25 to 175 °C. A 250 W, 155–48 V buck converter operating at 100 kHz is built and tested to demonstrate the application potential of the proposed technique.**

***Index Terms*—Drain current extraction, Kelvin source, parasitic parameters extraction, silicon carbide (SiC) MOSFETs.**

I. Introduction

SILICON CARBIDE (SiC) power MOSFETs are attractive for high-voltage high-frequency power systems due to their fast-switching speed and low switching loss [1]. When compared to Si insulated gate bipolar transistoris (IGBTs), SiC MOSFETs can operate at a higher junction temperature with a more compact package [2]. However, SiC MOSFETs still encounter numerous challenges in practical applications. With the high drain current density and unsaturated drain current, the short circuit capacity of SiC MOSFETs is not as robust as the Si IGBTs [3]. Due to the SiC material properties, the gate oxide reliability is not as good as its silicon counterparts [4]. At the same time, the packages for many SiC MOSFETs are legacy silicon-based technologies. The parasitic parameters are not optimized for SiC MOSFETs' high-frequency capability [5]. Large parasitic parameters also induce electromagnetic interference (EMI) issues, interfering with the operation of the gate drivers and neighbouring circuits. In addition, the failure of SiC MOSFETs in the power system could be catastrophic. Therefore, a current monitoring circuit for SiC MOSFETs would be highly desirable to improve the reliability of power systems [7].

The typical power device packages contain parasitic components from the die layout, the bond wires, and the I/O pins [8]. Furthermore, the parasitic resistance changes with the case temperature [9], [10]. The parasitic inductance is also related to aging [11]. The parasitic capacitance affects the switching performance [12]. Moreover, the drain current can be deduced by analyzing the voltage waveforms across the parasitic components. Therefore, extracting the parasitic parameters is important for monitoring the drain current flowing through the SiC MOSFETs.

To exploit the fast-switching performance and to reduce the coupling between the power and driver loops, SiC MOSFETs can be packaged with a Kelvin source connection [13]. The connection between the Kelvin source and the power source is usually a bond wire. The bond wire can be modeled as a series branch of a resistor and an inductor [14]. Kelvin source connection are well suited for overcurrent detection and drain current measurement [15], [16]. Overcurrent detection methods based on the source parasitic inductance can have a very short response time, typically less than 100 ns [17]. Once the parasitic resistance and inductance are extracted, the drain current can be determined by analyzing the voltage drop across the parasitic resistor and inductor.

Many parasitic parameter extraction methods for SiC MOSFETs have been proposed [18], [19], [20], [21], [22]. These

Manuscript received 11 July 2023; revised 28 October 2023 and 9 December 2023; accepted 15 December 2023. Date of publication 21 December 2023; date of current version 16 February 2024. This work was supported in part by Youth Innovation Promotion Association CAS, the National Key Research and Development Program of China under Grants 2022YFB3604300, 2022YFB3604301, and 2022YFB3604303, in part by the National Natural Science Foundation of China under Grant 11705263, and in part by Shanghai Rising-Star Program under Grant 21QA1410900. Recommended for publication by Associate Editor K. Ngo. *(Corresponding author: Xinhong Cheng.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3345315.

Digital Object Identifier 10.1109/TPEL.2023.3345315

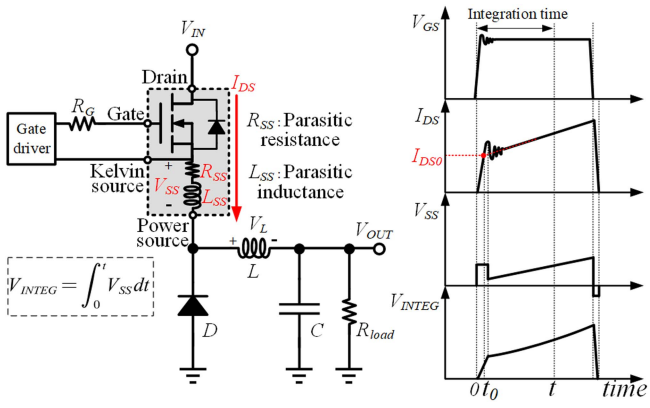

Fig. 1. SiC MOSFET under test with Kelvin source connection in a buck converter configuration and some key waveforms.

methods are based on an offline impedance analysis. The operating status, case temperature, and aging cannot be obtained during in-circuit operation.

Therefore, a real-time parasitic parameter extraction method is required to monitor the status of SiC MOSFETs during normal operation. The parasitic parameters should be extracted and refreshed periodically. In hard-switching applications, high *dv/dt* and *di/dt* switching behaviors contribute to severe EMI issues, making it more challenging to extract the parasitic parameters accurately.

To address the aforementioned problems, this article proposed a parasitic parameters and drain current extraction technique for SiC MOSFETs with Kelvin source connection. During each conduction period, the voltage V_{SS} between the Kelvin source and the power source is sent to an analog integrator. The output voltage V_{INTEG} is digitized and sent to an field programmable gate array (FPGA) for data processing. The least squares method is used to fit the V_{INTEG} to a quadratic function. After determining the coefficients, a, b, and c for the quadratic function, the source parasitic resistance R_{SS}, the source parasitic inductance L_{SS}, and the initial turn-ON drain current I_{DS0} can be calculated.

The rest of this article is organized as follows. Section II introduces the principle of the parasitic parameter and drain current extraction technique. Section III introduces the circuit design and implementation. Finally, Section IV concludes this article.

II. Principle of Parasitic Parameters and Drain Current Extraction Technique

A. Basic Principle

The parasitic components between the Kelvin source and the power source can be modeled as a series combination of a source parasitic resistor R_{SS} and a source parasitic inductor L_{SS}, as seen in Fig. 1. To illustrate the proposed technique, a buck converter shown in Fig. 1 is used as an application example. In hard-switching dc–dc converters, the drain current I_{DS} ramps up and down linearly. When the SiC power MOSFET conducts, the drain current I_{DS} ramps up, creating a nearly linear voltage ramp V_{SS} on the series combination of R_{SS} and L_{SS}. I_{DS} can be expressed as (1), and V_{SS} can be expressed as (2). I_{DS0} is the initial turn ON drain current before the overshoot oscillation, as seen in Fig. 1. t_0 is the time that the drain current rises from zero to I_{DS0}. V_L is the voltage on the power inductor L. This is approximately equal to V_{IN} minus V_{OUT} in the buck converter. R_{load} is the load of the converter. V_{SS} in (2.2) is a linear function of the SiC MOSFET conduction time t, with a coefficient term, and a constant term. In order to solve for I_{DS0}, R_{SS}, and L_{SS}, an integration operation for V_{SS} is used. V_{INTEG} is the integral of V_{SS}. It can be expressed as (4) and can be expanded to (5). Equation (5) is a quadratic function of the SiC MOSFETs' conducting time t. It is worth noting that the overshoot oscillation of the drain current will be eliminated in (4) and (5) since the integrator acts as a low-pass filter, reducing the high frequency noise

$$I_{DS}\ (t) = \begin{cases} \frac{I_{DS0}}{t_0} t & t \leqslant t_0 \ (1.1) \\ \frac{V_L}{L} t + \left(I_{DS0} - \frac{V_L}{L} t_0\right) & t > t_0 \ (1.2) \end{cases} \tag{1}$$

$$\begin{aligned} V_{SS}\ (t) &= R_{SS}\, I_{DS} + L_{SS} \frac{dI_{DS}}{dt} \\ &= \begin{cases} R_{SS} \frac{I_{DS0}}{t_0} t + L_{SS} \frac{I_{DS0}}{t_0} & t \leqslant t_0 \ (2.1) \\ \frac{V_L}{L} R_{SS} t + \left(R_{SS} I_{DS0} + L_{SS} \frac{V_L}{L}\right) & t > t_0 \ (2.2) \end{cases} \end{aligned} \tag{2}$$

$$V_L = V_{\text{IN}} - V_{\text{OUT}} \tag{3}$$

$$V_{INTEG} = \int_0^t V_{SS}\, dt = \int_0^{t_0} V_{SS}\, dt + \int_{t_0}^t V_{SS} dt \tag{4}$$

$$\begin{aligned} V_{INTEG} = {} & \frac{1}{2} R_{SS} \frac{V_L}{L} t^2 \\ & + \left[R_{SS} I_{DS0} + (L_{SS} - R_{SS} t_0) \frac{V_L}{L}\right] t \\ & + \left[L_{SS} I_{DS0} - \left(\frac{1}{2} R_{SS} I_{DS0} + 2 L_{SS} \frac{V_L}{L}\right) t_0\right]. \end{aligned} \tag{5}$$

To simplify the constant term of the quadratic function in (5), the switching process of a C3M0120065K (650 V/22 A SiC MOSFET) with $R_{SS} = 5.03\,\text{m}\Omega$ and $L_{SS} = 4.50\,\text{nH}$ is tested. A gate resistance of $R_G = 4.7\,\Omega$ is used. The gate voltage, V_G is 16 V. V_L is set to 200 V with $L = 200\,\mu\text{H}$. The time to $I_{\text{load}} = 20\,\text{A}$ is about 15 ns, as shown in Fig. 2.

Substituting the abovementioned parameters into (5), (6) can be obtained

$$\begin{cases} L_{SS} = 4.50\ \text{nH} \gg R_{SS}\, t_0 = 0.075\ \text{nH} \\ L_{SS}\, I_{DS0} = 89.96\ \text{V} \cdot \text{ns} \gg \\ \frac{1}{2} R_{SS} I_{DS0} t_0 + L_{SS} \frac{V_L}{L}\, t_0 = 0.90\ \text{V} \cdot \text{ns} \end{cases}. \tag{6}$$

As shown in (6), it is reasonable to approximate (5) as (7). This approximation becomes more accurate as the drain current rise time t_0 decreases. If t_0 equals zero, the primary term coefficient

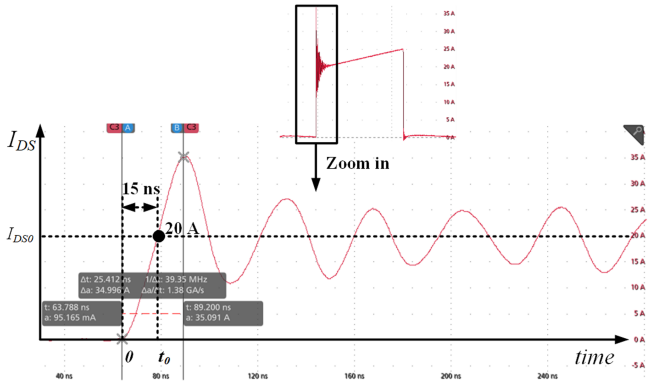

Fig. 2. Turn-ON drain current waveform for a C3M0120065K SiC power MOSFET with $R_G = 4.7\Omega$.

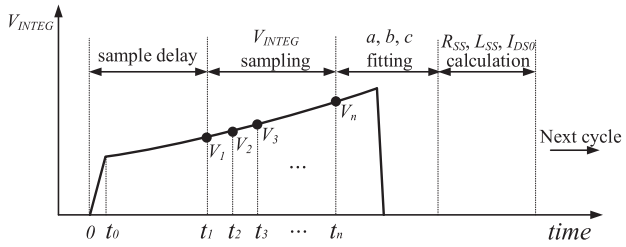

Fig. 3. Integration voltage sampling and subsequent parameters calculation timing scheme.

and constant term in (5) would equal to those in

$$V_{INTEG} = \frac{1}{2} R_{SS} \frac{V_L}{L} t^2 + \left(R_{SS} I_{DS0} + L_{SS} \frac{V_L}{L} \right) t + L_{SS} I_{DS0} = at^2 + bt + c. \quad (7)$$

Setting the coefficients of the quadratic function in (7) back to a, b, and c, the relationships between these coefficients and circuit parameters can be, as shown in

$$\begin{cases} a = \frac{1}{2} R_{SS} \frac{V_L}{L} & (8.1) \\ b = R_{SS} I_{DS0} + L_{SS} \frac{V_L}{L} & (8.2) \\ c = L_{SS} I_{DS0} & (8.3). \end{cases} \quad (8)$$

The source parasitic resistor R_{SS}, source parasitic inductor L_{SS}, and initial drain current I_{DS0} can be obtained by solving (8). This leads to the results, as shown in

$$\begin{cases} R_{SS} = 2a \frac{L}{V_L} & (9.1) \\ I_{DS0} = \frac{b \pm \sqrt{b^2 - 8ac}}{4a \frac{L}{V_L}} & (9.2) \\ L_{SS} = \frac{4ac \frac{L}{V_L}}{b \pm \sqrt{b^2 - 8ac}} & (9.3). \end{cases} \quad (9)$$

There are two groups of I_{DS0} and L_{SS} values (extraneous roots). It is unclear which group is correct. Therefore, further analysis is conducted by replacing a, b, and c in (9.2) with the initial load current I_{load0}. As shown in (10) shown at the bottom of this page. Here, a stimulus initial load current I_{load0} is applied to the SiC MOSFET. Therefore, the correctly extracted I_{DS0} should be I_{load0}

Based on (10), I_{DS0} and L_{SS} have two possible solutions. I'_{DS0} and L'_{SS} are the incorrect current and inductance in (11).

This is because the initial drain current I_{DS0} is only determined by the load current, not the circuit parameters. L_{SS} is the parasitic inductance which does not depend on the load current

$$\begin{cases} I_{DS0} = I_{\text{load0}} \\ L_{SS} = \frac{c}{I_{\text{load0}}} \end{cases} \text{ or } \begin{cases} I'_{DS0} = \frac{L_{SS} V_L}{R_{SS} L} \\ L'_{SS} = \frac{R_{SS} L}{V_L} I_{\text{load0}}. \end{cases} \quad (11)$$

During normal situations, I_{DS0} is independent from the parasitic parameters. L_{SS} is a fixed value and basically does not vary with the drain current. I_{DS0} and L_{SS} can be determined by setting an estimated limit for L_{SS}. The value for I_{DS0}, R_{SS}, and L_{SS} can be calculated after obtaining a, b, and c. Therefore, the next step is to obtain the coefficients for the quadratic function in (7).

In addition, the R_{load} is not used in (9) and other equations. The extraction results do not depend on the load of the converter. The power inductor L has a fixed value once the converter is designed. The approximation from (5) to (7) is a simplification of the switching time and parasitic parameters, independent of the load.

B. Algorithm Design

The least square method is used to fit the coefficients a, b, and c to the quadratic function in (7). V_{INTEG} is sampled for the curve fitting.

Once the SiC power MOSFET turns ON, the integrator starts to integrate V_{SS} until the device turns OFF. A blanking delay is added before sampling to reduce the interference of switching oscillation. The SiC MOSFET can be turned OFF immediately or later after the sampling is finished, as shown in Fig. 3.

During the V_{INTEG} sampling process, the sampling time is recorded as well. For n V_{INTEG} sampling data corresponding to n time points, n equations can be obtained. These equations are

$$I_{DS0} = \frac{\left(R_{SS} I_{\text{load0}} + L_{SS} \frac{V_L}{L} \right) \pm \sqrt{\left(R_{SS} I_{\text{load0}} + L_{SS} \frac{V_L}{L} \right)^2 - 4 R_{SS} I_{\text{load0}} L_{SS} \frac{V_L}{L}}}{2 R_{SS}}$$

$$= \frac{\left(R_{SS} I_{\text{load0}} + L_{SS} \frac{V_L}{L} \right) \pm \left(R_{SS} I_{\text{load0}} - L_{SS} \frac{V_L}{L} \right)}{2 R_{SS}} = \begin{cases} I_{\text{load0}} \\ or \\ \frac{L_{SS} V_L}{R_{SS} L}. \end{cases} \quad (10)$$

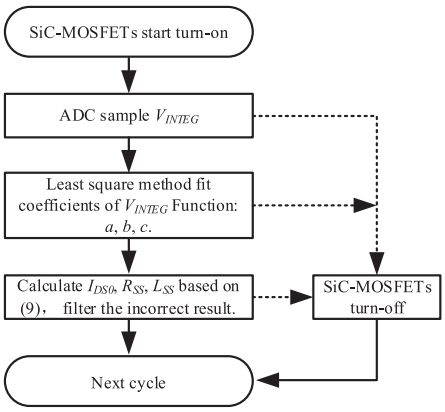

Fig. 4. Flowchart of the I_{DS0}, R_{SS}, and L_{SS} calculations.

shown in

$$\begin{cases} V_1 = at_1^2 + bt_1 + c & (12.1) \\ V_2 = at_2^2 + bt_2 + c & (12.2) \\ \dots & \\ V_n = at_n^2 + bt_n + c & (12.n). \end{cases} \tag{12}$$

To solve a, b, and c, the matrix equivalence transformation of (12) is performed and the result is shown in (13).

After obtaining a, b, and c, I_{DS0}, R_{SS}, and L_{SS} can be calculated based on (9). The flowchart for calculating I_{DS0}, R_{SS}, and L_{SS} is shown in Fig. 4

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} \sum_{i=1}^n t_i^4 & \sum_{i=1}^n t_i^3 & \sum_{i=1}^n t_i^2 \\ \sum_{i=1}^n t_i^3 & \sum_{i=1}^n t_i^2 & \sum_{i=1}^n t_i \\ \sum_{i=1}^n t_i^2 & \sum_{i=1}^n t_i & n \end{bmatrix}^{-1} \begin{bmatrix} \sum_{i=1}^n V_i t_i^2 \\ \sum_{i=1}^n V_i t_i \\ \sum_{i=1}^n V_i \end{bmatrix}. \tag{13}$$

C. Theoretical Error Analysis

All subsequent calculations are based on the V_{INTEG} function in (7). However, there are some approximations made in (7), as seen in (6). Since there are several variables in this approximation process, an error analysis of this approximation is performed.

From (6), the shorter the drain current rise time t_0, the larger the drain current rising slope I_{DS0}/t_0. In this case, with smaller R_{SS} and larger L_{SS}, the approximation would become more accurate. These trends are shown in Table I.

From (9), R_{SS}, L_{SS}, and I_{DS0} are determined by a, b, c, and V_L/L. V_L/L is the slope of the drain current ramp. R_{SS} and L_{SS} are inversely proportional to V_L/L. I_{DS0} is proportional to V_L/L. Therefore, the inductance and voltage variation of the power inductor will cause errors on R_{SS}, L_{SS}, and I_{DS0}. To eliminate

TABLE I
ERROR ANALYSIS

t_0	I_{DS0}/t_0	R_{SS}	L_{SS}	Accuracy of approximation in (7)
↓	↑	↓	↑	↑

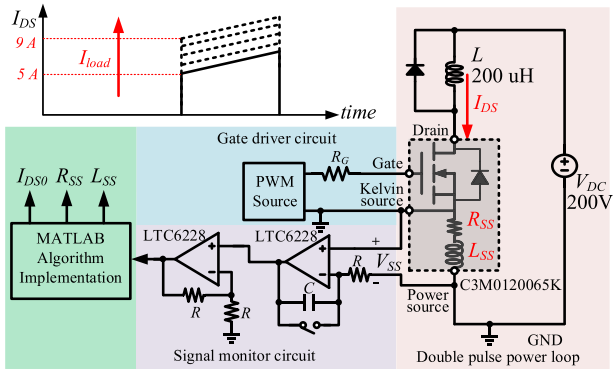

Fig. 5. LTspice double pulse test simulation circuit and I_{DS} waveform.

these errors, a calibrated V_L/L can be used. At the same time, V_L/L is considered a constant value during the calculation. The power inductor should avoid magnetic saturation, which could cause the inductance value to drop significantly. The errors of the fitted coefficients a, b, and c come from the limited calculation accuracy and sampling errors.

According to the discussion abovementioned, the overall error of the proposed technique comes from the approximation error in (7) and the calculation error in (9). A short drain current rising time can reduce the approximation error in (7). High-accuracy analog signal sampling and digital calculation circuits would also reduce the error in the calculated coefficients a, b, and c. The slope of the drain current ramp should remain constant during V_{INTEG} sampling.

Following the abovementioned qualitative analysis, additional quantitative analyses are conducted to further investigate the main sources of error. A LTspice double pulse test circuit was built to evaluate the proposed extraction technique, as seen in Fig. 5. The SiC MOSFET in the simulation circuit is a C3M0120065K and some parameters in the spice model are modified to evaluate their influence on the extracted results. The second drain current pulse is used to extract the I_{DS0}, R_{SS}, and L_{SS} of the SiC MOSFET. The values for I_{DS0}, R_{SS}, and L_{SS} are 5 A, 4.50 nH, and 5.03 mΩ, respectively, unless noted. The load current was increase from 5 to 9 A to evaluate the influence of the load on the extraction accuracy. The following accuracy calculation of the extraction results are conducted under these conditions. MATLAB is used to implement the proposed extraction algorithm. The equation for the extraction accuracy is shown in

$$\text{Accuracy} = 100\% - \frac{|\text{Extraction value} - \text{True value}|}{\text{True value}} \times 100\%. \tag{14}$$

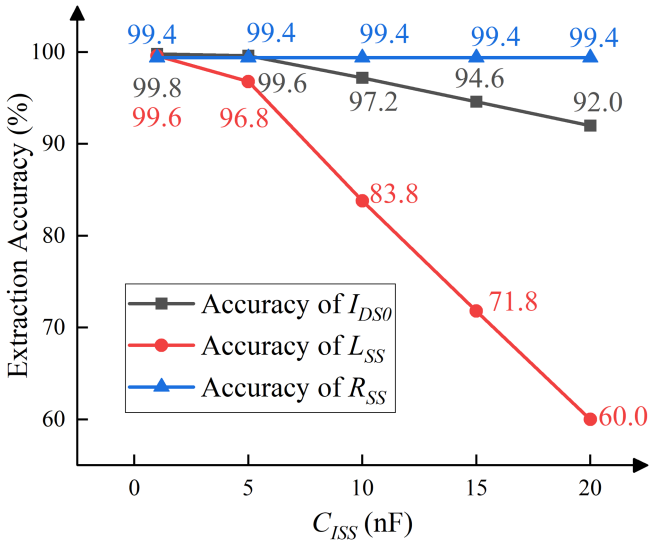

Fig. 6. I_{DS0}, R_{SS}, and L_{SS} extraction accuracy with different values of C_{ISS} for the SiC MOSFET.

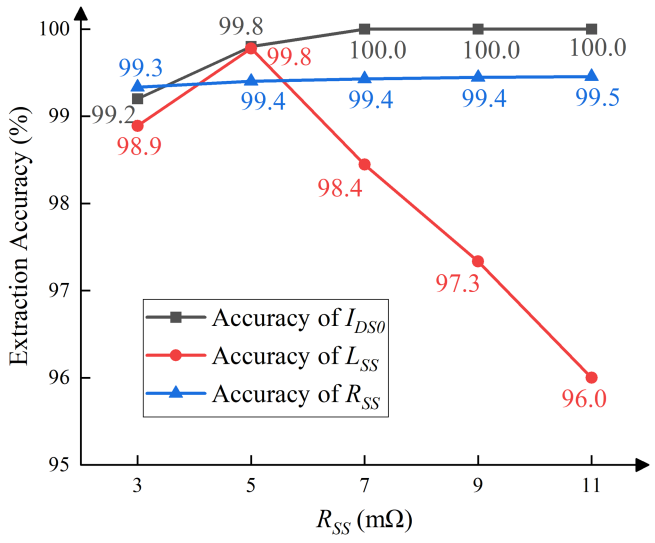

Fig. 7. I_{DS0}, R_{SS}, and L_{SS} extraction accuracy with different values of R_{SS} for the SiC MOSFET.

Based on (5) and (7), (7) will be exactly equal to (5) if the drain current rise time t_0 or the device switching time equals to 0. For the SiC MOSFET, its switching time mainly depends on the input capacitance C_{ISS}. The value for C_{ISS} of the SiC MOSFET is changed to evaluate its influence on the extraction results. As seen in Fig. 6, the L_{SS} extraction accuracy drops rapidly as C_{ISS} increases from 5 to 20 nF. The I_{DS0} extraction accuracy also drops but is still above 90%. The R_{SS} extraction accuracy does not change because the calculation of R_{SS} is not related to the switching time. The quadratic coefficients are obtained directly from (5) to (7).

In the primary and constant coefficients in (5), $(L_{SS} - R_{SS}t_0)\frac{V_L}{L}$ and $(\frac{1}{2}L_{SS}I_{DS0} + 2L_{SS}\frac{V_L}{L})t_0$ are dropped. The calculation of I_{DS0} and L_{SS} are based on the primary and constant coefficients in (5). The influences of R_{SS} and L_{SS} on the extraction results are analyzed. As seen in Fig. 7 as R_{SS} increases from 3 to 11 mΩ, the L_{SS} extraction accuracy drops to 96% and the I_{DS0} and R_{SS} extraction accuracies are basically unchanged. The order of magnitude for L_{SS} (10^{-9}) is too small compared to that of R_{SS} (10^{-3}) and I_{DS0} (10^{0}). Under this condition, the approximation error and calculation error have the greatest impact from L_{SS}. Therefore, it is reasonable that the L_{SS} extraction accuracy drops as its value decreases. As seen in Fig. 8, the L_{SS} extraction accuracy is only 29.6% when it is 1 nH.

According to (9), the calculation of I_{DS0}, R_{SS}, and L_{SS} are based on the power load inductor L. The variation of L will influence the extraction results. Simulation of the of the extraction accuracy with varying L was conducted. The benchmark inductor is 200 μH. As seen in Fig. 9, the I_{DS0}, R_{SS}, and L_{SS} extraction errors are close to the variation of L, and this is consistent with (9).

The voltage drop on the power inductor V_L will decrease as the ON-state voltage of SiC MOSFET increase. This will induce extraction error according to (9). The influence of ON-resistance

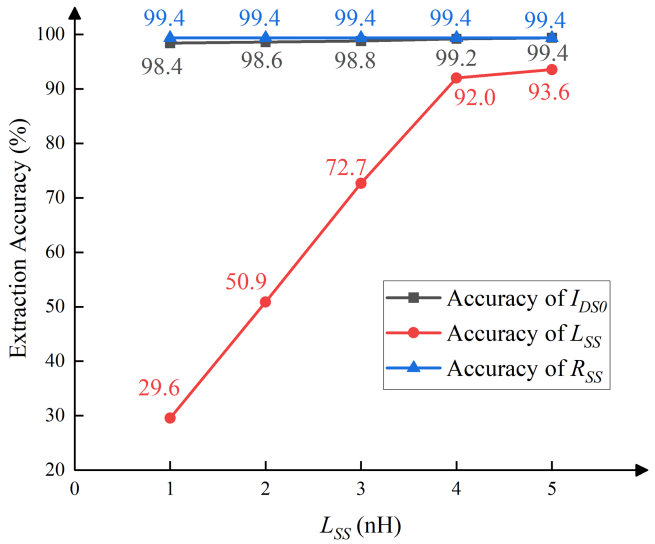

Fig. 8. I_{DS0}, R_{SS}, and L_{SS} extraction accuracy with different values of L_{SS} for the SiC MOSFET.

on extraction accuracy was simulated. As the ON-resistance of the SiC MOSFET increases, the I_{DS0}, R_{SS}, and L_{SS} extraction all decrease, as seen in Fig. 10. The ON-resistance has greater and similar impact on the extraction accuracy for R_{SS} and L_{SS} when compared to I_{DS0} extraction accuracy. This is reasonable because the R_{SS} and L_{SS} are both inversely proportional to V_L while I_{DS0} is proportional to V_L.

The influence of different I_{DS} overshoot and oscillation conditions to the extraction technique were analyzed. The junction capacitor of the freewheeling diode in Fig. 5 were modified to set different I_{DS} percentage overshoot and oscillation conditions. As seen in Fig. 11, V_{INTEG} is the output of the integrator, the oscillation cannot be fully filtered by the integrator. This will induce a dc offset to the following steady state of V_{INTEG}. To

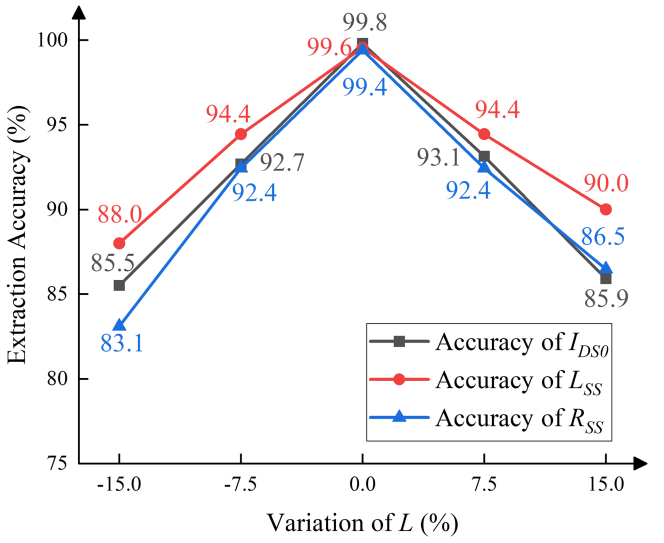

Fig. 9. I_{DS0}, R_{SS}, and L_{SS} extraction accuracy with different variations of power inductor L.

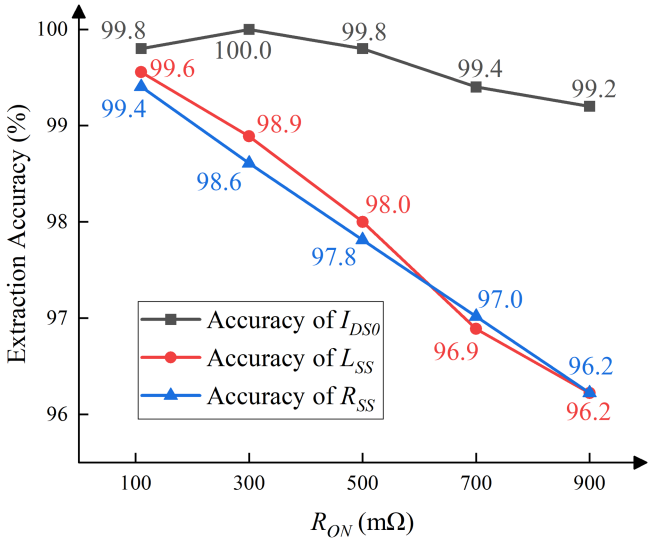

Fig. 10. I_{DS0}, R_{SS}, and L_{SS} extraction accuracy with different R_{ON} for the SiC MOSFET.

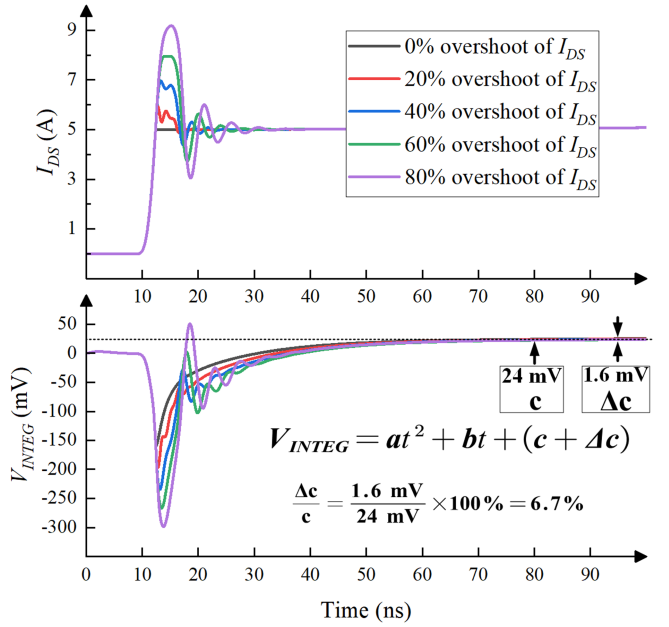

Fig. 11. I_{DS} and V_{INTEG} waveforms under different overshoot and oscillation conditions.

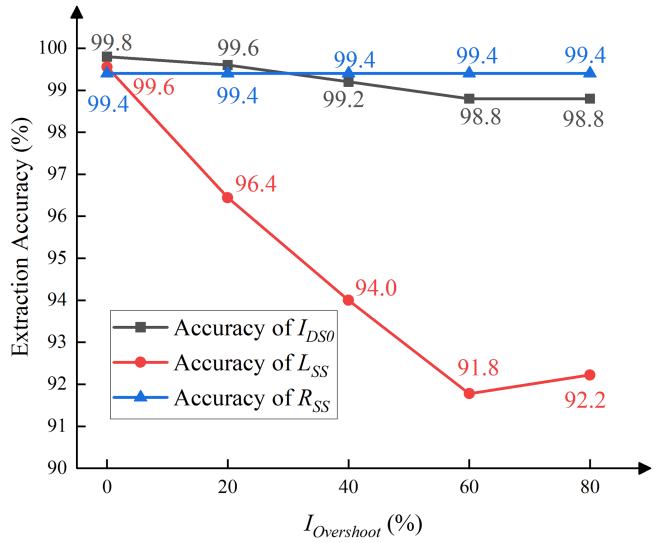

Fig. 12. I_{DS0}, R_{SS}, and L_{SS} extraction accuracy under different overshoot and oscillation conditions.

reduce the influence of overshoot and oscillation on the extraction results, a sampling delay for V_{INTEG} is necessary. However, the delayed sampling cannot completely eliminate the dc offset of V_{INTEG}. The 80% overshoot of I_{DS} introduces a 1.6 mV dc offset of V_{INTEG}. At the same time, the V_{INTEG} without I_{DS} overshoot and oscillation is 24 mV. An 80% overshoot and oscillation of I_{DS} can cause 6.7% variation in the constant term c in (7), as seen in Fig. 11.

According to (9.1), the variation of c will not influence the extraction accuracy of R_{SS}, and this is consistent with the simulation result, as seen in Fig. 12. In (9.2) and (9.3), the situations become more complicated because there is a c term under the root sign. According to the simulation results in Fig. 12, the extraction accuracy for I_{DS0} only decreases from 99.8% to 98.8% as the I_{DS} percentage overshoot increases from 0% to 80%. Therefore, it is reasonable to ignore the variation of the coefficient c under the root sign in (9.2) and (9.3). Under this condition, L_{SS} is proportional to c in (9.3) and this is consistent with the simulation results. The extraction accuracy for L_{SS} is decreased to 92.2% when the I_{DS} percentage overshoot increased to 80%. Based on the previous analysis, the accuracy of c is 93.3% (100%–6.7%), which is close to the L_{SS} extraction accuracy 92.2%.

Fig. 13 shows the extraction accuracies under different load current conditions. The accuracies for the extracted I_{DS0} and R_{SS} only decrease slightly as the load current increases. The decrease in extraction accuracies for I_{DS0}, R_{SS}, and

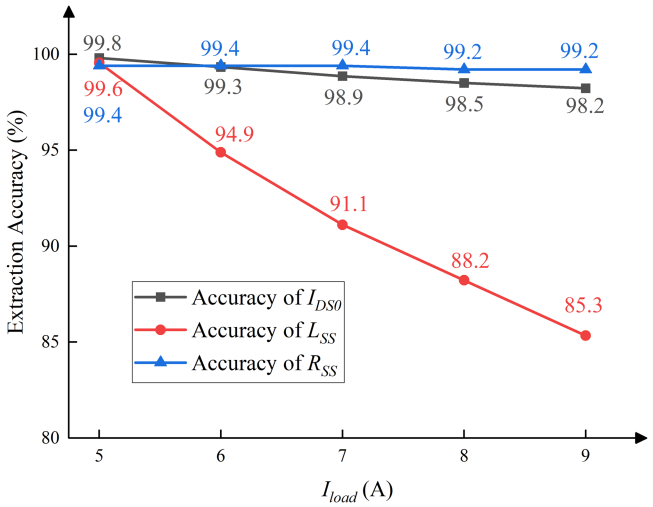

Fig. 13. I_{DS0}, R_{SS}, and L_{SS} extraction accuracy under different load current conditions.

TABLE II
EXTRACTION ACCURACY WITH DIFFERENT DIODE TYPE

Diode type	I_{DS0}	R_{SS}	L_{SS}
PIN (RFN2LAM6S)	63%	99.4%	-109.6%
Schottky (UPSC600)	99.8%	99.4%	94.2%

L_{SS} are mainly caused by the severe oscillation and overshoot when the load current increases from 5 to 9 A. The significant decrease in the extraction accuracy for L_{SS} is more sensitivity due to its very small value, in the order of nH.

In some practical applications, the reverse recovery process of diode will introduce I_{DS} overshoot current of the SiC MOSFET. Figs. 11 and 12 have shown the influence of overshoot current on the extraction results. To obtain more insights of the proposed extraction method, the extraction results with different freewheeling diode in Fig. 5 were also simulated. A p-i-n diode (RFN2LAM6S, 600 V/1.5 A/40 A) and a Schottky diode (UPSC600, 600 V/1 A/10 A) were used in the simulation for comparison. The I_{DS0}, R_{SS}, and L_{SS} extraction results are shown in Table II. The I_{DS0} and L_{SS} extraction accuracy with the p-i-n diode is 63% and −109.6%, respectively. The extraction accuracy for R_{SS} with the p-i-n diode is not changed when compared to that with the Schottky diode. The larger overshoot current caused by the reverse recovery of the p-i-n diode only influences the constant term c in (7). The error in c will decrease the extraction accuracy of I_{DS0} and L_{SS}. Therefore, a SiC Schottky diode or synchronous rectification MOSFET would be preferred over the p-i-n diode to decrease the reverse recovery current in the proposed extraction method, especially in all-SiC applications.

Therefore, to guarantee the extraction accuracy of the proposed method, small input capacitance, and low on-state resistance for the SiC MOSFET, a constant load inductance, and small I_{DS} overshoot and oscillation are required.

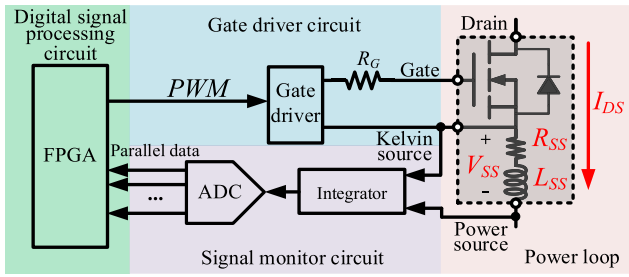

Fig. 14. Main circuit block design of the proposed extraction technique.

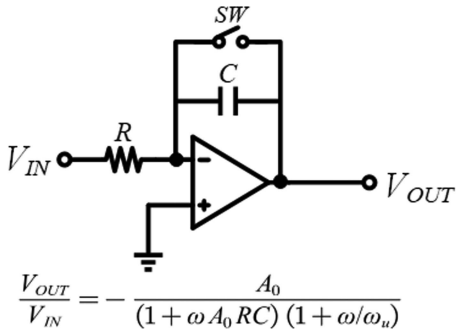

Fig. 15. *RC* integrator and its transfer function.

III. CIRCUIT DESIGN AND IMPLEMENTATION

Gate driving, signal monitoring, and digital signal processing circuits are designed to perform the proposed parasitic parameters and drain current extraction system. The schematic of the designed circuit is shown in Fig. 14.

To exploit the high-speed switching characteristics of SiC MOSFETs, a high-current capacity gate driver IC is used. The gate resistor is selected to be 4.7 Ω.

As discussed in the theoretical error analysis section, a small gate resistor can reduce the switching time t_0 and the switching loss and improve the accuracy of the proposed technique. An active *RC* integrator is built using the op-amp circuit in Fig. 14.

Considering a 25 ns drain current rise time t_0, the corresponding signal bandwidth is 15.8 MHz. According to the transfer function of the integrator shown in Fig. 15. For a 15.8 MHz input signal, if a 97% accuracy of final output value is desired, the unit gain bandwidth of the op-amp should be at least 510 MHz (e.g., LTC6228). Meanwhile, the larger the op-amp gain, the better output accuracy. However, an op-amp with large gain bandwidth product (GBW) will lead to large power consumption, and susceptible to high-frequency noise. Therefore, an op-amp with just a sufficient GBW should be selected to satisfy the accuracy requirement. In addition, a dual rail power supply should be used to decrease signal distortion.

A 12-bit 20 MHz pipeline analog to digital converter (ADC) is employed to sample the output of the integrator. The output of the pipeline ADC is parallel data, which is suitable for high-speed data processing. The output data of the ADC is processed by an FPGA to operate the least squares method and subsequent calculations, as seen in Fig. 16. The FPGA also controls the pulse width modulation (PWM) signal, the short circuit protection

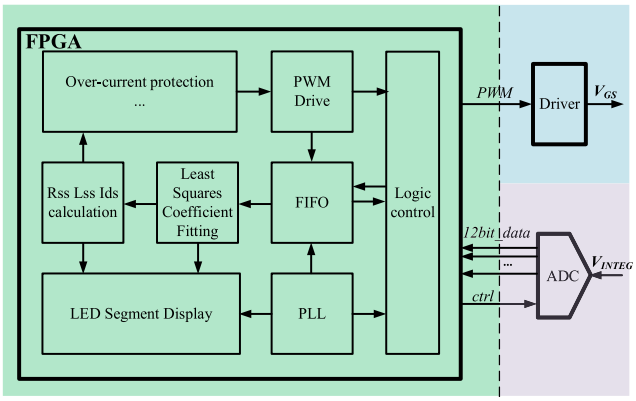

Fig. 16. FPGA functional block design for the proposed extraction technique.

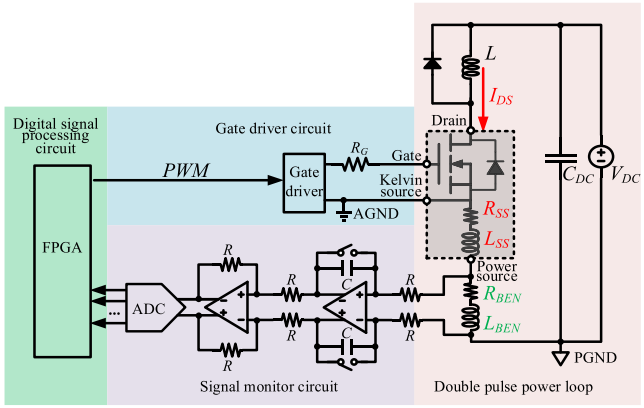

Fig. 17. Double pulse test circuit schematic for the benchmark devices.

TABLE III
DEVICES USED IN THE EXTRACTION CIRCUIT

Component	Type
Gate driver	UCC5390
Op-amp	LTC6228
ADC	ADS805E
FPGA	EP4CE15F17C8

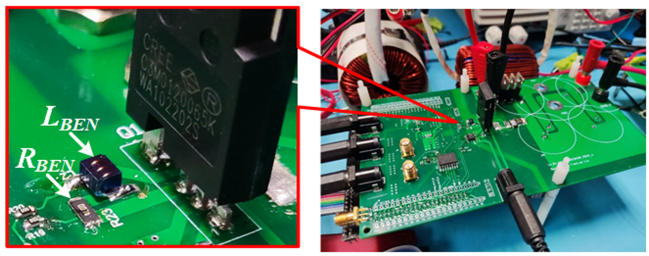

Fig. 18. Testbench of the double pulse test circuit for the benchmark devices.

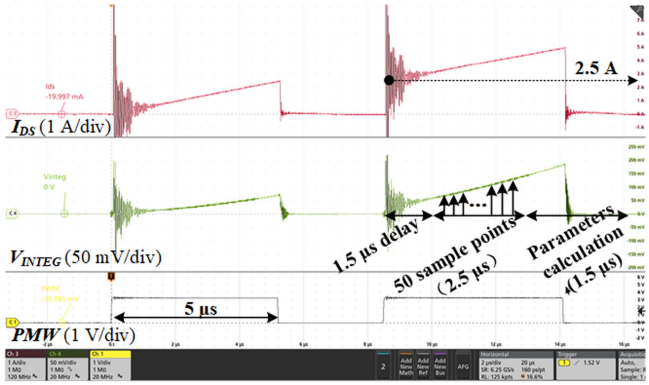

Fig. 19. Drain current and integral voltage waveforms of the double pulse test for the benchmark devices.

signal and some other functional signals. Considering power consumption and operating speed, the clock frequency of the FPGA is set to 200 MHz.

The specific devices used are shown in Table III. To verify the proposed technique, a double pulse testing (DPT) circuit was built. The power inductor is 200 μH with 4 mΩ DCR. A 1200 V/20 A SiC Schottky diode is used as the freewheeling diode to minimize the reverse recovery current. The device under test (DUT) is a C3M0120065K SiC MOSFET with ratings of 650 V and 22 A. The maximum bus voltage is set at 200 V. The double pulse tests were also conducted under different case temperatures to investigate the thermal properties of the proposed technique.

A low-side dc–dc buck converter with the proposed parasitic parameters and drain current extraction technique was also designed and implemented on PCB.

A. *Double Pulse Test for the Benchmark Resistor and Inductor*

Before extracting the parasitic Kelvin source parameters of the SiC MOSFET. A benchmark resistor R_{BEN} and a benchmark inductor L_{BEN} were inserted in series into the double pulse power loop for verifying the feasibility of the proposed technique, as shown in Figs. 17 and 18. The first pulse is used to set the initial drain current I_{DS0} of the second pulse. The drain current I_{DS} and the integral voltage V_{INTEG} waveforms are shown in Fig. 19. The switching overshoot and oscillation are severe due to the small gate resistor. The initial drain current I_{DS0} of the second pulse is set to 2.5 A. A fully differential signal monitor circuit was built to improve the common mode rejection of the integrator.

To eliminate the switching noise interface, a 1.5 μs sampling delay time is added before sampling V_{INTEG}. The ADC samples 50 data points for curve fitting. After V_{INTEG} sampling is completed, the subsequent parameter calculation process takes approximately 1.5 μs. Finally, the initial drain current I_{DS0}, benchmark resistor R_{BEN}, and benchmark inductor L_{BEN} of the second pulse are calculated. The entire sampling and calculation process can be finished within 5.5 μs. Since the calculation results are susceptible to random noise in the analog signal path, 10 independent double-pulse tests are performed. The test and calculation results are shown in Table IV. The real values of I_{DS0} is measured using a current probe. The real values of R_{BEN} is determined by measuring the voltage on the series combination of R_{BEN} and L_{BEN} when applying a 1 A current. The real values of L_{BEN} contains the air core inductance and PCB trace stray inductance. The extraction accuracies of I_{DS0}, R_{BEN}, and L_{BEN}

TABLE IV
EXTRACTION RESULTS OF THE BENCHMARK DEVICES

Parameter	I_{DS0}	R_{BEN}	L_{BEN}
Real value	2.5 A	5.9 mΩ	10 nH
Calculated value	2.43–2.74 A	5.62–5.91 mΩ	9.64–11.02 nH
Accuracy	>90%	>95%	>89%

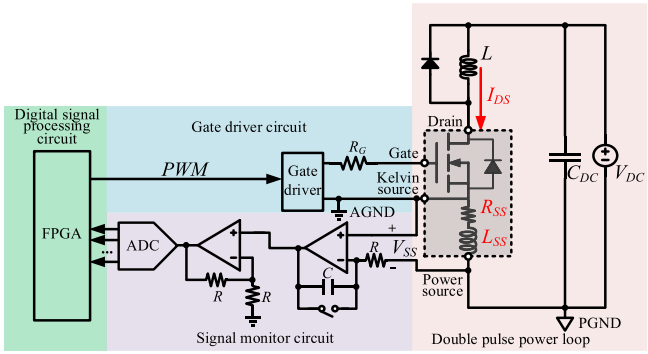

Fig. 20. Double pulse test circuit schematic for the SiC MOSFET.

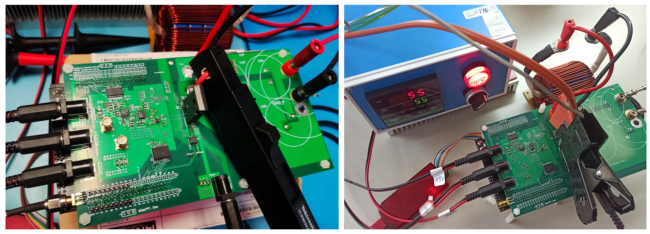

Fig. 21. Room-temperature testbench (left) and high-temperature testbench (right) of the double pulse test circuit for the SiC MOSFET.

under severe overshoot and oscillation conditions are higher than 90%, 95%, and 89%, respectively, indicating that proposed technique is feasible with reasonable noise immunity.

B. Double Pulse Test for SiC MOSFETs

The Kelvin source parameters R_{SS} and L_{SS} of the SiC MOSFET are then extracted under different drain current conditions. A single-end signal monitor circuit is built since the Kelvin source is connected to the signal ground, as shown in Fig. 20.

The testbench of the double pulse test is shown in Fig. 21. Five switching pulses are applied to the SiC MOSFET, the waveforms of drain current I_{DS} and integral voltage V_{INTEG} are shown in Fig. 22. The PWM period is 10 μs for a switching frequency of 100 kHz. This is typical for SiC MOSFETs applications. During each pulse period, R_{SS}, L_{SS}, and I_{DS0} are calculated by the proposed technique. The drain current calculation does not require temperature compensation since the calculation is based on real-time parasitic parameters, which will be verified by the following temperature test.

Table V shows the extraction results corresponding to the five pulses in Fig. 22. The I_{DS0} calculation accuracy is above 90% over a current range of 20 A. Notice that R_{SS}, L_{SS}, and I_{DS0} extracted in the last pulse have a bit more error than the previous pulses. This error mainly comes from the reduction of

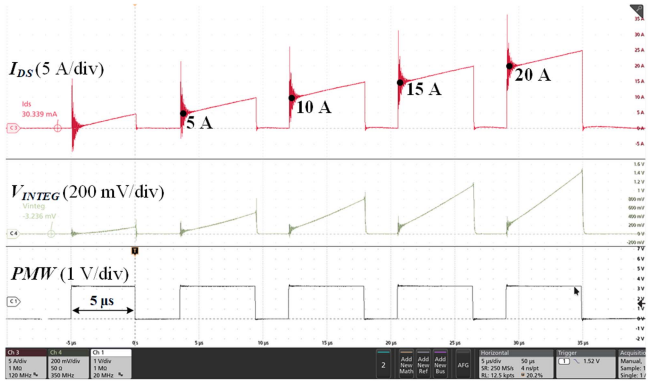

Fig. 22. Drain current and integral voltage waveforms of the double pulse test for the SiC MOSFET.

TABLE V
EXTRACTED DRAIN CURRENT AND PARASITICS

Pulse	Second	Third	Fourth	Fifth
I_{DS0}	5.30 A	10.86 A	15.16 A	18.57 A
R_{SS}	4.25 mΩ	4.27 mΩ	4.55 mΩ	4.91 mΩ
L_{SS}	4.75 nH	4.44 nH	4.65 nH	5.13 nH

V_L/L due to the magnetic saturation induced by high current. In addition, the increment of R_{SS} may be caused by the increase in case temperature. The variation of L_{SS} comes from the random error of the extraction technique, which can be eliminated by averaging multiple measurements.

C. Double Pulse Test for SiC MOSFETs Under Different Temperatures

R_{SS}, L_{SS}, and I_{DS0} are extracted with a device case temperature between 25 °C and 175 °C to investigate the temperature effect. The SiC DUTs are heated using a thermal pad to different case temperatures, as shown on the right of Fig. 21. Testing every 10 °C, a total of 16 temperature points are obtained. Five switching pulses are applied to the SiC MOSFET and 10 repetitive measurements are used to average I_{DS0}, R_{SS}, and L_{SS} calculation results under each case temperature. The I_{DS0}, R_{SS}, and L_{SS} extraction results under different case temperatures are shown in Figs. 23–25, respectively. R_{SS} increases by about 1 mΩ as the case temperature increased from 25 °C to 175 °C. R_{SS} comes from the Al or Cu bond wires with a positive temperature coefficient. Therefore, the rising trend of R_{SS} with the increase in case temperature is reasonable. As the temperature increases, the slope reduction of R_{SS} in the fifth pulse is caused by the fluctuation of V_L/L. The variations of L_{SS} from each pulse is within 0.5 nH over the entire temperature range. This is reasonable since the parasitic inductor mainly depends on the bond wire length. As the number of pulses increases, the extracted value of R_{SS} and L_{SS} show a small reduction. This is mainly caused by the magnetic saturation and L reduction when the current increase. The accuracies of the extracted drain current under different temperatures are all above 90%, indicating that the proposed drain current extraction technique does not require temperature compensation.

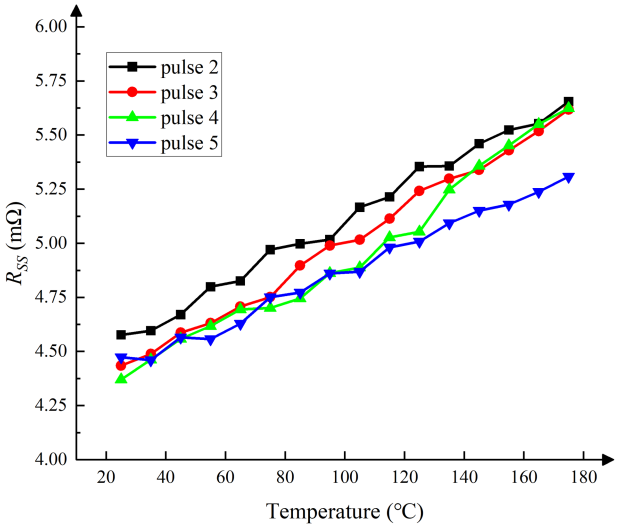

Fig. 23. Extracted source parasitic resistor R_{SS} under different temperatures.

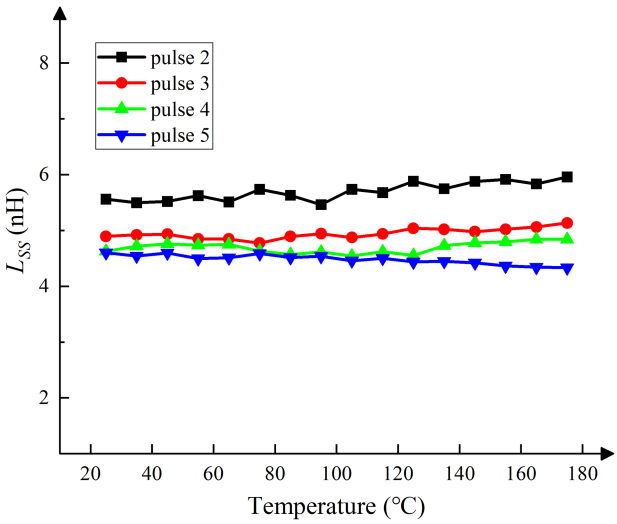

Fig. 24. Extracted source parasitic inductor L_{SS} under different temperatures.

D. Proposed Technique in Buck DC–DC Converter

In order to demonstrate the practicality of the proposed technique, an open-loop buck dc–dc converter is built with the parasitic parameters and drain current extraction circuit.

To simplify the driver and monitor circuit design, a low-side switching buck converter is designed. The input voltage of the buck is 155 V dc (equals to the rectified 110 V ac input). The output power of the buck converter is 250 W and the output voltage is 48 V. The switching frequency is 100 kHz. The power inductor is selected to be 100 μH. A 10 Ω power resistor is used as the load. The schematic of the buck converter is shown in Fig. 26. The input voltage of the buck converter is monitored by a low-power ADC for the initialization of the proposed extraction system. A high-speed comparator and a digital potentiometer were added to perform fast and adjustable overcurrent protection. A four-digit display is built to provide readout of the values of R_{SS}, L_{SS}, and

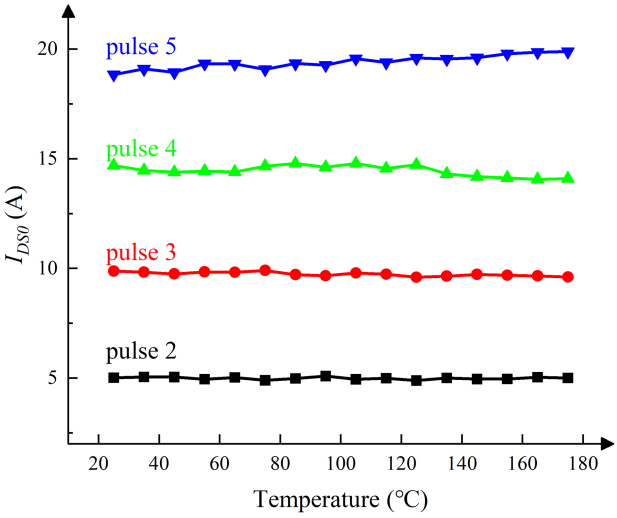

Fig. 25. Extracted initial drain current I_{DS0} under different temperatures.

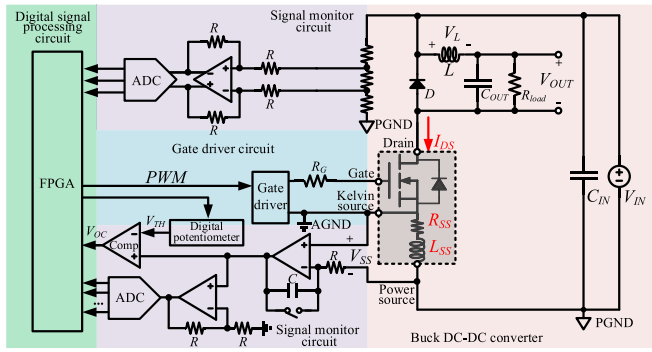

Fig. 26. Buck converter with the proposed extraction circuit.

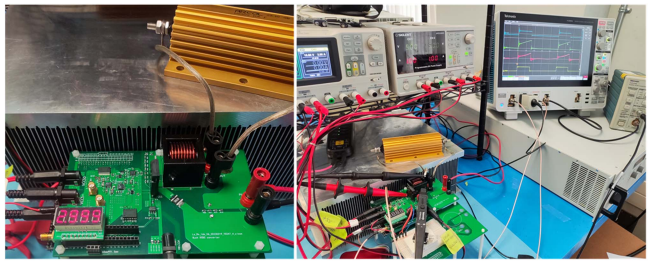

Fig. 27. Testbench of the buck converter.

I_{DS0} in real time. The buck converter and its testbench are shown in Fig. 27. The flowchart of the proposed technique in the buck converter is shown in Fig. 28. After the converter is powered up, the extraction circuit is enabled. The input voltage of the buck converter is sampled for parameter initialization. V_{INTEG} is then sampled during each PWM period. The coefficients of the quadratic function a, b, and c are calculated during each PWM cycle. The values for R_{SS}, L_{SS}, and I_{DS0} are calculated based on a, b, and c. L_{SS} can be used to set the overcurrent protection threshold $V_{TH,OC}$, which equals $(L_{SS} \times I_{TH,OC})/T_{RC}$, where $I_{TH,OC}$ is the overcurrent threshold, and T_{RC} is the integration

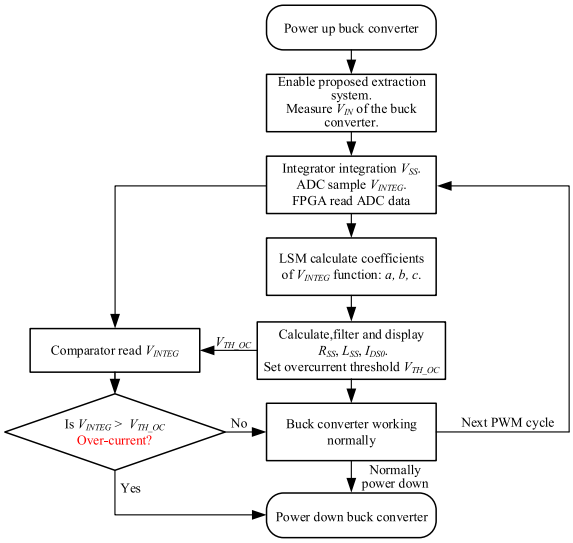

Fig. 28. Working flowchart of the buck converter.

TABLE VI
TEST RESULT OF THE BUCK CONVERTER

Parameter	Value
Input voltage	155 V
Input current	1.53 A
Output voltage	48 V
Output current	4.8 A
Output power	230 W
Efficiency	97.15 %
Switching frequency	100 kHz

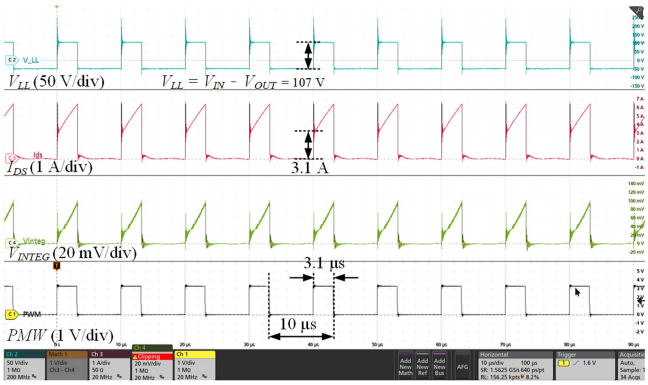

Fig. 29. Some key waveforms of the buck converter.

time constant. A high-speed comparator is employed to compare V_{INTEG} and $V_{TH,OC}$ for fast overcurrent detection. The buck converter can be powered down quickly if there is an overcurrent situation. The extraction for R_{SS}, L_{SS}, and I_{DS0} can start again in the next PWM cycle if the fault condition is removed. The extraction circuit can be disabled and enabled at any time to reduce the overall system power consumption.

The operating parameters of the buck converter are shown in Table VI. Some key signal waveforms are shown in Figs. 29 and 30. It is clear that V_{INTEG} is a quadratic function when the drain current I_{DS} is a linear ramp. V_L is the voltage across the

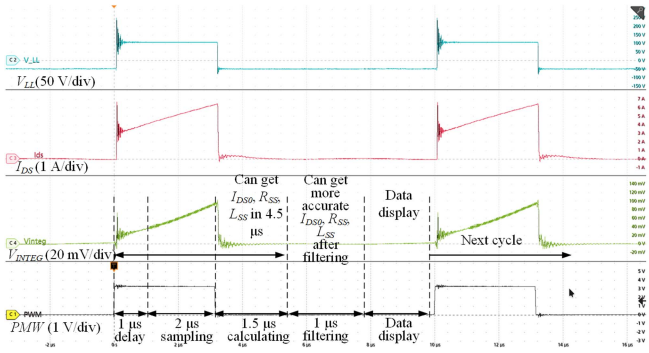

Fig. 30. Timing scheme of the extraction circuit during the operating of the buck converter (Timing zoom of Fig. 29).

TABLE VII
EXTRACTION RESULTS FROM THE BUCK CONVERTER

Parameter	I_{DS0}	R_{SS}	L_{SS}
Value	3.1 ± 0.2 A	4.9 ± 0.5 mΩ	3.5 ± 0.4 nH

TABLE VIII
MAIN SPECIFICATIONS OF THE TEST INSTRUMENTS

Testing instrument	Type and specification
Dc power supply	Siglent SPD3303, 0–32 V/3.2 A
HV power supply	Keysight N8937 A, 1500 V/30 A
Oscilloscope	Tektronix MSO44, 500 MHz
Current probe	Tektronix TCP0030A, 30 A/120 MHz
HV differential probe	Tektronix THDP0200, 1500 V/200 MHz

power inductor, which determines the slope of the drain current ramp. The detailed operation timing of the extraction circuit in the buck converter is shown in Fig. 30. This timing is similar to those in the DPT, as shown in Fig. 19. The extraction results from a single PWM cycle are unstable due to the noise interference from the power loop. Therefore, an averaging filter is added. The averaged R_{SS}, L_{SS}, and I_{DS0} can be displayed in real time.

The extraction results for the buck converter are shown in Table VII. The real I_{DS0} measured using a current probe is 3.1 A. The extracted I_{DS0} is in the range of 2.9–3.3 A. The current extraction accuracy is above 90%. The SiC MOSFETs tested are all C3M0120065K but from different batches. Based on the proposed extraction technique, R_{SS} of different devices may vary by 1 mΩ and L_{SS} of different devices may vary by 1 nH.

The overcurrent test is conducted by setting a 12 A overcurrent limit. To prevent false triggering, an $L_{SS} = 4$ nH is used. This is slightly larger than the L_{SS} extracted in the buck converter. The overcurrent protection threshold $V_{TH,OC}$ is set to 96 mV according to

$$V_{TH,OC} = \frac{L_{SS} I_{TH,OC}}{T_{RC}} = \frac{4\ \text{nH} \times 12\ \text{A}}{500\ \text{ns}} = 96\ \text{mV}. \quad (15)$$

As seen in Fig. 31, V_{OC} is the overcurrent flag signal which will pull up when I_{DS} reaches the overcurrent limit. The overcurrent detection time is 72 ns.

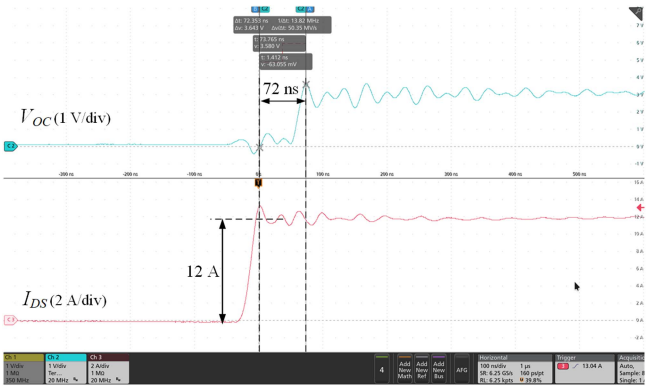

Fig. 31. Overcurrent detection time test result.

The main specifications of the test instruments are shown in Table VIII.

IV. Conclusion

An in-circuit real-time parasitic parameters and drain current extraction technique for SiC MOSFETs with Kelvin source connection is proposed. The extraction circuit includes an analog integrator, an ADC sampling circuit, and a FPGA. Based on a fixed power inductance, the proposed technique can extract the series resistance and inductance between Kelvin source and power source of SiC MOSFETs without any calibration procedure. The initial drain current of each switching period can also be extracted in real time. Without any offline pretesting data or look up table, the proposed extraction technique only relies on the voltage between the Kelvin source and the power source. The extraction process does not affect the normal switching operation of SiC MOSFETs.

The limitation of the proposed technique is based on a fixed power inductor. According to theoretical error analysis, the error in the parameter extraction is basically equal to the inductance variations. Therefore, changes to the power inductance due to saturation from over current should be avoided. According to the theoretical analysis, the extraction results rely on the power inductance and its voltage drop (or the drain current slope), not the load of the converter. The extraction accuracy for I_{DS0} and R_{SS} decrease slightly as the load current increases as verified by the simulation results. The accuracy of the extracted L_{SS} may decrease significantly due to severe oscillation and overshoot as the load current increases.

Double pulse tests under different temperatures were performed to verify the accuracy of the proposed technique. The parasitic parameters and drain current extraction time is less than 5 μs. The resistance and inductance extraction accuracies for the benchmark devices are greater than 90% and 89%, respectively. The drain current extraction accuracy is greater than 90% over a current range of 2.5–20 A between 25 °C to 175 °C.

In addition, R_{SS}, L_{SS}, and I_{DS0} of the SiC MOSFET are extracted in real time for a 100 kHz buck converter. The current extraction accuracy is above 90%.

An overcurrent protection circuit is designed and tested based on the proposed technique, and the overcurrent detection time is 72 ns.

Future work is to integrate the proposed circuit into a single chip gate driver IC. Different packages of SiC MOSFETs with Kelvin source connection will be tested to further validate the proposed technique. The extraction accuracy can be further improved by optimizing the integrating and sampling circuit design.

Acknowledgment

The authors would like to thank J. Liang and R. Li from the University of Toronto and also like to thank Q. Liu from Southeast University, China for their help in PCB fabrication and testing.

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