A Clamped Interlocking Isolated Resonant Gate Driver for High-Frequency LLC-DCX

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***Abstract*—This article proposes a clamped interlocking isolated resonant gate driver (CIRGD) to provide multiple isolated complementary drive signals for the *LLC* dc transformer (LLC-DCX). The CIRGD clamps the gate voltage to 0–V_g using clamped MOSFETs, reducing conduction loss caused by the circulation current in the drive circuit and further improving system efficiency. With appropriate parameter design, the CIRGD generates gate drive signals with the necessary deadtime, enabling soft switching of the LLC-DCX. The working principle, parameter design, loss analysis, and comparative study of the CIRGD are presented in detail. Finally, a prototype with an operating frequency of 1.3 MHz, and a power output of 48 V–6 V/30 A was developed. The experimental results show that compared with the traditional voltage source drive circuit, the proposed CIRGD can significantly enhance efficiency and reduce gate drive power loss by nearly 85%.**

***Index Terms*—DC transformer (DCX), high efficiency, high frequency, high power density, *LLC*, resonant gate driver (RGD).**

I. Introduction

EVOLUTION in complementary metal oxide semiconductor (CMOS) technology has continually lowered the core voltage but increased the core current of microprocessors [1]. High currents result in more line loss, whereas low voltages require power converters with higher step-down ratios. In scenarios where there is low voltage but high current, the duty cycle of traditional buck converters that use pulsewidth modulation (PWM) technology becomes smaller, resulting in a higher ratio of loss to energy transmission power. This has a negative impact on the overall efficiency of the system [2], [3]. Therefore, the 48-V power supply architecture is proposed to replace the traditional 12-V power supply architecture [4], *LLC* dc transformer (LLC-DCX) operates at a fixed resonant frequency point, enabling soft switching for all MOSFETs and achieving high conversion efficiency and power density at high switching frequencies [5], [6], [7]. When traditional voltage source driver ICs are employed, the driver losses in LLC-DCX are relatively substantial at high switching frequencies. Additionally, both the high-side and low-side drives of LLC-DCX require isolated power supplies, leading to an increased proportion of auxiliary power, thereby limiting the further enhancement of power density and efficiency. Consequently, for the gate driver in LLC-DCX, achieving multiple isolated drives, reducing footprint, and enhancing energy recovery efficiency are critical factors for improving system power density and efficiency. For high-switching-frequency LLC-DCX, resonant gate drivers (RGDs) must possess the following characteristics:

1) energy recovery at high operating frequencies;
2) provision of multiple complementary gate drive signals;
3) high-side and low-side drive isolation capability;
4) simple control logic for integration;
5) level clamping functionality to prevent false triggering and enhance system reliability.

In the past two decades, many RGDs have been introduced [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], but very few have been reported for dedicated use in LLC-DCX [23]. RGDs proposed in the literature [9], [10], [11], [12], [13], [14], [15], [16], [17], [18] are predominantly designed for individual MOSFET drivers and are primarily intended for PWM-based high-switching-loss topologies. These RGDs necessitate large drive currents to mitigate MOSFET switching losses, exhibit relatively low gate energy recovery ratios, and require isolation or bootstrapping circuits to drive high-side MOSFETs in the half-bridge branch [17]. This increases component count and reduces system power density. On the other hand, literature [19] presents a dual-channel isolated RGD suitable for full-bridge zero voltage switching (ZVS) topologies, optimizing the control circuitry to achieve the same functionality at lower cost while reducing the number of MOSFETs in the gate driver circuit [20]. Building upon [19] and [20], a level-shifting circuit is introduced to implement asymmetric gate drive voltages, benefiting SiC devices with asymmetric breakdown voltages, thus improving converter efficiency and reliability, as demonstrated in [21] and [22]. Nevertheless, these RGDs require additional resonant inductors and substantial magnetic component designs [19], [20], [21], [22], making it challenging to achieve miniaturization in high-frequency layouts. A novel transformer-based isolated RGD for LLC-DCX is proposed in [23], which achieves multiple isolated drives through the transformer while reducing drive losses in the RGD. This significantly enhances system

Manuscript received 15 May 2023; revised 26 August 2023 and 8 October 2023; accepted 11 November 2023. Date of publication 15 November 2023; date of current version 16 February 2024. This work was supported in part by Jiangsu Provincial Key R&D Program (Industry Anticipation and Generic Key Technologies) under Grant BE2022048-3 and in part by the programs of the National Natural Science Foundation of China under Grants 52177172, 62234005, and 52207192. Recommended for publication by Associate Editor T. Mishima. *(Corresponding author: Qinsong Qian.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3332876.

Digital Object Identifier 10.1109/TPEL.2023.3332876

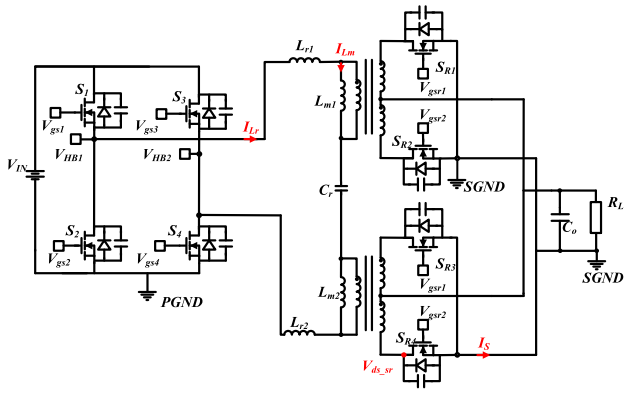

Fig. 1. Schematic of the full-bridge LLC-DCX.

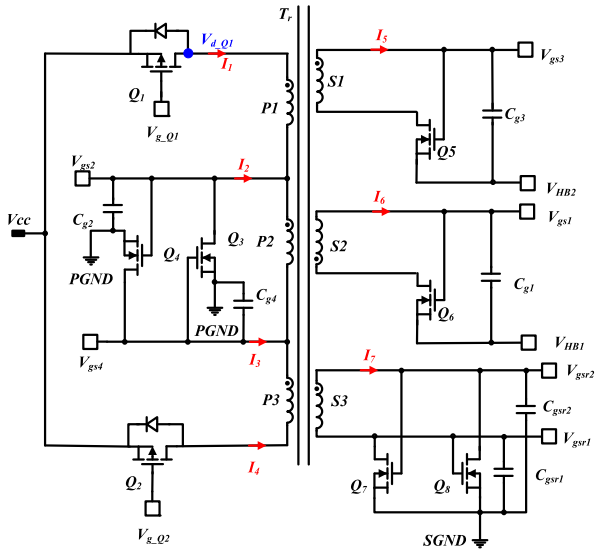

Fig. 2. Schematic of the proposed CIRGD.

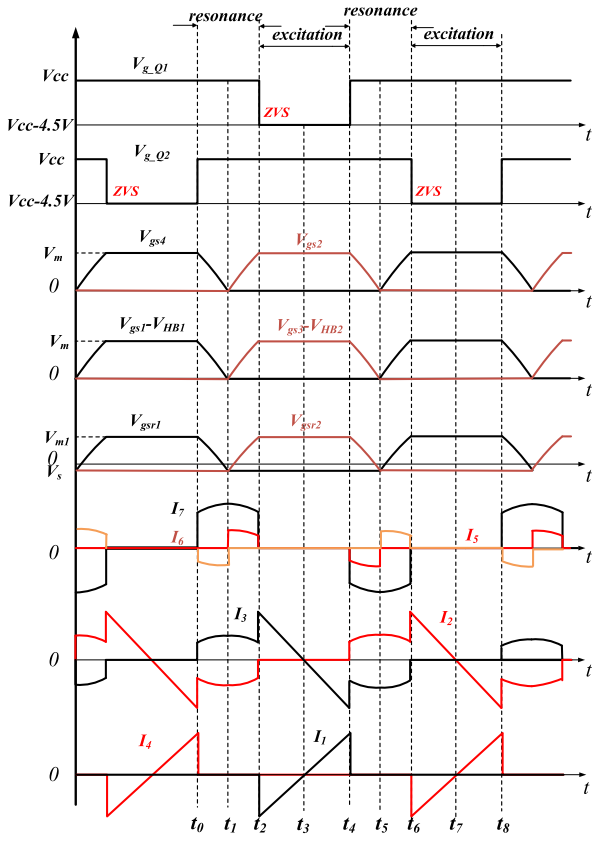

Fig. 3. Key waveforms of the proposed CIRGD.

conversion efficiency and power density. However, the driver implements a drive voltage of -V_g to V_g, resulting in substantial circulating current losses in the driver circuit and large magnetic component volumes. There is still room for further improvement in efficiency and power density.

This article introduces a clamped interlocking isolated RGD (CIRGD) tailored for LLC-DCX. CIRGD requires only two external drivers, one for the power supply. All MOSFETs achieve soft switching, and the transformer provides multiple complementary isolated resonant gate drive signals for LLC-DCX. The clamped interlock circuit clamps the drive voltage to 0–V_g, reducing the volume of magnetic components and achieving lower conduction losses with reduced switching stress. This results in improved efficiency, power density, and reliability of the system. The working principle, parameter design, loss analysis, and comparative study of CIRGD are covered in detail in this article. Finally, a 48–6 V/30 A experimental prototype is presented to validate the proposed circuit's effectiveness.

II. Proposed Resonant Gate Driver Circuit

The proposed CIRGD provides the drive signals for MOSFETs in the full-bridge LLC-DCX illustrated in Fig. 1. As depicted in Fig. 2, the CIRGD is composed of two P-MOSFETs, six N-MOSFETs, and a multiwinding transformer T_r, and C_{g1}-C_{g4} and C_{gsr1} and C_{gsr2} refer to the gate capacitors of the primary-side and secondary-side MOSFETs in the full-bridge LLC-DCX, respectively. The use of six N-MOSFETs eliminates the need for additional control signals, and the transformer T_r provides the necessary isolation function to obtain both the high-side drive signals of the half-bridge leg and the drive signals of the secondary-side MOSFETs. By switching the two P-MOSFETs accordingly, the CIRGD can supply drive signals for all of the MOSFETs in the full-bridge LLC-DCX circuit.

As shown in Fig. 3, the key waveform signals of the proposed CIRGD are as follows: the red logo indicates the positive direction of the current in Fig. 2. V_{g_Q1} and V_{g_Q2} represent the gate-to-source voltage of Q_1 and Q_2, respectively. V_{gs2} and V_{gs4} are the driving signals of S_2 and S_4, V_{gsr1} and V_{gsr2} are the driving signals of $S_{R1,3}$ and $S_{R2,4}$, and V_{gs1}-V_{HB1} and V_{gs3}-V_{HB2} are the driving signals of S_1 and S_3, respectively.

The proposed CIRGD is divided into eight intervals throughout one switching cycle, as illustrated in Fig. 4(a)–(h). The transformer turns ratio is set to $P1$: $P2$: $P3$: $S1$: $S2$: $S3 = N_{P1}$: N_{P2}: N_{P3}: N_{S1}: N_{S2}: N_{S3}, and the winding coupling coefficient is $K = 1$. Since the primary-side switch tube model is identical, the winding $P2$: $S1$: $S2$ is equal to N_{P2}: N_{S1}: N_{S2}, resulting in a 1:1:1

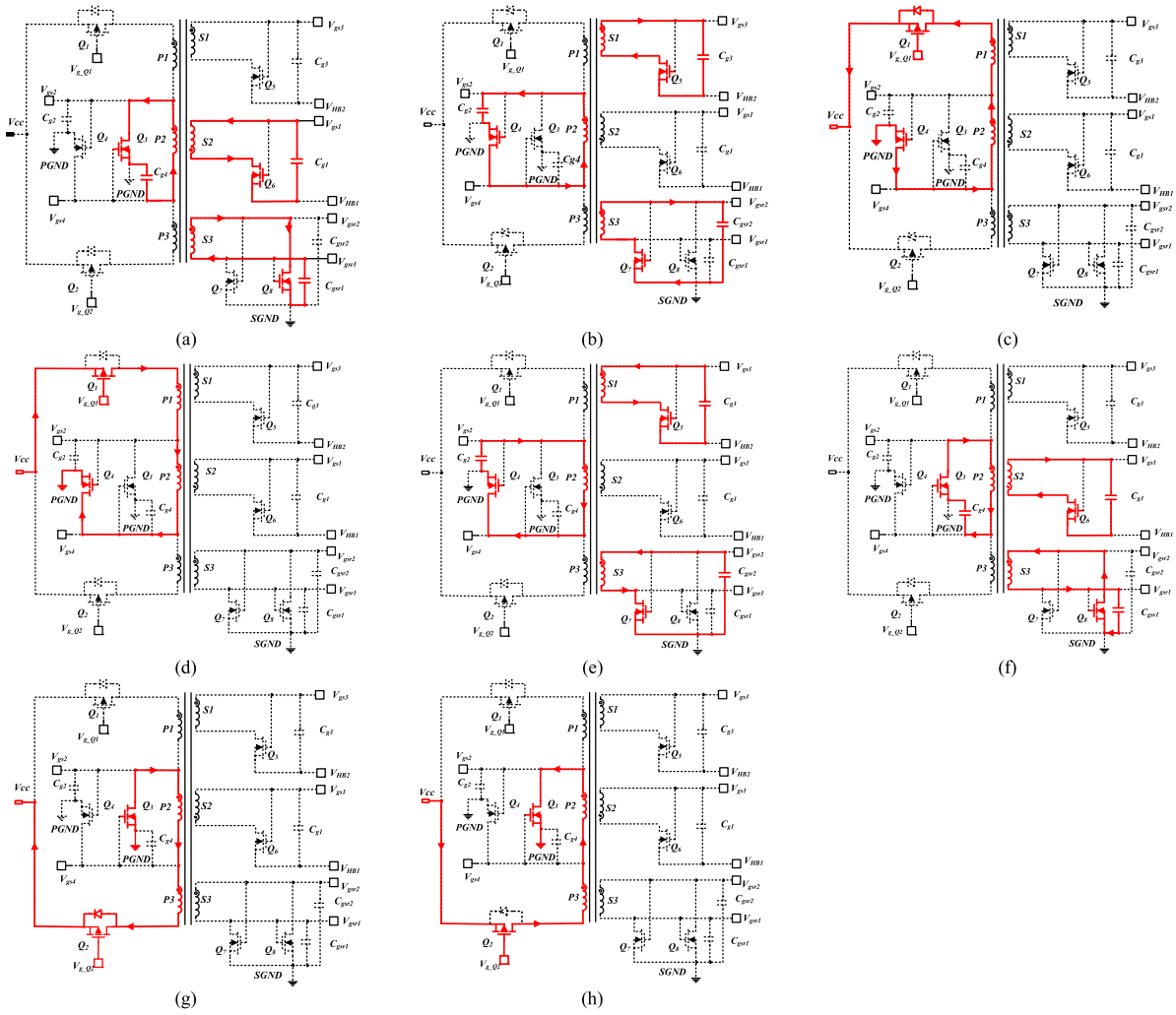

Fig. 4. Critical current loops at each interval in a switching cycle. (a) Interval 1 [t_0–t_1]. (b) Interval 2 [t_1–t_2]. (c) Interval 3 [t_2–t_3]. (d) Interval 4 [t_3–t_4]. (e) Interval 5 [t_4–t_5]. (f) Interval 6 [t_5–t_6]. (g) Interval 6 [t_6–t_7]. (h) Interval 8 [t_7–t_8].

ratio. Additionally, the gate capacitors of the secondary-side MOSFETs are greater than those of the primary-side MOSFETs, and the parasitic parameters are disregarded.

Each modal equivalent of the circuit is shown in Fig. 4, where the red part is the current loop. The analysis of each interval is presented below:

Interval 1 [t_0–t_1]: The initial voltage on C_{g4}, C_{g1}, and C_{gsr1} is high, the clamped MOSFETs Q_3, Q_6, and Q_8 are turned ON, and all other MOSFETs are turned OFF, resulting in the formation of an LC resonant loop with the gate capacitors and transformer. The simplified equivalent circuit diagram shown in Fig. 5(a) illustrates that the transformer is equivalent to the resonant inductor L_{rd}, and the gate capacitors of the secondary-side MOSFETs are equivalent to $C_{gsr1'}$. As a result, C_{g4}, C_{g1}, and $C_{gsr1'}$ discharge in resonance, the resonant inductor charges in a resonant manner, the gate-source voltage $v_{Cg}(t)$ drops, and the current on the resonant inductor rises. Energy transfer from the gate capacitors to the resonant inductor continues until the gate capacitance is discharged completely.

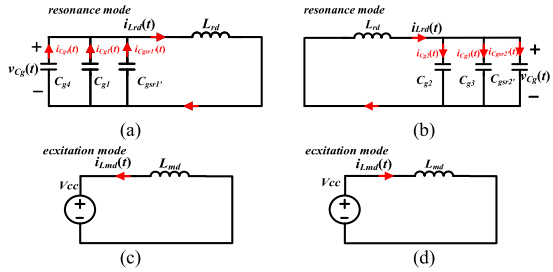

Fig. 5. Simplified equivalent circuit. (a) Interval 1 [t_0–t_1]. (b) Interval 2 [t_1–t_2]. (c) Interval 3 [t_2–t_3]. (d) Interval 4 [t_3–t_4].

Interval 2 [t_1–t_2]: The transformer's equivalent resonant inductor current, i_{Lrd}(t), is continuous and charges the gate capacitors of the clamped MOSFETs, namely Q_4, Q_5, and Q_7 (not elaborated here). The outcome is that the drain-source voltage of Q_4, Q_5, and Q_7 decreases to 0 V, and the gate-source voltage of Q_4, Q_5, and Q_7 begins to rise, resulting in the achievement of ZVS for

Q_4, Q_5, and Q_7, and C_{g3}, C_{g2}, and $C_{gsr2'}$ (where $C_{gsr2'}$ represent the equivalent gate capacitors of the secondary-side MOSFETs) are charged until the clamped MOSFETs are fully turned ON, the simplified *LC* resonant loop is shown in Fig. 5(b). As there is an initial current i_{rp} on the resonant inductor, the current on the resonant inductor L_{rd} charges the gate capacitors C_{g3}, C_{g2}, and $C_{gsr2'}$. Subsequently, the resonant inductor current, i_{Lrd}(t), drops, and energy is transferred from the resonant inductor to the gate capacitors until the voltage of V_{gs2}, V_{gs3}-V_{HB2}, and V_{gsr2} is clamped by *Vcc*.

Interval 3 [t_2–t_3]: The gate voltage V_{gs2} is clamped by *Vcc*, triggering Q_1 to turn ON for ZVS. In this operation, the transformer energy is recuperated, and its current flows into the power supply until it reaches zero. Simplifying this equivalent circuit results in Fig. 5(c), where the inductance transforms into the *P*1 and *P*2 windings and is identified as the magnetic inductor L_{md}.

Interval 4 [t_3–t_4]: The power supply charges the magnetic inductor L_{md}, and the magnetic inductor current i_{Lmd}(t) rises in reverse until Q_1 is turned OFF.

In the second half of the cycle, which is also a similar resonant process, no further explanation is needed. It can be observed that the clamped MOSFETs Q_3-Q_8 require no additional control to achieve ZVS throughout the working cycle. The switching sequence of the two P-MOSFETs is controlled by 180° and the duty cycle setting ensures that ZVS is maintained, allowing for efficient operation and a simple control mechanism for all MOSFETs during the duty cycle.

Based on the aforementioned analysis of the current working states in the drive transformer, the working mode of CIRGD can be divided into two modes. The first is the resonant mode, as indicated in Fig. 4(a), (b), (e), and (f). During this mode, the current in the transformer changes through resonance and can be represented by the resonant inductor L_{rd}. The gate capacitors of the MOSFETs are charged and discharged. The other mode is the excitation mode, shown in Fig. 4(c), (d), (g), and (h), where the current in the transformer operates through excitation, and the transformer can be represented by the magnetic inductor L_{md}. The magnetic inductor L_{md} is excited and demagnetized through the power supply *Vcc*.

III. Parameter Design and Loss Analysis

To ensure the proper functioning of the LLC-DCX, the designed driver must fulfill the following fundamental requirements:

1) an appropriate drive voltage for ensuring normal switching;
2) suitable drive timing to facilitate synchronous rectification;
3) suitable deadtime to enable the implementation of ZVS conditions.

The LLC-DCX design should include the implementation of switch transistors, excitation inductance, resonance parameters, and deadtime in the main topology *LLC*. These design parameters are provided before the design of the CIRGD. Section III-A introduces the design of the transformer winding and the power supply *Vcc* to satisfy conditions (1) and (2). Section III-B analyzes the influence of the key parameter L_{rd} on the deadtime T_{dead} to ensure that the designed CIRGD offers an appropriate deadtime. It also examines the impact of L_{rd} on i_{rp} to facilitate subsequent loss analysis. In Section III-C, the focus is on the design of the drive transformer, ensuring the attainment of a suitable L_{rd}. Section III-D evaluates the loss of the proposed driver, achieving an 85.9% improvement compared to conventional driver ICs. Finally, Section III-E compares relevant literature to exemplify the use of clamping transistors in reducing power consumption.

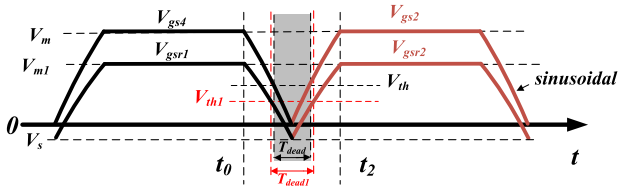

Fig. 6. Simplified voltage waveforms of gate capacitors.

A. Design of Transformer Turns Ratio and Power Supply V_{cc}

To ensure high efficiency, the LLC-DCX must operate at the resonant frequency, enabling synchronous rectification, as shown in Fig. 6. In the proposed CIRGD design, the drive signals of the primary-side and secondary-side MOSFETs of the LLC-DCX are coupled through the drive transformer but remain isolated from each other. To maintain synchronous rectification at the resonant frequency, the secondary-side deadtime T_{dead1} is not less than the primary-side deadtime T_{dead}. To satisfy this requirement, the following formula must be satisfied:

$$\frac{T_{\mathrm{dead1}}}{T_{\mathrm{dead}}} = \frac{V_{\mathrm{th1}} - V_s}{V_{\mathrm{th}}} \times \frac{V_m}{V_{m1} - V_s} \geq 1 \tag{1}$$

$$\frac{V_m}{V_{m1} - V_s} = \frac{N_{P2}}{N_{S3}} \tag{2}$$

where V_m is the amplitude of the primary drive voltage, V_{th} is the threshold voltage of the primary-side MOSFETs, V_{m1} is the amplitude of the secondary drive voltage, V_{th1} is the threshold voltage of the secondary-side MOSFETs, and V_s is the shift level of the secondary side, selected to ensure that the deadtime of the secondary side is not less than the deadtime of the primary side. Level-shifting circuits are not the focus of this article and are not covered in detail here. V_m and V_{m1} need to be able to make MOSFETs fully turned ON. Because the circuit waveform is symmetrical, the design $P1{:}P3 = 1{:}1$; according to the above analysis, it can be known that the design of the primary winding affects the ratio of *Vcc* and V_m, and the following equation is satisfied:

$$\frac{Vcc}{V_m} = \frac{N_{P1} + N_{P2}}{N_{P2}}. \tag{3}$$

Considering the limitation of the number of transformer layers and the influence of the power supply *Vcc*, the power supply *Vcc* is selected according to the system design 12 V, the driving voltage of the primary-side MOSFETs in LLC-DCX is designed to

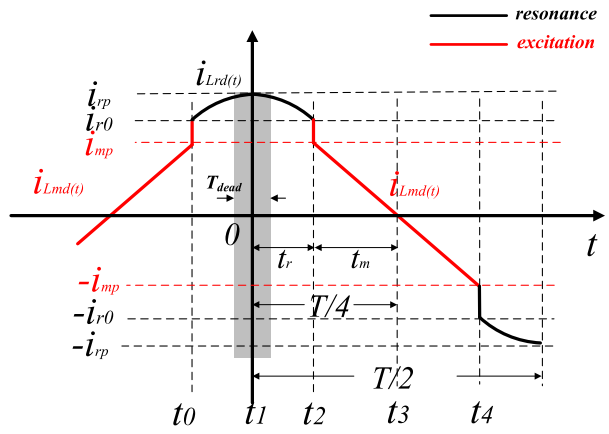

Fig. 7. Equivalent current waveform in transformer.

be 8 V to fully turn ON, and the driving voltage of the secondary-side MOSFETs is designed to be 5 V to make them fully turned ON, so the turn ratio of the transformer is designed as $P1$: $P2$: $P3$: $S1$: $S2$: $S3 = N_{P1}$: N_{P2}: N_{P3}: N_{S1}: N_{S2}: $N_{S3} = 2$: 4: 2: 4: 4: 3.

B. Design of Resonant Inductor L_{rd}

To design the right deadtime for the LLC-DCX, the resonant inductor L_{rd} needs to be carefully designed. According to the previous analysis, as shown in Fig. 3, during the interval t_0–t_2, the driving voltage changes, and the resonant inductor L_{rd} and the gate capacitors resonate at this time, ignoring the parasitic parameters in the circuit, and the simplified equivalent circuit diagram is shown in Fig. 5(a) and (b), where C_{g1}-C_{g4} are the gate capacitors of S_1–S_4, $C_{gsr1'}$ is the equivalent value of C_{gsr1}, which is the sum of the gate capacitance of secondary-side S_{R1} and S_{R3}, and $C_{gsr2'}$ is the equivalent value of C_{gsr2}, which is the sum of the gate capacitance of secondary-side S_{R2} and S_{R4}. The resonant inductance L_{rd} is the inductance value of winding $P2$, and the magnetic inductance L_{md} is the inductance value of the sum of the windings $P1$ and $P2$. The relationship between the magnetic inductor L_{md} and the resonant inductor L_{rd} is given as

$$L_{md} = (N_{P1} + N_{P2})^2 / N_{p2}^2 \times L_{rd}. \tag{4}$$

The relationship between C_{gsr1} and $C_{gsr1'}$ is given as

$$C_{gsr1'} = \frac{N_{S3}^2}{N_{P2}^2} C_{gsr1}. \tag{5}$$

Similarly, the relationship between C_{gsr2} and $C_{gsr2'}$ is given as

$$C_{gsr2'} = \frac{N_{S3}^2}{N_{P2}^2} C_{gsr2}. \tag{6}$$

The equivalent current waveform in the transformer is shown in Fig. 7, where the black line indicates that the transformer is equivalent to the resonant inductor L_{rd} at this time, and the red line indicates that the transformer is equivalent to the magnetic inductor L_{md} at this time. According to the law of conservation of energy, at the time of t_2, the resonant inductance L_{rd} and the magnetic inductance L_{md} are converted to each other, where the current relationship satisfies the following formula:

$$\frac{1}{2} L_{md} \times i_{mp}^2 = \frac{1}{2} L_{rd} \times i_{r0}^2 \tag{7}$$

where i_{mp} is the current value of the magnetic inductor L_{md} at the moment t_2 and i_{r0} is the current value of the resonant inductor L_{rd} at the time of t_2.

According to the previous analysis, during the interval t_0–t_1, the resonant inductor L_{rd} forms a resonant loop with C_{g4}, C_{g1}, and $C_{gsr1'}$, ignoring the influence of other parasitic parameters, and the simplified equivalent circuit is shown in Fig. 5(a), at this stage, the initial value of the voltage across the gate capacitor is V_m, which is discharged in the form of resonance until the t_1 moment, and is completely discharged to zero potential. Similarly, during the interval t_1–t_2, the resonant inductor L_{rd} forms a resonant loop with C_{g2}, C_{g3}, and $C_{gsr2'}$, ignoring the influence of other parasitic parameters, and the simplified equivalent circuit diagram obtained is shown in Fig. 5(b), at this stage, the initial voltage across the gate capacitor is zero, charged in the form of resonance, until the moment t_2, the voltage of the gate capacitor reaches V_m is clamped. Because the primary-side MOSFETs are the same and the secondary-side MOSFETs are the same, ideally, the resonance process is completely symmetrical

$$C_{gsall} = C_{g1} + C_{g4} + C_{gsr1'} = C_{g3} + C_{g2} + C'_{gsr2} \tag{8}$$

$$L_{rd} \times \frac{di_{Lrd}(t)}{dt} = v_{Cgs}(t) \tag{9}$$

$$C_{gsall} \times \frac{dv_{Cgs}(t)}{dt} = -i_{Lrd}(t). \tag{10}$$

As shown in Fig. 7, i_{rp} is the current of the resonant inductor L_{rd} at time t_1, i_{r0} is the current of the resonant inductor L_{rd} at time t_0, and at time t_1, all the energy on the gate capacitor is converted into energy on the resonant inductor, ignoring other losses. According to the law of conservation of energy

$$\frac{1}{2} L_{rd} \times i_{rp}^2 = \frac{1}{2} L_{rd} \times i_{r0}^2 + \frac{1}{2} C_{gsall} \times V_m^2. \tag{11}$$

As shown in Fig. 6, V_{th} is the threshold voltage of the switching transistor, and T_{dead} is the deadtime. Combining (9) and (10) and then solving, we get

$$v_{Cgsall}(t) = \sqrt{\frac{L_{rd}}{C_{gsall}}} \times i_{rp} \sin\left(\frac{1}{\sqrt{L_{rd} \times C_{gsall}}} t\right). \tag{12}$$

So there is

$$T_{\text{dead}} = 2\sqrt{L_{rd} \times C_{gsall}} \arcsin\left(\sqrt{\frac{C_{gsall}}{L_{rd}}} \times \frac{V_{\text{th}}}{i_{rp}}\right) \tag{13}$$

$$t_r = \sqrt{L_{rd} \times C_{gsall}} \arcsin\left(\sqrt{\frac{C_{gsall}}{L_{rd}}} \times \frac{V_m}{i_{rp}}\right). \tag{14}$$

As shown in Fig. 7, where t_r is the length of time from t_1–t_2 and the period of LLC-DCX is T and t_m is the length of time from t_2–t_3. During the t_2–t_3 time period, the current i_{Lmd} expression

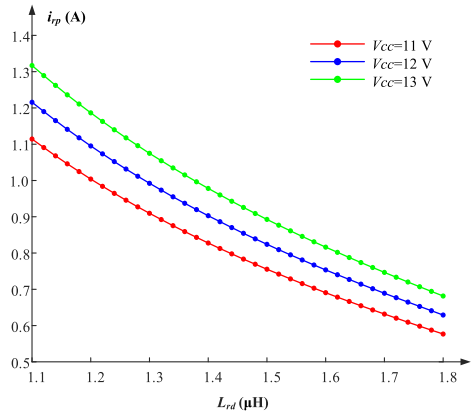

Fig. 8. Calculated i_{rp} under different Vcc and L_{rd}.

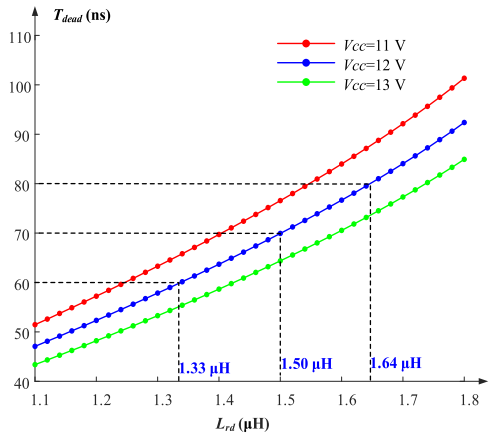

Fig. 9. Calculated deadtime $T_{\rm dead}$ under different Vcc and L_{rd}.

of the magnetic inductor is as follows:

$$L_{md}\frac{di_{Lmd}(t)}{dt} = Vcc \tag{15}$$

$$t_m = \frac{L_{md} \times i_{mp}}{Vcc} \tag{16}$$

$$t_r + t_m = \frac{T}{4}. \tag{17}$$

It is worth noting that in the actual design process, it is necessary to consider the equivalent capacitance associated with the MOSFET's gate and the parasitic capacitor of the clamped switch Q_3–Q_8. Due to space restrictions, this will not be further elaborated on in this article. Assuming a switching frequency of $f_s = 1.3$ MHz, using (8)–(17), Fig. 8 illustrates the relationship between i_{rp}, resonant inductance L_{rd}, and drive voltage Vcc. Furthermore, Fig. 9 demonstrates the relationship between deadtime $T_{\rm dead}$, resonant inductance L_{rd}, and driving voltage amplitude Vcc. It can be observed that the current i_{rp} decreases as the resonant inductance L_{rd} increases, whereas it increases with the rise in driving voltage Vcc. Deadtime increases as resonant inductance L_{rd} increases but decreases with the rise in driving voltage Vcc. It is evident that larger current i_{rp} results in greater losses, requiring MOSFETs with higher current ratings and larger core designs while still requiring a faster drive speed and smaller deadtime.

In LLC-DCX, the deadtime needs to be carefully designed to ensure the implementation of ZVS, as shown in Fig. 9. The larger the inductance value of L_{rd}, the longer the deadtime $T_{\rm dead}$, through different drive voltages Vcc, can also affect the deadtime $T_{\rm dead}$. The larger the drive voltage Vcc, the smaller the deadtime $T_{\rm dead}$. In the case of driving voltage $Vcc = 12$ V, the theoretical analysis shows that the resonant inductors L_{rd} of 1.33 μH, 1.50 μH, and 1.64 μH correspond to deadtime $T_{\rm dead}$ of 60 ns, 70 ns, and 80 ns, respectively. However, for the proposed resonant gate driver CIRGD, it is necessary to ensure that the resonance period of the equivalent resonant circuit LC is less than the switching period of LLC-DCX, so the following equation should be satisfied:

$$2\pi\sqrt{L_{rd} \times C_{gsall}} < T. \tag{18}$$

where L_{rd} needs to be less than 2.01 μH when the total gate capacitance C_{gsall} is 7.44 nF and the period of LLC-DCX is 769 ns.

C. Design of Transformer Core and Winding Layout

The proposed CIRGD design operates at 1.3 MHz, and the high-frequency magnetic material 3F46 is selected as the core material for the transformer. To facilitate the winding layout, the drive transformer core in CIRGD adopts the UI core design scheme. The maximum flux density ($B_{\rm max}$) inside the core is selected to be 50 mT, and the core loss density (p_v) is approximately 200 mW/cm^3. Limited by process limitations, the distance between the middle columns of the UI core L_W should be greater than 2 mm, and the height of the middle column h_c should be greater than 2.5 mm, by increasing the air gap l_g to reduce the maximum magnetic flux density of the core, increasing the air gap will reduce the inductance of L_{rd}, and compensate for the inductance of L_{rd} by increasing the area of the central column A_e. It can be seen from the following formula [24]:

$$B_{\rm max} = \frac{\mu_0 \mu N_{P2}}{l} i_{rp} \tag{19}$$

$$L_{rd} = \frac{\mu_0 \mu N_{p2}^2 A_e}{l} \tag{20}$$

$$l = \mu l_g + \text{MPL} \tag{21}$$

where μ is the relative permeability of the core material, l represents the equivalent length of the magnetic circuit, and magnetic path length (MPL) indicates the length of the magnetic circuit inside the core.

As shown in Fig. 10, after the transformer core and winding are designed, the required resonant inductance is obtained by changing the air gap thickness, as shown in Fig. 10. The longer the deadtime required by LLC-DCX, the larger the resonant inductance L_{rd} can be obtained by selecting a smaller air gap length l_g.

To make the magnetic flux density in the I plate equal to the magnetic flux density in the core column, the cross-sectional area is designed to be equal to the area of the central column A_e,

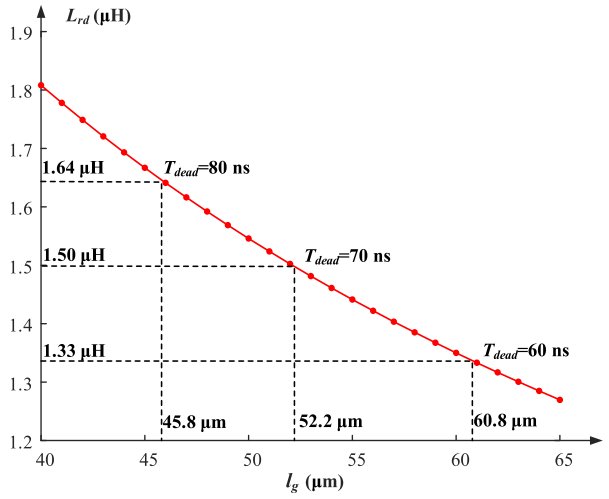

Fig. 10. Calculated resonant inductor L_{rd} under different air gap l_g.

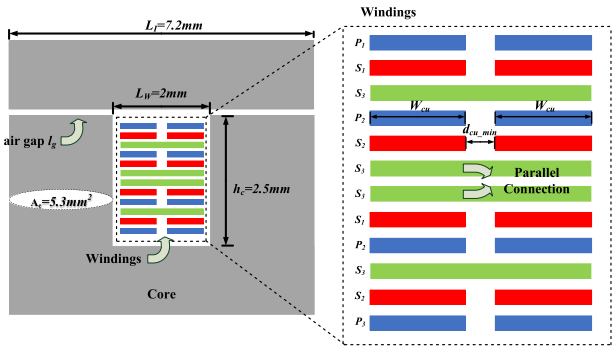

Fig. 11. Cross-sectional view of the drive transformer and arrangement of the windings.

and the length L_I is the sum of the distance between the core and the diameter of the column. The volume of the UI core is expressed as [24]

$$V_{\text{core}} = 2 \times A_e \times (L_I + h_c). \tag{22}$$

The use of the limit design of process parameters of the core to increase the power density of the system, the winding arrangement of the drive transformer, and the size of the core structure as shown in Fig. 11, the UI-type core window width L_W is 2 mm, the height h_c of the middle column should be 2.5 mm, and the cross-sectional area A_e of the middle column calculated according to (19) and (20) is 5.3 mm^2.

To minimize leakage inductance between windings, a staggered arrangement of the windings in a stacked structure is used. Winding $S3$, which carries a large flow of current, uses single-layer traces and an increased parallel winding scheme to reduce the winding impedance and increase system efficiency. To maximize the utilization of window area and reduce the dc resistance of copper windings, the linewidth of each winding layer should fill the column spacing of the UI-type core, as shown in Fig. 12. The relationship between the winding width of each layer and the window width can be seen in Fig. 12, and

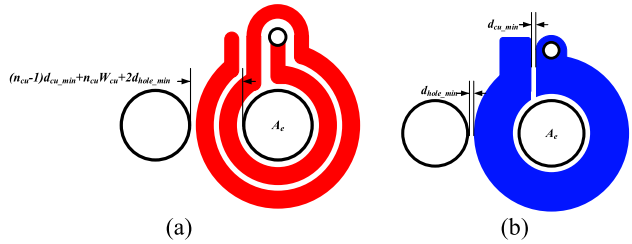

Fig. 12. Trace diagram of the windings. (a) Single-layer two-turn winding. (b) Single-layer one-turn winding.

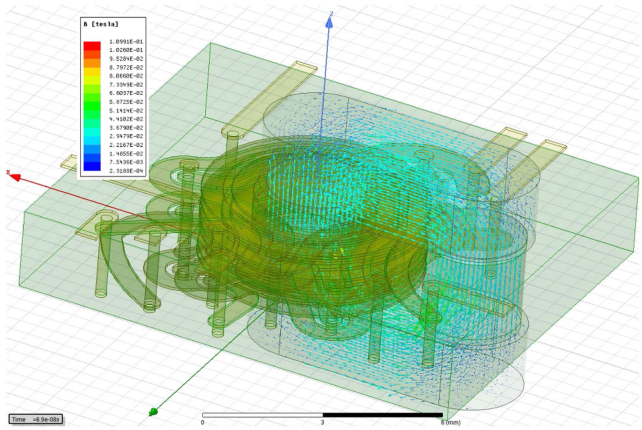

Fig. 13. Magnetic flux density distribution within the core.

is expressed as follows [24]:

$$L_W \geq (n_{\text{cu}} - 1)d_{\text{cu\_min}} + n_{\text{cu}}W_{\text{cu}} + 2d_{\text{hole\_min}}. \tag{23}$$

Limited by printed circuit board (PCB) processing technology, the minimum copper trace spacing $d_{\text{cu\_min}}$ and copper trace to through-hole spacing $d_{\text{hole\_min}}$ are 0.2 mm. Based on the limitations of the processing process and the consideration of circuit layout and routing, the linewidth of the winding $S3$ of $n_{\text{cu}} = 1$ is designed to be 1.6 mm for each single turn, and the linewidth of the remaining windings of $n_{\text{cu}} = 2$ is designed to be 0.7 mm for each layer of two turns.

Maxwell 3-D finite element simulation can verify the designed drive transformer parameters, where the parameters of the transformer core material 3F46 are obtained according to the relevant diagrams and characteristic curves provided by Ferroxcube, and the winding model is created by the PCB drawing software Altium Designer and imported into the simulation software. As shown in Fig. 13, the internal flux density distribution of the transformer core is relatively uniform when the drive transformer is operated, so the transformer core does not generate local hot spots. In addition, the maximum magnetic flux density of the transformer core does not reach the magnetic saturation point of material 3F46, so the transformer will not undergo a magnetic saturation phenomenon and can work normally. The simulation results of the current density of the windings are shown in Fig. 14; the current density distribution in the windings is relatively uniform, but there are a few maximum points that are caused by sudden changes in the cross-sectional

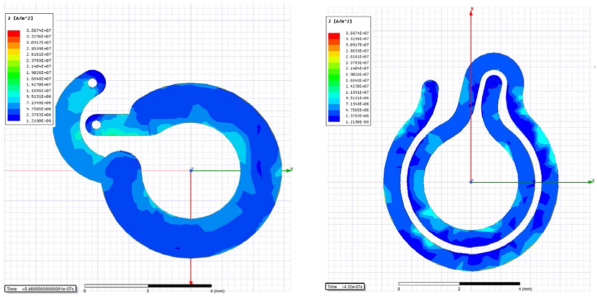

Fig. 14. Current density distribution diagram in the winding. (a) Winding *S*3. (b) Winding *S*2.

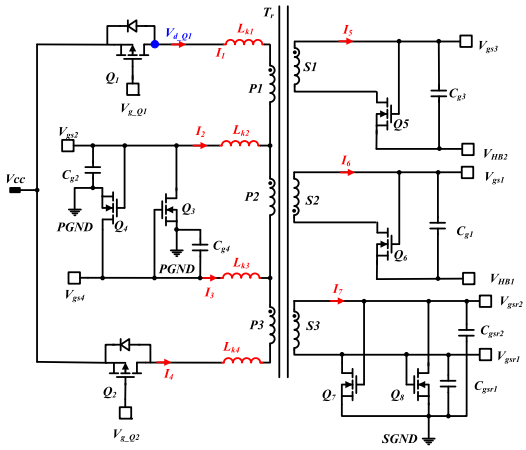

Fig. 15. CIRGD circuit diagram with transformer leakage inductance.

area of the windings at the maximum points or the inevitable proximity of the through-holes between the stacks of other windings. This phenomenon may cause a slight increase in losses in the transformer windings, but it will not affect the function of the drive transformer overall.

As shown in Fig. 15, the leakage inductance (L_k) of the transformer was measured using an impedance analyzer. Specifically, L_{k1}, L_{k2}, L_{k3}, and L_{k4} were determined to be 15 nH, 10 nH, 11 nH, and 14 nH, respectively. Transformer leakage inductance L_k will actually introduce oscillation into the working waveform of the circuit but does not affect our normal modal analysis, so in the process of designing CIRGD, although we cannot eliminate the influence of leakage inductance, we need to reduce the leakage inductance as much as possible.

D. Loss Analysis of the Proposed CIRGD

In the proposed CIRGD, since the ZVS condition can be obtained for all MOSFETs, the switching losses of MOSFETs are not considered. In addition, the clamped MOSFETs Q_3–Q_8 do not require additional drive control, their parasitic capacitance participates in the resonance during the resonance process, and the gate energy can be recovered. The losses discussed in this section are mainly the drive loss P_{d_Q} of the two P-MOSFETs, the conduction loss P_C of CIRGD, which includes the loss caused by the ON-resistance of P-MOSFETs Q_1 and Q_2, the loss caused

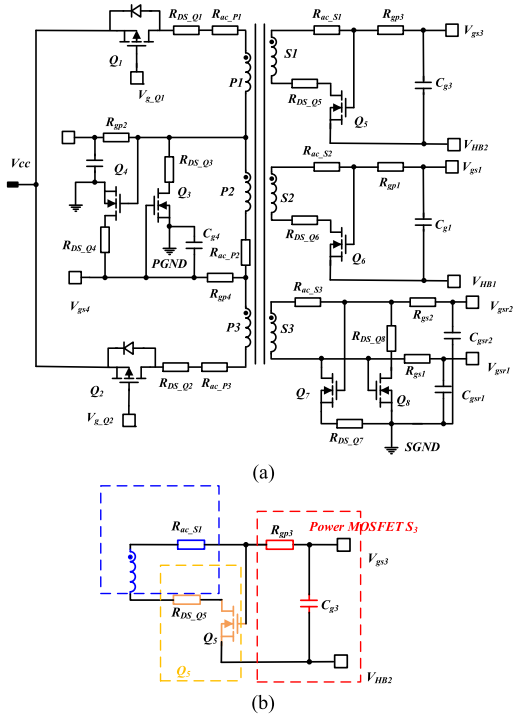

Fig. 16. Schematic of the proposed CIRGD considering parasitic resistance. (a) Circuit diagram considering parasitic resistance. (b) Resonant branch considering parasitic resistance.

by the ON-resistance of the clamped MOSFETs Q_3–Q_8, the loss caused by the gate resistance of the MOSFETs in LLC-DCX, the loss caused by the parasitic resistance in the transformer winding, and the core loss of the resonant drive transformer, where the drive losses of the P-MOSFETs are expressed as

$$P_{d\_Q} = f_s \times Q_{g\_Q} \times |V_{GS\_P}| \tag{24}$$

where f_s is the switching frequency of the P-MOSFETs, V_{GS_P} is the driving voltage of the P-MOSFETs and Q_{g_Q} is the total gate charge of the two P-MOSFETs with the driving voltage of *Vcc*.

To calculate the conduction loss of CIRGD, the current across the resistor needs to be calculated. As shown in Fig. 16(a), all parasitic resistance is considered to be used to calculate the conduction loss of CIRGD. Taking one of the resonant branches as an example, as shown in Fig. 16(b), in this resonant branch, the ON-resistance R_{DS_Q5} of Q_5, the parasitic resistance R_{ac_S1} of the winding *S*1, and the gate resistance R_{gp3} will produce losses. The conduction loss of resistance can be calculated according to the following formula:

$$P_{\text{average}} == \frac{\int_0^T I^2(t) \times R}{T} dt. \tag{25}$$

For clamped MOSFET Q_4, during the time t_1–t_2, t_r is the time from t_1 to t_2, the circuit is in the resonance phase, and the energy loss of Q_4 is $W_{C\_Q4\_R}$, and during the time t_2–t_3, t_m is the time from t_2 to t_3, the circuit is in the magnetization phase, and the energy loss of Q_4 is $W_{C\_Q4\_M}$, and the total conduction loss of Q_4 is P_{C_Q4}. The current on the two P-MOSFETs is present only during transformer excitation. The current on the Q_5–Q_8 is present only during transformer resonance.

According to the symmetry of the circuit, we only need to require the conduction loss of Q_1, Q_4, Q_5, and Q_7, and the conduction loss of Q_2, Q_3, Q_6, and Q_8 to be equal to theirs

$$\begin{aligned} W_{C\_Q4\_R} &= R_{DS\_Q4} \times \int_{t_1}^{t_2} i_{Lrd}^2(t)dt \\ &= R_{DS\_Q4} \times \left(\frac{C_{g4}}{C_{\text{gsall}}} i_{rp}\right)^2 \\ &\quad \times \left(\frac{1}{2}t_r + \frac{\sqrt{L_{rd} \times C_{\text{gsall}}}}{4}\right. \\ &\quad \left. \times \sin\left(\frac{2}{\sqrt{L_{rd} \times C_{\text{gsall}}}} t_r\right)\right) \end{aligned} \tag{26}$$

$$\begin{aligned} W_{C\_Q4\_M} &= R_{DS\_Q4} \times \int_{t_2}^{t_3} \left(\frac{i_{mp}}{t_m}\right)^2 t^2 dt \\ &= \frac{1}{3} R_{DS\_Q4} \times \left(\frac{i_{mp}}{t_m}\right)^2 \times t_m^3 \end{aligned} \tag{27}$$

$$P_{C\_Q4} = P_{C\_Q3} = \frac{2W_{C\_Q4\_R} + 2W_{C\_Q4\_M}}{T} \tag{28}$$

$$P_{C\_Q1} = P_{C\_Q2} = \frac{2R_{DS\_Q1} \times \frac{1}{3} \times \left(\frac{i_{mp}}{t_m}\right)^2 \times t_m^3}{T} \tag{29}$$

$$\begin{aligned} P_{C\_Q5} &= \frac{2 \times R_{DS\_Q5} \times \left(\frac{C_{g4}}{C_{gsall}} i_{rp}\right)^2}{T} \\ &\quad \times \left(\frac{1}{2}t_r + \frac{\sqrt{L_{rd} \times C_{\text{gsall}}}}{4}\right. \\ &\quad \left. \times \sin\left(\frac{2}{\sqrt{L_{rd} \times C_{\text{gsall}}}} t_r\right)\right) \end{aligned} \tag{30}$$

$$\begin{aligned} P_{C\_Q7} &= \frac{2 \times R_{DS\_Q7} \times \left(\frac{C_{gsr1}{}'}{C_{\text{gsall}}} i_{rp}\right)^2 \times \left(\frac{N_{P2}}{N_{S3}}\right)^2}{T} \\ &\quad \times \left(\frac{1}{2}t_r + \frac{\sqrt{L_{rd} \times C_{\text{gsall}}}}{4}\right. \\ &\quad \left. \times \sin\left(\frac{2}{\sqrt{L_{rd} \times C_{\text{gsall}}}} t_r\right)\right). \end{aligned} \tag{31}$$

The total gate resistance loss for the four MOSFETs on the primary side of the LLC-DCX is P_{C_Rgp}. The total gate resistance loss for the four MOSFETs on the secondary side of the LLC-DCX is P_{C_Rgs}. The current on the gate resistance is only present when the gate capacitor is charged and discharged, where R_{gp} is the gate resistance of a single MOSFET on the primary side, and R_{gs} is the gate resistance of a single MOSFET on the secondary side.

$$P_{C\_Rgp} = 4 \times \frac{2P_{C\_Q4\_R}}{T} \times \frac{R_{gp}}{R_{DS\_Q4}} \tag{32}$$

$$P_{C\_Rgs} = 2 \times P_{C\_Q7} \times \frac{R_{gs}}{2 \times R_{DS\_Q7}} = P_{C\_Q7} \times \frac{R_{gs}}{R_{DS\_Q7}}. \tag{33}$$

For the conduction loss of the parasitic resistance of the transformer winding in CIRGD, considering the skin effect of the transformer winding, to accurately calculate the winding loss and consider the influence of skin depth on the winding, according to the loss model proposed in [25], the relationship between the ac resistance R_{AC} of the transformer winding and the dc resistance R_{DC} is given by

$$R_{\text{AC}} = R_{\text{DC}} \left(1 + \frac{(ro/\delta)^4}{48 + 0.8(ro/\delta)^4}\right) \tag{34}$$

$$\delta = 1/\sqrt{\pi f_s \mu \sigma} \tag{35}$$

$$R_{\text{DC}} = \frac{L}{\sigma W d} \tag{36}$$

where radius r_o is a round conductor, δ is the skin depth, μ is the magnetic permeability, σ is the conductivity of the conductor material, L is the length of the copper foil winding, W is the line width of the copper foil winding, and d is the copper thickness of the PCB trace layer. The rms value of the current passed through each winding in the first half of the cycle is the same as in the second half of the cycle, so the conduction loss of the transformer winding in the first half of the cycle is the same as that of the second half cycle. Therefore, the conduction loss table of the transformer winding P_{C_Rp} is given by

$$\begin{aligned} P_{C\_Rp} = \frac{2}{T} &\left(\int_{t_0}^{t_2} i_3^2(t) R_{\text{ac\_}P2} dt + \int_{t_2}^{t_4} i_3^2(t)(R_{\text{ac\_}P2} + R_{\text{ac\_}P1}) dt \right. \\ &\left. + \int_{t_0}^{t_2} i_5^2(t) R_{\text{ac\_}S1} + i_6^2(t) R_{\text{ac\_}S2} + i_7^2(t) R_{\text{ac\_}S3} dt\right) \end{aligned} \tag{37}$$

where $R_{\text{ac\_}Pi}$ and $R_{\text{ac\_}Si}$ represent the ac resistance of windings *Pi* and *Si* ($i = 1, 2, 3$), respectively, and $i_j(t)$ ($i = 1, 2, 3, 4, 5, 6, 7$) represents the respective branch currents noted in Fig. 2.

The drive transformer is one of the most critical components in CIRGD and one of the main sources of loss. Calculate the losses generated by the transformer core. The Steinmetz formula is often used to generalize the sum of core losses [26] given as

$$p_v = C_m f^{\alpha} B_{\text{max}}^{\beta} \tag{38}$$

where p_v is the unit core volume loss power, f is the alternating magnetic field frequency, B_{max} is the maximum flux density of the alternating magnetic field, C_m is the core material loss coefficient, and the α and β are the frequency index and magnetic induction intensity index of the core material, respectively.

In CIRGD, the current driving the transformer windings is not sinusoidal, so the transformer core loss calculation needs to be performed using the modified Steinmetz formula [26], which is now calculated as follows:

$$p_v = \left(C_m f_{eq}^{\alpha-1} B_{\text{max}}^{\beta}\right) f \tag{39}$$

$$f_{\text{eq}} = \frac{2}{\Delta B^2 \pi^2} \cdot 2 \int_{t_2}^{t_4} \left(\frac{dB}{dt}\right)^2 dt = \frac{1}{\pi^2} \frac{2}{t_m} \tag{40}$$

$$P_{\text{core}} = p_v \cdot V_{\text{core}} = \left[C_m \left(\frac{1}{\pi^2} \frac{2}{t_m}\right)^{\alpha-1} \left(\frac{\mu N}{l} i_{mp}\right)^{\beta}\right] f \cdot V_{\text{core}} \tag{41}$$

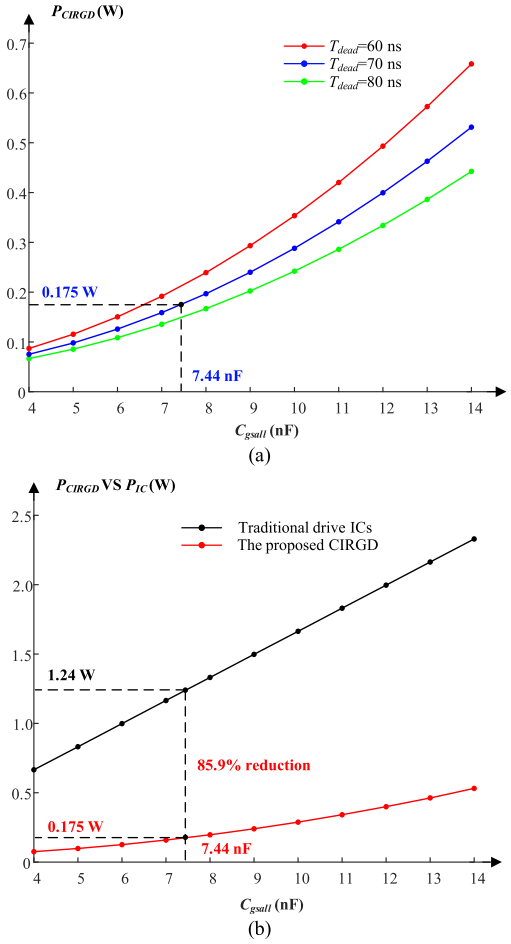

Fig. 17. Comparison of gate drive losses under different C_{gsall}. (a) Comparison of gate drive losses under different $T_{\rm dead}$. (b) Comparison of gate drive losses between CIRGD and traditional drive ICs.

where $P_{\rm core}$ is the transformer core loss, $V_{\rm core}$ is the volume of the transformer, μ is the relative permeability of the core material, N represents the number of winding turns, and l represents the length of the magnetic circuit of the core. Therefore, the overall loss $P_{\rm CIRGD}$ of the proposed CIRGD can be expressed by the following equation:

$$P_{\rm CIRGD} = 2(P_{C\_Q4} + P_{C\_Q1} + P_{C\_Q5} + P_{C\_Q7}) + P_{d\_Q} + P_{C\_Rgp} + P_{C\_Rgs} + P_{C\_Rp} + P_{\rm core}. \quad (42)$$

The proposed CIRGD achieves energy recovery and reduces gate drive losses, whereas the design of accurate deadtime $T_{\rm dead}$ is important, which determines the implementation of LLC-DCX's ZVS and the efficiency of the entire system. As shown in Fig. 17(a), in the case of 1.3 MHz operating frequency and supply voltage $Vcc = 12$ V, the larger the deadtime $T_{\rm dead}$ of the design, the lower the overall loss $P_{\rm CIRGD}$ of the proposed CIRGD, and the overall loss of CIRGD increases with the increase of the gate capacitance of the power MOSFET in LLC-DCX. As shown in Fig. 17(b), the proposed CIRGD is greatly reduced compared with the traditional voltage drive loss, taking the deadtime of 70 ns and the equivalent C_{gsall} selected as an example, compared with the drive loss of the traditional drive ICs, the loss of the proposed CIRGD is theoretically reduced by 85.9%.

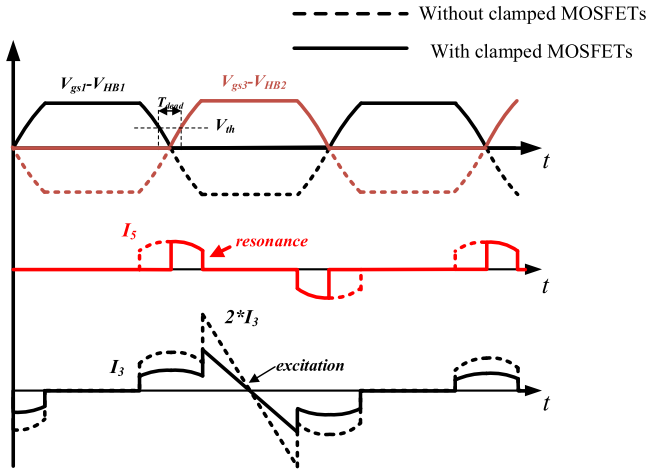

Fig. 18. Comparison of the main operating waveform of a resonant gate driver with clamped MOSFETs to a resonant gate driver without clamped MOSFETs.

E. Comparative Study of the Proposed CIRGD

During the CIRGD working process, it is observed that only half of the gate capacitors are charged or discharged when the resonant inductor L_{rd} and the gate capacitor are resonating. However, all the gate capacitors participate in charging and discharging when the RGD in [23] is working. The differences in the operating waveform of the RGD with and without clamped MOSFETs are shown in Fig. 18 based on theoretical analysis. The addition of clamped MOSFETs clamps the gate drive voltage to 0–V_g, resulting in a smaller cycle current than without clamped MOSFETs when the gate resistance flows through the current only half of the time. Consequently, the loss of the drive circuit is further reduced while maintaining the same deadtime design.

For example, the resonant branch of CIRGD, as shown in Fig. 16(b), incurs additional on-resistance loss due to the clamped MOSFET Q_5. However, the loss caused by gate resistance R_{gp3} is halved, making the overall loss negligible as long as R_{DS_Q5}<0.5R_{gp3} is ensured. Therefore, the clamped MOSFET Q_5 can improve the efficiency of the RGD.

IV. Simulation and Experimental Verifications

To validate the accuracy of the aforementioned theoretical analysis, both a 48 V–6 V/30 A SIMetrix simulation and prototype were created. Table I presents the key parameter design and device selection of the system prototype. By importing the SPICE model of the device and building the circuit in SIMetrix, the simulation results of CIRGD are displayed in Fig. 19. The key waveform simulation results effectively confirm the analysis of the CIRGD working principle. It should be noted that since the device model is not ideal, and the threshold voltage of the clamped MOSFET has an impact, the ZVS part of the clamped MOSFET is activated when the voltage from drain to source equals

TABLE I
DESIGN PARAMETERS OF THE PROPOSED CIRGD

The proposed CIRGD	The power supply Vcc	Vcc=12 V
	Switching frequency f_s	f_s =1.3 MHz
	P-MOSFETs Q_1,Q_2	IRFHS9351 Q_g=2.0 nC $R_{ds(ON)}$=0.235 Ω
	N-MOSFETs Q_3–Q_8	BSD235N V_{th}=0.9 V $R_{ds(ON)}$=0.266 Ω
	Turns ratio N_{P1}: N_{P2}: N_{P3}: N_{S1}: N_{S2}: N_{S3}	2:4:2:4:4:3
	The resonant inductor L_{rd}	1.50 μH
The LLC-DCX	Primary-side MOSFETs S_1–S_4	BSZ110N08NS5 R_g=1.4 Ω, V_{th}=3.8 V
	Secondary-side MOSFETs S_{R1}–S_{R4}	BSZ013NE2LS5I R_g=0.7 Ω, V_{th}=2.0 V
	The resonance parameters L_r/C_r	112 nH/80 nF
	The magnetized inductance L_m	7.0 μH

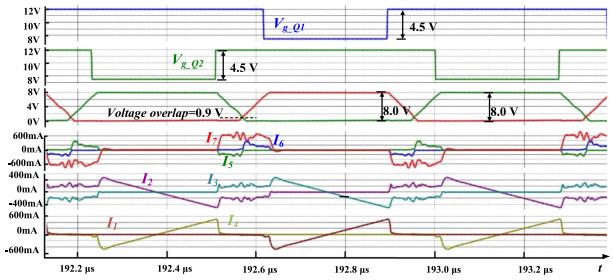

Fig. 19. Key simulation waveforms for CIRGD are in SIMetrix.

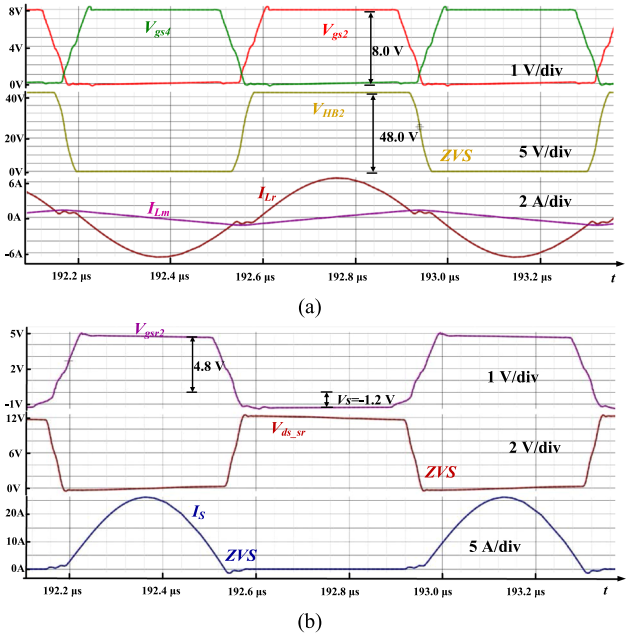

Fig. 20. Key simulation waveforms for LLC-DCX are in SIMetrix. (a) Key waveform on the primary side. (b) Critical waveform on the secondary side.

that threshold voltage. As soon as the clamped MOSFET turns ON, an oscillation is introduced into the circuit, and a voltage overlap forms in the driving voltage; this overlapping voltage is equivalent to the threshold voltage of the clamped MOSFET, which is about 0.9 V. This voltage overlap makes the deadtime about 10 ns smaller than the design. Therefore, compensation is required during the actual prototype design process. Fig. 20 displays the key simulation waveform of LLC-DCX based on CIRGD. The primary-side MOSFETs achieve ZVS, whereas the level shift circuit shifts the drive voltage of the secondary side down by 1.2 V, which enables the zero current switching (ZCS) and ZVS of the secondary-side MOSFETs to be effectively executed.

The results of the full load test of the prototype are presented in Figs. 21 and 22 show the results of the 10% load test of the prototype and Fig. 23 shows the actual picture of the prototype, where Fig. 21(a) displays the drain voltage of the P-MOSFET Q_1, depicted by the blue curve, and its driving signal, illustrated by the yellow curve. It is evident that Q_1 attains ZVS and experiences no apparent body diode conduction. In Fig. 21(b), the current I_1+I_4 is measured, and unlike modal analysis, the current oscillates slightly due to the parasitic parameters of the circuit. Additionally, in Fig. 21(c), it is noticeable that the driving signal supplied to LLC-DCX is not very different from the simulation outcomes. There is a voltage overlap of 0.9 V. Furthermore, due to the impact of parasitic parameters in the actual prototype, the high-side and low-side levels of the driving voltage V_{gs2} and V_{gs4} are slightly inclined, but it will not affect the proper driving operation. Moreover, due to the influence of the Miller platform and capacitor nonlinearity, the driving voltage does not rise or fall in a resonant manner, but this has a minimal effect on the deadtime; as per theoretical analysis, voltage overlap affects the prototype's deadtime design, which is 60.5 ns.

Fig. 21(d) shows the key waveform on the primary-side MOSFETs S_1 and S_3. It can be seen that the driving waveforms of $S1$ and $S3$ oscillate well, but still realize ZVS.

Fig. 21(e) shows the primary-side's crucial waveform of LLC-DCX, where the operating frequency is close to the resonant frequency point, and the primary-side MOSFET attains ZVS with no apparent body diode conduction. The excitation current recorded is about 0.8 A, which accomplishes low turn-OFF loss and conduction loss, thus achieving high-efficiency conversion.

Fig. 21(f) displays the primary waveform on the secondary side of LLC-DCX, where the driving signal of the secondary-side MOSFET adds a 1.6 V level shift, causing the actual effective driving voltage to be approximately 5.0 V, enabling the full turn-ON of the MOSFET. Despite the introduction of parasitic inductance due to the long path of signal transmission to the MOSFET, the voltage overshoot (as shown in the red curve) does not significantly impact the normal drive function. The blue curve represents the voltage from the drain to the source of the synchronous rectifier, which shows no noticeable body diode on-voltage drop or oscillation caused by current backfilling. This indicates that the secondary-side MOSFETs can effectively implement ZCS and ZVS.

Fig. 22 shows the key waveforms for LLC-DCX at 10% load. It can be seen that under light load, the LLC-DCX based on CIRGD can work normally, there is no current backfilling, and the driving signal is normal.

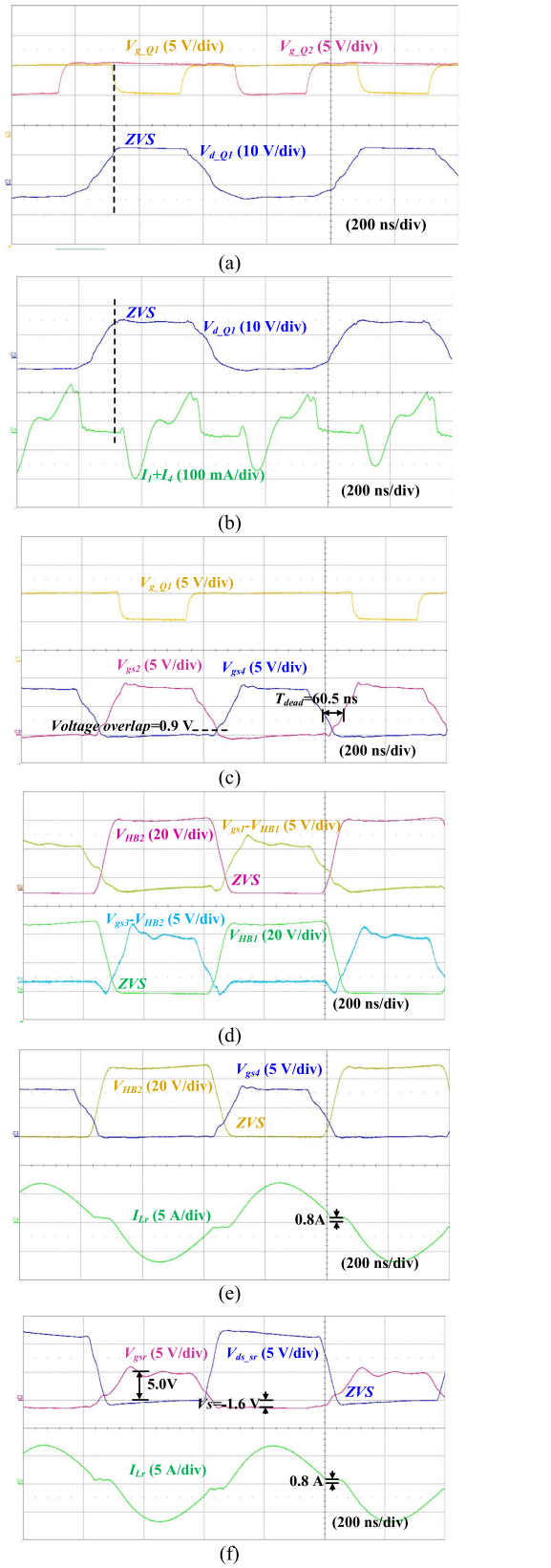

Fig. 21. Key waveforms for LLC-DCX at full load. (a) P-MOSFET implements ZVS. (b) Critical current waveform for CIRGD. (c) Critical voltage waveform for CIRGD. (d) Key waveform on the primary-side MOSFETs. (e) Key waveform on the primary side. (f) Critical waveform on the secondary side.

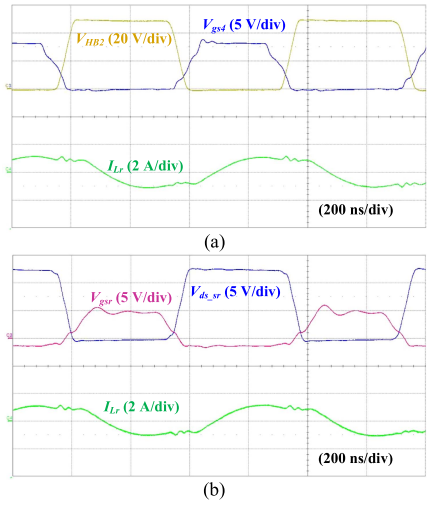

Fig. 22. Key waveforms for LLC-DCX at 10% load. (a) Key waveform on the primary side. (b) Critical waveform on the secondary side.

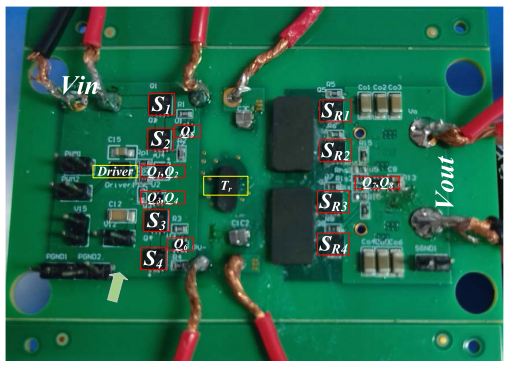

Fig. 23. Prototype proposed in this article.

The CIRGD loss measured by the actual prototype is 185 mW, which deviates by about 5% from the theoretical analysis of 175 mW. This result demonstrates the accuracy with which the theoretical analysis guides the design. Fig. 24 illustrates the loss breakdown of the proposed CIRGD at full system load, where the red portion represents actual measurements exceeding theoretical analysis. This can be attributed to the loss caused by leakage magnetism resulting from the air gap, shutdown loss of Q_1–Q_8, losses from clamped MOSFETs achieving a portion of ZVS, and loss ignored during the approximate processing of theoretical analysis. Although these losses are difficult to analyze, their proportion is insignificant and thus can be ignored. The drive loss of P-MOSFETs, gate resistance conduction loss of primary-side MOSFETs, and gate resistance conduction loss of secondary-side MOSFETs are the main sources of loss. Table II shows a comparison between the proposed CIRGD and RGDs in different literature. The proposed CIRGD requires only two external drive control signals, does not demand additional leakage inductance design, and achieves more gate-drive energy recovery by using clamped MOSFETs. Its measured result is 85%, higher than what other literature has suggested. The power density of an RGD is defined as the ratio of the power consumption of a conventional

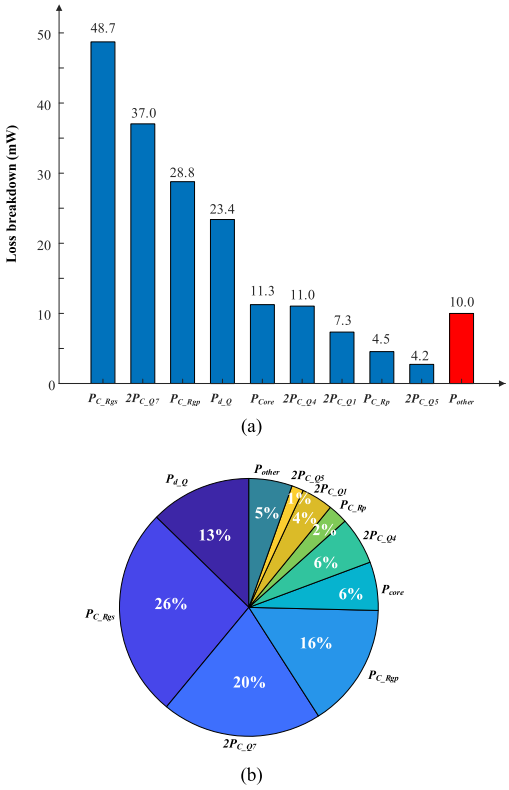

Fig. 24. Loss breakdown of the proposed CIRGD. (a) Histogram of different loss distributions. (b) Pie chart of different loss proportions.

TABLE II
COMPARISON OF RESONANT GATE DRIVERS IN DIFFERENT LITERATURE

	RDG in [19]	RDG in [20]	RDG in [23]	Proposed CIRGD
Number of external drivers	4	3	2	2
Switching frequency	500 KHz	500 KHz	1 MHz	1.3 MHz
Leakage design is required	Yes	Yes	No	No
Gate drive voltage range	$-V_g$–V_g	$-V_g$–V_g	$-V_g$–V_g	0–V_g
Proportion of energy recovery	79%	70.7%	80%	85%
Number of semiconductor devices	4	3	2	8
Power density	None	None	1.67 W/cm^2	2.75 W/cm^2

driver to the area occupied by the RGD. Through the number of semiconductor devices and the power density of the RGD, it can be seen that the proposed CIRGD increases the gate energy recovery ratio by increasing the clamping MOSFETs, despite the increase in the number of semiconductor devices, the circuit experiences a reduction in circulating current. Consequently, the size of the drive transformer decreases, and compared with the literature [23], the power density of the CIRGD is higher.

Finally, Fig. 25 demonstrates how the proposed CIRGD LLC-DCX facilitates a significant improvement in overall efficiency compared to traditional voltage gate drivers. At the peak efficiency point, the overall efficiency of the proposed CIRGD is

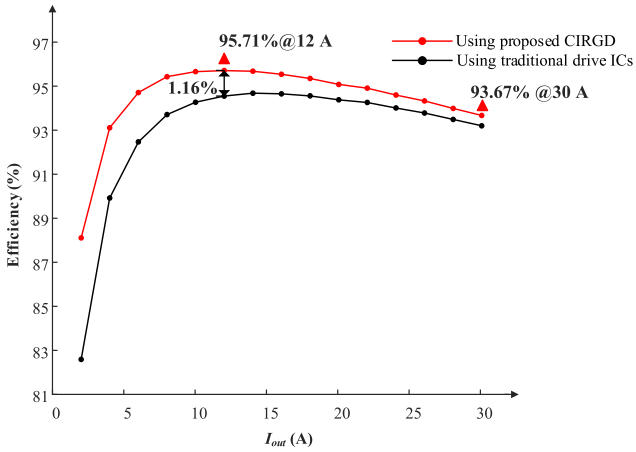

Fig. 25. Measured efficiency comparison between DCX using the proposed CIRGD and DCX using conventional driver ICs.

increased by 1.16%, and the efficiency is more considerable under light load.

V. CONCLUSION

This article proposes a CIRGD, which provides multiple complementary isolated gate drive signals. By incorporating clamped MOSFETs, a drive voltage of 0–V_g is achieved, resulting in lower cycle current and reduced conduction losses compared to the drive voltage that achieves -V_g to V_g. This article elaborates on the working principle, parameter design, and loss analysis of CIRGD. Moreover, the proposed driver achieves 85% energy recovery compared to conventional voltage drivers. Based on the proposed CIRGD, a 48 V–6 V/30 A LLC-DCX prototype system with a working frequency of 1.3 MHz is designed. The experimental results validate the theoretical analysis's rationality and accuracy of the proposed CIRGD.

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