Letters

ZVS Analysis and a Design Method for Unidirectional Medium-Voltage *LLC*-DCX With High Step-Up Ratio

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***Abstract*—The high step-up ratio in a medium-voltage dc transformer (DCX) amplifies the referred parasitic capacitance from the secondary side, resulting in an altered resonance mode. This letter analyzes the parasitic effect on the zero-voltage switching (ZVS) condition under rated load in an *LLC*-DCX. A rule of thumb is proposed to determine the main parameters in the system, including the magnetizing inductance, resonant inductance, and switching frequency. It is suggested to increase the resonant inductance to fully charge the equivalent parasitic capacitance (C_{eq}) prior to the deadtime for secure ZVS. The proposed design no longer requires to lower the magnetizing inductance and can adapt to a wide range of insulation design of the transformer core and windings. Scaled experimental results are presented to validate the analysis.**

***Index Terms*—*LLC* dc transformer (DCX), medium-voltage (MV), parasitic capacitance, transformer, zero-voltage switching (ZVS).**

I. Introduction

ISOLATED medium-voltage (MV) dc transformers (DCXs) are being deployed in dc-collection networks of renewable power generation farms. The series resonant *LLC* converter is a promising topology for its zero-voltage switching (ZVS) and zero-current switching capability [1], [2]. To ensure high efficiency and a relatively constant voltage ratio, it generally operates below the resonance frequency without the closed-loop control [3]. The topology of such a system is shown in Fig. 1, operating with an active low-voltage (LV) bridge and a passive MV bridge.

The ZVS condition is essential for efficient and reliability in medium-frequency (MV) or high-frequency systems. The design criterion of ZVS has been extensively discussed. Lu et al. [4] show an optimal design method of the *LLC* and define a constraint for ZVS, assuming that the MOSFET output capacitance is charged or discharged by a constant magnetizing current during the switching deadtime. The analysis was not complete and ignored some nonideal factors. For instance, the parasitic capacitance of the output diodes (C_j) and that of the transformer (C_p, C_s, and C_{ps}) will share the magnetizing current with C_{oss} [5], [6], [7]. To simplify the analysis, equivalent parasitic capacitance (C_{eq}) was introduced in Fig. 1. A common method was to decrease the magnetizing inductance (L_m) and increase the deadtime (t_d) to ensure ZVS. The previous analysis was mostly for LV or step-down DCX systems, where the impact of the parasitics was small.

In contrast, in an MV step-up DCX, there is always nonnegligible parasitic capacitance due to MV power semiconductors and MF transformer. For insulation, potting material is extensively used, which brings about large parasitic capacitance. Moreover, a high turns ratio (n) further amplifies the equivalent capacitance (C_{eq}) referred to the LV side. As a result, in the discontinuous conduction mode (DCM), the circuit oscillates sharply [8], and ZVS performance is hard to achieve [6].

Studies have investigated MV DCX regarding the ZVS condition and modulation scheme [8], [9]. Guillod et al. [8] introduce a magnetizing current splitting ZVS modulation scheme, which allows an active sharing of the magnetizing current between the H-bridges on both sides. Cao et al. [9] elaborate on how

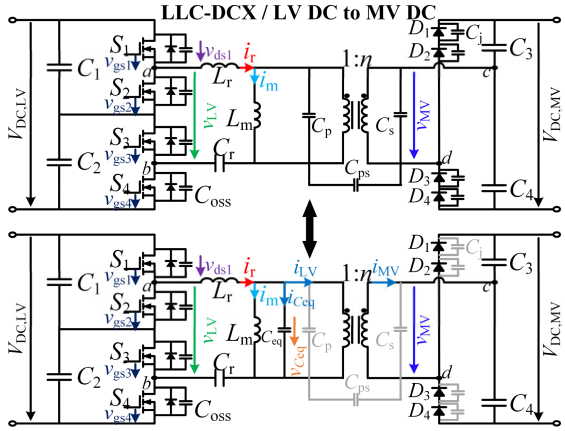

Fig. 1. Circuit diagram of *LLC*-DCX considering secondary parasitic capacitances.

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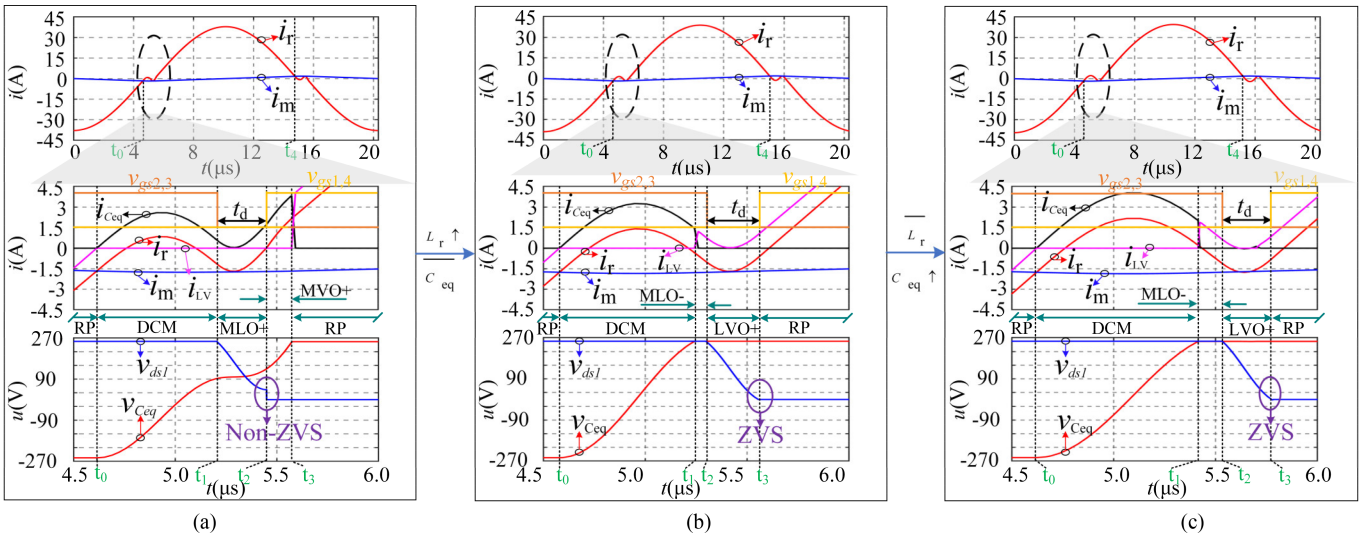

Fig. 2. Waveforms of the LLC converter (f_s<f_r). (a) $C_{\rm eq}$ is charged completely beyond the dead zone. (b) $C_{\rm eq}$ is charged completely before the dead zone by increasing L_r. (c) $C_{\rm eq}$ is still charged completely before the dead zone with the increasing $C_{\rm eq}$.

to determine the switching frequency, magnetizing inductance, and deadtime to achieve the "Sync-ZVS" transition. To ensure ZVS on both sides, a small L_m is required. However, previous efforts have focused on bidirectional topologies. In a unidirectional step-up system, active switches are not mandatory on the output MV side. Due to the diode effect, the switching mode significantly differs from the bidirectional case and this has not been studied.

In this letter, a time-domain model is derived for the *LLC* converter. It is found that tuning up the resonant inductance L_r helps $C_{\rm eq}$ be precharged prior to the deadtime so that it is free from resonance during the deadtime to facilitate ZVS. Different from the scheme for a bidirectional DCX in [8] and [9], the proposed design no longer requires low magnetizing inductance to achieve ZVS. It is also decoupled from the insulation design and the fabrication of the high-power MF transformer. Finally, the main design requirements on the magnetizing inductance L_m, resonant inductance L_r, and switching frequency f_s are given for ZVS. The experimental results validate the analysis.

II. Operating Principle

The equivalent parasitic capacitance ($C_{\rm eq}$) referred to the LV side, as shown in Fig. 1, is expressed in (1). $C_{\rm eq}$ is magnified dramatically with turns ratio n

$$C_{\rm eq,\,tr} = C_p + n^2 C_s + (n-1)^2 C_{\rm ps}, \quad C_{\rm eq,\,diode} = n^2 C_j,$$
$$C_{\rm eq} = C_{\rm eq,\,tr} + C_{\rm eq,\,diode}. \tag{1}$$

Fig. 2 shows the simulation waveforms of the *LLC* converter operating below resonant frequency (f_r). The switching period can be decomposed into several operating modes with corresponding equivalent circuits, as shown in Fig. 3. The details of the modes are explained as follows.

1) *Resonant Pulse (RP)*: The voltage difference between the MV and LV sides is applied on the resonant tank (between L_r and C_r), resulting in a sinusoidal current between the two bridges at f_r. This mode is used to transfer power.
2) *DCM*: As the resonant current (i_r) comes across the magnetizing current (i_m), the rectifier diodes block the current. Meanwhile, $C_{\rm eq}$ and L_m are no longer clamped by the MV side, and they participate in oscillation together with L_r.
3) The capacitance on the LV ($C_{\rm oss}$) and MV ($C_{\rm eq}$) sides participates in the oscillation (MLO+).
4) Only the capacitance on the MV side ($C_{\rm eq}$) participates in the oscillation (MVO+).
5) Only the capacitance of the LV side ($C_{\rm oss}$) participates in the oscillation (LVO+).
6) The capacitance of MV ($C_{\rm eq}$) and LV ($C_{\rm oss}$) sides escapes from the oscillation (MLO-).

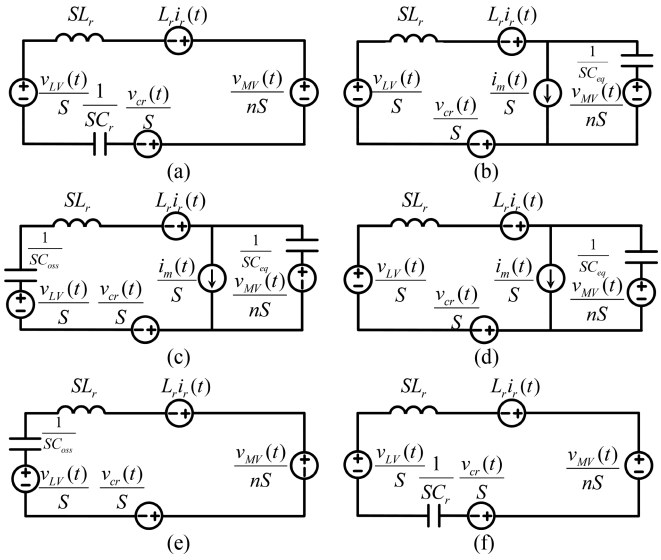

Fig. 3. Equivalent circuit corresponding to the modes introduced above. (a) RP mode. (b) DCM mode. (c) MLO+ mode. (d) MVO+ mode. (e) LVO+ mode. (f) MLO− mode.

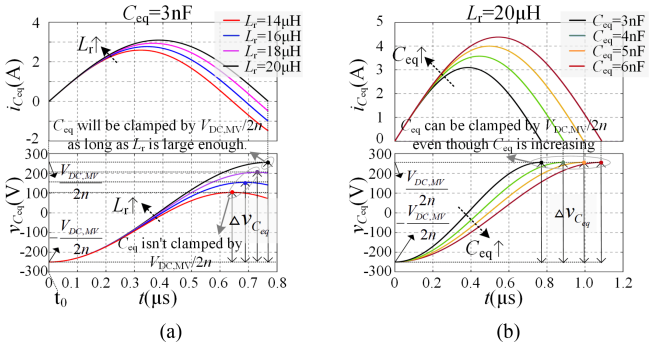

Fig. 4. Current and voltage waveforms of $C_{\rm eq}$ in DCM mode. (a) Varied L_r. (b) Varied $C_{\rm eq}$.

According to the equivalent circuit of DCM mode, the time-domain expressions during (t_0-t_1) are expressed as (2). The corresponding waveforms against varied parameters during this period are shown in Fig. 4

$$\begin{aligned} i_r(t) &= \frac{2\pi^2 P_0 f_r^2}{f_s V_{\rm DC,LV}\omega_1}\sin(\omega_1(t-t_0)) + i_r(t_0),\\ i_{C_{\rm eq}}(t) &= \frac{2\pi^2 P_0 f_r^2}{f_s V_{\rm DC,LV}\omega_1}\sin(\omega_1(t-t_0))\\ v_{C_{\rm eq}}(t) &= -\frac{V_{\rm DC,LV}}{2} + \frac{2\pi^2 P_0 f_r^2 L_r}{f_s V_{\rm DC,LV}}(1-\cos(\omega_1(t-t_0))),\\ \omega_1 &= \frac{1}{\sqrt{L_r C_{\rm eq}}}. \end{aligned} \tag{2}$$

In Fig. 4, the current (i_r) ringing is associated with $C_{\rm eq}$ and L_r. Generally, the transformer's leakage inductance (L_k) is used as a part of L_r. But due to the insulation need of the MF transformer, L_k cannot be overly reduced. In addition, due to the large turns ratio, $C_{\rm eq}$ is of an amplified value. As shown in Fig. 2(a), the circuit oscillation during the DCM mode is obvious and nonnegligible. In addition, $C_{\rm eq}$ remains to be charged during the deadtime, resulting in the magnetizing current being shared between the $C_{\rm oss}$ and $C_{\rm eq}$ branches. According to Fig. 2(a), i_r is insufficient to discharge $C_{\rm oss}$, bringing high risks of losing ZVS [5], [6], [7].

According to Fig. 4(b), it is apparent that $\Delta v_{C\rm eq}$ is independent of $C_{\rm eq}$ itself in the DCM mode, and $C_{\rm eq}$ can be fully charged before the deadtime if L_r is large enough. And the lower limit of L_r can be deduced through (3) based on (2)

$$\text{Maximum}(v_{C_{\rm eq}}(t)) = -\frac{V_{\rm DC,LV}}{2} + \frac{4\pi^2 P_0 f_r^2 L_r}{f_s V_{\rm DC,LV}} \geq \frac{V_{\rm DC,LV}}{2}. \tag{3}$$

Thereby, $C_{\rm eq}$ can escape from the resonance during the deadtime and enter the LVO+ mode. From the equivalent circuit, the time-domain expressions of each mode, as shown in Fig. 2(b)

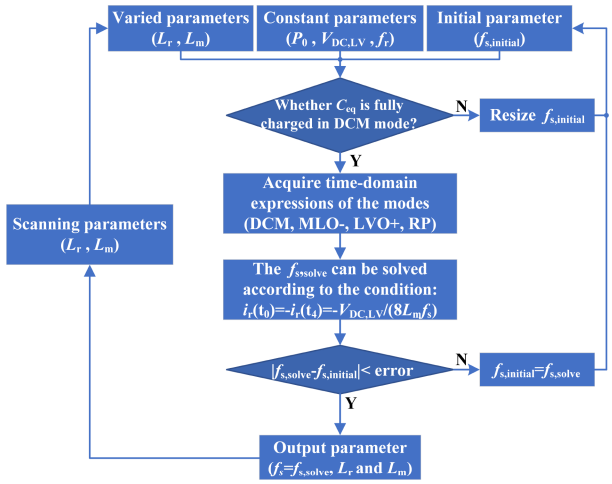

Fig. 5. Flowchart of parameters design.

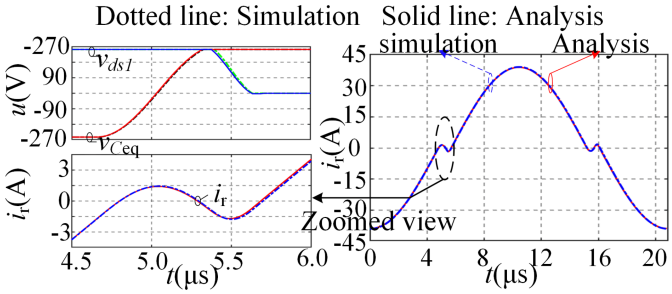

Fig. 6. Comparison of calculation and simulation waveforms.

and (c), are

$$\begin{cases} \text{DCM}: i_r(t) = \frac{2\pi^2 P_0 f_r^2}{f_s V_{\rm DC,LV}\omega_1}\sin(\omega_1(t-t_0)) + i_r(t_0)\\ \text{MLO}-: i_r(t) = i_r(t_1)\cos(\omega_2(t-t_1))\\ \quad + \frac{v_{\rm LV}(t_1)-v_{C_r}(t_1)-v_{C\rm eq}(t_1)}{L_r\omega_2}\sin(\omega_2(t-t_1))\\ \text{LVO}+: i_r(t) = i_r(t_2)\cos(\omega_3(t-t_2))\\ \quad + \frac{v_{\rm LV}(t_2)-v_{C_r}(t_2)-v_{C\rm eq}(t_2)}{L_r\omega_3}\sin(\omega_3(t-t_2))\\ \text{RP}: i_r(t) = i_r(t_3)\cos(\omega_4(t-t_3))\\ \quad + \frac{v_{\rm LV}(t_3)-v_{C_r}(t_3)-v_{C\rm eq}(t_3)}{L_r\omega_3}\sin(\omega_4(t-t_3))\\ \omega_1 = \frac{1}{\sqrt{L_r C_{\rm eq}}}, \omega_2 = \frac{1}{\sqrt{L_r C_r}}, \omega_3 = \frac{1}{\sqrt{L_r C_{oss}}}, \omega_4 = \frac{1}{\sqrt{L_r C_r}}\\ i_r(t_0) = -i_r(t_4) = -I_m = -\frac{V_{\rm DC,LV}}{8L_m f_s}. \end{cases} \tag{4}$$

Based on the derivation, an analysis method can be acquired. It is worth noting that f_s is unknown, and the solutions of f_s are obtained iteratively. Fig. 5 shows the flowchart of parameter design proposed in this letter. The switching frequency f_s is swept to secure ZVS and symmetric current waveform. Parameters are exhausted to identify feasible ones.

Fig. 6 shows the simulation and numerical results based on (4) and modes shown in Fig. 2(b). The simulation results basically agree with the curves obtained by the analytic formula, proving that the time-domain analysis is accurate.

$C_{\rm eq}$ is fully precharged, and all the charges generated (Q_r) by i_r are used to charge or discharge $C_{\rm oss}$ in LVO+ mode. The ZVS

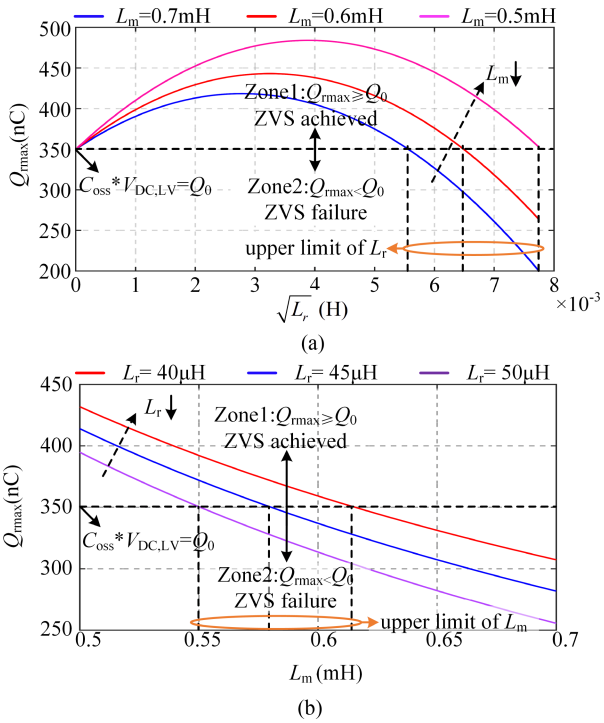

Fig. 7. $Q_{r\max}$ generated during LVO+ mode under variational parameters. (a) Varied L_r. (b) Varied L_m.

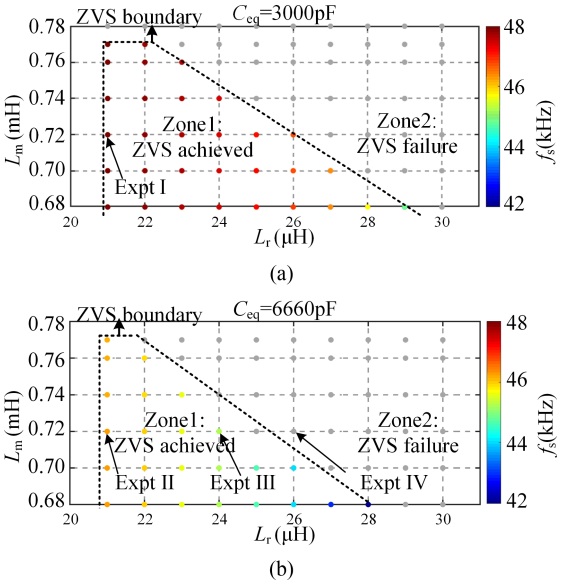

Fig. 8. All the design points under different parasitic capacitances. (a) $C_{\rm eq}$ = 3000 pF. (b) $C_{\rm eq}$ = 6660 pF.

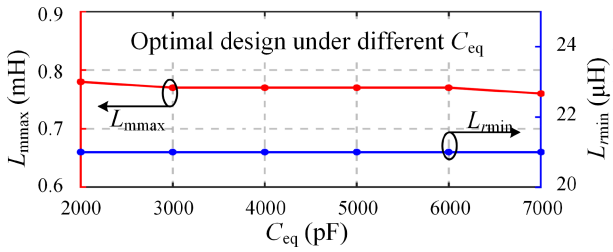

Fig. 9. $L_{m\max}$ and $L_{r\min}$ can be obtained under different $C_{\rm eq}$.

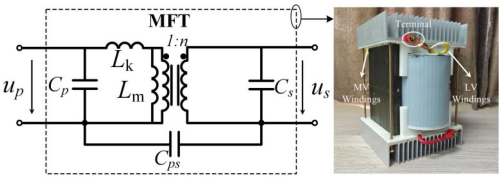

Fig. 10. Equivalent circuit model of MF transformer.

condition is expressed as follows:

$$\begin{aligned}
&\text{Condition 1 }:0>i_r(t)>i_m(t)\\
&=-\frac{V_{\rm DC,LV}}{8L_mf_s}\leftrightarrow\sqrt{(A^2+B^2)}<\frac{V_{\rm DC,LV}}{8L_mf_s}\\
&A=i_r(t_2),B=\frac{v_{\rm LV}(t_2)-v_{C_r}(t_2)-v_{C_{\rm eq}}(t_2)}{L_r\omega_3},\\
&v_{\rm LV}(t_2)=0\,{\rm V},v_{C_{\rm eq}}(t_2)=\frac{V_{\rm DC,MV}}{2n}\approx\frac{V_{\rm DC,LV}}{2},\\
&v_{C_r}(t_2)=\frac{V_{\rm DC,LV}}{2}-\frac{P_0}{2V_{\rm DC,LV}f_sC_r},\\
&\text{Condition 2 }:Q_{r\,\max}\geq V_{\rm DC,LV}C_{oss}.
\end{aligned}\tag{5}$$

The first condition guarantees that the voltage of $C_{\rm eq}$ remains clamped to $V_{\rm DC,MV}/2n$ during the deadtime (LVO+ mode). The second condition means that the maximum Q_r ($Q_{r\max}$) should be sufficient to achieve ZVS. Q_r and $Q_{r\max}$ are defined as follows:

$$\begin{aligned}
Q_r&=\left|\int_{t_2}^{t_3}i_r(t)dt\right|\\
&=\left|\frac{B-(A\sin(\omega_3(t_3-t_2))-B\cos(\omega_3(t_3-t_2))}{\omega_3}\right|\\
i_r(t_3)=0\rightarrow Q_r&=\left|\frac{B-\sqrt{(A^2+B^2)}}{\omega_3}\right|.
\end{aligned}\tag{6}$$

According to the first condition, as shown in (5), $Q_{r\max}$ can be defined as

$$\begin{aligned}
Q_{r\,\max}&=\left|\frac{B}{\omega_3}-\frac{V_{\rm DC,LV}}{8L_mf_s\omega_3}\right|\\
&=V_{\rm DC,LV}C_{oss}+\frac{V_{\rm DC,LV}\sqrt{C_{oss}L_r}}{8L_mf_s}-\frac{2\pi^2P_0f_r^2C_{oss}L_r}{V_{\rm DC,LV}f_s}.
\end{aligned}\tag{7}$$

Fig. 7 shows that with the increase of L_r and L_m, $Q_{r\max}$ will decrease gradually. In other words, the ZVS condition will lose beyond a certain value of L_r or L_m. To achieve ZVS, appropriate parameters (L_r and L_m) are required.

By scanning through the parameters (L_r and L_m), the corresponding f_s can be derived to achieve ZVS, and the feasible parameters are highlighted in Fig. 8. Upon a fixed L_m, there is an upper limit and a lower limit of L_r in zone 1. It can be explained as follows. To ensure that $C_{\rm eq}$ is completely charged in DCM mode, L_r has a baseline, as shown in Fig. 4(a). However, in the LVO+ mode, Fig. 7(a) shows that the generated charge will fall below the ZVS threshold given too high L_r, and this puts a ceiling to L_r.

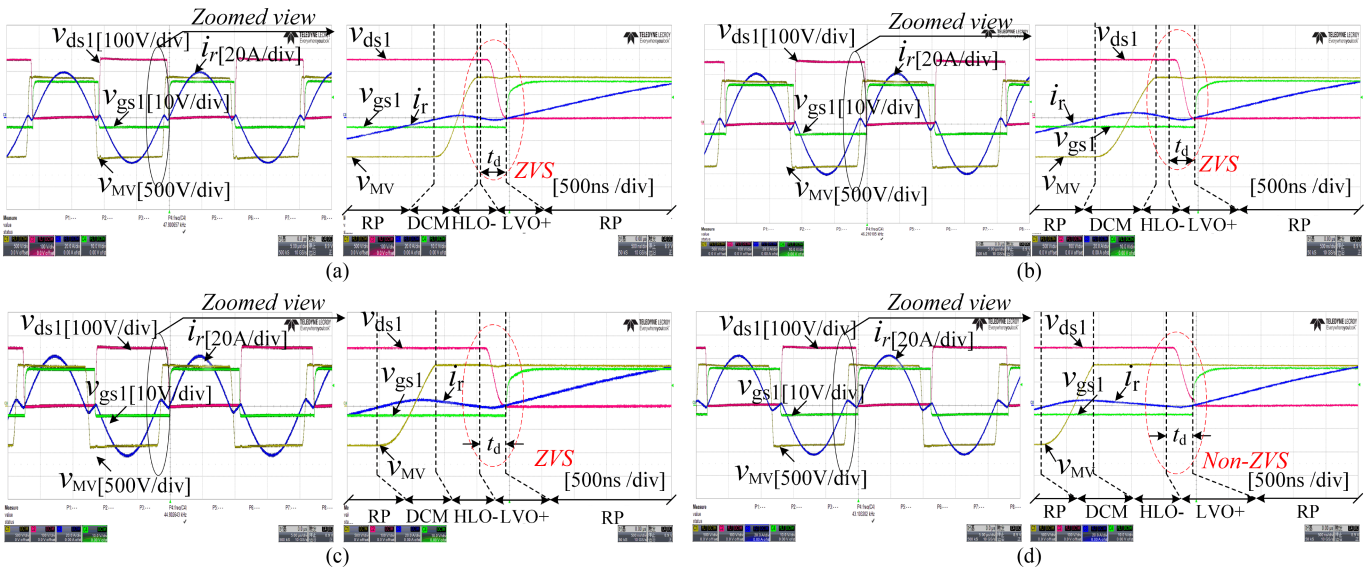

Fig. 11. Experimental results under different design points. (a) Experiment I. (b) Experiment II. (c) Experiment III. (d) Experiment IV.

TABLE I
KEY PARAMETER OF THE *LLC* CONVERTER

parameter	Values
MVDC bus ($V_{DC,MV}$)	1650 V
LVDC bus ($V_{DC,LV}$)	500 V
Rated power (P_0)	5.5 kW
Turns ratio	9:30
Resonant frequency (f_r)	52.6 kHz
Dead time (t_d)	390 ns
LV-side MOSFET (S_1–S_4)	CAB011M12FM3
MV-side diode (D_1–D_4)	MSC030SDA330B
Magnetizing inductance (L_m)	720 μH
Leakage inductance (L_k)	14 μH
Parasitic capacitors of MFT (C_p/C_s/C_{ps})	26 pF/72 pF/80 pF
Parasitic capacitors of devices (C_{oss}/C_j)	700 pF/160 pF
Extra capacitors paralleled on diode (C_{extra})	330 pF
Equivalent parasitic capacitance (C_{eq})	3000 pF/6660 pF

TABLE II
KEY PARAMETER OF EXPERIMENTS

parameter	Expt-I	Expt-II	Expt-III	Expt-IV
Resonant inductance (L_r)	21 μH	21 μH	24.2 μH	26.1 μH
Equivalent parasitic capacitance (C_{eq})	3000 pF	6660 pF	6660 pF	6660 pF
Switching frequency (f_s)	47.8 kHz	46.21 kHz	44.8 kHz	43.1 kHz
Efficiency (η)	98.8%	97.9%	97.7%	97.1%
Voltage ratio	0.994	0.99	0.99	0.9849

If L_k is less than the required L_r, an external inductor is necessary. However, an extra inductor will bring additional loss. In addition, a too low L_m is detrimental to the efficiency of converter. The optimal design scheme is that L_m is made large while covering zone 1, and L_r should be as small as possible in zone 1 while meeting the insulation requirement. Once L_r enters zone 1, C_{eq} can be fully charged in the DCM mode regardless of its value. Fig. 8 shows the design space (zone 1) against varied C_{eq}.

As presented in the previous paragraph, the optimal design represents the highest magnetizing inductance L_m and lowest resonant inductance L_r for high efficiency. Fig. 9 shows the optimal ones against parasitic capacitances. With the increase of C_{eq}, the ZVS boundary L_{mmax} is almost constant, which means that the design can achieve ZVS with most types of insulation structure and device selection.

III. EXPERIMENTAL VERIFICATION

The specifications of the *LLC*-DCX are shown in Table I. With a margin, the magnetizing inductance L_m is set to 720 μH rather than 770 μH. The parasitic parameters have a great influence on the circuit mode. The parasitic capacitance of switches and diode can be acquired through the datasheet. However, the parasitic parameters of transformer (C_p, C_s, and C_{ps}) can be measured through open-circuit and short-circuit tests, as diagramed in Fig. 10 [10].

To verify the ZVS conditions in the previous analysis and make a comparison, four experimental conditions are given in Table II. In experiments II–IV, C_{eq} is purposely increased through an extra capacitor ($C_{extra} = 330$ pF) paralleled on the diode. The design points within and beyond the boundary are labeled in Fig. 8 correspondingly.

Fig. 11 shows the experimental waveforms with the above parameters. Experiments I and II locate on the ZVS boundary and correspond to the optimal designs, with minimum resonant inductance L_r and maximum magnetizing inductance L_m. In experiment II, an additional capacitor is added to the rectifier bridge diode to increase the equivalent parasitic capacitance C_{eq}. Experiment II can also achieve ZVS with the same resonant inductance and magnetizing inductance even if the parasitic capacitance is increased. In experiment III, when the resonant inductance increases and approaches the ZVS boundary, ZVS can still be maintained. However, in experiment IV, the design point has exceeded the feasible region and ZVS is lost, as shown in Fig. 11(d). According to the test results, two conclusions can be drawn.

1) The analysis model is sufficiently accurate to predict ZVS boundary considering large parasitic capacitance in MV DCX applications.
2) The proposed design method for properly gauging resonant inductance can avoid unexpected ringing during deadtime so that the ZVS condition can be achieved independent of parasitic capacitance C_{eq}, i.e., insulation design.

IV. Conclusion

ZVS analysis and a design method for MV *LLC*-DCX with a high step-up ratio is proposed in this letter. The parasitic capacitances in an MV converter are nonnegligible due to high-voltage transformer and semiconductor devices, and their influence on switching mode is taken into consideration. It provides a guideline for ZVS design and the experimental results are given to verify the theory. Unlike the conventional method that extends bidirectional control to a unidirectional DCX, the proposed design method can achieve ZVS passively. It also enables ZVS under a loosen requirement on the transformer's parameter and insulation, thereby easing the fabrication of the MF transformer.

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