Si/WBG Hybrid Half-Bridge Converter Using Coupled Inductors for Power Quality Improvement and Control Simplification

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***Abstract*—The Si/WBG hybrid half-bridge (HHB) converter with hybrid frequency interleaved operation (HFIO) aims to offer an improved cost-performance tradeoff but suffers from uncompensable and low-frequency fluctuations in power quality issues and complicated control design. In this article, an Si/wide-bandgap (WBG) coupled half-bridge (CHB) is proposed, which coordinates the hybrid-frequency interleaved Si and WBG phase operation by a coupled inductor. By optimal configuring the coupling coefficient, the un-compensable, and low-frequency fluctuations of power quality issues can be completely addressed. Meanwhile, the HFIO controller is redesigned from the perspective of the modulated model predictive control, and the implementation can be greatly simplified under the selected optimal coefficient. A 3.3 kW Si insulated gate bipolar transistor (IGBT)/SiC MOSFET CHB totem-pole bridgeless PFC (TPBPFC) prototype is built as a case study to validate the proposed design concept. In comparison to conventional Si/SiC HHB TPBPFC, the proposed Si/SiC CHB TPBPFC can achieve a maximum 64.7% total harmonic distortion (THD) reduction, demonstrating the same low ripple and THD performance as full high-frequency two-phase all-SiC design in all operating ranges while with 16.7% cost reduction.**

***Index Terms*—Coupled inductor, high power quality, hybrid Si/WBG, power factor correction.**

I. Introduction

With the development of renewable energies and vehicles with electrified powertrains, there is an increasing demand for high power, high frequency, and cost-effective design in modern power supply applications. The emerging wide-bandgap (WBG) devices (such as SiC MOSFET, GaN HEMT) offer low ON-resistance, fast switching speed, and excellent reverse recovery properties, which makes the WBG-based converter become the center of attention in modern power supply applications [1], [2], [3]. However, the WBG devices have significantly higher cost/ampere ($/A), and their maximum current ratings and long-term reliability are considerably lower than their Si insulated gate bipolar transistor (IGBT) counterparts, which hinders their widespread employment in the commercial mainstream industry, especially in high-current applications [4], [5]. In addition, single WBG devices based half-bridges are still unable to operate at higher frequencies (usually$<$100 kHz) under hard-switching high-frequency processing for full power, resulting in a limited increase in converter effective frequency spectrum and hindering the size-reduction of the filter [6].

As an attractive solution to extend the effective frequency and enhance current capacity while reliving the high-cost issues for a full-WBG-based converter, the Si/WBG hybrid half-bridge (HHB) concept with a hybrid-frequency interleaving operation (HFIO) is proposed in [7], [8], [9], [10], [11], [12], [13], and [14]. Fig. 1(a) shows the basic topology of the Si/WBG HHB, in which the large-capacity Si IGBT phase operates at a low frequency to achieve the high-current and low-cost advantage, and the fractional power WBG phase operates at an ultrahigh frequency to compensate for low-frequency ripple of the Si IGBT phase, obtaining a high effective frequency with much-reduced cost. Several topology cases bear this concept have been proven to achieve fast dynamic response [7], [8], improved cost and performance tradeoff [9], [10], high frequency, and high power quality [11], which has implications for the limited rated capacity of WBG devices at this stage. Wu et al. [7], [8] propose a 3Φ4 W Si IGBT/SiC MOSFET grid-connected hybrid-frequency parallel inverter to achieve fast response and low current distortion. Similarly, the Si/SiC HHB-based totem-pole bridgeless PFC (TPBPFC) converters have been reported in [9] and [10], and Si/GaN MHz frequency power factor correction (PFC) in [11]. Based on those topology-specific case studies, Zhang et al. [14] offered a comprehensive discussion about the HHB approach, including the cost, power quality, and general control strategies.

However, as the soul of the Si/WBG HHB approach, the HFIO still has some key issues, complicated control design,

Manuscript received 18 July 2023; revised 28 October 2023; accepted 3 December 2023. Date of publication 13 December 2023; date of current version 26 January 2024. This work was supported in part by Guidateganghezi Project under Grant TGHZ 2022[45], in part by National Key Research and Development Program of China under Grant 2022YFE0205300, in part by Guizhou Provincial Science and Technology Projects under Grants ZK [2022] General 154 and [2022] General 012, and in part by National Natural Science Foundation of China under Grants 52067004, 52167007, and 52367019. Recommended for publication by Associate Editor C. DiMarino. *(Corresponding author: Xufeng Yuan.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3342133.

Digital Object Identifier 10.1109/TPEL.2023.3342133

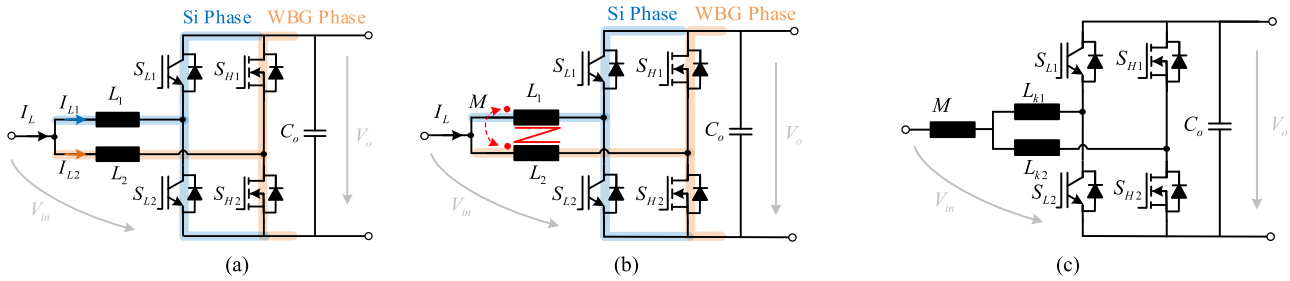

Fig. 1. Topologies of the conventional Si/WBG HHB circuit, proposed Si/WBG CHB circuit and equivalent circuit for Si/WBG CHB. (a) Si/WBG HHB circuit. (b) Proposed Si/WBG CHB circuit. (c) Equivalent circuit for Si/WBG CHB.

and power quality issues, that have not been addressed well. The key idea of HFIO is to use the high-frequency WBG phase to cancel the Si phase current ripple in real-time, achieving the hybrid-frequency interleaving benefits [10], [14]. To achieve a real-time ripple-cancellation task, many complex controllers are reported to compensate for the Si IGBT phase ripple, such as direct digital control in [7] and [8], Si IGBT phase switching signals feedback control in [9] and [14], and finite step model predictive current control in [13], which significantly increases the complexity of the controller. Furthermore, due to the sampling and calculation delay of the discrete control system [15], the WBG phase duty cycle cannot immediately respond to the rapid changes in the Si IGBT phase current (according to different Si IGBT phase switching functions), which results in low-frequency fluctuations in total current and seriously affects the power quality of the converter. Besides, the WBG phase may not fully compensate for the Si phase current ripple in some port voltage conditions, leading to the abnormal current and further affecting the power quality. Reference [14] tried to use a dynamically coordinated and variable operation mode strategy to address the uncompensable issues, but it further increases the complexity of the controller design and still cannot achieve full-range compensation.

In this article, a Si/WBG coupled half-bridge (CHB) approach is proposed, as shown in Fig. 1(b), which coordinates the HFIO of the Si IGBT and WBG phases by a coupled inductor to address the power quality issue and complicated control design issues. By optimal configuring the coupling coefficient, the proposed Si/WBG CHB design not only achieves the full-range compensation but also minimizes the low-frequency fluctuations, obtaining high power quality in the entire operating range. Meanwhile, the control implementation of hybrid-frequency interleaving operation can be significantly simplified based on the proposed Si/WBG CHB design with an optimal coupling coefficient. The authors recently reported the Si/WBG CHB concept in a Si IGBT/SiC MOSFET TPBPFC [16], but some important issues, such as the mechanism of the power quality issues, coupling coefficient optimization, etc., have not been comprehensively addressed. In this article, the general principle and design considerations of Si/WBG CHB are comprehensively discussed. The proposed Si/WBG CHB approach improves the power quality performance while maintaining the cost-effectiveness advantages, which is suitable for high power quality and cost-effectiveness applications.

The rest of this article is organized as follows. Section II first discusses the topologies and operation principles of the Si/WBG CHB, then the power quality issues are analyzed. Section III presents the optimal coefficient and implementation of the coupled inductor. In Section IV, a control strategy based on modulated model predictive control (MMPC) is proposed, and then the computational effort comparisons between the Si/WBG HHB and CHB are presented. In Section V, an Si/SiC CHB TPBPFC is selected as a case study, and topology and hardware prototypes are presented along with experimental results to validate the proposed concept. Finally, Section VI concludes this article.

II. Proposed Si/WBG CHB Approach

A. Topologies and Operation Principle

Fig. 1(b) shows the topologies of a Si/WBG CHB circuit, which is composed of a low-frequency large-capacity Si phase and a high-frequency small-capacity WBG phase. The Si phase consists of two large current Si IGBT with anti-parallel diodes (S_{L1}, S_{L2}), while the WBG phase uses only two small current WBG devices (S_{H1}, S_{H2}). Those two phases are coupled by the inductors L_1 and L_2 with a factor k, and the mutual inductor M and the voltage across the inductors can be expressed as follows:

$$\begin{cases} M = M_{12} = M_{21} = k\sqrt{L_1 L_2} \\ \dot{U}_{L1} = j\omega \underbrace{(L_1 - M)}_{L_{k1}} \dot{I}_{L1} + j\omega M \dot{I}_L \\ \dot{U}_{L2} = j\omega \underbrace{(L_2 - M)}_{L_{k2}} \dot{I}_{L2} + j\omega M \dot{I}_L \end{cases} \tag{1}$$

where k ($-1 < k < 1$) is the coupling coefficient. And $k = 0$ is for uncoupling, $k > 0$ is for positive coupling, and $k < 0$ is for negative coupling. Therefore, the coupled inductor can be simplified by an equivalent circuit with three decoupled inductors: mutual inductance M, and leakage inductors of windings L_{k1} and L_{k2}, as shown in Fig. 1(c). And the relation between those three decoupled inductors can be expressed as follows:

$$\begin{cases} L_{k1} = L_1 - M \\ L_{k2} = L_2 - M. \end{cases} \tag{2}$$

It should be noted that when the $k = 0$, the Si/WBG CHB degenerates to the Si/WBG HHB, thus the Si/WBG HHB can be seen as a special case of the Si/WBG CHB design.

TABLE I
CURRENT SLOPES FOR DIFFERENT OPERATION STATES

	State I ($S_L = 0, S_H = 0$)	State II ($S_L = 0, S_H = 1$)	State III ($S_L = 1, S_H = 0$)	State IV ($S_L = 1, S_H = 1$)
f_{L1}	$\frac{L_{k2}(V_{in}-V_o)}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$	$\frac{-MV_o+L_{k2}V_{in}-L_{k2}V_o}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$	$\frac{L_{k2}V_{in}+MV_o}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$	$\frac{L_{k2}V_{in}}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$
f_{L2}	$\frac{L_{k1}(V_{in}-V_o)}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$	$\frac{L_{k1}V_{in}+MV_o}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$	$\frac{-L_{k1}V_o+L_{k1}V_{in}-MV_o}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$	$\frac{L_{k1}V_{in}}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$
f_L	$\frac{(L_{k2}+L_{k1})(V_{in}-V_o)}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$	$\frac{L_{k1}V_{in}-L_{k2}V_o+L_{k2}V_{in}}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$	$\frac{-L_{k1}V_o+L_{k1}V_{in}-MV_o}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$	$\frac{L_{k2}V_{in}+L_{k1}V_{in}}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}}$

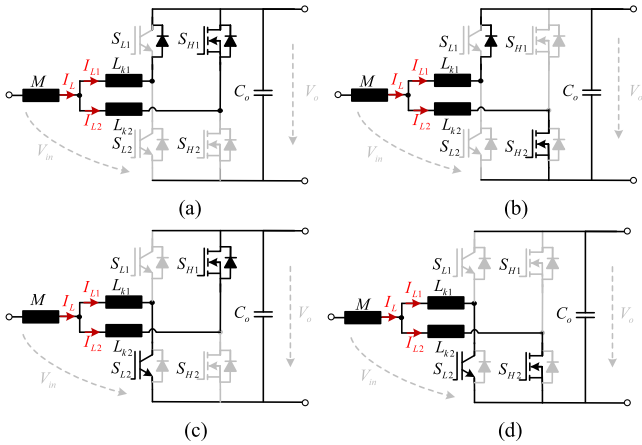

Fig. 2. Operation states of the proposed Si/WBG CHB circuit. (a) State I ($S_L = 0$, $S_H = 0$). (b) State II ($S_L = 0$, $S_H = 1$). (c) State III ($S_L = 1$, $S_H = 0$). (d) State IV ($S_L = 1$, $S_H = 1$).

For the sake of convenience and without loss of generality, the Si/WBG CHB applied to an ac application is analyzed. Two switching functions S_H and S_L are introduced to stand for the switching states. If S_L (S_H) $= 0$, S_{L2} (S_{H2}) is OFF and S_{L1} (S_{H1}) is ON, and vice versa. There are two pairs of power switches in the proposed Si/WBG CHB design, thus obtaining four different operation states, and the equivalent circuits are shown in Fig. 2.

State I (t_4-t_5), in which $S_L = 0$ and $S_H = 0$, the simplified circuit is shown in Fig. 2(a). Due to the forward conducting characteristics of the Si IGBT, although S_{L1} is ON, only the anti-paralleled diode is turned ON for reverse conduction. While the MOSFET channel can process the current bidirectionally, which means the MOSFET channel and body diode are paralleled to process the reverse current. Based on Kirchhoff's law, the state-space equations can be obtained as follows:

$$\begin{cases} M\frac{dI_L}{dt} + L_{k1}\frac{dI_{L1}}{dt} = V_{\text{in}} - V_o \\ M\frac{dI_L}{dt} + L_{k2}\frac{dI_{L2}}{dt} = V_{\text{in}} - V_o \end{cases} \tag{3}$$

where V_{in} stands for the input port voltage, and V_o stands for the output port voltage. Therefore, those three current slopes can be delivered as follows:

$$\begin{cases} f_{L1,\text{I}} = \frac{L_{k2}(V_{\text{in}}-V_o)}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}} \\ f_{L2,\text{I}} = \frac{L_{k1}(V_{\text{in}}-V_o)}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}} \\ f_{L,\text{I}} = \frac{(L_{k2}+L_{k1})(V_{\text{in}}-V_o)}{ML_{k1}+ML_{k2}+L_{k2}L_{k1}} \end{cases} \tag{4}$$

where $f_{L1,\text{I}}$, $f_{L2,\text{I}}$, and $f_{L,\text{I}}$ are the current slopes of the Si phase current, WBG phase current, and total current under the operation *State I*. The WBG phase adopts the synchronous rectifier mode, i.e., a turn-ON signal is applied to the WBG devices (usually MOSFET) during the reverse conduction period. Therefore, the MOSFET channel and the body diode are both in the ON state to conduct reverse currents during *State I* and *State III*. The equivalent circuits for operation *States II–IV* are shown in Fig. 2(b)–(d), and those current slopes can be obtained by the same derivation processes, the results are summarized in Table I.

B. Hybrid-Frequency Interleaving Operation

Fig. 3 shows the hybrid-frequency interleaving operation of the Si/WBG CHB design during an ac application with amplitude current value I_m, which allows the Si phase to process a large current at a low frequency and the WBG phase to process only a small fractional current at an ultrahigh frequency.

The Si phase operates at an extremely low frequency to relieve the high switching-losses issues, but the low-frequency operation will be resulting in a large current ripple, shown by the green line in Fig. 3(a). Different from the conventional Si/WBG HHB in which the Si phase current slope is constant at a fixed S_L, the Si phase current slope in Si/WBG CHB will vary with the WBG phase switching function S_H even with a fixed S_L due to the coupled inductor.

The WBG phase operates at an ultrahigh frequency to reduce the Si phase current ripple in terms of processing only a factional of the total current, shown by the orange line. Through the coupling of those two-phase currents, the Si phase current ripple can be completely eliminated. After combining those two currents, the total current exhibits a high effective frequency (the same as the WBG phase switching frequency) and excellent power quality performance, shown by the blue line.

In addition, the detailed waveforms for different operation states are plotted in Fig. 3(b), in which the ripples of the Si phase and WBG phase have been canceled each other, obtaining a high-quality total current performance, shown in the blue line.

C. Power Quality Issues for HFIO

1) Uncompensable Range Issue: In HFIO, the WBG phase is designed to cancel the Si phase current ripple, the ability to eliminate the Si phase current ripple is a critical issue affecting the high-power quality of the proposed Si/WBG CHB design.

The WBG phase switching frequency is much higher than that of the Si phase, the Si phase switching function S_L can be

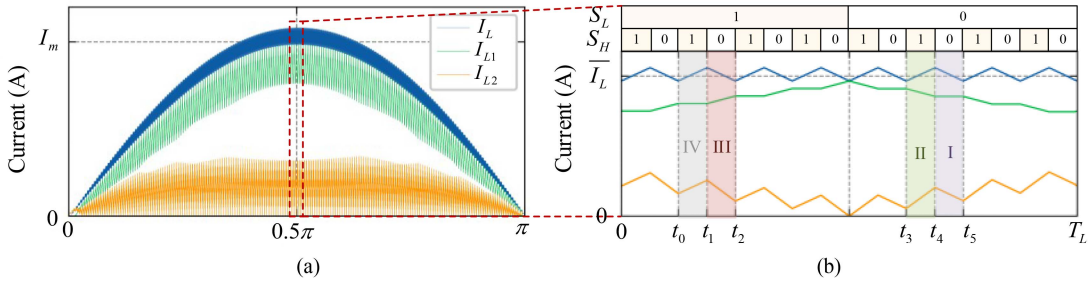

Fig. 3. Current waveforms for the proposed Si/WBG CHB during (a) a half-line cycle and (b) an Si phase switching cycle T_L.

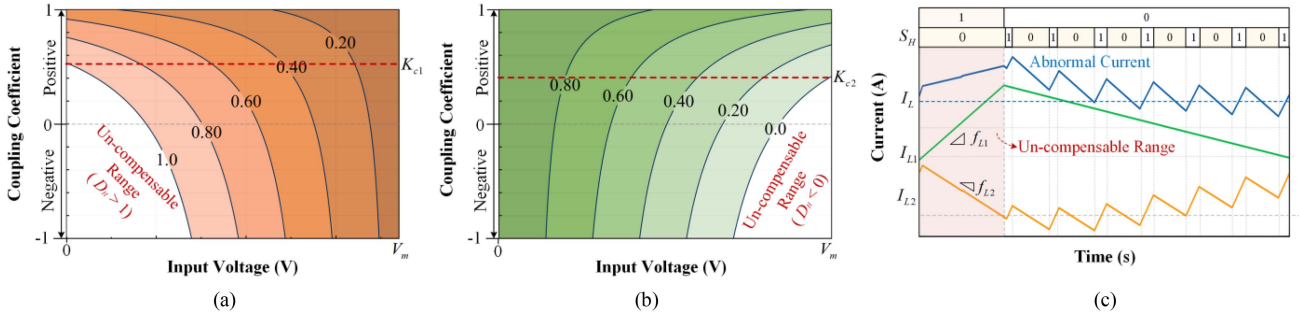

Fig. 4. Uncompensable range in a PFC application, note that the improper coupling coefficient selection will lead to abnormal input currents. (a) $D_H^{S_L=1}$ under different conditions. (b) $D_H^{S_L=0}$ under different conditions. (c) Abnormal current in un-compensable range.

regarded as constant during each WBG phase switching cycle T_H. Different operation state combinations should be selected according to different S_L. The details are as follows.

1) Switching cycle T_H with $S_L = 0$, in which *State I* and *II* are selected for modulation. The variation value for the total current can be expressed as follows:

$$\Delta I_L^{S_L=0} = f_{L,\mathrm{I}}\left(1 - D_H^{S_L=0}\right) T_H + f_{L,\mathrm{II}} D_H^{S_L=0} T_H \tag{5}$$

where $f_{L,\mathrm{I}}$ and $f_{L,\mathrm{II}}$ stand for the total current slopes in *State I* and *II*, which can be obtained from Table I. $D_H^{S_L=0}$ is the duty cycle for switching cycle T_H with $S_L = 0$.

2) Switching cycle T_H with $S_L = 1$, in which *State III* and *IV* are selected for modulation. The variation value for the total current can be expressed as follows:

$$\Delta I_L^{S_L=1} = f_{L,\mathrm{III}}\left(1 - D_H^{S_L=1}\right) T_H + f_{L,\mathrm{IV}} D_H^{S_L=1} T_H \tag{6}$$

where $f_{L,\mathrm{III}}$ and $f_{L,\mathrm{IV}}$ stand for the total current slopes in *States III* and *IV*, which can be obtained from Table I. $D_H^{S_L=1}$ is the duty cycle for switching cycle T_H with $S_L = 1$.

In the steady state, if the Si phase current ripple is completely canceled by the WBG phase, the total current variation value must be kept at zero in each switching cycle, i.e.

$$\Delta I_L^{S_L} = 0 \tag{7}$$

Substituting (2), (5), (6) into (7), the duty cycle for the WBG phase can be obtained as follows:

$$\begin{cases} D_H^{S_L=0} = \frac{(V_o - V_{\mathrm{in}})(L_{k1}+L_{k2})}{L_{k1} V_o} \\ D_H^{S_L=1} = \frac{L_{k1} V_o - (L_{k1}+L_{k2}) V_{\mathrm{in}}}{L_{k1} V_o} \end{cases} \tag{8}$$

The prerequisite for complete compensation of Si phase current ripple is that the WBG phase duty cycle D_H is always in the modulation range of [0, 1], which can be expressed as follows:

$$\begin{cases} 0 \le D_H^{S_L=0} \le 1 \\ 0 \le D_H^{S_L=1} \le 1 \end{cases} \tag{9}$$

Considering a general ac application with the sinusoidal input voltage with amplitude V_m and the fixed output voltage V_o. Fig. 4(a) and (b) show the duty cycle under different voltage conditions and coupling coefficients [–1, 1], respectively. If the duty cycle exceeds the limitation of (9), the Si phase current ripple cannot be completely compensated by the WBG phase, which is named as an *uncompensable range*, as shown by the white area in Fig. 4(a) and (b). The uncompensable range is determined by the port voltage and inductors, which is independent of the control strategy. It can be seen that there always have uncompensable ranges near the zero-crossing voltage and the peak voltage for a negative coupling ($k < 0$). In the uncompensable range, the Si phase current ripple cannot be compensated even if the WBG phase remains fully ON or OFF state during the entire operation cycle, i.e., the WBG phase current slope f_{L2} is smaller than that of Si phase f_{L1}, which will result in the abnormal current, shown in Fig. 4(c). The abnormal current will seriously affect the power quality and total harmonic distortion (THD) performance of the

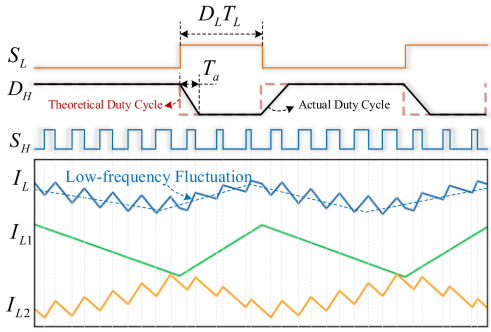

Fig. 5. Diagram of the low-frequency fluctuation issue. Note that the variation of the WBG phase duty cycle under different S_L will lead to low-frequency fluctuations, resulting in poor power quality issues.

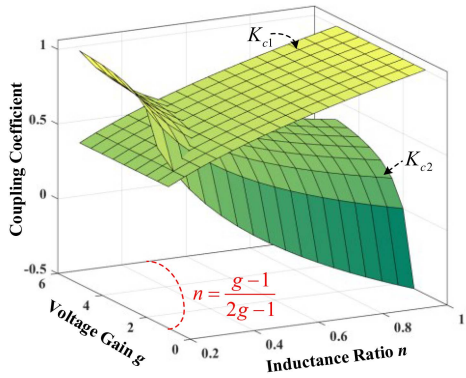

Fig. 6. Relationship between K_{c1}, K_{c2}, g, and n.

proposed Si/WBG CHB design. Furthermore, by subtracting (2), (8) into (9), the boundary conditions of the compensable range can be expressed as follows:

$$\begin{cases} K_{c1} = \sqrt{\frac{L_2}{L_1}} \\ K_{c2} = \frac{L_1 V_m + L_2 V_m - L_1 V_o}{2(V_m - V_o)\sqrt{L_1 L_2}}. \end{cases} \tag{10}$$

2) Low-Frequency Fluctuation Issue: As shown in Fig. 5, the duty cycle of the WBG phase must be renewed in real-time according to the Si phase switching function S_L. Due to the one-cycle delay and duty cycle adjustment time of the discrete control system, the actual duty cycle will have a delay time of T_a and cannot immediately follow the high-frequency sudden change of the S_L signal. It will lead to small low-frequency fluctuations in the total current waveform, as shown by the blue line in Fig. 5. Therefore, the variation of the WBG phase duty cycle under different S_L must be minimized to decrease the impact of the T_a and eliminate low-frequency fluctuations.

III. Coupled Inductor Design

In this section, the optimal coupling coefficient is derived from the compensable range and duty cycle variation aspects. Based on the selected optimal coefficient, a simple implementation scheme and loss analysis of coupled inductors, current ripple analysis are presented. The details are as follows.

A. Optimal Coupling Coefficient

Different from conventional coupled inductor design, the proposed coupled inductor design in the proposed Si/WBG CHB have two windings with different operation frequency and processed power. Thus, the coupling coefficient should be carefully designed to address the uncompensable, and low-frequency fluctuations of power quality issues.

First, to ensure complete cancelation for Si phase current ripple under all the input voltage range, the coupling coefficient must satisfy the following formula as follows:

$$1 \geq k \geq \max(K_{c1}, K_{c2}) \tag{11}$$

From (10), it can be seen that the K_{c1} is fixed with a selected inductance, while K_{c2} is varied under different port voltages. Thus, the limitation relation between the inductance and voltage should be analyzed.

To simplify the analysis, define the inductance ratio $n = L_2 / L_1$ and the voltage gain $g = V_o / V_m$, thus the boundary conditions of the compensable range can be simplified as follows:

$$\begin{cases} K_{c1} = \sqrt{n} \\ K_{c2} = \frac{1-g+n}{2(1-g)\sqrt{n}} \end{cases} \tag{12}$$

Since the WBG phase inductance is smaller than the Si phase, thus n belongs to the (0, 1). The voltage gain is bigger than 1. Fig. 6 shows the curves of K_{c1} and K_{c2} under different n and g, in which K_{c1} is bigger than K_{c2} in most cases. To obtain a stable full-range compensation range, $K_{c1} > K_{c2}$ must be guaranteed at all port voltage conditions, thus the inductance design of the Si/WBG CHB should satisfy those following constraints:

$$n \geq \frac{g-1}{2g-1} \tag{13}$$

After following the constraint in (13), the coupling coefficient only needs to satisfy the following formula to achieve the full range compensation

$$k \geq K_{c1} \tag{14}$$

Therefore, the inductance design process must check whether the inductances meet (13) at all port voltages to ensure that K_{c1} is always greater than K_{c2}, further covering all the uncompensable ranges to ensure complete compensation under full port voltage conditions.

Second, the variation of the WBG phase duty cycle under different S_L must be minimized to eliminate low-frequency fluctuations of the total current. According to (8), the duty cycle variation value can be expressed as follows:

$$\Delta D_H = \left| D_H^{S_L=1} - D_H^{S_L=0} \right| = \left| \frac{L_2 - k\sqrt{L_1 L_2}}{L_1 - k\sqrt{L_1 L_2}} \right| \tag{15}$$

Equation (15) indicates that the duty cycle variation is only determined by the self-inductance and coupling coefficient and is not dependent on the operation voltage. To minimize the low-frequency fluctuations, the duty cycle variation should be

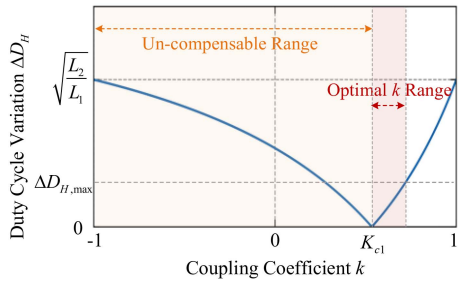

Fig. 7. Range of the optimal coupling coefficient.

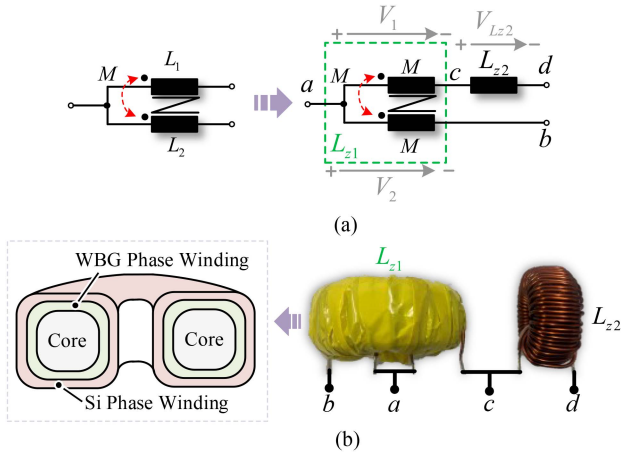

Fig. 8. Implementation of the coupled inductor. (a) The simplification of the coupled inductor. (b) The structure and photo of the coupled inductor.

smaller than the limitation value $\Delta D_{H,\max}$, which can be expressed as follows:

$$\Delta D_H \le \Delta D_{H.\max} \tag{16}$$

Fig. 7 shows the duty cycle variation under different coefficients, the optimal coupling coefficient can be obtained by combining the uncompensable range in (14), shown by the red part, which can be expressed as follows:

$$k \in \left[\sqrt{\frac{L_2}{L_1}}, \frac{L_2 - \Delta D_{H,\max} L_1}{\sqrt{L_1 L_2} - \Delta D_{H,\max}\sqrt{L_1 L_2}}\right] \tag{17}$$

Note that k in the range can achieve a full range of compensation and greatly reduce the low-frequency fluctuation, obtaining significant power quality improvement. Especially, when $k = K_{c1}$, the duty cycle variation is equal to 0, which can eliminate low-frequency fluctuations.

B. Implementation of Coupled Inductor

Based on the optimal coupling coefficient discussion, if $k = K_{c1}$, the mutual inductor M equals L_2, thus the L_2 can be considered as a fully coupled inductor. Therefore, the coupled inductors L_1 and L_2 can be divided into a fully coupled inductor L_{z1}, and a noncoupled inductor L_{z2}, as shown in Fig. 8(a). The fully coupled inductor L_{z1} can be regarded as a single inductor with two unequal-current windings, and the coupling coefficient $k_{z1} = 1$ can be well implemented and met by a toroidal core with a laminated winding method without complex air gaps design, as shown in Fig. 8(b).

Compared to conventional Si/WBG HHB, the fully coupled inductor introduced a strong dc current into the WBG inductors, which may cause concern about core loss. Therefore, the core loss of the inductor is analyzed, which is mainly consisting of hysteresis loss, eddy current loss, and residual loss. Under the pulsewidth modulation (PWM) modulation with nonsinusoidal excitation, the core loss can be calculated by modified Steinmetz equation [17], [18] as follows:

$$P_{\text{core}} = \frac{1}{T_m}\int_0^{T_m}\left[V_c K_c\left(\frac{2}{\Delta B^2\pi^2}\int_0^{T_s}\left(\frac{dB}{dt}\right)^2 dt\right)^{\alpha-1}\left(\frac{\Delta B}{2}\right)^{\beta} f_s\right] \tag{18}$$

where V_c is the volume of the core, T_s and f_s are the switching period cycle and switching frequency, T_m is the integration cycle, which can be a line cycle in an ac application, and α and β are the fit parameters of core loss density, which can be found in the core datasheets. Equation (18) indicates that the core loss is not only related to the dc bias current, but also related to the amplitude and slope of magnetic flux peak—peak value ΔB. Due to the influence of a re-magnetization, the core loss is different under the equal ΔB but different dc-bias, thus the K_c should be regulated under different dc biases as a fitness function of the B_{DC} and ΔB, which should be expressed as follows [18]:

$$K_c = K_{cd}\left(1 + K_1 B_{\text{dc}} e^{(-\Delta B/K_2)}\right) \tag{19}$$

where K_{cd} is the fitness parameters under no dc bias conditions, which can be found in the core datasheets. K_1 and K_2 are fitness parameters, which can be obtained by measurements at different frequencies and magnetization. B_{dc} is the dc magnetic flux, which can be calculated as follows:

$$B_{\text{dc}} = F(H_{\text{dc}}) = F\left(\frac{4\pi N I_{\text{dc}}}{l_e}\right) \tag{20}$$

where N and l_e are the turns number and magnetic length of the inductor, I_{dc} stands for the dc average current, $F(H)$ is the B–H fitness function, which can be found on the core datasheets. ΔB is the ac magnetic flux peak–peak amplitude, which corresponds to volt-sec law, and can be expressed as follows [19]:

$$\Delta B = \frac{Vt}{NA} = \frac{L\Delta i}{NA} \tag{21}$$

where V and t are the voltage and corresponding applied time for the inductors, ΔI is the current ripple, L is the inductance, and N and A are the turns number and cross-sectional area of the inductors. Equation (21) indicates that the ac magnetic flux peak–peak amplitude ΔB also can be expressed in the form of a current ripple.

Table II summarizes the applied voltage the voltage across the inductors in Si/WBG design. It can be seen that the voltage of the two windings in L_{z1} always remains the same, which can be seen as those two windings in a parallel mode. Due to the effect of coupling inductance L_{z1}, the voltages applied to inductor L_{z2}

TABLE II
VOLTAGES ACROSS THE INDUCTORS IN SI/WBG HHB DESIGN

States	Applied Time	V_1	V_2	V_{Lz2}
State I	$(1-D_L)(1-D_H)T_L$	$V_{\text{in}}-V_o$	$V_{\text{in}}-V_o$	0
State II	$(1-D_L)\,D_HT_L$	V_{in}	V_{in}	$-V_o$
State III	$D_L\,(1-D_H)T_L$	$V_{\text{in}}-V_o$	$V_{\text{in}}-V_o$	V_o
State IV	$D_L\,D_HT_L$	V_{in}	V_{in}	0

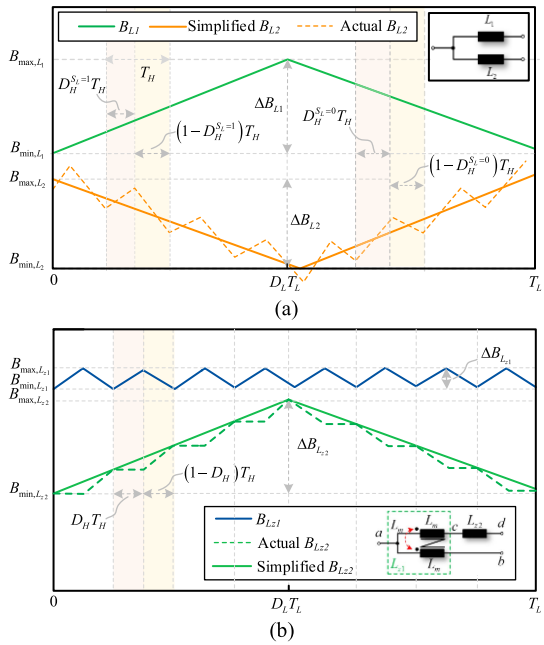

Fig. 9. Magnetic flux comparison between the conventional HHB and proposed CHB. (a) Conventional Si/WBG HHB. (b) Proposed Si/WBG CHB.

under *States I* and *IV* are equal to zero, only *States II* and *III* have the applied voltages.

Fig. 9(a) shows the magnetic flux of the inductors in conventional Si/WBG HHB. Since the Si phase has a large low-frequency current ripple, it results in a large peak–peak value of magnetic flux ΔB_{L_1}. The WBG phase operates in a high-frequency manner to cancel the Si phase ripple, thus the WBG phase current consists of a large low-frequency ripple and a small high-frequency ripple, and the high-frequency ripple can be simplified for convenience analysis. Therefore, it can be seen that the ac flux densities for both inductor L_1 and L_2 in conventional HHB are related to the Si phase switching period T_L. Based on the volt-sec law of the ac flux density, both two inductors in conventional HHB have a large ac magnetic flux due to the long applied period.

Fig. 9(b) shows the magnetic flux of the inductors in the proposed Si/WBG CHB. Due to the coupled effect, the Si phase current will be varied with the WBG phase switching cycle, thus the Si phase current consists of a large low-frequency ripple and a small high-frequency ripple, and the high-frequency ripple can be simplified for convenience analysis. The ac flux density for inductor L_{z2} in the proposed CHB design is the same as the Si phase inductors in the HHB design. Note that the effect of two-phase current positive coupling in L_{z1} is equivalent to the total current applied into the core, which has a strong dc bias but with a smaller current ripple. The voltage on L_{z1} is only varied with the WBG phase switching function S_H and is independent of the Si phase switching function S_L, which has a much-reduced applied time due to the high-frequency operation of the WBG phase.

Therefore, although the positive coupling operation introduces a strong dc bias flux into the coupled inductor core (L_{z1}), the peak–peak value of magnetic flux $\Delta B_{L_{z1}}$ and the core loss will not significantly increase because the current ripple is greatly decreased by the hybrid-frequency interleaving operation, and the detailed loss comparison of a specific case study can be found in Section V.

C. Current Ripple Analysis

The Si phase current ripple in Si/WBG CHB design can be expressed based on the operation principle and current slopes for different operation states as follows:

$$\Delta I_{Lz2,\text{CHB}} = f_{L1,\text{IV}} D_H^{S_L=1} D_L T_L + f_{L1,\text{III}} \left(1-D_H^{S_L=1}\right) D_L T_L \tag{22}$$

where $f_{L1,\text{IV}}$, and $f_{L1,\text{III}}$ are the Si IGBT phase current scope under operation states *IV* and *III*. D_L and T_L are the Si IGBT phase duty cycle and switching period. Substituting the current scope and duty cycle into (22), the Si phase current ripple in Si/WBG CHB can be simplified as follows:

$$\Delta I_{Lz2,\text{CHB}} = \frac{V_{\text{in}} D_L T_L}{L_{z2}} \tag{23}$$

It can be seen that the expression Si phase current ripple in Si/WBG CHB is the same as that of conventional Si/WBG HHB.

The total current ripple in Si/WBG CHB design needs to be expressed according to different low switching function S_L, which can be obtained as follows:

$$\begin{cases} \Delta I_L^{S_L=1} = D_H^{S_L=1} f_{L,\text{IV}} T_H \\ \Delta I_L^{S_L=0} = D_H^{S_L=0} f_{L,\text{II}} T_H \end{cases} \tag{24}$$

where T_H is the switching cycle for the high-frequency WBG phase. $f_{L,\text{IV}}$ and $f_{L,\text{II}}$ stand for the total current scope under operation states IV and II, respectively. The conventional Si/WBG HHB can be seen as the special case of the CHB with $k=0$. Substituting (8) and current slopes into (23), the conventional Si/WBG HHB design shows two ripple behaviors under different S_L [14], thus the total current ripple for conventional Si/WBG HHB should take the larger value of current ripple under different Si phase switching functions, which can be expressed as follows:

$$\Delta I_{L,\text{HHB}} = \max\left(\Delta I_L^{S_L=1}(k=0), \Delta I_L^{S_L=0}(k=0)\right) \tag{25}$$

For the proposed Si/WBG CHB, if $k=K_{c1}$ and substituting (8) into (24), the $\Delta I_{L,\text{CHB}}$ can be expressed as follows:

$$\Delta I_{L,\text{CHB}}^{S_L=1} = \Delta I_{L,\text{CHB}}^{S_L=0} = \frac{V_{\text{in}}\,(V_o - V_{\text{in}})\,T_H}{V_o L_2} \tag{26}$$

Different from the conventional Si/WBG HHB design showing two ripple behaviors under different S_L [14], the total current

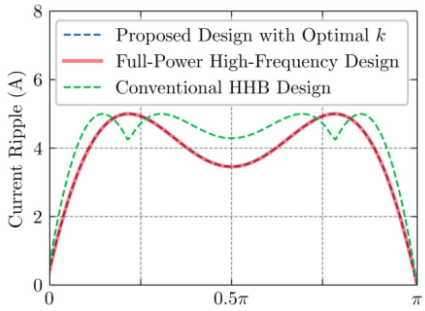

Fig. 10. Total current ripple comparison between the conventional Si/WBG CHB, the proposed Si/WBG CHB design, and the conventional full-power high-frequency design.

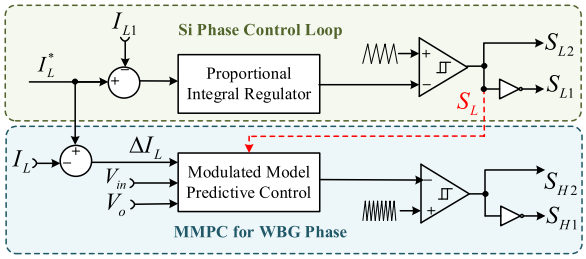

Fig. 11. Proposed control structure for HFIO-based Si/WBG CHB design from the perspective of modulated model predictive control.

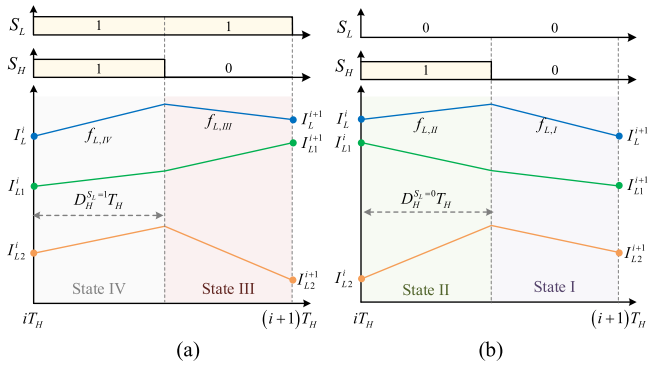

Fig. 12. Current waveforms during a WBG phase switching cycle T_H. (a) $S_L = 1$. (b) $S_L = 0$.

ripple exhibits the same behavior under different S_L, which is only determined by the high-frequency WBG phase. Furthermore, Fig. 10 shows the total current ripple quality comparison between conventional Si/WBG CHB, the proposed Si/WBG CHB design, and conventional full-power high-frequency processing. Compared to conventional Si/WBG HHB, the proposed Si/WBG CHB can reduce the current ripple under the whole line cycle. And two current ripple curves of the proposed CHB design and the full-power high-frequency design overlap perfectly, which means the proposed Si/WBG CHB design can obtain the same benefits as a full-power high-frequency processing design by only a fractional high-frequency power processing, obtaining an improved tradeoff between the cost and power quality performance.

Therefore, the coupled inductance L_{z1} is selected to meet the input current ripple requirements. Based on the Si/WBG CHB ripple model and general PFC design guidelines [20], [21], the WBG phase inductance design must ensure that the maximum total current ripple is always lower than the allowable ripple ratio, which can be expressed as follows:

$$L_{z1} \geq \frac{V_{\text{in}}^2 \left(V_o - V_{\text{in}}\right) T_H}{2 P_o V_o r_{L,\max}} \tag{27}$$

where $r_{L,\max}$ is the allowable maximum current ripple ratio for total current. The design of the Si phase inductance L_{z2} is the same as the conventional PFC design, except that the Si phase is allowed to operate at a larger ripple ratio since its current ripple can be canceled by the high-frequency WBG phase.

IV. Control Strategy

This section redesigns the high-frequency WBG phase controller from the perspective of MMPC, and then the computational effort of the WBG phase controller in the conventional Si/WBG HHB and the proposed Si/WBG CHB are compared. The details are as follows.

A. Control Strategy

Fig. 11 shows the master–slave control structure for the proposed Si/WBG CHB design, in which the Si phase is used as the master phase to initially track the total current reference value, while the WBG phase is used as the slave phase to refine the total current.

The master Si phase is using the conventional proportional-integral (PI) regulator to track the difference between the Si phase current and the total reference current, ensuring that the Si phase current always follows the reference value.

The slave WBG phase is designed to achieve the Si phase switching ripple real-time compensation, which requires the WBG phase controller to have a high enough bandwidth to be sensitive to Si phase current ripple variations. Zhang et al. [14] use the Si phase switching function S_L to predict the Si phase current variation in advance, and then take consideration into the WBG phase controller, but it will increase the complexity of the WBG phase controller design. Meanwhile, the two-phase currents for Si/WBG CHB design are interfaced with each other due to the coupled inductor, thus it's difficult for conventional PI controllers to achieve these requirements. This article redesigned the WBG phase control loop from the perspective of MMPC, the controller diagram is shown in the blue box. The MMPCs are widely used in a variety of power electronic controllers, which have strong robustness and fast-tracking response and can easily handle multivariable cases, system constraints, and nonlinearities in a very intuitive way [22], [23].

The key function of the WBG phase is to track the total current reference value and meet the ripple requirements, thus the total current is directly used for the WBG phase control feedback. Similarly, different operation state combinations should be selected for model prediction modulation according to different S_L, as shown in Fig. 12. If an initial measured total inductor

current value I_L^i at the time (i) is considered, a one-step-ahead prediction for the total current value at a time (i+1) can be expressed as follows:

$$I_L^{i+1} = \begin{cases} I_L^i + f_{L,\mathrm{IV}} D_H^{S_L=1} T_H + f_{L,\mathrm{III}} \left(1 - D_H^{S_L=1}\right) T_H, \text{if } S_L = 1 \\ I_L^i + f_{L,\mathrm{II}} D_H^{S_L=0} T_H + f_{L,\mathrm{I}} \left(1 - D_H^{S_L=0}\right) T_H, \text{if } S_L = 0 \end{cases} \tag{28}$$

where $f_{L,\mathrm{I}}$,$f_{L,\mathrm{II}}$,$f_{L,\mathrm{III}}$, and $f_{L.\mathrm{IV}}$ stand for the total current slope under *State IV-I*, which can be founded in Table I.

To release the zero-error tracking for the total current, the prediction value must satisfy the following equation:

$$I_L^{i+1} = I_L^* \tag{29}$$

where I_L^* is the reference value of the total current. Substituting (8), (28) into (29), the WBG phase duty cycle can be expressed as follows:

$$\begin{cases} D_H^{S_L=0} = \frac{\Delta I_L A + (L_{k1}+L_{k2})\left(V_o^i - V_{\mathrm{in}}^i\right) T_H}{L_{k1} T_H V_o^i} \\ D_H^{S_L=1} = \frac{\Delta I_L A - (L_{k1}+L_{k2}) V_{\mathrm{in}}^i T_H + L_{k1} T_H V_o^i}{L_{k1} T_H V_o^i} \end{cases} \tag{30}$$

where V_o^i and V_{in}^i are the measured output voltage and input voltage values at the time (i), respectively. And A, ΔI_L can be expressed as follows:

$$\begin{cases} A = M L_{k1} + M L_{k2} + L_{k2} L_{k1} \\ \Delta I_L = I_L^* - I_L^k. \end{cases} \tag{31}$$

Equation (31) can be directly used to calculate the WBG phase duty cycle. After evaluating the D_H according to the different Si phase switching function S_L, a PWM module is used to generate the optimal switching signals for zero-error tracking.

B. Computational Effort Comparison

The conventional Si/WBG HHB is a special case ($k = 0$) of the Si/WBG CHB design, thus comminating the (2), (30) and $k = 0$, the duty cycle for conventional Si/WBG HHB can be expressed as follows:

$$D_H^{S_L} = \frac{\Delta I_L L_2}{T_H V_o^i} - \frac{(L_1 + L_2) V_{\mathrm{in}}^i}{L_1 V_o^i} + \frac{(L_1 + (1 - S_L) L_2)}{L_1} \tag{32}$$

It can be seen that the WBG phase duty cycle for conventional Si/WBG HHB is a function of the Si phase switching function S_L. Thus, different WBG phase duty cycle under different Si phase switching function S_L is different, which is also consistent with the previous analysis in [10] and [14]. Therefore, the WBG phase duty cycle must use the feedback of the Si phase switching function S_L, which will increase the complexity of the WBG phase controller.

While in the proposed Si/WBG CHB design with optimal coupling coefficient ($k = K_{c1}$), the duty cycle under different Si phase switching functions can be simplified as follows:

$$D_H^{S_L=0} = D_H^{S_L=1} = \frac{\Delta I_L L_2 + \left(V_o^i - V_{\mathrm{in}}^i\right) T_H}{T_H V_o^i} \tag{33}$$

TABLE III
FPGA RESOURCE UTILIZATION OF THE WBG PHASE CONTROL

Resources	Proposed Si/WBG CHB	Si/WBG HHB [14]	Reduction (%)
DSP48E	5	8	37.5%
Flip Flops	1158	1882	38.5%
Slice LUTs	1784	2711	34.1%

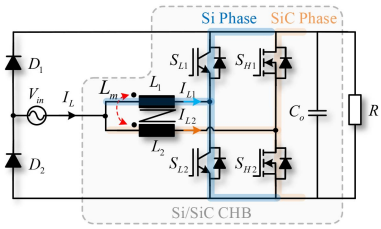

Fig. 13. Topology of the Si/SiC CHB TPBPFC.

Therefore, the WBG phase duty cycle in the proposed Si/WBG CHB design can be directly calculated using (33) without the feedback of the Si phase switching function S_L, which significantly simplifies the difficulty of the WBG phase control design.

To highlight the control simplification effect of the proposed WBG phase control loop, both control schemes are implemented using the identical field-programmable gate array (FPGA) optimization method, that is, the high-level-synthesis technique. And the FPGA resource utilization comparison is compared under the same operation latency with 31 clocks, the results are listed in Table III. Compared to the conventional Si/WBG HHB design, the WBG phase control loop in the Si/WBG CHB design can achieve a 35% average calculation resource reduction.

V. CASE STUDY AND EXPERIMENT VALIDATION

To validate the distinct advantages of the proposed Si/WBG CHB approach, a TPBPFC converter, which are widely used in OBC system [24], [25] and data-center power supply [26], is selected as an experimental case study.

A. Si/SiC CHB TPBPFC

Using the Si IGBT and SiC MOSFET, the Si/SiC CHB TPBPFC are built, and the circuit topologies are shown in Fig. 13, which consist of the Si/SiC CHB structure and a line-frequency diode phase (D_1, D_2). According to the polarity of the input voltage, different boost circuits are constructed to realize the function of power factor correction, the details operation principle has been fully discussed in the previous literature [10] and will not be repeated here.

Fig. 14 shows the control diagram of the Si/SiC CHB TPBPFC converter. The most commonly used average current mode control is adopted in the Si phase to lightly process the input current as conventional TPBPFCs. The output voltage is regulated by a PI controller to maintain the reference value, and its output is the amplitude of the reference current. The amplitude value is multiplied by the phase information of the input voltage to generate the total current reference value. Then, a PI controller

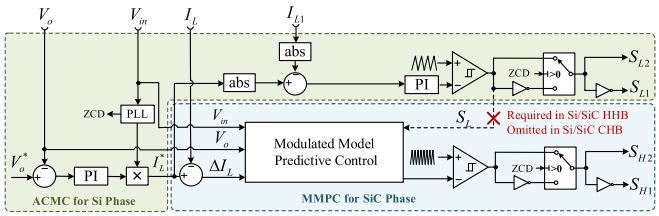

Fig. 14. Control diagram for Si/SiC CHB TPBPFC.

TABLE IV
DESIGN PARAMETERS OF THE PROPOSED CHB TPBPFC PROTOTYPE

Parameters	Value	Parameters	Value
Input	AC 220–265 V RMS	Output	DC 400 V
Power	3 kW@220 V	Capacitors	940 μH
L_{z1}	full coupled 200 μH	L_{z2}	450 μH
Frequencies	20 kHz/160 kHz		

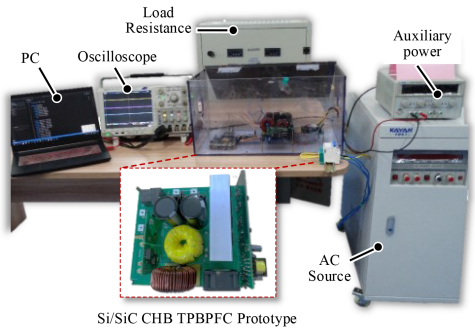

Fig. 15. Experimental test step and prototype.

is used to track the Si phase current error and generate the Si phase duty cycle. And the duty cycle of the SiC phase can be directly obtained by the MMPC controller as the description in Section IV. Finally, PWM modules are used to generate the switching singles and choose the correct sets of boost circuits according to the polarity of the input voltage. Since the control structures and basic control methods between the Si/WBG CHB design and Si/WBG HHB design are kept the same, which means that the proposed Si/WBG CHB design will not sacrifice the dynamic performance.

B. Experiment Validation

To validate the proposed Si/SiC CHB TPBPFC, a 3.3 kW laboratory prototype is designed and built. The specifications, power stage components, and other parameters of the prototype are specified in Table IV. The inductance in the proposed CHB design is selected by (24) with the $r_{L,\max} = 0.2$, and $r_{L1,\max} = 0.5$. Furthermore, the inductances are checked to satisfy (14) at full operation ranges to achieve a stable compensable range. The test step is configured as Fig. 15, which compromises the ac source, load resistance, FPGA control board, and test prototype. The Infineon SiC MOSFETS (IMW65R107M1) are used for the SiC phase and Infineon Si IGBT with an anti-parallel diode (IKW40N65H5) is for the Si phase. An FPGA (Artix-7 100T AX7102) is used as the controller.

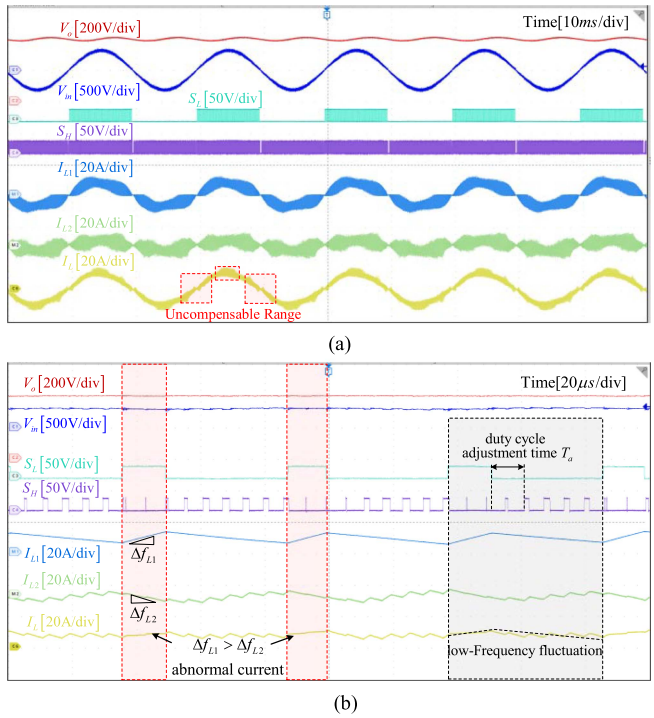

Fig. 16. Experimental waveforms of Si/SiC HHB TPBPFC with separate inductors ($k = 0$), in which the uncompensable range and low-frequency ripple seriously affect the power quality of the total current. (a) Steady-state waveform. (b) Detailed waveforms in an un-compensable range.

Fig. 16 shows the experimental waveform of the Si/SiC HHB-based TPBPFC with separate inductors, i.e., $k = 0$. The operating conditions are 220 V RMS input voltage and 400 V output voltage. It can be seen that the uncompensable issues appear near both the zero-crossing and peak range, which lead to abnormal currents in the total current, leading to abnormal currents with large harmonics. Fig. 16(b) shows the detailed waveform during the uncompensable range. Under the period of Si phase switching function $S_L = 1$, even if the SiC phase operates with the minimum duty cycle during the whole period, the SiC phase current falling slope is still less than the Si phase current rising slope and cannot achieve the full compensation for Si phase current ripple, which leads to an abnormal current overshoot in the total current. Furthermore, as shown by the gray box, the duty cycle of the SiC phase varies greatly under different S_L, and the duty cycle adjustment time T_a is longer, which leads to a certain low-frequency ripple in the total current, and further decreases the power quality of the total current.

Fig. 17 shows the steady-state experimental results of the proposed Si/SiC CHB TPBPFC prototype with 220 V RMS input voltage and 400 V output voltage. The output voltage is well regulated to the reference value, and the input current I_L follows the input voltage without phase difference, achieving a high power factor of over 0.99. The detailed waveforms are shown in Fig. 17(b). The Si phase processes most of the total current at only 20 kHz frequency, resulting in a large current ripple, shown by the yellow line. The SiC phase operates at an ultrahigh frequency up to 160 kHz to cancel the Si phase current ripple, obtaining a high power-quality total current with

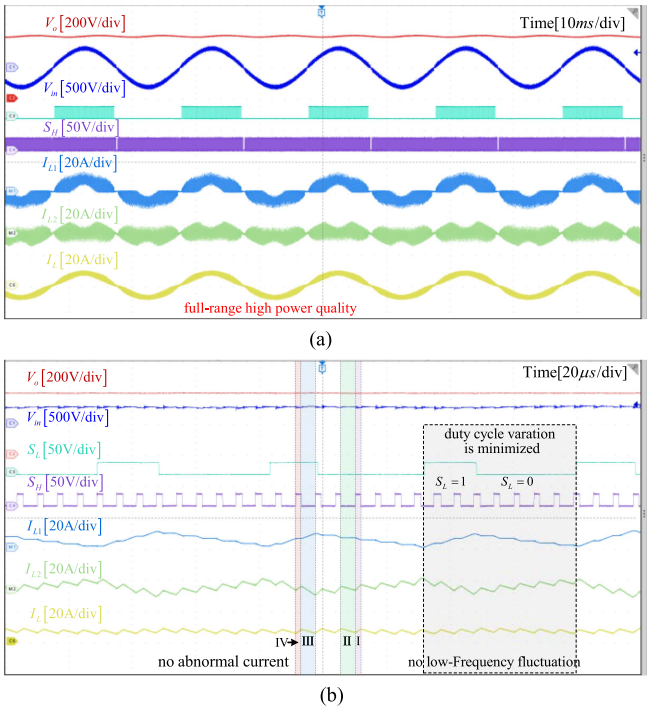

Fig. 17. Experimental waveforms of Si/SiC CHB TPBPFC with optimal coupling coefficient, in which the un-compensable range and the low-frequency ripple are addressed, the full-range high power quality is achieved. (a) Steady-state waveforms. (b) Detailed waveforms.

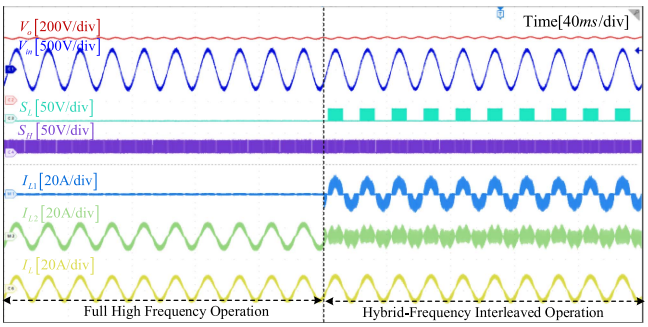

Fig. 18. Experimental waveforms comparison between full-power high-frequency operation and hybrid-frequency interleaving operation in proposed Si/SiC CHB TPBPFC prototype.

160 kHz frequency, shown by the green line. Even when S_L is fixed, the change slope of the Si phase current will still vary under different SiC phase switching functions S_H, so the uncompensable problem is avoided by such a current coupling effect. Furthermore, the duty cycle of the SiC phase remains almost the same under different Si phase switching functions S_L, which can minimize the low-frequency fluctuation caused by the control delay and duty cycle adjustment time, and further improve the power quality of the total current. Meanwhile, those experiment waveforms verify the effectiveness of the proposed MMPC control strategy.

Fig. 18 shows the experimental ripple performance comparison between the full-power high-frequency operation and hybrid frequency interleaving operation in the proposed Si/SiC CHB

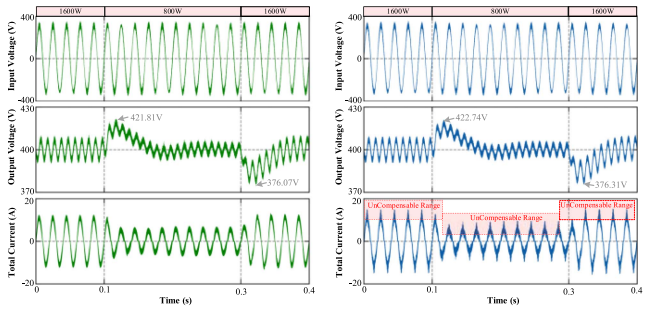

Fig. 19. Dynamic waveforms comparison between the Si/WBG CHB design and Si/WBG HHB design. (a) Proposed Si/WBG CHB Design. (b) Conventional Si/WBG HHB design.

TPBPFC prototype. In full-power high-frequency operation, the SiC phase operates at 160 kHz to process all the input current, and the Si phase is bypassed. It is observed that the power quality of input current has not significantly deteriorated after adopting the hybrid frequency interleaving operation, which fully demonstrates that the proposed Si/SiC CHB TPBPFC can achieve nearly the same performance as the full-SiC high-frequency operation by only a small-capacity SiC phase.

Fig. 19 shows the waveforms for the step changes of the output power (1600–800–1600 W), in which the proposed Si/WBG CHB design is conducted with the same control parameters (voltage loop PI parameters, Si phase loop PI parameters) as the conventional Si/WBG HHB design except for the simplification of the WBG control loop. When the load is stepped down from 1600 to 800 W, the output voltage rises to 421.81 V (CHB) and 422.74 V (HHB), respectively. When the load is stepped up from 800 to 1600 W, the output voltage is down to 376.07 V (CHB) and 376.31 V (HHB), respectively. Furthermore, it can be seen that the proposed Si/WBG CHB design shares the same transient performance as the conventional Si/WBG HHB design, which is mainly because the proposed CHB design only reduces computation burden of the WBG phase control loop and does not change control structures and basic control methods.

To demonstrate the cost-effective and power quality performance of the proposed Si/SiC CHB TPBPFC solution, comprehensive comparisons between the proposed Si/WBG CHB design, and conventional Si/WBG HHB, and two-phase all-SiC interleaved design have been carried out.

First, the detailed components and cost comparisons are summarized in Table V. The inductance L_{z2} selected the same inductance value (450 μH) as conventional Si/WBG HHB design aims to keep the same Si phase current ripple and for a convenience cost comparison. The proposed Si/SiC CHB design can achieve a 16.7% total cost reduction in comparison to the all-SiC interleaved design, exhibiting strong cost-effectiveness advantages.

Second, the efficiencies of those three prototypes are compared in Fig. 20(a). Under the light load conditions (<1500 W), those three prototypes can operate only the SiC phase to improve the light load efficiency, thus those three prototypes can obtain the same efficiency under light conditions. Under heavy load

TABLE V
DETAILED COMPONENTS AND COST COMPARISONS

	Conventional Si/SiC HHB TPBPFC	Proposed Si/SiC CHB TPBPFC	Two phase interleaved all-SiC Design
SiC Devices	IMW65R107 × 2 ($6.11 × 2)	IMW65R107 × 2 ($6.11 × 2)	IMW65R107 × 4 ($6.11 × 4)
Si Devices	IKW40N65H5 × 2 ($2.02 × 2)	IKW40N65H5 × 2 ($2.02 × 2)	\
Gate Drivers	Si: UCC27714 ($1.21 × 1) SiC: Si8261 ($1.35 × 2)	Si: UCC27714 ($1.21 × 1) SiC: Si8261 ($1.35 × 2)	Si8261 × 4 ($1.35 × 4)
Inductors	Si: 450μH / 20 A ($5.87 × 1) SiC: 200$\mu$H / 10 A ($1.52 × 1)	*Lz2*: 450 μH / 20 A ($5.87 × 1) *Lz1*: 200 μH / equivalent 20 A ($3.68× 1)	200µH / 15A × 2 ($3.06 × 2)
Total Cost	$27.56	$29.72 (**16.7%**↓)	$35.69

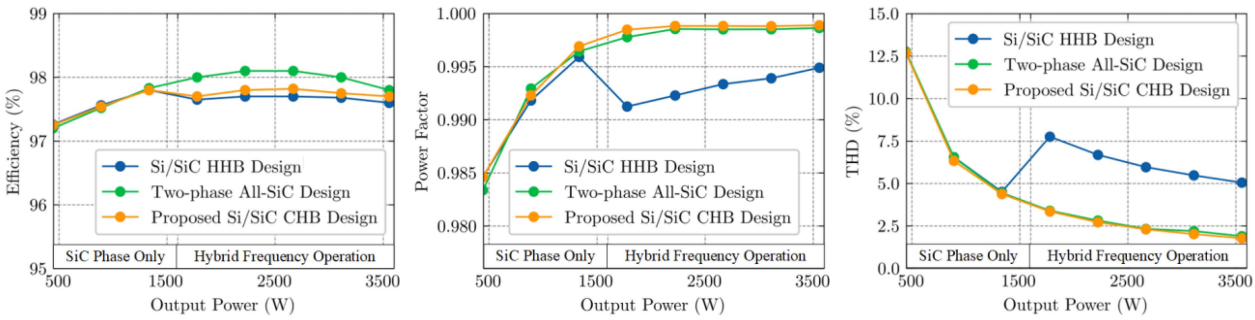

Fig. 20. Measured power quality and efficiency according to the load variation under the high line 220 V conditions. (a) Power Efficiency. (b) Power factor. (c) iTHD.

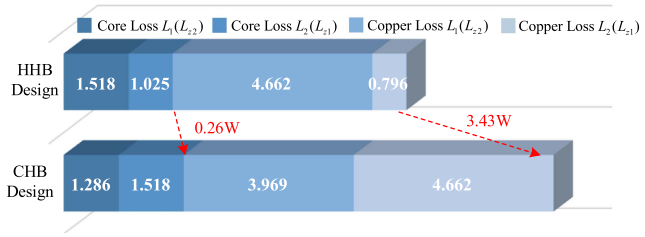

Fig. 21. Inductor loss comparison at 220 V RMS current and 3 kW rated power.

conditions, the efficiencies of both Si/SiC hybrid designs are lower (<0.3%) than the two-phase interleaved all-SiC design. While the efficiencies of the Si/SiC CHB design are slightly lower than the Si/SiC HHB design, which is mainly affected by the inductors. Fig. 21 compares the inductor loss between the conventional Si/WBG HHB design and the proposed Si/WBG CHB design at 220 V RMS current and 3 kW rated power, in which the fitness parameters in the core loss calculation process can be obtained by the datasheets and official power loss calculation tool from the core manufacturers [27]. Although a strong dc bias flux is introduced into the coupled inductor core (L_{z1}), the core loss only increases by 0.26 W benefiting from the small equivalent current ripple and smaller slope of magnetic flux value. Since L_{z1} is equivalent to processing all the input current, the copper loss is increased about 3.14 W, thus total loss for the proposed CHB is increased by about 3.43 W.

Third, the power factor and THD performance of those three prototypes are compared, shown in Fig. 20(b) and (c). The PF and THD performance are the same under light conditions since only the SiC phase is enabled. Under the heavy load conditions, in comparison to the conventional Si/SiC HHB design, the proposed Si/SiC CHB design can achieve 64.7% THD reduction with only a few efficiencies and cost penalties, which has comparable THD and PF performances to the two-phase interleaved all-SiC design across the whole load range.

In summary, the proposed Si/WBG CHB TPBPFC design offers a better cost-performance tradeoff than interleaved all-SiC design, which is suited for high power quality and cost-effectiveness applications.

VI. CONCLUSION

In this article, an Si/WBG CHB converter design was proposed, which introduces the coupled inductors to coordinate the HFIO of the Si and WBG phase, achieving significant power quality improvement and control simplification. The detailed optimal design of the coupling coefficient was presented, which not only resolves the uncompensable range and low-frequency fluctuations issues, but also simplifies the WBG phase controller design. A 3.3 kW hybrid Si/SiC CHB TPBPFC prototype is built as a case study to validate the proposed Si/WBG CHB design concept. In comparison to conventional Si/SiC HHB TPBPFC, the proposed Si/SiC CHB TPBPFC can achieve a maximum 64.7% THD reduction, demonstrating the same low ripple and THD performance as full high-frequency two-phase all-SiC design in all operating ranges while with 16.7% cost reduction.

Furthermore, the proposed Si/WBG CHB design can be applied to different kinds of converters, and applied toward a high current-carrying capacity, high power quality, and low-cost applications.

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