Potential Failure Risk of Fault Location for Modular Multilevel Converters Under Light Loads and a Current Reshaping-Based Solution

Yaqian Zhang, *Member, IEEE*, Yi Zhang, *Member, IEEE*, Jianzhong Zhang, *Senior Member, IEEE*, Fujin Deng, *Senior Member, IEEE*, and Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—In the state-of-the-art fault location of modular multilevel converters, capacitor voltage deviations between the faulty and healthy submodules are extensively utilized to identify open-circuit faults. However, there is a potential risk of overlooking the ineffectiveness of the fault location under light load conditions. This article presents an analytical model that reveals the fault phenomena and mechanisms specific to light load scenarios. A crucial finding is the strong coupling among faulty arm current, voltage deviations between faulty and healthy submodules, and load conditions. Ignoring this effect can result in underperformance of the fault location, such as seriously delayed detection or missing detection. To address this issue, a current-reshaping-based solution is proposed to ensure optimal fault location performance across the full power range. The effectiveness of the proposed analysis and method is validated through simulations and a downscale experimental platform.**

***Index Terms*—Current injection, fault location, light load condition, modular multilevel converter (MMC), open-circuit fault location.**

I. Introduction

Modular multilevel converters (MMCs) have been widely used in medium- or high-voltage applications due to their modularity, scalability, and superior ac performance [1]. For example, the MMC has attracted attention in high-voltage direct current transmission, renewable energy integration, and motor drive [2], [3], [4].

In general, the MMC consists of a large number of submodules (SMs) with massive reliability-critical components (e.g., power semiconductors, capacitors, etc.). In particular, the insulated gate bipolar transistor (IGBT) is one of the most fragile components in the MMC, with a malfunction rate of over 30% [5], [6]. The IGBT faults in the MMC are generally classified into two categories: short-circuit and open-circuit faults. The short-circuit fault is more destructive but easier to detect due to the short-circuit protection of the gate drivers [7]. By contrast, the open-circuit faults would not cause immediate damage to the SM and remain undetected for a relatively long time [8]. However, it deteriorates the output power quality and may cause subsequent damages to the whole system [9], [10], [11]. Therefore, the quick fault location and bypass of the SMs with open-circuit faults are essential for the reliable operation of the MMC.

The existing studies have made considerable efforts to locate the open-circuit fault in the MMC. The first category is based on the additional hardware, such as additional or rearranged voltage sensors [12], [13], [14], [15], and additional detection circuits embedded in each SM [16], [17]. However, these hardware-based methods cannot be directly applied to commissioned projects due to their invasive nature, and the additional hardware might increase the possibility of malfunctions.

The second category of fault location methods of the MMC is based on the existing signals, known as the software-based methods, which are preferred by the industry due to their non-invasive nature. The SM capacitor voltages are used to identify the faulty SMs, which usually show apparent voltage deviations from the healthy SMs [18], [19]. To locate the faulty SMs within a short time, a number of methods have been proposed to better capture the voltage deviations, including the model-based methods [20], [21], [22], the statistics-based methods [23], [24], and the artificial intelligence-based methods [25], [26], [27]. Especially, the conduction of the neural-network-based algorithm in [25] requires massive training data, which might be challenging for the MMC project already in commission. Moreover, the prerequisite of successfully performing these mentioned software-based methods is the presence of voltage deviations between the faulty and healthy SMs. Otherwise, the above different techniques of fault location might suffer from failure.

The underlying assumption of the aforementioned software-based methods is that the MMC usually operates under full loading conditions, which lacks a comprehensive and theoretical consideration of the wide-range load conditions, especially when the MMC operates under low power levels [3], [4]. In [28], it is observed that the capacitor voltage differences between the

Manuscript received 23 July 2023; revised 27 October 2023; accepted 7 December 2023. Date of publication 19 December 2023; date of current version 26 January 2024. The work of Yaqian Zhang, Jianzhong Zhang, and Fujin Deng was supported by the Science and Technology Projects of Jiangsu Province under Project BE2022016. Recommended for publication by Associate Editor S. Mekhilef. *(Corresponding authors: Yi Zhang; Jianzhong Zhang.)*

Yaqian Zhang, Jianzhong Zhang, and Fujin Deng are with the School of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: yqzh@seu.edu.cn; jiz@seu.edu.cn; fdeng@seu.edu.cn).

Yi Zhang and Frede Blaabjerg are with AAU Energy, Aalborg University, 9220 Aalborg, Denmark (e-mail: yiz@energy.aau.dk; fbl@et.aau.dk).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3344268.

Digital Object Identifier 10.1109/TPEL.2023.3344268

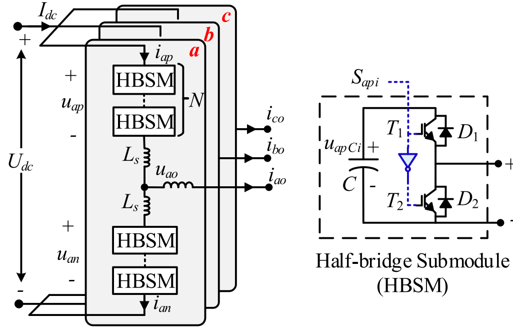


Fig. 1. Three-phase configuration of MMC and SM topology.

faulty and healthy SMs may disappear under the light loads, resulting in the underperformance of the voltage-deviations-based fault location methods. However, it is only a rough disclosure of this potential risk, lacking concise theoretical analysis and convincing experimental verifications. Liu et al. [17] employed a hardware-based solution based on the rearranged resistors and additional voltage detection circuit to quickly locate the faulty SM under light load conditions. However, the SM configuration becomes more complex and costly. Moreover, the essential mechanism is still unclear for why the capacitor voltage difference between the faulty and healthy SMs disappears under the light load conditions, making it difficult to solve this challenge from the root cause.

In this article, the potential failure risk of the fault location methods is revealed when the MMC operates under light load conditions, and the underlying mechanism is elaborated. Based on the root-cause understanding, an enhanced solution based on the current reshaping method is proposed with no additional hardware. The main contributions are threefold as follows.

1) The analytical model is established to uncover the mechanism behind the fault phenomena of arm currents and capacitor voltage when the MMC operates under light load conditions.
2) The quantitative analysis is conducted to reveal the potential risk and evaluate the fault location time under light load conditions.
3) The current-reshaping-based solution is proposed to guarantee the existing fault location methods perform well over a wide range of power conditions.

Finally, it is worth mentioning that the proposed current-reshaping-based solution does not aim to replace the existing fault location methods. Instead, it serves as a complementary tool to enhance the performance of these existing various fault location algorithms under light load conditions.

II. Open-Circuit Fault of MMC

A. Basic Operation of MMC

The configuration of the three-phase MMC is shown in Fig. 1. Each phase of the MMC consists of the upper and lower arms. Each arm is cascaded by one arm inductor L_s and N identical half-bridge (HB) SMs. Each HBSM contains one upper and lower IGBT/freewheeling diode, T_1/D_1 and T_2/D_2, and one capacitor C.

TABLE I
Healthy SM Behavior

Mode	i_{ap}	S_{api}	u_{api}	State	u_{Capi}
1	≥ 0	1	u_{Capi}	Insert	Increase
2	≥ 0	0	0	Bypass	Unchange
3	< 0	1	u_{Capi}	Insert	Decrease
4	< 0	0	0	Bypass	Unchange

TABLE II
SM Behavior Under T_1 Fault

Mode	i_{ap}	S_{api}	u_{api}	State	u_{Capi}
1	≥ 0	1	u_{Capi}	Insert	Increase
2	≥ 0	0	0	Bypass	Unchange
3	< 0	1	0	Bypass	Unchange
4	< 0	0	0	Bypass	Unchange

Table I lists the healthy SM behavior of MMC in four different modes. Taking the upper arm in phase a as an example, i_{ap} is the arm current, and each healthy SM has the output of $u_{api} = S_{api} \cdot u_{Capi}$, where S_{api} is the switching mode of the ith SM ($i = 1, 2 \ldots N$), indicating two states of the SM, namely, inserted state ($S_{api} = 1$: T_1 is ON and T_2 is OFF) and bypassed state ($S_i = 0$: T_1 is OFF and T_2 is ON), respectively. u_{api} and u_{Capi} are the output voltage and capacitor voltage of the ith SM, respectively. Under $i_{ap} \geq 0$, the capacitor voltage is increased under the insert state and unchanged under the bypass state. Under $i_{ap} < 0$, the capacitor voltage is decreased under the insert state and unchanged under the bypass state.

The arm voltage and current in phase a are expressed as

$$\begin{cases} u_{ap/n} = \dfrac{U_{dc}}{2} \mp U_m \sin(\omega t) \\ i_{ap/n} = \dfrac{I_{dc}}{3} \pm \dfrac{I_m}{2} \sin(\omega t + \varphi) \end{cases} \quad (1)$$

where $u_{ap/n}$ and $i_{ap/n}$ are the arm voltage and current, respectively. The subscriptions p and n denote the upper and the lower arms. I_{dc} and U_{dc} are the dc current and voltage of the MMC, respectively. U_m and I_m are the amplitude of the ac voltage and current, respectively. ω is the angular frequency. φ is the power angle of the MMC. Usually, the arm currents only contain the dc component and fundamental ac component, where the harmonic components are suppressed to zero in order to decrease the power losses of the MMC.

B. SM Behaviour Under Open-Circuit Fault

Table II gives the SM behavior under T_1 open-circuit fault, where Mode 3 failed to perform. Under $i_{ap} < 0$, the arm current cannot pass T_1 and can only flow through the freewheeling diode D_2, as shown in Fig. 2(a). As a result, the faulty SM cannot output positive voltage $+U_C$ under $i_{ap} < 0$, leading to arm voltage level lack. Besides, the capacitor of the faulty SM cannot be discharged under $i_{ap} < 0$, causing abnormal voltage increase, which becomes the basis to perform the existing fault location methods [23], [25], [26], [27].

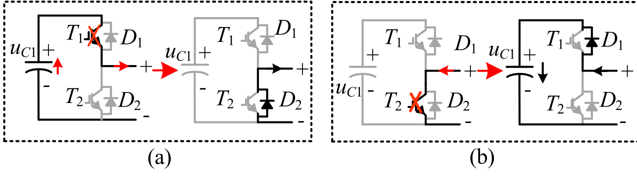


Fig. 2. SM behavior under open-circuit fault. (a) T_1 fault under $i_{ap} < 0$: From insert state to bypass state. (b) T_2 fault under $i_{ap} \geq 0$: From bypass state to insert state.

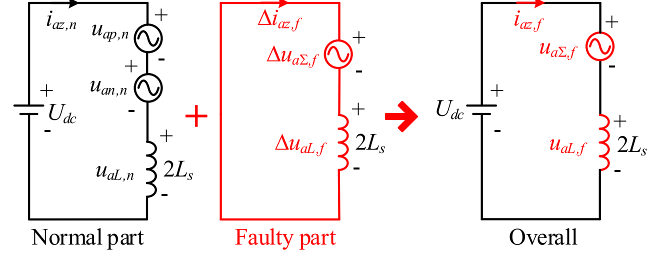


Fig. 3. Equivalent circuit of DC side under open-circuit fault.

TABLE III
SM BEHAVIOR UNDER T_2 FAULT

Mode	i_{ap}	S_{api}	u_{api}	State	u_{Capi}
1	≥ 0	1	u_{Capi}	Insert	Increase
2	≥ 0	0	u_{Capi}	Insert	Increase
3	< 0	1	u_{Capi}	Insert	Decrease
4	< 0	0	0	Bypass	Unchange

Table III gives the SM behavior under T_2 open-circuit fault, where Mode 2 failed to perform. The SM cannot be bypassed (output zero voltage) by T_2 under $i_{ap} > 0$, and the arm current flows via the freewheeling diode D_1 to continuously charge the capacitor voltage, as shown in Fig. 2(b). Consequently, the arm voltage suffers from the wrong output, and the faulty SM suffers from abnormal capacitor voltage increase compared with the healthy SMs, which is the prerequisite of the well-performed fault location.

The above open-circuit fault phenomenon is widely accepted to be adaptable for full load conditions of MMC, where the capacitor voltage of the faulty SM is featured by an obvious increase compared with the healthy SMs, and the fault location could be well performed [23], [25], [26], [27]. However, the influence of the power level on fault phenomena is not fully considered or analytically revealed, which leads to potential risks of fault location failure under light load conditions. This research gap will be made up in the later sections of this article.

III. Analysis of Fault Characteristics for MMCs Under Light Load Conditions

This section reveals and explains the fault characteristics of the MMCs under light loads, where the faulty arm current will become unipolar and the capacitor voltage deviations between the faulty and healthy SMs will disappear, which causes the underperformance risk of the existing fault location methods.

A. Equivalent Circuit on DC Side Under Open-Circuit Fault

Taking phase a as the example, Fig. 3 illustrates the equivalent circuit on dc side after the open-circuit fault occurs within the upper arm. According to (1), under normal operations without any open-circuit fault, the voltage variables satisfy the following relations:

$$\begin{cases} U_{\mathrm{dc}} = u_{a\Sigma,n} = u_{ap,n} + u_{an,n} \\ u_{a\Sigma,n} = NU_C, u_{aL,n} = 0 \end{cases} \tag{2}$$

where the subscript n behind the comma indicates the variables under normal operations. $u_{aL,n}$ is the voltage drop on the two arm inductors, and $u_{a\Sigma,n}$ is the overall voltage output of the SMs in both the upper and lower arms. U_C is the nominal voltage of the SM capacitor.

The open-circuit faults, i.e., T_1 or T_2 fault, will introduce faulty components, as shown in Fig. 3, which are

$$\begin{cases} U_{dc} = u_{aL,f} + u_{a\Sigma,f} \\ u_{a\Sigma,f} = u_{ap,f} + u_{an,f} \\ u_{aL,f} = -\Delta u_{a\Sigma,f} = U_{dc} - u_{a\Sigma,f} \end{cases} \tag{3}$$

where the subscript f indicates the variables under open-circuit faults. $\Delta u_{a\Sigma,f}$ is the voltage difference between the overall SM voltage output and U_{dc}. $u_{aL,f}$ is the faulty voltage imposed on the two arm inductors, which will generate the faulty component of the circulating current, $\Delta i_{az,f}$. It is expressed as

$$\Delta i_{az,f} = \int \frac{\Delta u_{aL,f}}{2L_s} dt = -\int \frac{\Delta u_{a\Sigma,f}}{2L_s} dt. \tag{4}$$

This will be superimposed on both the upper and lower arm currents, having

$$\begin{cases} i_{ap,f} = i_{ap,n} + \Delta i_{az,f} \\ i_{an,f} = i_{an,n} + \Delta i_{az,f}. \end{cases} \tag{5}$$

To figure out the influence of the T_1 or T_2 open-circuit faults on the arm current, it is crucial to investigate the variation of $\Delta i_{az,f}$ under different conditions.

B. Analysis of Nonnegative Faulty Arm Current Under T_1 Open-Circuit Fault

Under T_1 fault, the faulty SMs cannot output $+U_C$ under negative arm currents, i.e., $i_{ap} < 0$. In addition, the capacitor voltage variations of the healthy SMs in both upper and lower arms will be affected by distorted arm currents. As a result, the faulty component of overall voltage output in phase a, $\Delta u_{a\Sigma,f1}$ is mainly composed of two parts, which is

$$\Delta u_{a\Sigma,f1} = -N_{f1}U_C + \Delta u_{Ca\Sigma,f1} \tag{6}$$

where the subscript $_{f1}$ indicates the variables under T_1 faults. The first term on the right-hand side of (6) is caused by the wrong voltage output of faulty SMs under $i_{ap} < 0$, where N_{f1} is the number of SMs with T_1 open-circuit fault. The second term $\Delta u_{Ca\Sigma,f1}$ is the summarized voltage increment of the healthy SM capacitors in phase a, which is increased along with time.

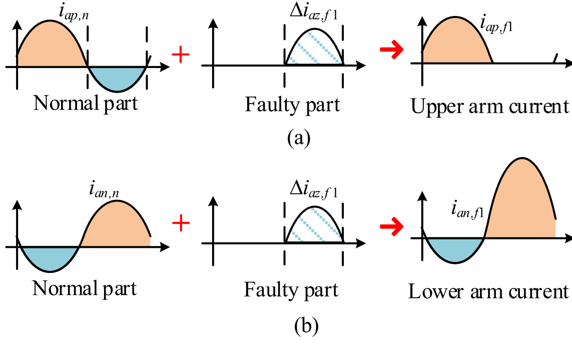


Fig. 4. Arm current with T_1 fault in upper arm. (a) Upper arm current becomes nonnegative. (b) Lower arm current has enlarged positive part.

Combining (3), (4), and (6), $\Delta i_{az,f1}$ is derived as

$$\Delta i_{az,f1} = \int \frac{N_{f1} U_C - \Delta u_{Ca\Sigma,f1}}{2L_s} dt \tag{7}$$

which illustrates that the faulty component of the circulating current is positive under $i_{ap} < 0$, as shown in Fig. 4. Based on the superposition principle, as shown in Fig. 4(a), the negative part of the upper arm current $i_{ap,n}$ might be completely suppressed by $\Delta i_{az,f1}$, when the following condition is satisfied:

$$\begin{cases} \Delta I_{az,f1} \geq I_{\text{neg}} \\ I_{\text{neg}} = -\frac{I_{\text{dc}}}{3} + \frac{I_m}{2} \end{cases} \tag{8}$$

where $\Delta I_{az,f1}$ is the peak value of $\Delta i_{az,f1}$, and I_{neg} is the negative peak value of the arm current under normal operations. At the same time, the positive part of the lower arm current is extended by the superposition of $\Delta i_{az,f1}$, as shown in Fig. 4(b). As a result, with the increasing cycles after the fault occurrence, the capacitor voltage of all the SMs in the upper and lower arms will be increased.

Fig. 5 shows the capacitor voltage variations when the faulty arm current is nonnegative in continuous N_{cyc1} fundamental cycles after the T_1 fault occurrence. All the SMs in the upper arm cannot be discharged due to $i_{ap,f1} \geq 0$, and all the SMs in the lower arm are overcharged with the enlarged positive part. The capacitor voltage in N_{cyc}th cycle ($N_{\text{cyc}} \leq N_{\text{cyc1}}$) can be expressed as

$$\begin{cases} u_{Cap,f1} = U_C + \lambda \cdot \Delta U_C \cdot N_{\text{cyc}} \\ u_{Cap,h1} = U_C + \lambda \cdot \Delta U_C \cdot N_{\text{cyc}} \\ u_{Can,h1} = U_C + \lambda \cdot \Delta U_C \cdot N_{\text{cyc}} \end{cases} \tag{9}$$

where $u_{Cap,f1}$ is the capacitor voltage of the faulty SMs in upper arm. $u_{Cap,h1}$ and $u_{Can,h1}$ are the capacitor voltage of the healthy SMs in the upper and lower arms, respectively. ΔU_C is the nominal voltage ripple range, i.e., 10% U_C. λ is the coefficient of the voltage ripple and proportional to the power levels, i.e., $\lambda = 1$ under $P = 1$, and $\lambda = 0.5$ under $P = 0.5$.

Under the unity power factor, the overall voltage on dc side in phase a is almost all supported by the upper arm under $i_{ap} < 0$. Combining with (9), $\Delta u_{Ca\Sigma,f1}$ in (6) can be expressed by

$$\Delta u_{Ca\Sigma,f1} = (N-1)\,\Delta u_{Cap,h1} = (N-1)\,\lambda \cdot \Delta U_C \cdot N_{\text{cyc}}. \tag{10}$$

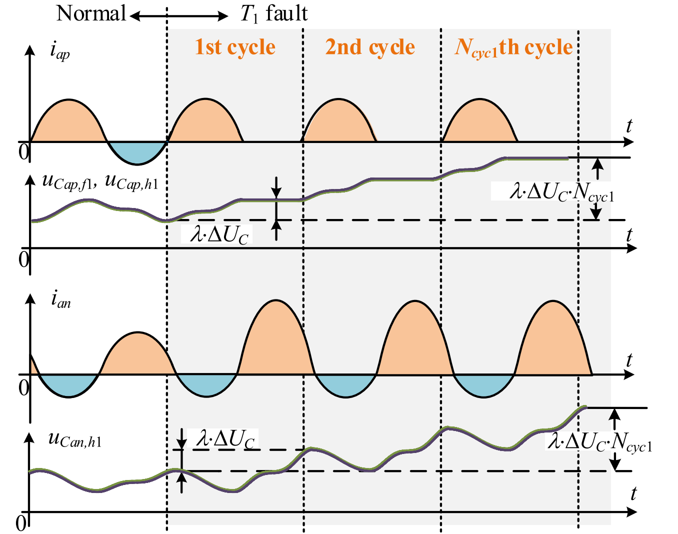


Fig. 5. Fault phenomena under nonnegative faulty arm current when T_1 fault occurs in upper arm. N_{cyc1} represents the number of fundamental cycles with nonnegative faulty arm current under T_1 fault. $u_{Cap,f1}$ and $u_{Cap,h1}$ are the capacitor voltage of faulty SMs and healthy SMs in upper arm, respectively. Because of nonnegative faulty arm current i_{ap}, all the SMs in upper arm can only be charged, and then, $u_{Cap,f1}$ is the same as $u_{Cap,h1}$, leading to difficulty in fault location. (*From top to bottom:* Upper arm current with nonnegative value, capacitor voltage of upper arm, lower arm current with enlarged positive part, and capacitor voltage of upper arm.)

Combining (3), (4), (7), and (10), the faulty component of the arm current $\Delta i_{az,f1}$ and its peak value $\Delta i_{az,f1}$ are, respectively, expressed as

$$\begin{cases} \Delta i_{az,f1} = \int \frac{N_{f1} U_C - (N-1)\lambda \cdot \Delta U_C \cdot N_{\text{cyc}}}{2L_s} dt \\ \Delta I_{az,f1} = \frac{N_{f1} U_C - (N-1)\lambda \cdot \Delta U_C \cdot N_{\text{cyc}}}{2L_s} \cdot \frac{\Delta T_{\text{neg}}}{2} \end{cases} \tag{11}$$

where ΔT_{neg} is the time interval of the negative arm current under normal operations. It shows that the increase of N_{cyc} will reduce the value of $\Delta I_{az,f1}$. Combining (8) and (11), N_{cyc1}, namely, the maximum value of N_{cyc} that is possessed with the unipolar faulty arm current, can be acquired as

$$N_{\text{cyc1}} = \frac{N_{f1} U_C T_0 - 6 I_m L_s}{(N-1)\,\lambda \cdot \Delta U_C \cdot T_0} \tag{12}$$

which has: 1) $N_{\text{cyc}} \leq N_{\text{cyc1}}$—the faulty arm current is distorted to be nonnegative, having $i_{ap,f1} \geq 0$ in each cycle, and 2) $N_{\text{cyc}} > N_{\text{cyc1}}$—the faulty arm current becomes bipolar, having both $i_{ap,f1} \geq 0$ and $i_{ap,f1} < 0$ in each cycle. Within the first N_{cyc1} cycles, the healthy and faulty SMs have identical voltage variations, increasing the difficulty of identifying the faulty SMs. In other words, the existing fault location methods can only be well performed until $t > T_0 \cdot N_{\text{cyc1}}$, where T_0 is the period of one fundamental cycle. t represents the time delay from the moment of fault occurrence.

The analytical and simulated results of N_{cyc1} are compared in Fig. 6 based on the parameters in Table IV. The discrete dots represent the simulated results, which show a high consistency with the theoretical results under different numbers of faulty

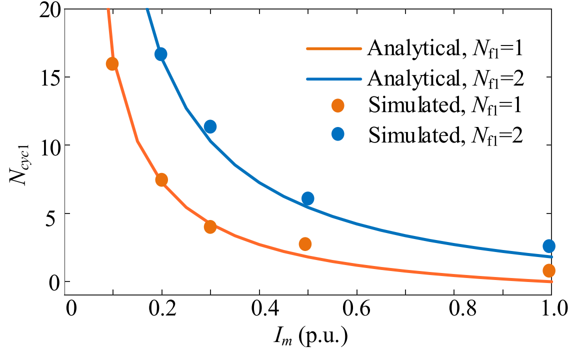


Fig. 6. Comparison of analytical and simulated results of N_{cyc1}.

TABLE IV
SIMULATION PARAMETERS

Parameters and symbols	Values and units
Rated power P	7.2 MW
DC voltage U_{dc}	24 kV
AC voltage U_m	10 kV
Number of SMs N	12
SM capacitance C	3.2 mF
Rated SM voltage U_C	2 kV
Arm inductance L_s	8 mH

SMs, i.e., $N_{f1} = 1$ and $N_{f1} = 2$. It shows that the fault location time of MMC suffers from an intensive increase with the decrease of load levels.

C. Analysis of Nonpositive Faulty Arm Current Under T_2 Open-Circuit Fault

Under T_2 fault, the faulty SMs cannot be bypassed under positive arm current, i.e., $i_{ap} > 0$, causing the actual output voltage of the upper arm higher than the reference. This will distort the arm currents, then the capacitor voltage variations of the healthy SMs in both upper and lower arms will also be affected consequently. In this case, the faulty component of overall voltage output on dc side, $\Delta u_{a\Sigma,f2}$ is mainly composed of two parts, which is

$$\Delta u_{a\Sigma,f2} = N_{f2} \cdot u_{C,f2} + \Delta u_{Ca\Sigma,f2}. \tag{13}$$

where the subscript $_{f2}$ indicates the variables under T_2 open-circuit faults. The first term on the right-hand side of (13) is caused by the wrong output of the faulty SMs under $i_{ap} > 0$, where N_f2 is the number of SMs with T_2 open-circuit fault. The second term, $\Delta u_{Ca\Sigma,f2}$ in (13) is the summarized voltage decrease of the healthy SM capacitors under T_2 faults, which becomes more prominent with time increasing.

Combining (3), (4), and (13), $\Delta i_{az,f2}$ is expressed as

$$\Delta i_{az,f2} = \int \frac{-N_{f2}U_C + \Delta u_{Ca\Sigma,f2}}{2L_s} dt \tag{14}$$

which means the faulty component of the circulating current is negative under $i_{ap} > 0$, as shown in Fig. 7. According to the superposition principle, the positive part of the upper arm current might be completely suppressed by $\Delta i_{az,f2}$, as shown

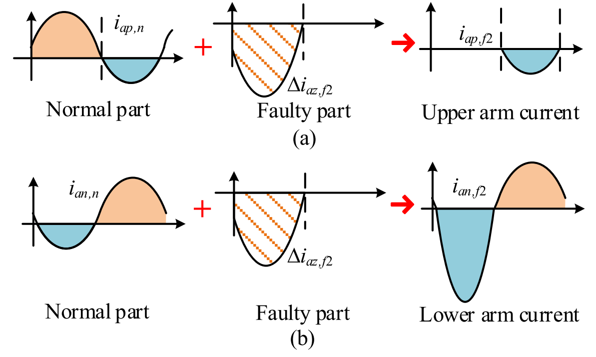


Fig. 7. Arm current with T_2 fault in upper arm. (a) Upper arm current becomes nonpositive. (b) Lower arm current has enlarged negative part.

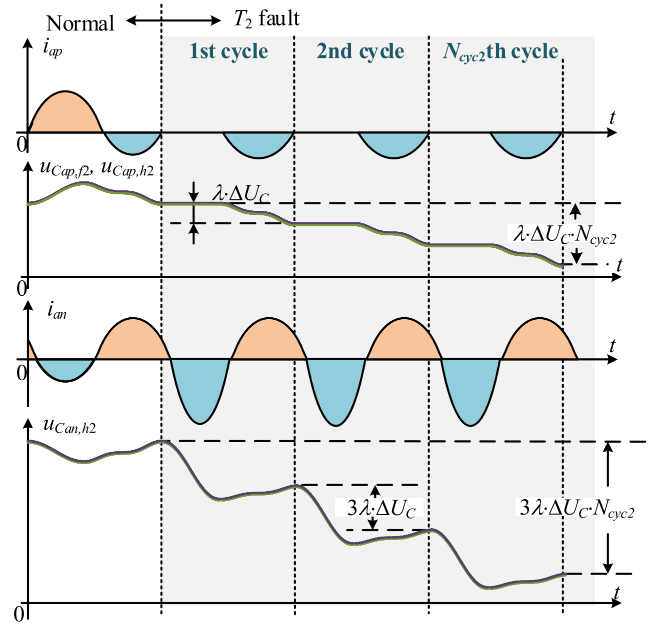


Fig. 8. Fault phenomena under nonpositive faulty arm current when T_2 fault occurs in upper arm. N_{cyc2} represents the number of fundamental cycles with nonpositive faulty arm current under T_2 fault. $u_{Cap,f2}$ and $u_{Cap,h2}$ are the capacitor voltage of faulty SM and healthy SMs in upper arm, respectively. Because of the nonpositive faulty arm current i_{ap}, all the SMs in upper arm can only be discharged, and then, $u_{Cap,f2}$ is the same as $u_{Cap,h2}$, leading to difficulty in fault location. (*From top to bottom:* Upper arm current with nonpositive value, capacitor voltage of upper arm, lower arm current with enlarged negative part, and capacitor voltage of upper arm.)

in Fig. 7(a), when the following relation is fulfilled:

$$\begin{cases} \Delta I_{az,f2} \geq I_{\mathrm{pos}} \\ I_{\mathrm{pos}} = \frac{I_{\mathrm{dc}}}{3} + \frac{I_m}{2} \end{cases} \tag{15}$$

where $\Delta I_{az,f2}$ is the negative peak value of $\Delta i_{az,f2}$, and I_{pos} is the positive peak value of the arm current under normal operations. Meanwhile, the negative part of the lower arm current is extended, as shown in Fig. 7(b). As a result, the capacitor voltage of all the SMs in the upper and lower arms will be decreased from the nominal value.

Fig. 8 shows the capacitor voltage variations when the faulty arm current is nonpositive in continuous N_{cyc2} fundamental cycles after the T_2 fault occurrence. All the SMs in the upper arm cannot be charged due to $i_{ap,f2} \leq 0$, and all the SMs in the lower arm are overdischarged by the enlarged negative part. The capacitor voltage in N_{cyc}th cycle ($N_{\text{cyc}} \leq N_{\text{cyc2}}$) are expressed as

$$\begin{cases} u_{Cap,f2} = U_C - \lambda \cdot \Delta U_C \cdot N_{\text{cyc}} \\ u_{Cap,h2} = U_C - \lambda \cdot \Delta U_C \cdot N_{\text{cyc}} \\ u_{Can,h2} = U_C - 3\lambda \cdot \Delta U_C \cdot N_{\text{cyc}} \end{cases} \tag{16}$$

where $u_{Cap,f2}$ is the capacitor voltage of the faulty SMs in upper arm. $u_{Cap,h2}$ and $u_{Can,h2}$ are the capacitor voltage of the healthy SMs in the upper and lower arms, respectively.

Since the overall output voltage on the dc side is almost all supported by the lower arm under $i_{ap} > 0$, $\Delta u_{Ca\Sigma,f2}$ in (12) can be expressed as

$$\Delta u_{Ca\Sigma,f2} = -3N \cdot \Delta u_{Can,h2} = -3N \cdot \lambda \cdot \Delta U_C \cdot N_{\text{cyc}}. \tag{17}$$

Combining (3), (4), (13), and (17), the faulty component of the arm current $\Delta i_{az,f2}$ and its peak value $\Delta i_{az,f2}$ are, respectively, expressed as

$$\begin{cases} \Delta i_{az,f2} = -\int \frac{N_{f2} \cdot u_{Cap,f2} - 3N\lambda \cdot \Delta U_C \cdot N_{\text{cyc}}}{2L_s} dt \\ \Delta I_{az,f2} = \frac{N_{f2} \cdot u_{Cap,f2} - 3N\lambda \cdot \Delta U_C \cdot N_{\text{cyc}}}{2L_s} \cdot \frac{\Delta T_{\text{pos}}}{2} \end{cases} \tag{18}$$

where ΔT_{pos} is the time interval of the positive arm current under normal operations. It denotes that the increase of N_{cyc} will suppress the value of $\Delta I_{az,f2}$. Combining (15) and (18), N_{cyc2}, namely, the maximum value of N_{cyc} having the nonpositive faulty arm current under T_2 fault, is derived as

$$N_{\text{cyc2}} = \frac{N_{f2} U_C T_0 - 9 I_m L_s}{(3\,N + N_f)\,\lambda \cdot \Delta U_C \cdot T_0} \tag{19}$$

which has: 1) $N_{\text{cyc}} \leq N_{\text{cyc2}}$—the faulty arm current is distorted to be nonpositive, having $i_{ap,f2} \leq 0$ in each cycle, and 2) $N_{\text{cyc}} > N_{\text{cyc2}}$—the faulty arm current becomes bipolar, having both $i_{ap,f2} \leq 0$ and $i_{ap,f2} > 0$ in each cycle. Within N_{cyc2} cycles after the fault occurs, the healthy and faulty SMs have identical voltage decreases, increasing the difficulty of identifying the faulty SMs. In other words, the fault location methods of SMs with the T_2 open-circuit fault can only be well performed until $t > T_0 \cdot N_{\text{cyc2}}$.

The analytical and simulated results of N_{cyc2} are compared in Fig. 9, which roughly agree with each other under both $N_{f2} = 1$ and $N_{f2} = 2$. Similar to the T_1 fault in Fig. 6, the light loads lead to a higher number of cycles without capacitor voltage deviations of the faulty and healthy SMs. It shows that the value of N_{cyc2} is zero under the load range of 0.5–1.0 per unit (p.u.), which means the fault location can perform well. However, the value of N_{cyc2} reaches three when the load level is 0.1 p.u. Note that the value of N_{cyc2} is smaller than N_{cyc1} under the same load condition, meaning that the potential risk of fault location underperformance of T_1 is higher than T_2 under the same power levels.

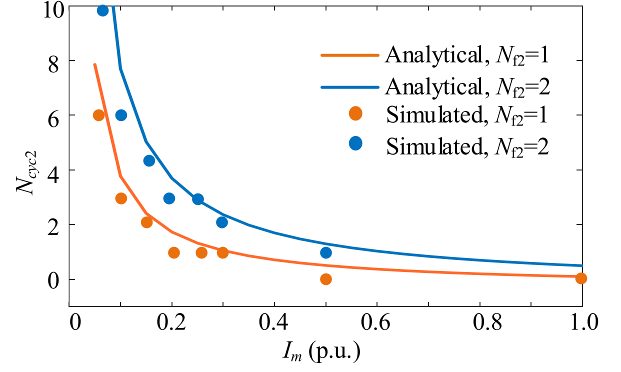


Fig. 9. Comparison of analytical and simulated results of N_{cyc2}.

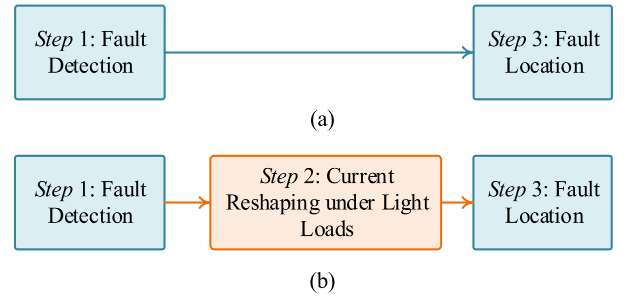


Fig. 10. Overall flowchart of fault location under light load conditions based on (a) traditional approaches and (b) proposed approach.

IV. Proposed Current-Reshaping-Based Solution of Fault Location Under Light Load Conditions

In general, the fault location is conducted by a hierarchical process, including the fault detection of faulty arms and the fault location of faulty SMs. In this article, to solve the potential risk of fault location failure under light load conditions, another step of current-reshaping-based control is inserted before the fault location of faulty SMs so that the fault location time under light load conditions can be reduced to the same level as the rated power level.

A. *Proposed Current-Reshaping-Based Solution*

Based on the above analysis, the root cause of the voltage deviation disappearance between the faulty and healthy SMs lies in the unipolarity of the faulty arm current under light loads. This unipolarity might last for several continuous fundamental cycles when the T_1 or T_2 open-circuit fault of the MMC occurs under light load conditions. Therefore, the key point to distinguish faulty SMs from healthy ones is to reshape the bipolar arm current under light loads, i.e., to produce the negative part of arm current for T_1 fault and produce the positive part of arm current for T_2 fault.

Fig. 10 presents the main difference between the traditional two-step fault location methods and the proposed three-step fault locations. As shown in Fig. 10(b), a current-reshaping-based solution is proposed based on the second-order circulating current injection, which can rebuild the faulty arm current to be bipolar

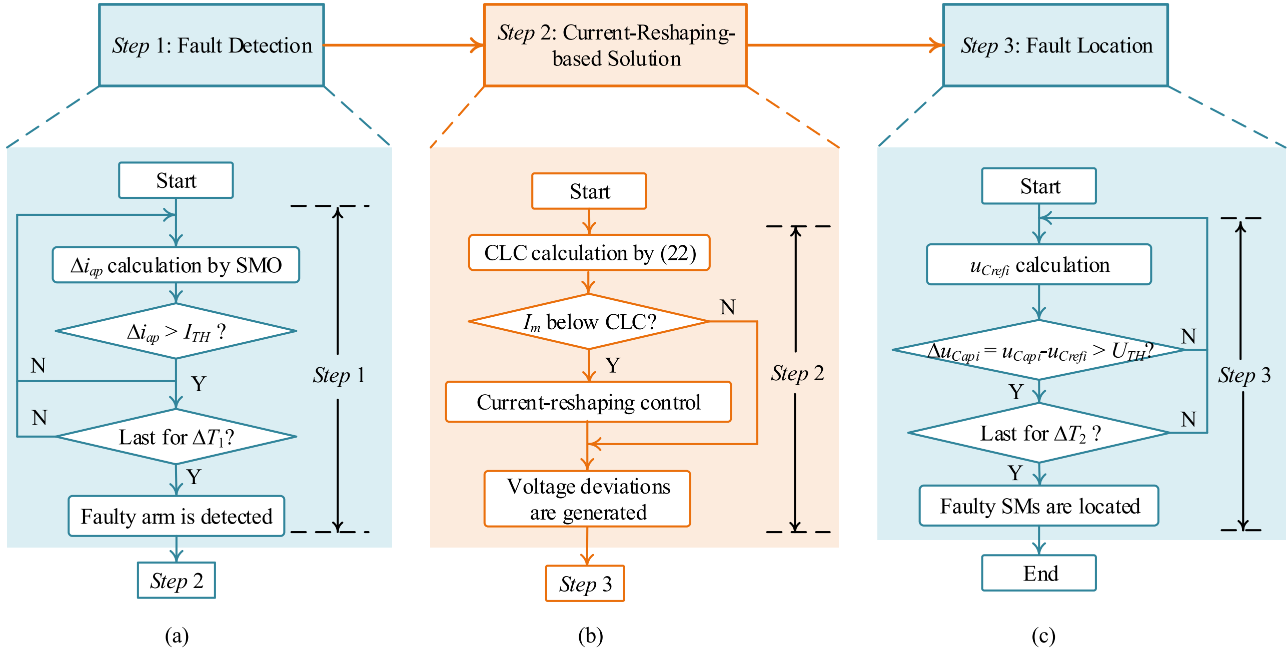


Fig. 11. Overall diagram for proposed fault location approach of MMC. (a) Fault detection. (b) Proposed current-reshaping-based control. (c) Fault location. CLC is critical load condition of MMC.

under the light loads. Then, the capacitor voltage deviations are generated between the healthy and faulty SMs, which provide the essential prerequisite for the existing voltage-deviations-based fault location techniques.

Fig. 11 shows the conduction of each step for the proposed current-reshaping-based solution.

1) Step 1: The fault diagnosis is performed to detect and confirm the faulty arm according to the distortion of circulating and ac currents under open-circuit faults. In this article, the sliding-mode-observer-based method is adopted in *Step 1*, as shown in Fig. 11(a). Δi_{ap} refers to the current error between the estimated and actual values of the upper arm current. I_{TH} is the preset threshold of current error. When the current error exceeding the threshold last for the time duration ΔT_1, the observed arm is confirmed to be faulty. More technical details of the fault detection methods can be found in [20] and [29]. Meanwhile, in these mentioned methods, the type of fault can be identified, i.e., T_1 or T_2 open-circuit faults, and the number of faulty SMs can also be calculated, i.e., N_{f1} and N_{f2}.

2) Step 2: The circulating current injection is only enabled on the following two prerequisites: 1) the open-circuit fault is confirmed to happen in *Step 1*, so the normal operation of the MMC is not affected by the circulating current injection, and 2) the power level of MMC is below the critical load conditions (CLC). As shown in Fig. 11(b), the CLC is used to identify the light load condition of the MMC and to trigger the proposed current-reshaping solution. More specifically, the CLC has the following features.

1) *Below CLC:* The faulty arm current might lose the bipolar features, and the capacitor voltage deviations between the faulty and healthy SMs are disappearing. It means the MMC operates under light load conditions and suffers from high risk of fault location underperformance.
2) *Above CLC:* The faulty arm current is bipolar, and the existing fault location methods perform well based on the capacitor voltage deviations between the faulty and healthy SMs.

The principle to select the CLCs of MMC will be discussed in detail in the following analysis.

When the circulating current injection is enabled in *Step 2*, the injected circulating current $i_{2\mathrm{nd},x}$ is expressed as

$$\begin{cases} i_{2\mathrm{nd},x} = I_{2\mathrm{nd}} \sin\left(2\omega t + \varphi_{2\mathrm{nd},x}\right) \\ \varphi_{2\mathrm{nd},x} = \varphi_x \end{cases} \tag{20}$$

where $I_{2\mathrm{nd}}$ and $\varphi_{2\mathrm{nd},x}$ are the amplitude and phase of the second-order circulating current, respectively ($x = a, b, c$). The determination of $\varphi_{2\mathrm{nd},x}$ can realize the bipolar arm currents regardless of the fault type. φ_x is the ac current phase of phase x. To ensure the safe range of arm current and the maximum current injection simultaneously, the amplitude of the injected circulating current is decided by

$$I_{2\mathrm{nd}} = \max\left(\; I_{\mathrm{pos}0} - I_{\mathrm{pos}}, \quad I_{\mathrm{neg}0} - I_{\mathrm{neg}} \;\right) \tag{21}$$

where $I_{\mathrm{neg}0}$ and $I_{\mathrm{pos}0}$ are the negative and positive peak values of the arm current under full load, respectively.

With the circulating current injection, the faulty arm current becomes bipolar under the light load conditions, where the negative or positive part is compensated for the T_1 or T_2 fault, respectively. Then, the voltage deviations between the faulty and healthy SMs will be quickly generated after the circulating current injection is triggered.

3) Step 3: The fault location is conducted after the circulating current injection. Here, the existing software-based fault location methods can be directly applied to identify the faulty SMs based on the generated capacitor voltage deviations. In this article, the method in [18] is adapted, as shown in Fig. 11(c).

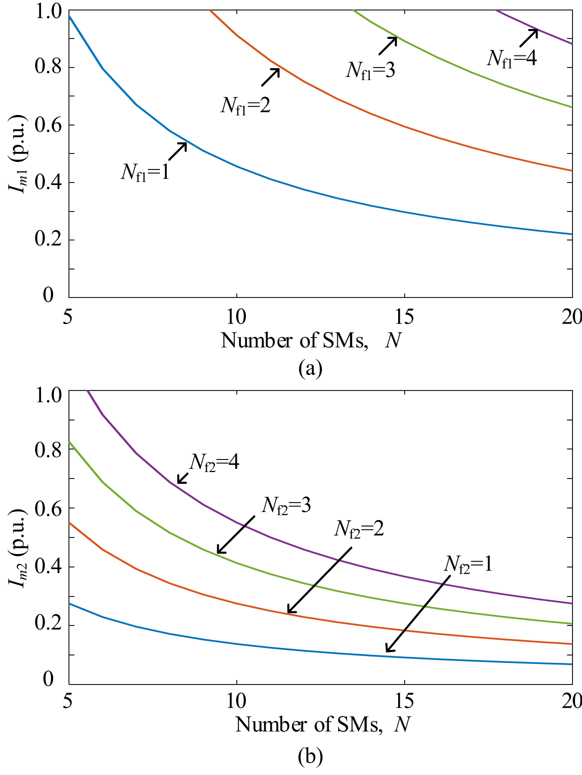


Fig. 12. CLC of (a) T_1 and (b) T_2 open-circuit faults. N_{f1} and N_{f2} refer to the number of faulty SMs with T_1 and T_2 fault, respectively. Higher values of CLC indicate higher risk of fault location failure.

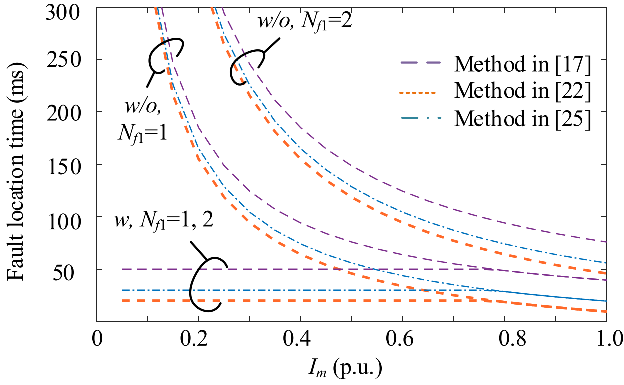


Fig. 13. Fault location time of existing methods with and without proposed solution. (w/o: Without proposed approach. w: With proposed solution.)

u_{Capi} is the capacitor voltage of the ith SM. $u_{\text{ref}i}$ is the reference voltage of the ith SM, which is valued as the average voltage of the other SMs in the same arm. Δu_{Capi} is the voltage deviations between the detected ith SM and reference voltage. The ith SM would be confirmed to be faulty when $\Delta u_{Capi} > U_{\text{TH}}$ can last for a duration of ΔT, where U_{TH} is the preset threshold of the voltage deviation.

B. Discussion on CLCs of MMC

The CLC in Fig. 11 is used to identify the light load condition of the MMC and to trigger the current-reshaping solution. According to (12) and (19), the CLCs of T_1 and T_2 faults can be decided by setting an appropriate threshold of N_{cyc1} and N_{cyc2}. To make sure that the fault location time will not be increased too much before triggering the current injection, the threshold value of N_{cyc1} and N_{cyc2} is selected as three in this article, which is $N_{\text{cyc1}} = 3$ or $N_{\text{cyc2}} = 3$. Then, according to (12) and (19), the CLCs of two types of faults are, respectively, derived as

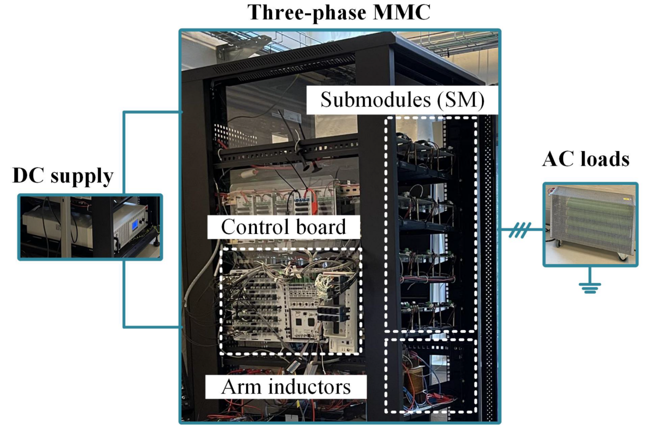


Fig. 14. Three-phase MMC setup. Each phase has two symmetric arms, and each arm is cascaded by four identical HBSMs and one arm inductor. The system control is realized by DSP plus FPGA (DSP: digital signal processor; FPGA: field programmable gate arrays).

$$\begin{cases} I_{m1} = \dfrac{N_{f1} U_C T_0 - 3\,(N-1)\,\lambda \cdot \Delta U_C \cdot T_0}{6L_s} \\ I_{m2} = \dfrac{N_{f2} U_C T_0 - 3\,(3\,N + N_f)\,\lambda \cdot \Delta U_C \cdot T_0}{9L_s} \end{cases} \tag{22}$$

where I_{m1} and I_{m2} indicate the CLCs under T_1 and T_2 faults, respectively. The derived CLCs can be used to identify the light load conditions of T_1 and T_2 fault in Fig. 11.

The CLCs of the MMC in (22) are affected by various factors, i.e., the fault type, the number of SMs, and the number of faulty SMs. Fig. 12 demonstrates the CLCs of the T_1 and T_2 faults under different conditions. All the cases are carried out based on the parameters listed in Table IV. A higher value of the CLC curve means a higher potential underperformance risk of the software-based fault location methods.

Based on the comparisons in Fig. 12, the following conclusions can be drawn. First, the CLC of T_1 fault is multiple times higher than that of T_2 fault, which means the failure of the fault location is more likely to occur with T_1 fault. Second, the CLC curves for T_1 and T_2 faults both become higher when the total number of SMs in each arm is smaller. This implies that the potential risk of fault location failure is higher for the MMC with a few numbers of SMs, e.g., motor drive applications. Third, the CLC is increased with the rising number of faulty SMs. Multiple SM faults happening at the same time are more likely to cause underperformance of the existing fault location methods.

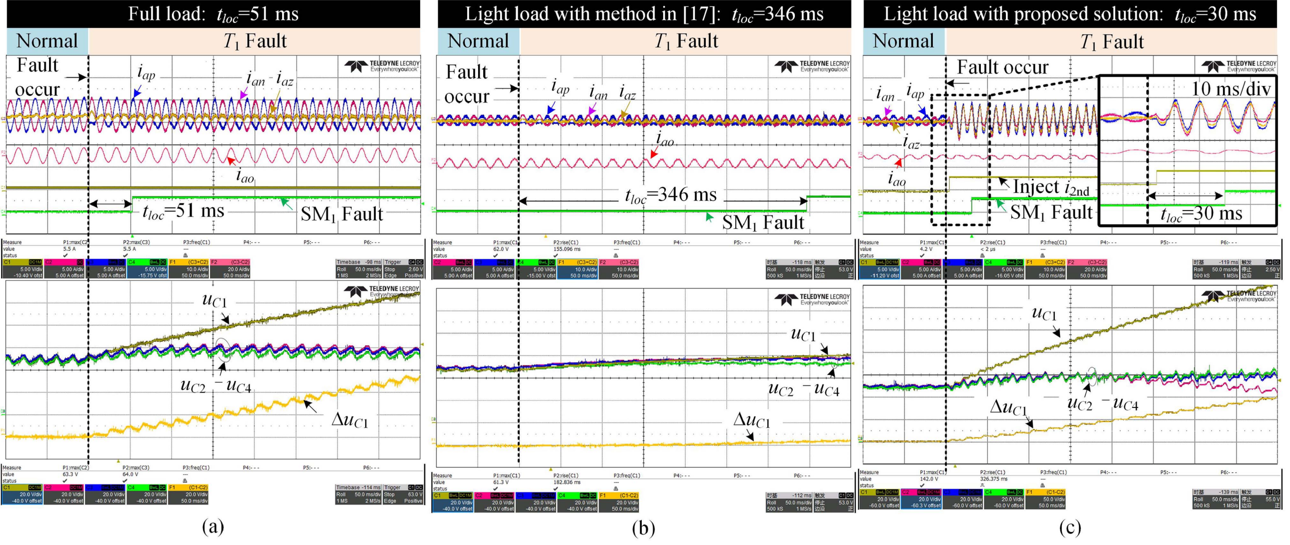


Fig. 15. Experimental results of T_1 fault location under different load conditions. (a) Full loads, the capacitor voltage of the faulty SM u_{C1} has an obvious deviation. (b) Light load of $P = 0.25$ p.u., the conventional method is difficult to locate fault quickly because of zero voltage deviation Δu_{C1}. (c) Light load of $P = 0.25$ p.u., the proposed solution is adopted and fault location is achieved by the rapid increase of the voltage deviation Δu_{C1}. (Time scale: 50 ms/div, voltage scale: 20 V/div, and current scale: 5 A/div.)

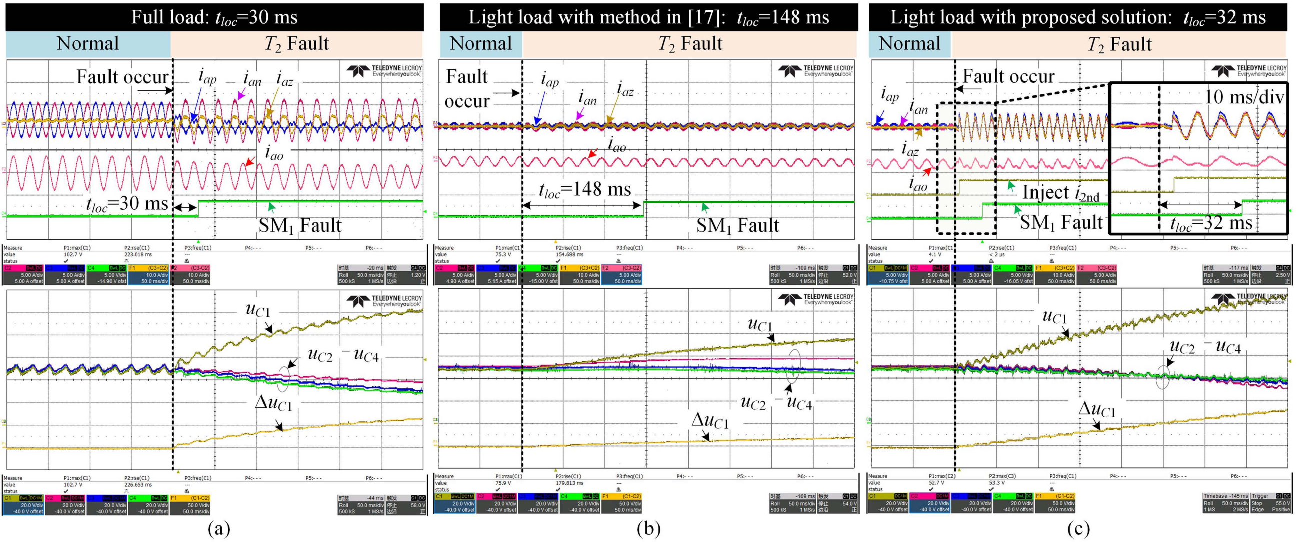


Fig. 16. Experimental results of T_2 fault location under different load conditions. (a) Full loads, the capacitor voltage of the faulty SM u_{C1} has an obvious deviation. (b) Light load of $P = 0.125$ p.u., the conventional method is difficult to locate fault quickly because of almost zero voltage deviation Δu_{C1}. (c) Light load of $P = 0.125$ p.u., the proposed solution is adopted and fast fault location is achieved by the rapid increase of the voltage deviation Δu_{C1}. (Time scale: 50 ms/div, voltage scale: 20 V/div, and current scale: 5 A/div.)

C. Comparison of Fault Location Time

The fault location time without and with the proposed current-reshaping-based solution is denoted as $t_{\text{loc,w/o}}$ and $t_{\text{loc},w}$, respectively. They are calculated by

$$\begin{cases} t_{\text{loc,w/o}} = t_{\text{loc},r} + N_{\text{cyc1}} \cdot T_0 \\ t_{\text{loc},w} = t_{\text{det,arm}} + (t_{\text{loc},r} - t_{\text{det,arm}}) = t_{\text{loc},r} \end{cases} \tag{23}$$

where $t_{\text{loc},r}$ is the fault location time under full loads, and it includes the time of faulty arm detection. The value of $t_{\text{loc},w}$ is composed of two parts, i.e., $t_{\text{det,arm}}$ and $(t_{\text{loc},r} - t_{\text{det,arm}})$. The first part $t_{\text{det,arm}}$ represents the time of detecting the faulty arm and triggering the current injection, which is usually not exceeding 10 ms [19], [29]. The second part $(t_{\text{loc},r} - t_{\text{det,arm}})$ is the fault location time after the current injection. Finally, the fault location time with the proposed solution $t_{\text{loc},w}$ is theoretically the same as that under full loads $t_{\text{loc},r}$.

Based on the analytical derivation in (23), three existing fault location techniques of MMC are taken as examples to evaluate the effectiveness of the proposed solution. Since the value of N_{cyc1} is usually higher than N_{cyc2}, N_{cyc1} is used in the above calculation to get the maximum fault location time. According

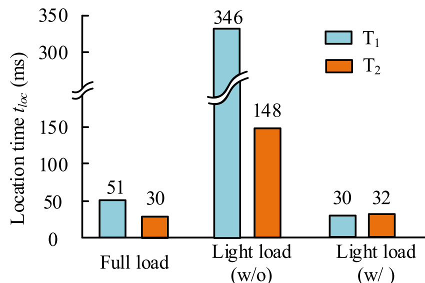


Fig. 17. Comparison of fault location time under different load conditions. (w/o: Without proposed solution. w: With proposed solution.)

TABLE V
EXPERIMENTAL PARAMETERS

Parameters and symbols	Values and units
Rated power P	1080 W
DC voltage U_{dc}	200 V
AC voltage amplitude U_m	80 V
Number of SMs N	4
SM capacitance C	1.64 mF
Rated SM voltage U_C	50 V
Arm inductance L_s	4 mH

to the parameters of MMC in Table IV, Fig. 13 compares the fault location time before and after the proposed approaches are adopted. It is shown that the fault location time of these three approaches will be all greatly increased due to the unipolar faulty arm current under light loads. By enabling the proposed approach of circulating current injection, the fault location time will be almost immune to the power level variations.

D. Discussion of Influence of Proposed Solution on Normal Operation

It is worth emphasizing that the proposed current-reshaping approach is put forward for the faulty conditions to locate the faulty SMs under the light load conditions. As shown in Fig. 11(a), the proposed current-reshaping-based control would not be conducted under normal operations but only triggered after the open-circuit fault is detected under light load conditions. Therefore, whatever circulating current control is conducted under the normal operations of MMC, there would not be interference from the proposed current-reshaping-based control.

V. EXPERIMENTAL VERIFICATIONS

Experiments are conducted on a small-scale prototype to verify the effectiveness of the proposed current-reshaping-based solution to the fault location of MMC under light load conditions. Fig. 14 shows the setup of the three-phase MMC with the parameters listed in Table V. There are four identical HBSMs in each arm of the MMC, and in the experiments, the first SM in the upper arm of phase a is set as the faulty SM, whose capacitor voltage is marked by u_{C1}.

The fault location principle in [18] is employed to evaluate the performance of the proposed method under light load conditions. The capacitor voltage of the SM$_i$ (the i th SM) is compared with the average voltage of rest SMs, and the voltage deviation of the ith SM Δu_{Ci} is compared with the preset threshold U_{TH}. If $\Delta u_{Ci} > U_{\mathrm{TH}}$ lasts for a certain duration ΔT, the ith SM will be confirmed to be faulty. In the following experiments, U_{TH} is set as 6% of the rated capacitor voltage, and ΔT is set as 5 ms.

A. T_1 Open-Circuit Fault Location

Fig. 15 shows the experimental results of T_1 fault under different load conditions. In Fig. 15(a), T_1 open-circuit fault occurs under the full load of $P = 1.0$ p.u., where the upper arm current is distorted but still bipolar. The capacitor voltage of the faulty SM u_{C1} rises rapidly and shows apparent deviations from that of the healthy SM. About 51 ms after the fault occurs, the fault flag of SM$_1$ is triggered and the faulty SM is located. In Fig. 15(b), the T_1 fault occurs under the light load of $P = 0.25$ p.u. The faulty arm current becomes nonnegative, and all the SM capacitors are charged without obvious voltage deviations. As a result, it takes 346 ms to locate the faulty SM under the light load condition. To address this problem, the proposed solution utilizes the control freedom of the second-order circulating current to reshape the faulty arm current to be bipolar. After the faulty arm is confirmed and the load level is below CLC, the circulating current is injected, as shown in Fig. 15(c). It rebuilds the negative magnitude of the faulty arm current, and the capacitor voltage deviations between the faulty and healthy SMs are increased in a short time. As a result, the total fault location time under the light load is reduced to 30 ms, which is even lower than that under the full load condition.

B. T_2 Open-Circuit Fault Location

Fig. 16 shows the experimental results for the T_2 fault. As shown in Fig. 16(a), the fault location time is 30 ms under full load, where the voltage deviations between the faulty and healthy SMs are apparent. However, when the power level is low as $P =$ 0.125 p.u. in Fig. 16(b), the positive interval of the arm current is suppressed to almost zero. The voltage deviations between the faulty SM capacitors and the healthy SM capacitors are relatively small, causing a fault location time of 148 ms. In Fig. 16(c), the proposed method injects the circulating current based on the principle in Section IV. Then, the positive magnitude of the faulty arm current is established. As a result, the voltage of the faulty SM capacitor is quickly increasing while the healthy SM voltage is decreasing, making the fault location time reduced from 148 ms to 32 ms.

C. Experimental Comparison

According to the experimental results, Fig. 17 compares the fault location time of the MMC without and with the proposed solution. It can be seen that the maximum fault location time is 346 ms under the light load for the conventional fault location method without the proposed solution. By adopting the proposed solution based on the circulating current injection, the fault location time under the light load can be significantly reduced to 30 ms, which is close to that under the full load. It should be emphasized that the proposed approach is not an alternative

approach to the existing voltage-deviations-based fault location techniques but a promotion to better facilitate them under light loads.

VI. Conclusion

In this article, a comprehensive analysis is conducted on the fault characteristics of MMC under light load conditions, which has rarely been studied yet. It indicates that the capacitor voltage deviations between the faulty and healthy SMs might disappear under the light loads because the faulty arm current is distorted to be unipolar for several continuous fundamental cycles. Also, the potential risk of fault location failure under light loads is revealed by the quantitative relation of fault location time increase and power levels. To address this risk under light load conditions, the current-reshaping-based solution of fault location is proposed by injecting the second-order circulating current to rebuild the bipolar arm current and generate the voltage deviations of the faulty SMs. In this way, the fault location time under light loads can be reduced to the same level as that under full loads, then the voltage-deviation-based fault location methods of the MMC can be well performed over a wide power range. Finally, the simulations and experiments are performed to validate the effectiveness of the proposed theory and solutions.

It should be noted that this article mainly focuses on the fault location of the faulty SMs in the MMC, which is conducted based on the prerequisites that the faulty type in MMC is confirmed to be the open-circuit fault of IGBTs. In future work, multitype fault diagnosis should be paid more attention since this is the foundation to further locate the faulty point of the MMC, for example, the sensor fault, IGBT fault, arm-level fault, and even grid-level fault.

References

[1] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

[2] B. Li, Y. Zhang, G. Wang, W. Sun, D. Xu, and W. Wang, "A modified modular multilevel converter with reduced capacitor voltage fluctuation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6108–6119, Oct. 2015.

[3] S. Debnath and M. Saeedifard, "A new hybrid modular multilevel converter for grid connection of large wind turbines," *IEEE Trans. Sustain. Energy*, vol. 4, no. 4, pp. 1051–1064, Oct. 2013.

[4] L. Zhou, C. Chen, J. Xiong, and K. Zhang, "A robust capacitor voltage balancing method for CPS-PWM-based modular multilevel converters accommodating wide power range," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14306–14316, Dec. 2022.

[5] B. Lu and S. K. Sharma, "A literature review of IGBT fault diagnostic and protection methods for power inverters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 5, pp. 1770–1777, Sep./Oct. 2009.

[6] Y. Zhang, H. Wang, Z. Wang, F. Blaabjerg, and M. Saeedifard, "Mission profile-based system-level reliability prediction method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6916–6930, Jul. 2020.

[7] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2413–2426, May 2015.

[8] U.-M. Choi, F. Blaabjerg, and K.-B. Lee, "Study and handling methods of power IGBT module failures in power electronic converter systems," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2513–2536, May 2015.

[9] J. Wang, H. Ma, and Z. Bai, "A submodule fault ride-through strategy for modular multilevel converters with nearest level modulation," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1597–1608, Feb. 2018.

[10] S. Shao, P. W. Wheeler, J. C. Clare, and A. J. Watson, "Fault detection for modular multilevel converters based on sliding mode observer," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4867–4872, Nov. 2013.

[11] G. Li, S. Xu, Z. Sun, C. Yao, G. Ren, and G. Ma, "Open-circuit fault diagnosis for three-level ANPC inverter based on predictive current vector residual," *IEEE Trans. Ind. Appl.*, vol. 59, no. 6, pp. 6837–6851, Nov./Dec. 2023.

[12] X. Chen, J. Liu, Z. Deng, S. Song, S. Du, and D. Wang, "A diagnosis strategy for multiple IGBT open-circuit faults of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 191–203, Jan. 2021.

[13] R. Picas, J. Zaragoza, J. Pou, and S. Ceballos, "Reliable modular multilevel converter fault detection with redundant voltage sensor," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 39–51, Jan. 2017.

[14] S. Yang, Y. Tang, and P. Wang, "Seamless fault-tolerant operation of a modular multilevel converter with switch open-circuit fault diagnosis in a distributed control architecture," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7058–7070, Aug. 2018.

[15] J. Zhang, X. Hu, S. Xu, Y. Zhang, and Z. Chen, "Fault diagnosis and monitoring of modular multilevel converter with fast response of voltage sensors," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 5071–5080, Jun. 2020.

[16] K. Bi, Q. An, J. Duan, L. Sun, and K. Gai, "Fast diagnostic method of open circuit fault for modular multilevel DC/DC converter applied in energy storage system," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3292–3296, May 2017.

[17] C. Liu, F. Deng, X. Cai, Z. Wang, Z. Chen, and F. Blaabjerg, "Submodule open-circuit fault detection for modular multilevel converters under light load condition with rearranged bleeding resistor circuit," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4600–4613, Apr. 2022.

[18] F. Deng, Z. Chen, M. R. Khan, and R. Zhu, "Fault detection and localization method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2721–2732, May 2015.

[19] B. Li, Y. Zhang, R. Yang, R. Xu, D. Xu, and W. Wang, "Seamless transition control for modular multilevel converters when inserting a cold-reserve redundant submodule," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4052–4057, Aug. 2015.

[20] S. Shao, A. J. Watson, J. C. Clare, and P. W. Wheeler, "Robustness analysis and experimental validation of a fault detection and isolation method for the modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3794–3805, May 2016.

[21] D. Zhou, S. Yang, and Y. Tang, "A voltage-based open-circuit fault detection and isolation approach for modular multilevel converters with model-predictive control," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9866–9874, Nov. 2018.

[22] C. Liu et al., "Fault localization strategy for modular multilevel converters under submodule lower switch open-circuit fault," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5190–5204, May 2020.

[23] Y. Jin et al., "A novel detection and localization approach of open-circuit switch fault for the grid-connected modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 112–124, Jan. 2023.

[24] W. Zhou, J. Sheng, H. Luo, W. Li, and X. He, "Detection and localization of submodule open-circuit failures for modular multilevel converters with single ring theorem," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3729–3739, Apr. 2019.

[25] S. Kiranyaz, A. Gastli, L. Ben-Brahim, N. Al-Emadi, and M. Gabbouj, "Real-time fault detection and identification for MMC using 1-D convolutional neural networks," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8760–8771, Nov. 2019.

[26] X. Hu, H. Jia, Y. Zhang, and Y. Deng, "An open circuit faults diagnosis method for MMC based on extreme gradient boosting," *IEEE Trans. Ind. Electron.*, vol. 70, no. 6, pp. 6239–6249, Jun. 2023.

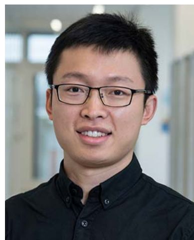
[27] F. Deng, Y. Chen, J. Dou, C. Liu, Z. Chen, and F. Blaabjerg, "Isolation forest based submodule open-circuit fault localization method for modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 3090–3102, Mar. 2023.

[28] Y. Zhang, Y. Zhang, F. Blaabjerg, and J. Zhang, "A non-invasive fault location method for modular multilevel converters under light load conditions," in *Proc. 48th Annu. Conf. IEEE Ind. Electron. Soc.*, 2022, pp. 1–6.

[29] D. Zhou, H. Qiu, S. Yang, and Y. Tang, "Submodule voltage similarity-based open-circuit fault diagnosis for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 8008–8016, Aug. 2019.

Yaqian Zhang (Member, IEEE) received the B.S. degree in electrical engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2016, and the Ph.D. degree in electrical engineering from Southeast University, Nanjing, China, in 2023.

During 2021–2022, she was a Visiting Ph.D. Student with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. She is currently a Lecturer with Southeast University. Her research focuses on medium- and high-voltage power electronic converters including modular multilevel converter and the solid-state transformer.



Yi Zhang (Member, IEEE) received the B.S. and M.S. degrees from the Harbin Institute of Technology, Harbin, China, in 2014 and 2016, respectively, and the Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2020, all in electrical engineering.

He is currently an Assistant Professor with Aalborg University, in 2023. During 2020–2023, he was affiliated with multiple institutions as a Postdoctoral Researcher with the support of the Danish Research Council for Independent Research, including RWTH-Aachen University, Germany, Swiss Federal Institute of Technology Lausanne, Switzerland, and Massachusetts Institute of Technology, USA. He was also a Visiting Scholar with the Georgia Institute of Technology, Atlanta, GA, USA, in 2018. His research focuses on the reliability of power electronics.

Dr. Zhang was the recipient of the First Place Prize Paper Award of IEEE TRANSACTIONS ON POWER ELECTRONICS in 2021, and IEEE Power Electronics Society Ph.D. Thesis Award in 2020.

Jianzhong Zhang (Senior Member, IEEE) received the M.Sc. and Ph.D. degrees in electrical engineering from the Department of Electrical Engineering, Southeast University, Nanjing, China, in 2005 and 2008, respectively.

From 2006 to 2007, he was a Visiting Scholar with the Department of Energy Technology, Aalborg University, Aalborg, Denmark. Since 2008, he has been with Southeast University, where he is currently a Research Professor with the School of Electrical Engineering. He was a Visiting Professor with the Worcester Polytechnic Institute, Worcester, MA, USA, and the University of British Columbia, Vancouver, BC, Canada, in 2012 and 2017, respectively. His research interests include power electronics, electrical machines, and renewable power generation.

Dr. Zhang was the recipient of the Institution Premium Award with the Institution of Engineering and Technology, Stevenage, U.K.

Fujin Deng (Senior Member, IEEE) received the B.Eng. degree in electrical engineering from the China University of Mining and Technology, Jiangsu, China, in 2005, the M.Sc. degree in electrical engineering from Shanghai Jiao Tong University, Shanghai, China, in 2008, and the Ph.D. degree in energy technology from the Department of Energy Technology, Aalborg University, Aalborg, Denmark, in 2012.

From 2013 to 2015 and from 2015 to 2017, he was a Postdoctoral Researcher and an Assistant Professor, respectively, with the Department of Energy Technology, Aalborg University. He joined the Southeast University in 2017 as a Professor with the School of Electrical Engineering, Southeast University, Nanjing, China. His main research interests include wind power generation, multilevel converters, high-voltage direct-current technology, dc grid, and offshore wind farm-power systems dynamics.

Frede Blaabjerg (Fellow, IEEE) received the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 1995.

From 1987 to 1988, he was with ABB-Scandia, Randers, Denmark He was an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998 with AAU Energy. From 2017, he has been a Villum Investigator. He was Honoris Causa with University Politehnica Timisoara, Romania, in 2017 and Tallinn Technical University, Estonia, in 2018. He has authored or coauthored more than 600 journal papers in the fields of power electronics and its applications. He is the coauthor of eight monographs and editor of 14 books in power electronics and its applications, e.g., the series (four volumes) Control of Power Electronic Converters and Systems published by Academic Press/Elsevier. His current research interests include power electronics and its applications, such as in wind turbines, PV systems, reliability, Power-2-X, power quality, and adjustable speed drives.

Dr. Blaabjerg was the recipient of the 38 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019, and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been a Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019–2020, he was the President of IEEE Power Electronics Society. He has been the Vice-President of the Danish Academy of Technical Sciences. He was nominated in 2014–2021 by Thomson Reuters to be among the most 250 cited researchers in engineering in the world.