Low-Complexity Heun's Method-Based FCS-MPC With Reduced Common-Mode Voltage for a Five-Level Inverter

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***Abstract*—The conventional finite control-set model predictive control (FCS-MPC) methods need a cost function with weighting factors to minimize the common-mode voltage (CMV) in the multilevel inverter (MLI) fed electric drive systems. Moreover, these methods require a higher sampling time for real-time implementation, resulting in a rich harmonic content in the inverter ac currents. This article addresses these concerns by proposing a low-complexity FCS-MPC with CMV minimization for a five-level inverter (FLI). The per-phase philosophy is adopted in the design and implementation of the proposed FCS-MPC for an FLI, resulting in a maximum number of predictions of 6 per phase only (a total of 18 predictions in a three-phase FLI system). Moreover, the proposed FCS-MPC minimizes the CMV without using a cost function, leading to superior current harmonic performance. Additionally, the Heun's integration method is introduced in the formulation of discrete-time models of the FLI, and they are used in real-time implementation of the proposed FCS-MPC. The superiority of the proposed method is demonstrated through a dSPACE-controlled FLI laboratory prototype. Furthermore, a comparative analysis of the proposed and the conventional FCS-MPC methods is presented in terms of total demand distortion of the current, inverter CMV, and the computational burden.**

***Index Terms*—Common-mode voltage (CMV), computational burden, discretization methods, multilevel inverter (MLI), power conversion harmonics, predictive control, total demand distortion (TDD).**

I. Introduction

THE common-mode voltage (CMV) induces bearing currents and shaft voltages in the multilevel inverter (MLI) fed electric drive systems (EDSs) and causes bearing failure and shaft breakdown [1]. To minimize the CMV, the control-based solutions are preferred over the hardware-based solutions due to their ability to reduce the cost and size of the EDS [2], [3]. Over the past decade, several control-based solutions, including pulse width modulation-based methods [4], finite control-set model predictive control (FCS-MPC) [5], [6], and sequential model predictive control (SMPC) methods [7] have been developed for CMV minimization in EDS.

The conventional FCS-MPC methods have been formulated with Euler and Heun's discretization techniques to regulate the MLI ac currents as a primary control objective [8], [9], [10]. These FCS-MPC methods are designed to control the three-phase objectives of an MLI by using a single cost function, and they exhibit robust performance in practice [11], [12]. Particularly, Heun's method-based FCS-MPC minimizes the reference current tracking error while operating at a low-switching frequency in comparison to the Euler method-based FCS-MPC. However, Heun's method-based FCS-MPC involves twice the number of calculations compared with its counterpart, resulting in a significant rise in its computational burden [10], [13]. On the other hand, the Euler and Heun's method-based FCS-MPCs need a cost function with weighting factors to minimize the CMV, and consequently, it affects the MLI's ac current quality [14], [15], [16].

The Euler method-based FCS-MPC is further simplified to control the objectives of each phase in an MLI by using an independent cost function [17]. The method in [17] reduces the computational burden, but it produces a higher current and voltage harmonic distortion compared to the single cost function-based FCS-MPC methods [18]. Moreover, the FCS-MPC method in [17], mainly focuses on the MLI ac currents and floating capacitors (FCs) voltage control only. Alternatively, the single cost function-based FCS-MPC methods are formulated in terms of inverter ac voltages as a primary objective [19], [20]. These methods are implemented in the $\alpha\beta$-reference frame by using the space vector (SV) philosophy, and it requires sector/triangle detection to locate the voltage vectors (VVs) for the cost function optimization [19]. In addition, they utilize offline selection of VVs to minimize the CMV and affect the MLI's performance due to the reduction in available VVs for the cost function optimization process [20].

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On the other hand, the SMPC methods have gained tremendous popularity for MLIs over the FCS-MPC methods due to their low computational burden [21], [22]. Similar to the FCS-MPC methods, the SMPC methods have also been formulated in terms of inverter ac currents or inverter ac voltages as a primary objective and employed either cost function or offline selection of VVs to minimize the CMV [7], [13], [23], [24], [25], [26], [27]. In [23], the current-controlled SMPC is reported for MLIs. This method has superior harmonic performance, but it has a poor transient response when compared with the FCS-MPC method [23].

On the other hand, the voltage-controlled SMPC methods for MLIs are reported in [7], [24], [13], [25], [26], and [27]. In [7], the SV philosophy together with the coordination transformation and sector identification has been employed to implement the voltage-controlled SMPC methods for MLIs. This method produces a higher current harmonic distortion in comparison to the Euler method-based FCS-MPC [7]. On the other hand, the virtual SV-based voltage-controlled SMPC method is reported in [24]. This method minimizes the FC voltage ripple, but it leads to a high switching frequency operation. Moreover, the methods in [7] and [24] need a cost function with weighting factors to minimize the CMV, which affects the overall system performance and its controllability in comparison to the FCS-MPC methods.

Alternatively, the low-computational voltage-controlled SMPC methods in [13], [25], [26], and [27], minimize the CMV without using a cost function. In these methods, the suitable VVs are selected offline by considering the lowest CMV criteria. This philosophy affects the controllability of the inverter ac currents and FCs voltage due to the reduction in the available VVs for the cost function optimization process [13], [25], [26], [27]. Moreover, the offline selection philosophy becomes cumbersome with the rise in the MLI output levels. In addition, all the existing SMPC methods have employed the MLI models based on the Euler method in their implementation. These models exhibit poor performance under a large sampling time operation [28]. To improve the MLI performance and FCs voltage controllability, Heun's method-based FCS-MPC is a better choice over the Euler method-based FCS-MPC and SMPC methods. To the best of the author's knowledge, there are no studies on the low-complexity Heun's method-based FCS-MPC that can minimize the CMV without using a cost function and offline selection of VVs for MLIs. Furthermore, the literature lacks a comprehensive comparison study of various FCS-MPC methods with CMV minimization.

To fill this research gap, the authors have proposed a low-complexity Heun's method-based FCS-MPC, which can minimize the CMV without using a cost function or offline selection of VVs for a five-level inverter (FLI). The discrete-time models of an FLI are derived by using the Heun's integration method, and they are used in real-time implementation of the proposed FCS-MPC. The steady-state and transient performances of the proposed FCS-MPC are demonstrated through a dSPACE-DS1103-controlled FLI prototype. In addition, the proposed FCS-MPC performance is evaluated experimentally in terms of total demand distortion (TDD) of the current, the CMV, and the computational burden. The main contributions of the proposed research work are summarized as follows:

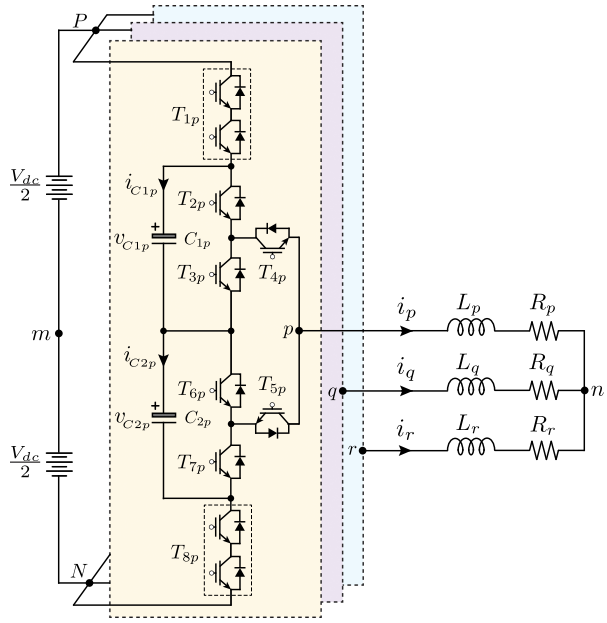

Fig. 1. Circuit configuration of an FLI.

1) the discrete-time models of the FLI are developed by using the Heun's integration method;
2) the control objectives of each phase in an FLI are achieved by using an independent cost function, resulting in a significant reduction in the computational burden in comparison to the existing FCS-MPC methods;
3) the proposed FCS-MPC minimizes the CMV without using a cost function or offline selection criteria, and it produces the lowest CMV when compared with the existing FCS-MPC methods;
4) the proposed method produces a low TDD in the inverter ac current and has superior FC voltage controllability;
5) a comprehensive comparative analysis of the proposed and the existing FCS-MPC methods is presented. In this study, the existing FCS-MPC methods are designed with a CMV minimization objective, and a cost function is formulated.

II. Formulation of the Proposed Low-Complexity FCS-MPC Method

The FLI consists of switching devices T_{1x}–T_{8x} and FCs C_{1x}–C_{2x} only, and their electrical connections are shown in Fig. 1. The devices T_{1x} and T_{8x} are formed with a series connection of two devices with a blocking voltage of $V_{\rm dc}/4$ each, to handle a net blocking voltage of $V_{\rm dc}/2$, where $V_{\rm dc}$ is the dc-bus voltage. The voltages of FCs C_{1x} and C_{2x} are denoted with v_{C1x} and v_{C2x}, respectively, and their nominal values are $V_{\rm dc}/4$ each. The FLI load is formed with a resistor (R_x) and an inductor (L_x), where $x \in \{p, q, r\}$ represents the inverter ac terminal.

A. Discrete-Time Models of the FLI AC Currents

The proposed low-complexity FCS-MPC is formulated to control the inverter ac currents, FCs voltage, and CMV in the FLI, and their respective mathematical models are given in the discrete-time domain by using Heun's integration method [28].

In this study, the three-phase inverter ac currents are defined as state variables to control each phase independently. From Fig. 1, the inverter ac currents trajectory in the continuous-time domain can be written as

$$\frac{d}{dt}\begin{bmatrix} i_p(t) \\ i_q(t) \\ i_r(t) \end{bmatrix} = \begin{bmatrix} \frac{1}{L_p} & 0 & 0 \\ 0 & \frac{1}{L_q} & 0 \\ 0 & 0 & \frac{1}{L_r} \end{bmatrix} \begin{bmatrix} v_{pm}(t) \\ v_{qm}(t) \\ v_{rm}(t) \end{bmatrix} - v_{nm}(t) \begin{bmatrix} \frac{1}{L_p} \\ \frac{1}{L_q} \\ \frac{1}{L_r} \end{bmatrix} - \begin{bmatrix} \frac{R_p}{L_p} & 0 & 0 \\ 0 & \frac{R_q}{L_q} & 0 \\ 0 & 0 & \frac{R_r}{L_r} \end{bmatrix} \begin{bmatrix} i_p(t) \\ i_q(t) \\ i_r(t) \end{bmatrix} \tag{1}$$

where $v_{nm}(t)$ is the CMV, $i_p(t)$, $i_q(t)$, $i_r(t)$ are the inverter ac currents, and $v_{pm}(t)$, $v_{qm}(t)$, $v_{rm}(t)$ are the inverter ac voltages.

In the conventional FCS-MPC methods, the cost function has been employed to minimize the CMV $v_{nm}(t)$ and its magnitude depends on the reference value of the CMV ($v^*_{nm}(t)$). On the contrary, in the proposed method, the objective of $v_{nm}(t)$ minimization is integrated into the inverter's ac current control objective by considering the following assumption of $v^*_{nm}(t) = v_{nm}(t) \approx 0$, thereby the CMV can be minimized without using a cost function. From (1), the inverter ac currents trajectory with an integrated CMV minimization objective can be written as

$$\frac{d}{dt}\begin{bmatrix} i_p(t) \\ i_q(t) \\ i_r(t) \end{bmatrix} = \begin{bmatrix} \frac{1}{L_p} & 0 & 0 \\ 0 & \frac{1}{L_q} & 0 \\ 0 & 0 & \frac{1}{L_r} \end{bmatrix} \begin{bmatrix} v_{pm}(t) \\ v_{qm}(t) \\ v_{rm}(t) \end{bmatrix} - \begin{bmatrix} \frac{R_p}{L_p} & 0 & 0 \\ 0 & \frac{R_q}{L_q} & 0 \\ 0 & 0 & \frac{R_r}{L_r} \end{bmatrix} \begin{bmatrix} i_p(t) \\ i_q(t) \\ i_r(t) \end{bmatrix}. \tag{2}$$

Typically, the inverter ac voltage ($v_{pm}(t)$, $v_{qm}(t)$, $v_{rm}(t)$) consists of load voltage ($v_{pn}(t)$, $v_{qn}(t)$, $v_{rn}(t)$) and CMV ($v_{nm}(t)$)) components. The load voltage component magnitude will be regulated by controlling the inverter ac currents or load currents, whereas the CMV limits are set by the user. According to (2), by controlling the inverter ac currents, the inverter produces an ac voltage equal to the load voltage component (i.e., $v_{pm}(t) = v_{pn}(t)$), which indirectly implies that the inverter ac voltage will have a CMV component close to zero (i.e., the lowest magnitude). This will be achieved through the proposed FCS-MPC method.

To implement the proposed FCS-MPC, Heun's integration method is employed to develop the sampled-data models from the continuous-time models. According to the principle of Heun's integration method, the effective value of the predicted control variable y can be expressed as [28]

$$y^p(n+1) = \frac{T_s}{2}\left[\frac{dy}{dt}\Big|_{t=t(n)} + \frac{dy}{dt}\Big|_{t=t(n+1)}\right] + y(n) \tag{3}$$

where superscript "p" represents the effective value of the predicted variable, T_s is the sampling time, $dy/dt|_{t=t(n)}$ represents the control variable trajectory in the predictor stage, and $dy/dt|_{t=t(n+1)}$ represents the control variable trajectory in the corrector stage.

TABLE I
FLI SWITCHING STATES AND FC VOLTAGES

T_{1x}	T_{2x}	T_{3x}	T_{4x}	T_{5x}	T_{6x}	T_{7x}	T_{8x}	v_{C1x}	v_{C2x}	v_{xm}
1	1	0	1	0	0	0	0	NC	NC	$\frac{V_{dc}}{2}$
1	0	1	1	0	0	0	0	CH ($i_x > 0$)	NC	$\frac{V_{dc}}{4}$
0	1	0	1	0	0	0	1	DCH ($i_x > 0$)	DCH ($i_x > 0$)	0
1	0	0	0	1	0	1	0	CH ($i_x > 0$)	CH ($i_x > 0$)	0
0	0	0	0	1	1	0	1	NC	DCH ($i_x > 0$)	$-\frac{V_{dc}}{4}$
0	0	0	0	1	0	1	1	NC	NC	$-\frac{V_{dc}}{2}$

NC — No Change; CH — Charging; DCH — Discharging

From (2) and (3), the effective value of predicted inverter ac currents with an integrated CMV minimization can be written as

$$\begin{bmatrix} i^p_p(n+1) \\ i^p_q(n+1) \\ i^p_r(n+1) \end{bmatrix} = \begin{bmatrix} \frac{T_s}{2L_p} & 0 & 0 \\ 0 & \frac{T_s}{2L_q} & 0 \\ 0 & 0 & \frac{T_s}{2L_r} \end{bmatrix} \begin{bmatrix} v_{pm}(n) + v_{pm}(n+1) \\ v_{qm}(n) + v_{qm}(n+1) \\ v_{rm}(n) + v_{rm}(n+1) \end{bmatrix} - \begin{bmatrix} \frac{T_s R_p}{2L_p} & 0 & 0 \\ 0 & \frac{T_s R_q}{2L_q} & 0 \\ 0 & 0 & \frac{T_s R_r}{2L_r} \end{bmatrix} \begin{bmatrix} i_p(n) + i_p(n+1) \\ i_q(n) + i_q(n+1) \\ i_r(n) + i_r(n+1) \end{bmatrix} + \begin{bmatrix} i_p(n) \\ i_q(n) \\ i_r(n) \end{bmatrix}. \tag{4}$$

From Table I, the calculation of inverter ac voltages in the predictor stage can be expressed as

$$\begin{bmatrix} v_{pm}(n) \\ v_{qm}(n) \\ v_{rm}(n) \end{bmatrix} = V_{dc}\begin{bmatrix} T_{1p} \\ T_{1q} \\ T_{1r} \end{bmatrix} - \frac{V_{dc}}{2}\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} + \begin{bmatrix} T_{2p} - T_{1p} & 0 & 0 \\ 0 & T_{2q} - T_{1q} & 0 \\ 0 & 0 & T_{2r} - T_{1r} \end{bmatrix} \begin{bmatrix} v_{C1p}(n) \\ v_{C1q}(n) \\ v_{C1r}(n) \end{bmatrix} + \begin{bmatrix} T_{8p} - T_{7p} & 0 & 0 \\ 0 & T_{8q} - T_{7q} & 0 \\ 0 & 0 & T_{8r} - T_{7r} \end{bmatrix} \begin{bmatrix} v_{C2p}(n) \\ v_{C2q}(n) \\ v_{C2r}(n) \end{bmatrix}. \tag{5}$$

Similarly, the calculation of inverter ac voltages in the corrector stage can be expressed as

$$\begin{bmatrix} v_{pm}(n+1) \\ v_{qm}(n+1) \\ v_{rm}(n+1) \end{bmatrix} = V_{dc}\begin{bmatrix} T_{1p} \\ T_{1q} \\ T_{1r} \end{bmatrix} - \frac{V_{dc}}{2}\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$

$$+\begin{bmatrix} T_{2p}-T_{1p} & 0 & 0 \\ 0 & T_{2q}-T_{1q} & 0 \\ 0 & 0 & T_{2r}-T_{1r} \end{bmatrix} \begin{bmatrix} v_{C1p}(n+1) \\ v_{C1q}(n+1) \\ v_{C1r}(n+1) \end{bmatrix}$$
$$+\begin{bmatrix} T_{8p}-T_{7p} & 0 & 0 \\ 0 & T_{8q}-T_{7q} & 0 \\ 0 & 0 & T_{8r}-T_{7r} \end{bmatrix} \begin{bmatrix} v_{C2p}(n+1) \\ v_{C2q}(n+1) \\ v_{C2r}(n+1) \end{bmatrix}. \tag{6}$$

On the other hand, the calculation of the predicted inverter ac currents in the predictor stage can be written as

$$\begin{bmatrix} i_p(n+1) \\ i_q(n+1) \\ i_r(n+1) \end{bmatrix} = \begin{bmatrix} \frac{T_s}{L_p} & 0 & 0 \\ 0 & \frac{T_s}{L_q} & 0 \\ 0 & 0 & \frac{T_s}{L_r} \end{bmatrix} \begin{bmatrix} v_{pm}(n) \\ v_{qm}(n) \\ v_{rm}(n) \end{bmatrix}$$
$$-\begin{bmatrix} \frac{T_s R_p}{L_p} & 0 & 0 \\ 0 & \frac{T_s R_q}{L_q} & 0 \\ 0 & 0 & \frac{T_s R_r}{L_r} \end{bmatrix} \begin{bmatrix} i_p(n) \\ i_q(n) \\ i_r(n) \end{bmatrix}$$
$$+\begin{bmatrix} i_p(n) \\ i_q(n) \\ i_r(n) \end{bmatrix}. \tag{7}$$

B. Discrete-Time Models of the FLI FC Voltages

The FLI has two FCs in each phase, and their voltages should be regulated at $V_{\text{dc}}/4$. The trajectory of the kth FC voltage in phase-x can be written as

$$\frac{d\, v_{Ckx}}{dt} = \frac{i_{Ckx}}{C_{kx}} \tag{8}$$

where v_{Ckx}, i_{Ckx}, and C_{kx} are the kth FC's voltage, current, and capacitance in phase-x, respectively, and $k \in \{1, 2\}$ is the FC index.

From (3) and (8), the effective value of predicted FLI's FCs voltage can be written as

$$\begin{bmatrix} v^p_{C1p}(n+1) \\ v^p_{C1q}(n+1) \\ v^p_{C1r}(n+1) \end{bmatrix} = \begin{bmatrix} v_{C1p}(n) \\ v_{C1q}(n) \\ v_{C1r}(n) \end{bmatrix} + \begin{bmatrix} \frac{T_s}{2C_{1p}} & 0 & 0 \\ 0 & \frac{T_s}{2C_{1q}} & 0 \\ 0 & 0 & \frac{T_s}{2C_{1r}} \end{bmatrix}$$
$$\begin{bmatrix} i_{C1p}(n)+i_{C1p}(n+1) \\ i_{C1q}(n)+i_{C1q}(n+1) \\ i_{C1r}(n)+i_{C1r}(n+1) \end{bmatrix}$$
$$\begin{bmatrix} v^p_{C2p}(n+1) \\ v^p_{C2q}(n+1) \\ v^p_{C2r}(n+1) \end{bmatrix} = \begin{bmatrix} v_{C2p}(n) \\ v_{C2q}(n) \\ v_{C2r}(n) \end{bmatrix} + \begin{bmatrix} \frac{T_s}{2C_{2p}} & 0 & 0 \\ 0 & \frac{T_s}{2C_{2q}} & 0 \\ 0 & 0 & \frac{T_s}{2C_{2r}} \end{bmatrix}$$
$$\begin{bmatrix} i_{C2p}(n)+i_{C2p}(n+1) \\ i_{C2q}(n)+i_{C2q}(n+1) \\ i_{C2r}(n)+i_{C2r}(n+1) \end{bmatrix}. \tag{9}$$

From Table I, the calculation of FCs current in the predictor stage can be written as

$$\begin{bmatrix} i_{C1p}(n) \\ i_{C1q}(n) \\ i_{C1r}(n) \end{bmatrix} = \begin{bmatrix} T_{1p}-T_{2p} & 0 & 0 \\ 0 & T_{1q}-T_{2q} & 0 \\ 0 & 0 & T_{1r}-T_{2r} \end{bmatrix}$$
$$\begin{bmatrix} i_p(n) \\ i_q(n) \\ i_r(n) \end{bmatrix}$$
$$\begin{bmatrix} i_{C2p}(n) \\ i_{C2q}(n) \\ i_{C2r}(n) \end{bmatrix} = \begin{bmatrix} T_{7p}-T_{8p} & 0 & 0 \\ 0 & T_{7q}-T_{8q} & 0 \\ 0 & 0 & T_{7r}-T_{8r} \end{bmatrix}$$
$$\begin{bmatrix} i_p(n) \\ i_q(n) \\ i_r(n) \end{bmatrix}. \tag{10}$$

Similarly, the calculation of FCs current in the corrector stage can be written as

$$\begin{bmatrix} i_{C1p}(n+1) \\ i_{C1q}(n+1) \\ i_{C1r}(n+1) \end{bmatrix} = \begin{bmatrix} T_{1p}-T_{2p} & 0 & 0 \\ 0 & T_{1q}-T_{2q} & 0 \\ 0 & 0 & T_{1r}-T_{2r} \end{bmatrix}$$
$$\begin{bmatrix} i_p(n+1) \\ i_q(n+1) \\ i_r(n+1) \end{bmatrix}$$
$$\begin{bmatrix} i_{C2p}(n+1) \\ i_{C2q}(n+1) \\ i_{C2r}(n+1) \end{bmatrix} = \begin{bmatrix} T_{7p}-T_{8p} & 0 & 0 \\ 0 & T_{7q}-T_{8q} & 0 \\ 0 & 0 & T_{7r}-T_{8r} \end{bmatrix}$$
$$\begin{bmatrix} i_p(n+1) \\ i_q(n+1) \\ i_r(n+1) \end{bmatrix}. \tag{11}$$

On the other hand, the calculation of the predicted FCs voltage in the predictor stage can be written as

$$\begin{bmatrix} v_{C1p}(n+1) \\ v_{C1q}(n+1) \\ v_{C1r}(n+1) \end{bmatrix} = \begin{bmatrix} v_{C1p}(n) \\ v_{C1q}(n) \\ v_{C1r}(n) \end{bmatrix} + \begin{bmatrix} \frac{T_s}{C_{1p}} & 0 & 0 \\ 0 & \frac{T_s}{C_{1q}} & 0 \\ 0 & 0 & \frac{T_s}{C_{1r}} \end{bmatrix} \begin{bmatrix} i_{C1p}(n) \\ i_{C1q}(n) \\ i_{C1r}(n) \end{bmatrix}$$
$$\begin{bmatrix} v_{C2p}(n+1) \\ v_{C2q}(n+1) \\ v_{C2r}(n+1) \end{bmatrix} = \begin{bmatrix} v_{C2p}(n) \\ v_{C2q}(n) \\ v_{C2r}(n) \end{bmatrix} + \begin{bmatrix} \frac{T_s}{C_{2p}} & 0 & 0 \\ 0 & \frac{T_s}{C_{2q}} & 0 \\ 0 & 0 & \frac{T_s}{C_{2r}} \end{bmatrix} \begin{bmatrix} i_{C2p}(n) \\ i_{C2q}(n) \\ i_{C2r}(n) \end{bmatrix}. \tag{12}$$

III. Implementation of the Proposed Low-Complexity FCS-MPC Method

The proposed Heun's method-based FCS-MPC is designed to handle the control objectives of each phase in an FLI independently, resulting in 6 predictions per phase (a total of 18 predictions in a three-phase FLI). Hence, the computational

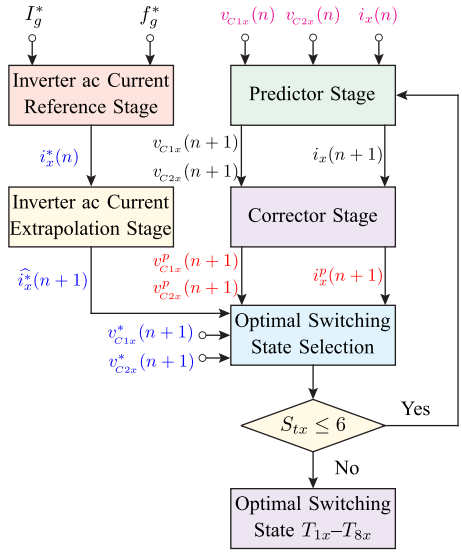

Fig. 2. Design steps of the proposed FCS-MPC.

burden of the proposed FCS-MPC is significantly reduced in comparison to the conventional FCS-MPC methods. In this study, the key control objectives of an FLI, such as inverter ac currents and FCs voltage are considered. Moreover, the CMV minimization objective is integrated into the inverter ac currents given in (2), thereby the proposed FCS-MPC can also minimize the CMV without using a cost function.

To implement the proposed FCS-MPC, the discrete-time models of the FLI are developed by using Heun's integration method [28]. Therefore, the prediction process of control variables involves the predictor and corrector stages in the implementation of the proposed FCS-MPC, along with the extrapolation of reference control variables and optimal selection of switching state, as depicted in Fig. 2. Among them, the predictor, corrector, and optimal switching state selection stages are executed iteratively for a total switching states (S_{tx}) of 6 per phase, as shown in Fig. 2. In the implementation of the proposed FCS-MPC, the inverter ac current references are generated with a peak magnitude of I_g^* and a frequency of f_g^*, and they can be written as

$$\begin{bmatrix} i_p^*(n) \\ i_q^*(n) \\ i_r^*(n) \end{bmatrix} = I_g^* \begin{bmatrix} \sin(2\pi f_g^* t) \\ \sin(2\pi f_g^* t - \frac{2\pi}{3}) \\ \sin(2\pi f_g^* t - \frac{4\pi}{3}) \end{bmatrix}. \tag{13}$$

The reference currents in (13) are time-varying signals, and they are extrapolated to the $(n+1)$th sampling point by using Lagrange extrapolation [10], and they can be written as

$$\begin{bmatrix} \widehat{i}_p^*(n+1) \\ \widehat{i}_q^*(n+1) \\ \widehat{i}_r^*(n+1) \end{bmatrix} = 3 \begin{bmatrix} i_p^*(n) \\ i_q^*(n) \\ i_r^*(n) \end{bmatrix} - 3 \begin{bmatrix} i_p^*(n-1) \\ i_q^*(n-1) \\ i_r^*(n-1) \end{bmatrix} + \begin{bmatrix} i_p^*(n-2) \\ i_q^*(n-2) \\ i_r^*(n-2) \end{bmatrix} \tag{14}$$

whereas the FCs voltage reference at (n)th sampling point is defined, and it is set to $v_{C1x}^*(n) = v_{C2x}^*(n) = V_{\text{dc}}/4$. These signals are dc in nature, and they remain constant at all sampling points. Hence, the $v_{C1x}^*(n+1) = v_{C1x}^*(n)$ and $v_{C2x}^*(n+1) = v_{C2x}^*(n)$ in this study.

On the other hand, the implementation of predictor and corrector stages to calculate the effective values of predicted inverter ac current ($i_x^p(n+1)$) and FCs voltage ($v_{C1x}^p(n+1)$ and $v_{C2x}^p(n+1)$) of phase-x is depicted in Fig. 3. The predictor stage is designed to predict the future behavior of the control variables. In this stage, the inverter ac voltage $v_{xm}(n)$ and FC currents $i_{C1x}(n)$, $i_{C2x}(n)$ are calculated by using (5) and (10), respectively, along with the measured inverter ac current $i_x(n)$, and FCs voltage $v_{C1x}(n)$ and $v_{C2x}(n)$. The calculated $v_{xm}(n)$, $i_{C1x}(n)$, and $i_{C2x}(n)$ and the measured $i_x(n)$, $v_{C1x}(n)$, and $v_{C2x}(n)$ values are used in (7) and (12) to predict the inverter ac current $i_x(n+1)$, and FCs voltage $v_{C1x}(n+1)$ and $v_{C2x}(n+1)$, respectively, in the predictor stage, as depicted in Fig. 3.

In addition, the corrector stage is designed to correct the predicted control variables of the predictor stage, as shown in Fig. 3. In this stage, the correction factors, such as inverter ac voltage $v_{xm}(n+1)$, and FCs current $i_{C1x}(n+1)$ and $i_{C2x}(n+1)$ are calculated by using (6) and (11), respectively, along with the predicted values of $v_{C1x}(n+1)$, $v_{C2x}(n+1)$, and $i_x(n+1)$ from the predictor stage as shown in Fig. 3. The predicted values from the predictor stage and the correction factors from the corrector stage along with the measured variables are used in (4) and (9) to calculate the effective values of the predicted inverter ac current $i_x^p(n+1)$, and FCs voltage $v_{C1x}^p(n+1)$ and $v_{C2x}^p(n+1)$. These variables are used in the optimal switching state selection process. In this stage, a cost function is formulated with the effective values of predicted control variables and their respective references, and it can be written as

$$\begin{aligned} \begin{bmatrix} J_p(n) \\ J_q(n) \\ J_r(n) \end{bmatrix} &= \left\| \begin{bmatrix} \widehat{i}_p^*(n+1) \\ \widehat{i}_q^*(n+1) \\ \widehat{i}_r^*(n+1) \end{bmatrix} - \begin{bmatrix} i_p^p(n+1) \\ i_q^p(n+1) \\ i_r^p(n+1) \end{bmatrix} \right\| \\ &+ \lambda_v \left\| \begin{bmatrix} v_{C1p}^*(n+1) \\ v_{C1q}^*(n+1) \\ v_{C1r}^*(n+1) \end{bmatrix} - \begin{bmatrix} v_{C1p}^p(n+1) \\ v_{C1q}^p(n+1) \\ v_{C1r}^p(n+1) \end{bmatrix} \right\| \\ &+ \lambda_v \left\| \begin{bmatrix} v_{C2p}^*(n+1) \\ v_{C2q}^*(n+1) \\ v_{C2r}^*(n+1) \end{bmatrix} - \begin{bmatrix} v_{C2p}^p(n+1) \\ v_{C2q}^p(n+1) \\ v_{C2r}^p(n+1) \end{bmatrix} \right\|. \end{aligned} \tag{15}$$

The FC voltage weighting factor λ_v in (15), is used to rank the FC voltage objective against the inverter ac currents control objective, and it is selected by using the per-unit method [16], [29]. The cost function of each phase given in (15), is independently evaluated for a total of six switching states. Finally, the optimal switching state that gives a favourable system response is selected and applied to the FLI. The selected optimal switching state guarantees the perfect regulation of the inverter ac currents and FCs voltage while generating the lowest CMV.

IV. Experimental Demonstration of the Proposed Low-Complexity FCS-MPC Performance

The performance of the proposed low-complexity Heun's method-based FCS-MPC is demonstrated through a scaled-down laboratory prototype of dSPACE-DS1103-controlled FLI

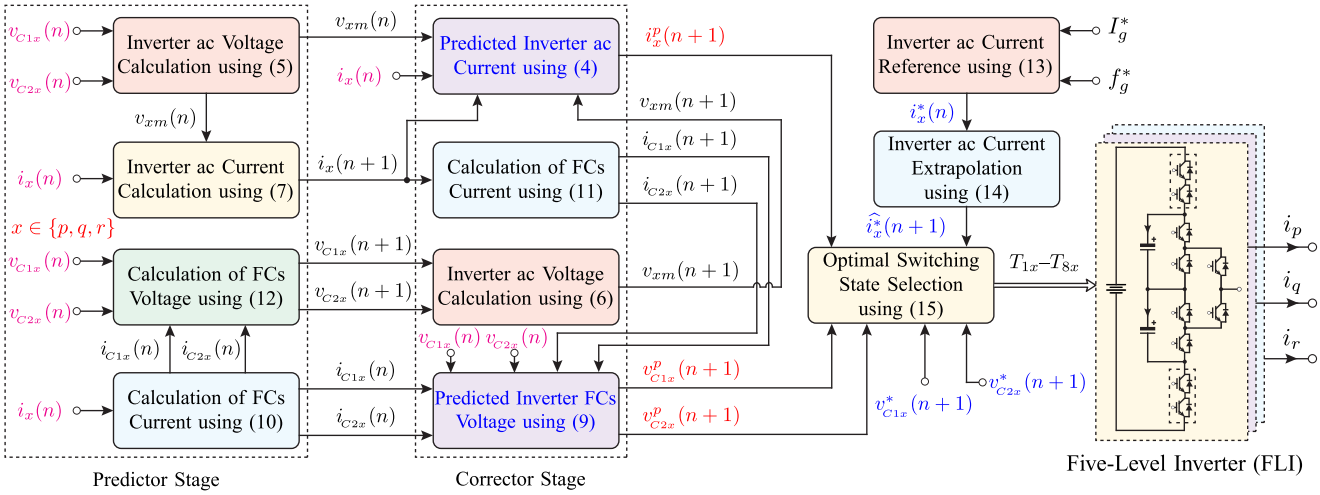

Fig. 3. Implementation steps of the proposed FCS-MPC for an FLI.

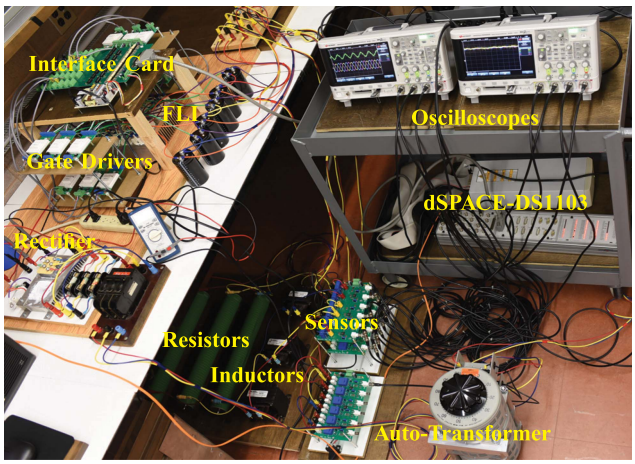

Fig. 4. Laboratory prototype of an FLI.

TABLE II
LABORATORY PROTOTYPE SPECIFICATIONS

Parameters Description	Value
Inverter rated power (S_{gr})	6.5 kVA
Inverter rated voltage (V_{gr})	208 V (L-L)
Inverter rated current (I_{gr})	17.68 A (rms)
Inverter rated frequency (f_{gr})	60 Hz
DC-bus voltage ($V_{\rm dc}$)	280 V
FC voltage (V_{Ckx})	70 V
FC capacitance (C_{kx})	2200 μF
Load inductance (L_x)	5 mH
Load resistance (R_x)	5 Ω
Sampling time (T_s)	200 μs

as depicted in Fig. 4. The specifications of the laboratory prototype are given in Table II. In this study, the proposed FCS-MPC is executed with a sampling time of 200 μs, which includes the time taken to complete the analog-to-digital signal conversion process, execution of the predictive algorithm, and gating signal generation tasks. The performance of the proposed FCS-MPC method is evaluated in terms of TDD of the inverter ac currents (%TDD$_i$), root mean square (RMS) value of the CMV ($V_{\rm cm}$), and the computational burden. Additionally, the proposed FCS-MPC performance is compared with the existing Euler method-based FCS-MPC [8] and Heun's method-based FCS-MPC methods [10] with CMV minimization. The existing Euler method-based FCS-MPC is referred to as FCS-MPC-I, whereas the existing Heun's method-based FCS-MPC is referred to as FCS-MPC-II in this manuscript. The existing FCS-MPC methods are designed to handle the control objectives of three phases together by using a single cost function, and it is given as

$$\begin{aligned} J(n) = & \sum_{x=p,q,r} \left|\left| \widehat{i}_x^*(n+1) - i_x^p(n+1) \right|\right| \\ & + \lambda_c \sum_{x=p,q,r} \left|\left| v_{C1x}^*(n+1) - v_{C1x}^p(n+1) \right|\right| \\ & + \lambda_c \sum_{x=p,q,r} \left|\left| v_{C2x}^*(n+1) - v_{C2x}^p(n+1) \right|\right| \\ & + \lambda_m \left|\left| v_{nm}^*(n+1) - v_{nm}^p(n+1) \right|\right| \end{aligned} \tag{16}$$

where λ_c and λ_m are the weighting factors of FC voltage and the CMV, respectively, and they are selected as per the per-unit method given in [16] and [29]. The cost function $J(n)$ is evaluated for a total of 216 switching states. As mentioned earlier, the inverter ac currents (i.e., load voltage component) and CMV are the function of inverter ac voltage, resulting in a coupling between these two objectives in (16). Hence, the minimization of CMV with the help of a cost function given in (16) affects the inverter ac current quality. This is one of the key problems in the existing FCS-MPC methods.

A. *Performance of FLI Under Current Magnitude and Frequency Variations*

The test results of the proposed FCS-MPC with the step change in I_g^* from 15 to 25 A and from 25 to 15 A at $f_g^* = 60$ Hz are depicted in Fig. 5. The actual inverter ac currents track well their respective references, irrespective of the I_g^*, as shown in Fig. 5(a). These currents have a %TDD$_i$ of 2.12 at $I_g^* = 15$ A,

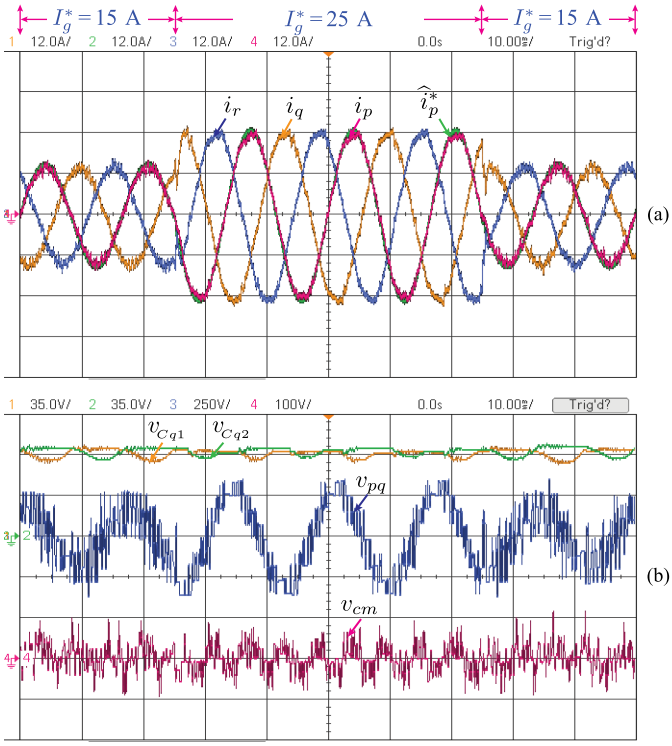

Fig. 5. Performance with a step change in current magnitude at $f_g^* = 60$ Hz. (a) Extrapolated reference and actual inverter ac currents. (b) Phase-q FC voltages, inverter line-line voltage, and the CMV.

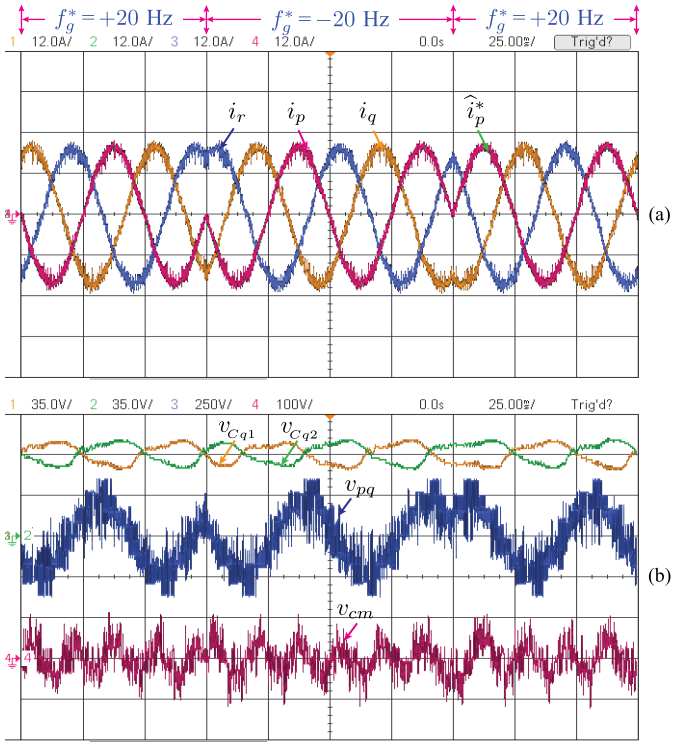

Fig. 6. Performance with frequency reversal operation at $I_g^* = 20$ A. (a) Extrapolated reference and actual inverter ac currents. (b) Phase-q FC voltages, inverter line–line voltage, and the CMV.

and it is reduced to 2.06 at $I_g^* = 25$ A. Following Ohm's law, the inverter ac voltage magnitude increases with the rise in I_g^* as shown in Fig. 5(b). The inverter ac voltage has a total harmonic distortion (THD) of 76.2% at $I_g^* = 15$ A and 29.09% at $I_g^* = 25$ A. The FCs voltage is perfectly regulated at 70 V each, irrespective of I_g^* as depicted in Fig. 5(b). With the proposed FCS-MPC, the FLI produces a CMV of 24.92 V at $I_g^* = 15$ A and 24.56 V at $I_g^* = 25$ A.

Similarly, the test results of the proposed FCS-MPC with the reversal of f_g^* from +20 Hz to −20 Hz and from −20 Hz to +20 Hz at $I_g^* = 20$ A are depicted in Fig. 6. Irrespective of the f_g^*, the reference and actual inverter ac currents closely follow each other as depicted in Fig. 6(a), and they have a $\%\text{TDD}_i$ of 2.53. The inverter produces a voltage waveform equivalent to a five-level operation as shown in Fig. 6(b), and it has a THD of 53.58%. During this process, the phase-q FCs voltage is perfectly regulated at an average voltage of 70 V each, as depicted in Fig. 6(b), while producing a CMV of 33.08 V. Overall, the test results are testimony to the proposed FCS-MPC method's superiority in regulating the inverter ac currents and FCs voltage objectives of each phase in an FLI, while minimizing the CMV without using a cost function.

B. Performance Comparison With the Existing FCS-MPC Methods

The superiority of the proposed low-complexity FCS-MPC is further demonstrated through a comprehensive comparison with the existing FCS-MPC-I [8] and FCS-MPC-II methods [10]. In these methods, the CMV is minimized by using a cost function given in (16), along with other control objectives. Fig. 7 shows the performance comparison of the proposed and existing FCS-MPC methods at $I_g^* = 10$ A and $f_g^* = 60$ Hz. Irrespective of the FCS-MPC methods, the actual inverter ac currents closely follow the reference inverter ac currents as depicted in Fig. 7(a-i), (b-i), and (c-i). However, the FCS-MPC-I and FCS-MPC-II produce a $\%\text{TDD}_i$ of 1.8 and 1.91, respectively, whereas the proposed FCS-MPC produces a $\%\text{TDD}_i$ of 1.92. Even though the proposed FCS-MPC has a slightly higher $\%\text{TDD}_i$ at low I_g^* values, it has a low $\%\text{TDD}_i$ at higher I_g^* values when compared with the existing FCS-MPC-I and FCS-MPC-II methods, as depicted in Fig. 8(a). On the other hand, the FCS-MPC-I and FCS-MPC-II produce a voltage THD of 69.23% and 70.33%, respectively, whereas the voltage THD with the proposed FCS-MPC is around 80.62% at $I_g^* = 10$ A. Moreover, the FLI operates at an average switching frequency of 643 Hz and 525 Hz with the FCS-MPC-I and FCS-MPC-II, respectively. On the other hand, the proposed FCS-MPC produces an average switching frequency of 725 Hz at $I_g^* = 10$ A and $f_g^* = 60$ Hz.

The phase-q FCs voltage controllability with the existing and the proposed FCS-MPC methods are depicted in Fig. 7(a-ii), (b-ii), and (c-ii). The FCS-MPC-I method balances the FCs voltage, but their average values are not exactly equal to the rated value of 70 V, as depicted in Fig. 7(a-ii). On the other hand, the FCS-MPC-II and the proposed FCS-MPC methods perfectly regulate each FC voltage at their nominal value of 70 V as depicted in Fig. 7(b-ii) and (c-ii), respectively. These results prove that the use of Heun's integration method in the

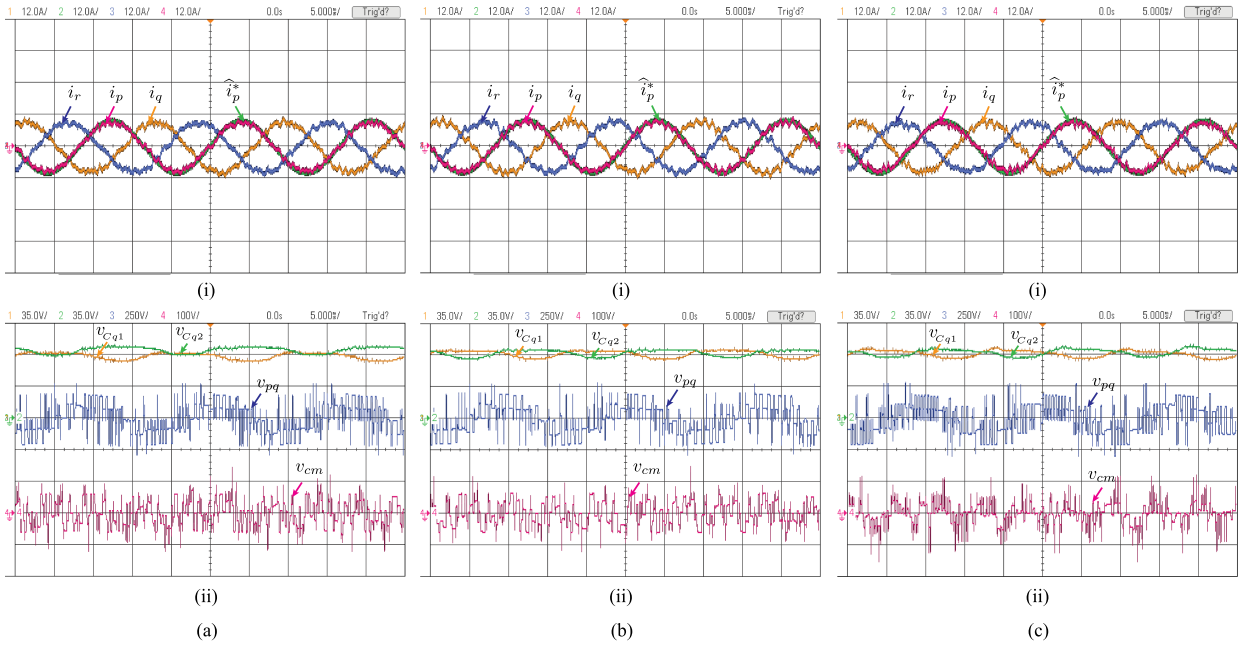

Fig. 7. Performance comparison with the existing FCS-MPC methods (with CMV minimization) at $I_g^* = 10$ A and $f_g^* = 60$ Hz: (i) Extrapolated reference and actual inverter ac currents, and (ii) Phase-q FC voltages, inverter line–line voltage, and the CMV. (a) FCS-MPC-I. (b) FCS-MPC-II. (c) Proposed FCS-MPC.

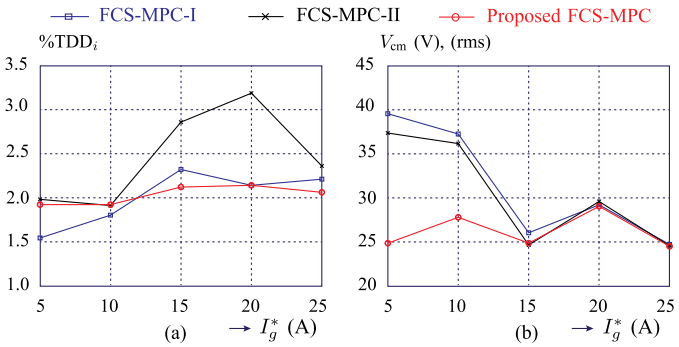

Fig. 8. Experimental performance analysis. (a) TDD of current (%TDD$_i$). (b) Inverter CMV (V_{cm} (rms)).

implementation of FCS-MPC methods (FCS-MPC-II and the proposed FCS-MPC) significantly improves the FCs voltage controllability in comparison to the forward Euler method-based FCS-MPC (FCS-MPC-I). In addition, in FCS-MPC-I and FCS-MPC-II methods, the weighting factors are designed to produce the same CMV peaks when compared with the proposed FCS-MPC as depicted in Fig. 7(a-ii), (b-ii), and (c-ii), but their rms values of CMV differ from each other. The FCS-MPC-I and FCS-MPC-II produce a CMV of 37.26 V and 36.18 V, respectively, whereas the proposed FCS-MPC produces a CMV of 27.84 V, as shown in Fig. 8(b). Moreover, the CMV of an FLI with the proposed FCS-MPC is less than the existing FCS-MPC methods, irrespective of the I_g^* values, as depicted in Fig. 8(b). These results also prove that the CMV minimization with the proposed FCS-MPC is highly effective in comparison with the existing FCS-MPC methods, which use a cost function with weighting factors.

TABLE III
COMPUTATIONAL BURDEN COMPARISON

MPC method	Maximum number of predictions	Minimum execution time
FCS-MPC-I [8]	$6^3 = 216$	68 μs
FCS-MPC-II [10]	$6^3 = 216$*	115 μs
Proposed FCS-MPC	$3 \times 6 = 18$	14 μs

* Twice the number of calculations are involved

C. Computational Burden

In the experimental studies, the dSPACE-DS1103 control platform is utilized to implement both the existing and the proposed FCS-MPC algorithms. They need a minimum sampling time referred to as a computational burden, to execute all tasks, including the sampling and conversion process of analog-to-digital signals, predictive algorithm execution, and gating signal generation without task overrun error in the dSPACE control platform. Table III shows the comparison of the computational burden between the existing and the proposed FCS-MPC methods. It shows the FCS-MPC-I and FCS-MPC-II methods involve the same number of predictions of 216, but they need different minimum sampling times of 68 μs and 115 μs, respectively, to complete all tasks. The increased sampling time in FCS-MPC-II is mainly due to the additional computations of the corrector stage in Heun's integration method-based prediction process when compared with the FCS-MPC-I that involves only predictor stage calculations due to the Euler integration method-based prediction process. On the other hand, the proposed FCS-MPC involves only 6 predictions per phase and a total of 18 predictions in a three-phase FLI as given in Table III. It takes a minimum sampling time of 14 μs to complete all tasks in dSPACE-DS1103

TABLE IV
COMPARISON SUMMARY OF FCS-MPC METHODS

Characteristics	FCS-MPC-I [8]	FCS-MPC-II [10]	Proposed FCS-MPC
Implementation philosophy	Three phase	Three phase	Per-phase
Discretization method	Forward Euler	Heun's	Heun's
Cost function for CMV minimization	Required	Required	Not required
CMV magnitude	High	Medium	Low
Computational burden	Medium (68 μs)	High (115 μs)	Low (14 μs)
Current TDD	Medium (for high I_g^*) Low (for low I_g^*)	High (for all I_g^*)	Low (for high I_g^*) Medium (for low I_g^*)
FC voltage controllability	Poor	Excellent	Excellent

without task overrun error. These results prove that the proposed FCS-MPC's computational burden is relatively low, which is 79.41% and 87.83% less in comparison to the FCS-MPC-I and FCS-MPC-II methods, respectively.

D. Summary of the Relative Comparison

A summary of the comparison between the existing and the proposed FCS-MPC methods is described in Table IV. The three-phase philosophy is adopted in the implementation of both FCS-MPC-I and FCS-MPC-II methods, but they use Euler and Heun's integration methods, respectively, in the prediction process of control variables. Additionally, they need a cost function to minimize the CMV, but the inverter CMV magnitude is high with the FCS-MPC-I and medium with the FCS-MPC-II when compared with the proposed FCS-MPC. On the other hand, the per-phase philosophy is adopted in the implementation of the proposed FCS-MPC, and it uses discrete-time models based on Heun's integration method in the prediction process of control variables. Also, it does not require a cost function to minimize the CMV and produces the lowest CMV magnitude as described in Table IV. Furthermore, the proposed FCS-MPC has a low computational burden in comparison to the existing methods. Moreover, the proposed FCS-MPC has a low current TDD at high I_g^* and a medium current TDD at low I_g^* values when compared with the existing FCS-MPC methods, as depicted in Table IV. In addition, the proposed FCS-MPC and FCS-MPC-II have excellent FCs voltage controllability due to the use of Heun's integration method in the prediction process.

V. CONCLUSION

In this article, a low-complexity Heun's method-based FCS-MPC is proposed for an FLI. The proposed method is highly effective in handling each phase control objectives of an FLI, independently, resulting in a significant reduction in the computational burden. Moreover, Heun's integration method is adopted to develop the discrete-time models of an FLI for the real-time implementation of the proposed method. Additionally, it does not require a cost function to minimize the CMV in comparison to the existing FCS-MPC methods. The proposed FCS-MPC method's superiority is demonstrated through several test cases on a dSPACE-DS1103 controlled laboratory prototype. The test results confirm that the FLI ac currents and FCs voltage are perfectly regulated as per their reference commands. Also, a comprehensive comparative study of the existing and the proposed FCS-MPC methods is presented. The results prove that the proposed FCS-MPC produces the lowest CMV without using a cost function and has shown an excellent controllability of the FCs voltage, along with a low TDD in the inverter ac currents. In addition, the computational burden of the proposed FCS-MPC is 79.41% and 87.83% lesser in comparison to the FCS-MPC-I and FCS-MPC-II methods, respectively. Overall, the proposed FCS-MPC is highly suitable for multiphase MLI-fed EDS applications due to its ability to handle each phase control objective independently and to minimize the CMV without using a cost function.

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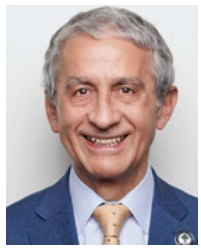

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