Design of 30 A Load Current and 93% Peak Efficiency for Active Clamping Forward Converter With Complete Protection

Tianyuan Tang, Ping Luo, *Member, IEEE*, Zhuangzhuang Wang, Chengxin Li, and Bo Zhang, *Senior Member, IEEE*

***Abstract*—A chip-level design of 30 A load current and 93% peak efficiency for active clamping forward (ACF) converter is presented in this paper to improve the system performance and compactness for all load range and different input voltages. The topology of the low side ACF and self-driven synchronous rectification is adapted to low output voltage and large load current applications. A homologous IC controller with proposed technique of adaptive maximum duty cycle, slope compensation, and optional driver logic is designed. The IC controller is turned into different working states to cooperate different states of the system and functions for complete protection of overcurrent protection, over temperature protection, under voltage lockout, and soft shutdown. The controller chip is fabricated in 0.18 μm BCD process. The experiment results show that 30 A full load current with a compact volume of 39 cm^3 and complete protection has been realized. The overshoot and undershoot of transient response are less than 200 mV at 5 A–25 A within 120 μs and the peak efficiency of 93.0% is achieved.**

***Index Terms*—Active clamp forward (ACF) converter, adaptive maximum duty cycle, chip-level design, complete protection, self-driven synchronous rectification.**

I. Introduction

NOWADAYS the forward converter has been widely used in medium power supply applications, such as server power, photovoltaic, communication base station because of its simplicity, and natural galvanic isolation [1], [2], [3], [4], [5]. Especially when the technologies and concept of GPT, 6G, big data come along, power supply is moving towards miniaturization, and high-power density [6], [7], [8]. Traditional topology of the forward converter is the derivation of buck system, which includes the transformer, the power switch of primary side, and buck in the secondary side. Since the transformer needs to be reset, some demagnetizing techniques has been put forward in [9], [10], [11], and [12]. Conventional methods including RCD clamping and *LC* resonant need to be traded OFF among efficiency, volume, and voltage spikes. The technique of active clamp has been universally used in isolated power supply such as flyback and forward converter due to its high performance [13]. A typical application topology of active clamp forward converter is shown in Fig. 1. The active clamp technique makes the main power switch M_A and active clamping forward (ACF) switch M_B operate in zero voltage switch (ZVS) to reduce the switching loss and voltage spike [14]. The ACF switch in the low side of Fig. 1 can also be substituted by ACF switch in the high side, but an additional bootstrap circuit is required [15].

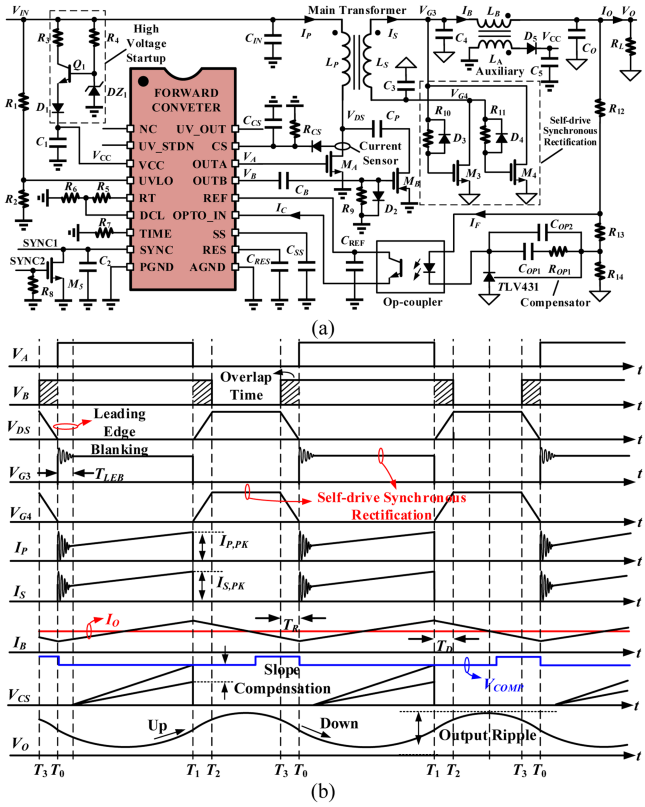


Fig. 1. (a) Block diagram of adopted ACF converter. (b) Key waveforms of ACF converter during the whole period in CCM.

Manuscript received 19 June 2023; revised 28 August 2023 and 26 October 2023; accepted 12 November 2023. Date of publication 21 November 2023; date of current version 26 January 2024. Recommended for publication by Associate Editor X. Ruan. *(Corresponding author: Ping Luo.)*

The authors are with the State Key Laboratory of Electronic Thin Film and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 611731, China (e-mail: tangtianyuan12@gmail.com; pingl@uestc.edu.cn; wang_z_z@126.com; hitlichengxin@163.com; zhangbo@uestc.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2023.3335113.

Digital Object Identifier 10.1109/TPEL.2023.3335113

Meanwhile, the rectifier circuit of the secondary side is similar to a buck converter. Considering the reverse recovery current and voltage drop of free-wheeling diode, great power loss cannot be ignored.

In previous work, some topologies have been put forward to solve the problems mentioned previously. The topology of three port forward converter has been proposed in [1], which has good bidirectional power flow characteristics. But extra diode and switch is needed, which means large volume and power loss. In [2], a self-driven of two-switch forward has been put forward to reset the transformer. However, a bootstrap driver is needed for the switch in the high side. Other improved techniques of active clamp are proposed in [16], [17], [18], and [19] and good performance for efficiency has been realized at the expense of volume or voltage spike. For the secondary side, the lossless-snubber has been proposed in [20] instead of free-wheeling diode. But the voltage drop and heat generation of diode cannot be avoided in large current applications. In [21], a novel resonant forward converter has been proposed and the number of secondary diodes has been reduced by one. However, the output inductor has been transferred to the primary side, which increases the complexity of the design. To sum up, the previous works focus on the topology of system and the efficiency has been well optimized. But some issues have not been mentioned or solved in those work.

1) The first issue is the generation of the driver circuits for all switches. Although the digital PWM controller has been realized in [22], additional circuits with huge volumes such as microcontrollers and PFGAs are needed, which is unrealistic in real application.
2) The second issue is the startup for high input voltage. The range of the input voltage for forward converter can vary from tens to hundreds of volts [23]. However, the driving level of the power transistor is generally within the range of 5–30 V. Meanwhile, the voltage spikes and switching stress of power transistor during the high voltage startup is of great significance in forward converter because breakdown often occurs during the startup period.
3) The third issue is the transient response of the forward converter. There will be large delay in closed-loop and bad transient response if the part of control circuits and part of the system circuits are separated.
4) The fourth issue is the protection in forward converter such as undervoltage lockout (UVLO), over temperature protection (OTP), and over current protection (OCP). These protections have not been introduced in previous work. All the issues mentioned previously can be solved in chip-level design proposed in this article.

The rest of this article is organized as follows. The operation principle of the proposed ACF converter is analyzed in Section II. The design and implementation of the proposed ACF converter are introduced and analyzed in detail in Section III. The analytical modeling and parameter design are built in Section IV. Verification and experimental results are presented in Section V to show the great feasibility and performance of the proposed forward converter. Finally, Section VI concludes this article.

II. Operation Principle of the Proposed Active Clamp Forward Converter

A. Architecture of Proposed Converter

The adopted ACF converter and the homologous key waveforms are shown in Fig. 1 Considering the specification and simplicity of the system, a low side active clamp with p-type MOSFET is adopted. Besides, the topology of secondary side is selected as the self-driven synchronous rectification because of the application of low output voltage and large load current [24]. Furthermore, an essential high voltage startup circuit is designed to provide a rough level of V_{CC} when the whole system and its controller IC are in the startup period. In order to improve the efficiency of the converter, the high voltage startup circuit is substituted by auxiliary winding when the output voltage is set up. An op-coupler and voltage regulator of T_{LV431} are used in the feedback loop to regulate the output voltage. The type-II compensator is adapted to the closed-loop and peripheral components of the IC controller are shown in Fig. 1.

B. Operational Principle for ACF Converter

According to the topology of the adopted ACF converter, the whole process can be divided into four periods. The waveforms and operation states are shown in Figs. 1 and 2, respectively.

Period 1($T_0 < t < T_1$): In Fig. 2(a), M_A is turned ON and M_B is turned OFF. During this interval, the current of primary winding is increasing linearly. Ignoring the conduction resistance of M_A, the voltage of V_{DS} is nearly zero. Simultaneously, the voltage of V_{GS3} is increasing through the transformer and can be derived as

$$V_{GS3} = V_{IN} N_{SP} \tag{1}$$

where N_{SP} is the turn ratio of the transformer. And M_3 is turned ON and the current transferred from primary winding to second winding flows into the output terminal. Ignoring the conduction resistance of M_3, the voltage of V_{G4} is nearly zero. In the first beginning of this period, a large current spike will occur because of the coupling of the parasitic capacitors [25]. Therefore, a homologous leading-edge blanking (LEB) circuit is needed to avoid false trigger under peak current mode control.

Period 2($T_1 < t < T_2$): In Fig. 2(b), M_A and M_B are both turned OFF. Considering the continuity of the inductive current, the magnetizing inductance of primary winding L_P and leakage conductance resonate continuingly with clamp capacitor C_P. According to the volt second equilibrium theorem, it can be obtained in CCM

$$V_{IN} \times T_{\mathrm{ON}} = (V_{DS} - V_{IN}) \times T_{\mathrm{OFF}} \tag{2}$$

where T_{ON} is the turn-ON time and T_{OFF} is the turn-OFF time. In order to obtain a more intuitive expression, another expression can be obtained through the volt second equilibrium theorem of output inductor

$$(V_{IN} N_{SP} - V_O)\, T_{\mathrm{ON}} = V_O T_{\mathrm{OFF}}. \tag{3}$$

By simplifying the abovementioned two expressions, it can be obtained as

$$\begin{cases} V_O = V_{IN} N_{SP} D \\ V_{DS} = \frac{V_{IN}}{1-D} \end{cases} \tag{4}$$

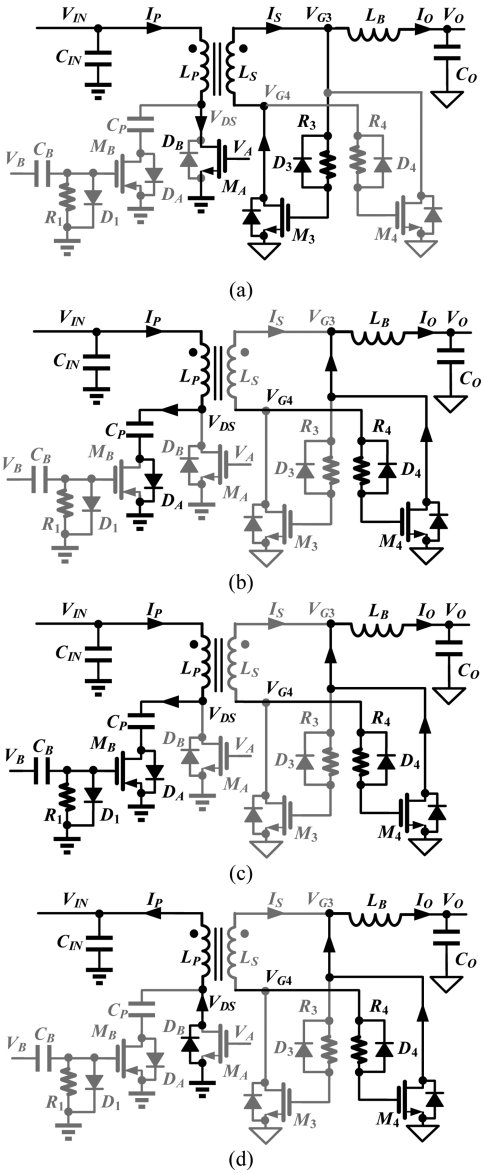


Fig. 2. Operating circuits of the adopted converter for each operational mode. (a) Mode 1(T_0-T_1). (b) Mode 2(T_1-T_2). (c) Mode 3(T_2-T_3). (d) Mode 4(T_3-T_0).

where D is the duty cycle. Meanwhile, with the voltage of V_{DS} increasing to V_{IN}/(1-D), the voltage of V_{G4} is increasing as well and it can be derived as [26]

$$V_{G4} = \frac{DV_{IN}N_{SP}}{1-D}. \tag{5}$$

M_4 is turned ON and M_3 is turned OFF. The current of output inductance L_B begins to continue flowing through M_4.

Period 3($T_2 < t < T_3$): In Fig. 2(c), M_A is turned OFF and M_B is turned ON. Due to the continuity of the capacitive voltage, the lower plate of C_P capacitor is pulled down to 0 V to avoid high voltage spikes. Therefore, the peak voltage of V_{DS} is no longer increasing and M_A will not be breakdown. Considering the driving method of p-type MOSFET, the voltage of the gate must be negative [27] when M_B is turned ON and the capacitive driving method is adopted.

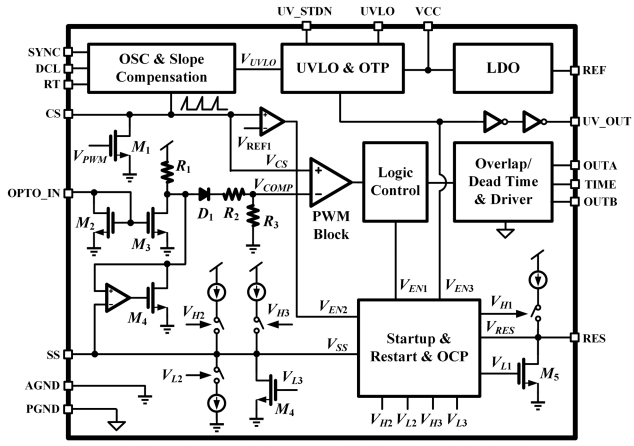


Fig. 3. Block diagram of IC controller for the proposed ACF converter.

Period 4($T_3 < t < T_0$): In Fig. 2(d), M_A and M_B are both turned OFF. As for the transformer has been reset, the voltage of V_{DS} starts to decrease. Due to the continuity of the capacitive voltage, the lower plate of C_P also decreases into negative level.

When Period 4 ends, the adopted converter operation returns to Period 1 to begin the next switching cycle. In order to prevent two power transistors M_A and M_B from being directly connected when they are alternately turned ON, Period 2 and Period 4 cannot be removed. When voltage of V_{G3} and V_{G4} flip from low to high or flop from high to low, there is a significant power loss during the overlap time because the conduction resistance is quite large comparing with complete conduction. An adaptive overlap time will be introduced in Section III to overcome this problem.

To realize the operations mentioned previously, a dedicated IC controller is needed for all the periods. The block diagram of IC controller for the adopted ACF converter is shown in Fig. 3. The block of OSC and slope compensation provides accurate frequency of clock signal and the slope compensation when the duty cycle is larger than 50% in CCM mode. The block of UVLO and OTP provides the function of under voltage lockout and overtemperature protection. The block of LDO provides the stable internal power rails. The block of overlap/dead time and driver provides the function of adaptive time and phase mismatch of driving signal. The block of startup, restart and OCP provides the function of soft startup and restart when the system is overcurrent. Other detail blocks and circuits will be illustrated in Section III.

III. Design and Implementation of the Proposed ACF Converter

A. Working State of Proposed ACF Converter

In order to cooperate with the operation of ACF converter system, there are five working states of the IC controller, which are respectively shown in Table I. And these working states are controlled by the signals of V_{H1}–V_{H3} and V_{L1}–V_{L3}. When the ACF converter turns into any abnormal states, it can be detected through the branch current or node voltage by the IC controller. Then, a series of actions will be done to avoid any damage or make the system go back into normal state. In the process of

TABLE I
STATE AND LOGIC OF CONTROL SIGNAL

Signal	State-1	State-2	State-3	State-4	State-5
V_{H1}	1	1	0/1	0→1	1
V_{L1}	1	1	0/1	0→1	1
V_{H2}	0	1	0	0→1	1
V_{L2}	0	0	0	0	1
V_{H3}	1	0	1	1→0	1
V_{L3}	0	0	0	0→1	0
Working State	Normal Operation	Slow Startup	Fast Startup	Over current	UVLO/ OTP

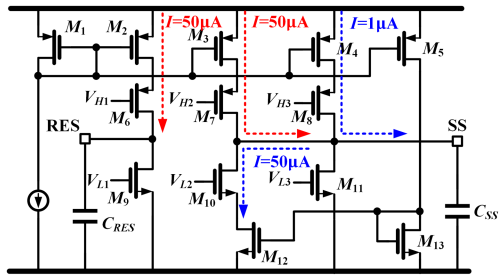


Fig. 4. Proposed circuits of startup and restart controller.

TABLE II
CLARIFICATION FOR ENABLE SIGNAL

Signal	Function
V_{EN1}	The enable signal of maximum duty and low level represents MOSFET turns OFF
V_{EN2}	The enable signal of counter for overcurrent state and high level represents adding one
V_{EN3}	The enable signal of under voltage or over temperature and low level represents MOSFET turns OFF

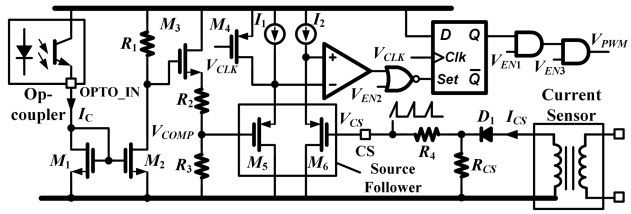


Fig. 5. Proposed circuits of PWM Block.

adjustment, the system will turn into the period of startup or restart. And the proposed circuits of startup and restart controller are shown in Fig. 4. The sink or source current is controlled by the six control signals and the magnitude of the current will be determined under different states. Meanwhile, the capacitors of C_{RES} and C_{SS} are OFF-chip, which can be changed easily. And the time of startup and restart are programmable to meet different practical applications. Besides these six control signals, there are three enable signals to assist the operation of the all the states. In Table II, three enable signals and their functions are demonstrated in detail. In Fig. 5, the proposed circuits of PWM block are shown in detail. The feedback current containing the information of output voltage is copied by the current mirror

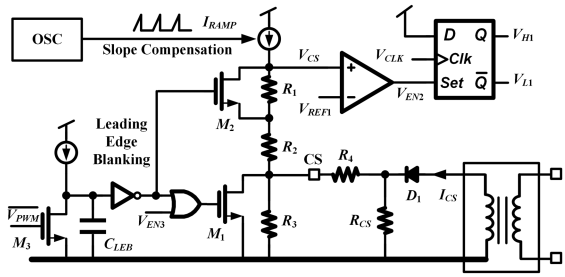


Fig. 6. Proposed circuits of LEB and counter for overcurrent.

first. Then, it is transformed into voltage and divided into low voltage level to satisfy the common mode input voltage of the comparator. On the other side, the current of the primary winding is sensed by the current sensor and it is also transformed into voltage. Meanwhile, an extra current of slope compensation is added in the node of CS. Among these, it is of great significance that the source follower must be designed to be completely consistent. Finally, the signal of PWM is determined by several logic gates and three enable signals. Under the peak current mode control, it is crucial to sample the peak current in every cycle, but some current spike interference shown in Fig. 1 cannot be eliminated. The dedicated circuits of LEB and counter for overcurrent are designed in Fig. 6. M_3 is turned ON by the opposite phase signal of V_{PWM}. When the main power switch M_A is turned ON, the C_{LEB} is charged to high slowly. The time delay is generated by the voltage of C_{LEB}. M_1 and M_2 will not be turned OFF until the voltage of C_{LEB} flip to high level. To avoid the subharmonic oscillations when the duty cycle is greater than 50% in peak current mode, the reasonable slope compensation is need to add into the voltage of V_{CS}. Then, the signal V_{CS} is compared with a designed voltage reference V_{REF1}. When the voltage of V_{CS} is larger than the voltage of V_{REF1}, the control signal V_{H1} and V_{L1} start to flip and flop to make the capacitor C_{RES} charged. Besides, the slope of slope compensation can be changed by adjusting the resistance of R_4 (see Fig. 6) and R_2 (see Fig. 6) provides an offset voltage for the comparator shown in Fig. 5 when both V_{COMP} and V_{CS} are zero. When the system is under voltage or over temperature, the enable signal V_{EN3} is turned to high level and pull the voltage of V_{CS} to zero to avoid mis-operation.

B. Complete Protection and Soft Shut Down Circuit

When the system is abnormal and out of work, it is very crucial that the controller takes the corresponding measures. The detail working waveforms of the controller is shown in Fig. 7. When the system is powered on, the capacitor C_{SS} is charged by 50 μA current and the voltage level of V_{CS} is sampled every cycle. V_{COMP} is clamped by V_{SS}, which is shown in Fig. 3 at the first beginning to generate a series of narrow pulse. When V_{SS} achieves to a certain voltage, V_{COMP} is pulled down by the feedback voltage and the loop control starts to work. When the load current is larger than the preset, the current of the primary winding will be increased as well, which is sampled by the current sensor. And the peak voltage of V_{CS} is larger

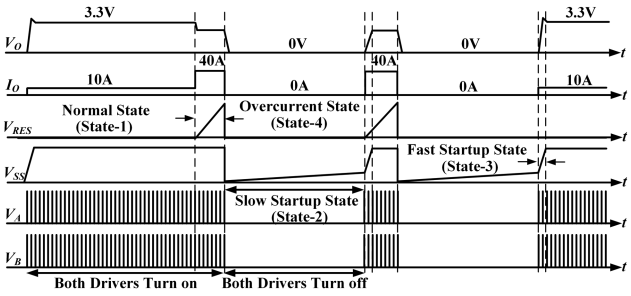


Fig. 7. Key waveforms of the working states for the controller.

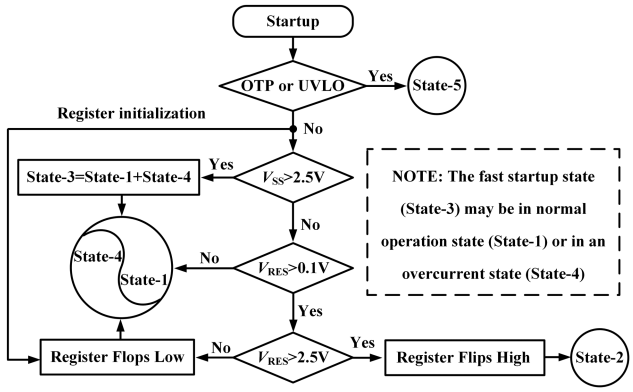


Fig. 8. Flow chart for judging the working state of ACF converter.

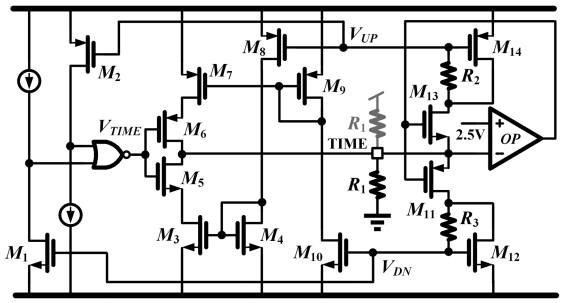


Fig. 9. Proposed circuits of driver current bias and logic.

than V_{REF1}, which makes M_6 (see Fig. 4) turned ON and M_9 (see Fig. 4) turned OFF. The OFF-chip capacitor C_{RES} starts to be charged in 50 μA current and V_{RES} keeps increasing. When V_{RES} is larger than 2.5 V, V_{SS} is discharged fast to zero, and V_{COMP} is clamped again. Meanwhile, V_{RES} is reset to zero and C_{SS} is charged in 1 μA current very slowly. The controller starts to work in the slow startup state and both drivers are turned off during this period. When V_{SS} is larger than 2.5 V, C_{SS} is turned to be charged in 50 μA current and all the signals restore to normal level. But if the system is over current and the peak voltage of V_{CS} is still larger than V_{REF1}, the C_{RES} is charged and keeps increasing. The working state returns into overcurrent state. It should be noted that the fast startup state may be in normal operation state or in an overcurrent state because the state of overcurrent must hold on for some time to avoid false trigger. Besides, it should be also noted that when the system is first powered ON, the charging current is 50 μA instead of 1 μA. Hence, the slow startup state after overcurrent is quite different from the normal startup. To sum up, the action of overcurrent is detected for duration. But the abnormal state of UVLO and OTP occur in an instant. There will be unpredictable large EMI when reducing the 30 A current to 0 suddenly. Besides, if M_A and M_B are turned OFF suddenly in the working process, the high power of output terminal may cause significant resonate between output inductor and output capacitor, which will make the IC controller breakdown through the auxiliary winding. A soft shut down technique is proposed to solve this problem. As shown in Fig. 4, the control signal V_{L2} makes the voltage of V_{SS} discharged in 50 μA. Besides, V_{COMP} is clamped by V_{SS} when V_{SS} decrease to make the conduction time shorter and shorter until the system is completely shut down. The flow chart for judging the working state of ACF converter is shown in Fig. 8. To realize the difference between restart after overcurrent and normal startup, the register is needed in the framework. Besides, the specific values of the time for slow and fast startup can be programmable by changing the capacitance of C_S and C_{RES}.

C. High/Low Side Optional Design of Driver Logic Circuit

In order to adapt to more application scenarios and needs, a high or low side optional design of driver is proposed in this section. The proposed circuits of driver current bias and logic is shown in Fig. 9. The optional resistor R_1 can be connected to the power or the ground for high side or low side ACF, respectively. The current is sampled by the operational amplifier and source follower. Taking the low side control for example and R_1 is connected to the ground. The negative input of the amplifier is clamped in 2.5 V so that M_{13} is turned ON and M_{11} is turned OFF. The lower current mirror is out of work, thus making the inputs of NOR gate turned to be one high level and one low level. Then, V_{TIME} is turned to be low level. On the contrary, M_{13} is turned OFF and M_{11} is turned ON when R_1 is connected to the power. And the upper current mirror is out of work, thus making the inputs of NOR gate turned to be both low level. Then, V_{TIME} is turned to be high level. Meanwhile the current bias can be determined by the resistance of R_1 which is OFF-chip and it can be easily trimmed. The proposed circuits of driver logic and its working waveforms are shown in Fig. 10, respectively. According to the voltage level of V_{TIME}, different charging and discharging schemes and signal paths are chosen. And different waveforms of V_{A1} and V_{B1} are generated by the charging or discharging current. Comparing with 2.5 V, there are four different outputs of V_{D1}–V_{D4}. Finally, the correct driving waveforms for output are selected by the multiplexer. The proposed driver logic circuits have offered an alternative and the overlap/dead time can be changed by the resistor R_{TIME} to realize ZVS control.

D. Maximum Duty and Slope Compensation Circuit

According to the expression (4), the voltage between source and drain of the power transistor is related to the duty cycle and input voltage. When V_{DS} is larger than the preset, the power transistor will be breakdown and it can be even worse because the ON-resistance is nearly zero when transistor is breakdown.

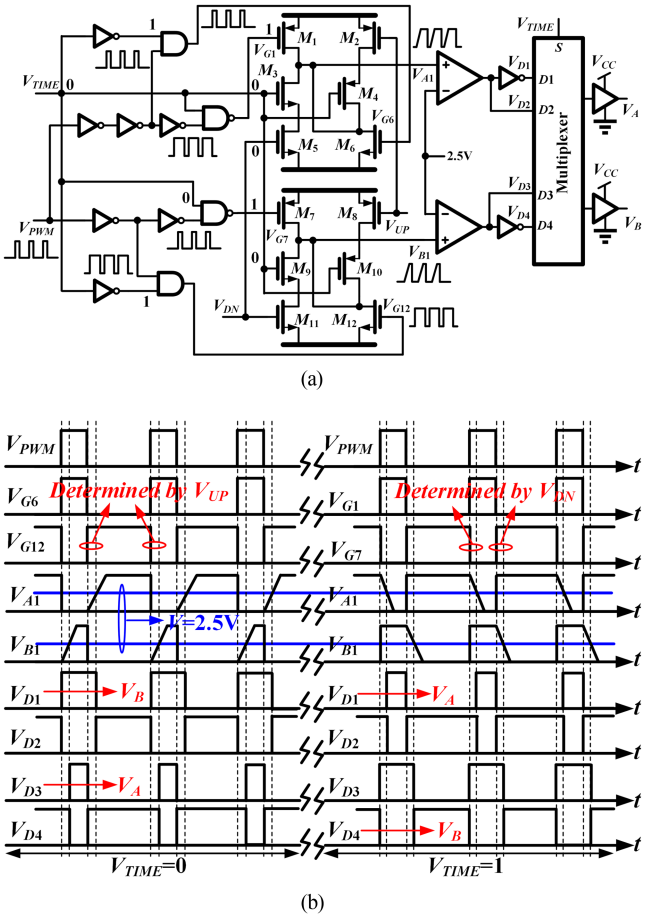


Fig. 10. (a) Proposed circuits of driver logic. (b) Key waveforms of driver logic when signal $V_{\mathrm{TIME}} = 0$.

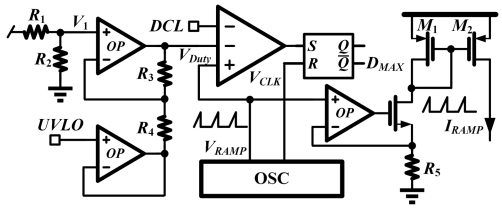


Fig. 11. Proposed circuits of adaptive maximum duty cycle and slope compensation.

Therefore, an appropriate maximum duty cycle circuit must be designed to assure the safety. As it is mentioned in Fig. 6, slope compensation must be required in peak current mode control with a duty cycle greater than 50%. The proposed circuits of adaptive maximum duty cycle and slope compensation are shown in Fig. 11. The voltage of UVLO pin is proportional to the input voltage and two amplifiers are used to generate the voltage of V_{Duty}, which has an inverse relationship with input voltage. Besides, a programmable maximum duty cycle can also be determined by the voltage of DCL for double insurance. Another amplifier is used to generate the ramp wave current to inject the current source shown in Fig. 6.

TABLE III
DESIGN SPECIFICATIONS

Parameter	Symbol	Value
Input voltage	V_{IN}	36–78 V
Output voltage	V_O	3.3 V
Load current	I_O	30 A
Primary winding	L_P	230 μH
Secondary winding	L_S	6.4 μH
Output inductor	L_B	2.2 μH
Output capacitor	C_O	1000 μF
Clamping capacitor	C_P	100 nF
Preset overlap time	T_R	100 ns
Main MOSFET	M_A	NCEP1520 K (V_{DS}=150 V, R_{DS}=65 mΩ, C_{OSS}=75 pF)
ACF MOSFET	M_B	BSP225 (V_{DS}=250 V, R_{DS}=10 Ω)
Synchronous rectifiers	M_3/M_4	AGM403 (V_{DS}=40 V, R_{DS}=3.2 mΩ)
Working frequency	f_{CLK}	230 kHz

IV. Analytical Modeling and Parameter Design

The design specifications of the proposed ACF converter are shown in Table III. Considering the design parameters, some key indicators must be calculated in detail.

According to the expression (4), it can be derived as

$$V_{DS} = \frac{V_O}{(1-D)\,DN_{SP}}. \tag{6}$$

Ignoring the efficiency loss of system, the range of D can be calculated through expression (4)

$$D = \frac{V_O}{V_{IN}N_{SP}} = 25\% - 55\%. \tag{7}$$

Therefore, based on the expression (6), the maximum value of V_{DS} is 105.6 V when $D = 25\%$

$$\begin{cases} V_{GS3,\mathrm{Max}} = V_{IN,\mathrm{Max}}N_{SP} = 13V \\ V_{GS4,\mathrm{Max}} = \frac{V_O}{1-D_{\mathrm{Max}}} = 7.3V \end{cases}. \tag{8}$$

Therefore, the main MOSFET is chosen as V_{DS} = 150 V because of the possible leakage induced voltage spikes. If the withstand voltage of MOSFET is too low, it has the risk of damage and if the withstand voltage of MOSFET is too high, the parasitic capacitance and conduction impedance are too large to lead to low efficiency. As for the synchronous rectifiers, the maximum of V_{GS3} and V_{GS4} can be obtained by expression (1) and (5). So, the MOSFETs of synchronous rectifiers are chosen as V_{DS} = 40 V because of the possible current, voltage spikes and negative voltage. In Fig. 11, V_{Duty} can be derived as

$$V_{\mathrm{Duty}} = \frac{(V_1 - V_{\mathrm{UVLO}})(R_3 + R_4)}{R_4} \tag{9}$$

where V_{UVLO} is proportional to V_{IN} and can be expressed as

$$V_{\mathrm{UVLO}} = k_1 V_{IN}. \tag{10}$$

And the maximum duty cycle can be obtained as

$$D_{\mathrm{Max}} = \frac{(V_1 - k_1 V_{IN})(R_3 + R_4)}{V_2 R_4} \tag{11}$$

where V_2 is the maximum voltage of V_{RAMP} shown in Fig. 11. The parameter k_1, V_1, V_2, R_3, and R_4 are constant so that D_{Max} has a linear inverse relationship with V_{IN}. Considering good performance of transient response for load step, the duty cycle cannot be restricted too small. As for the ZVS control, the principles of when and how ZVS works can be explained by energy conservation and resonant frequency. The detail waveforms of ACF converter are shown in Fig. 12. There are three periods according to the waveforms of V_{DS} and the diagram of energy flow are displayed in Fig. 13.

In the first period, the energy stored in the leakage inductor is transferred into the equivalent output capacitor (C_{OSS}) of M_A. Because both M_A and M_B are turned OFF, the energy cannot be stored in clamping capacitor (C_P). During this period, the frequency of V_{DS} can be derived as

$$f_1 = \frac{1}{2\pi\sqrt{L_K C_{OSS}}}. \tag{12}$$

In the second period, M_B is turned ON and the clamping capacitor C_P is connected to the ground. Then, the excitation inductor L_M, clamping capacitor and equivalent output capacitor starts to resonate. The frequency of V_{DS} can be obtained as

$$f_2 = \frac{1}{2\pi\sqrt{L_M\,(C_{OSS}+C_P)}}. \tag{13}$$

In the third period, M_B is turned OFF and the clamping capacitor (C_P) no longer participates in the resonance so the frequency of V_{DS} can be obtained as

$$f_3 = \frac{1}{2\pi\sqrt{L_M C_{OSS}}}. \tag{14}$$

To realize ZVS of M_A, the overlap time can be calculated as $T_R = 1/(4f_3) = 207.5$ ns, which is greater than the preset of 100 ns. To realize ZVS of M_A, the first method is to increase the overlap time to make M_A turned OFF until V_{DS} resonates near zero. However, this method is not worth because of the self-driven synchronous rectification in the secondary side. The longer overlap time is leading to longer time of the conduction of body diode in the secondary side. As for the 30 A load current, long conduction of body diode for secondary side will lead to low efficiency and poor heat dissipation. The second method is to decrease the conductance of L_M, which means larger current primary side and larger current ripple. This will lead to large conduction losses of primary side and the efficiency may be not increased in ZVS control. The third method is to decrease the equivalent output capacitor of M_A. However, tradeoffs are also needed among the capacitor, the ON-resistance and breakdown voltage. For the ACF MOSFET (M_B), ZVS can be realized easily because the period of f_1 is much smaller than the overlap time, which is shown in Fig. 12.

Besides, limitations shown in Fig. 17 on the extreme ends of the range or specific applications should be taken into consideration.

All these limitations can be divided into two categories for discussion. 1) The first category is the circumstance that input voltage and load current are not in the preset range (marked in red). For example, when the input voltage is higher or lower than the normal range, this voltage can be detected by IC controller. Then, the protection of OVP or UVLO can be triggered and both

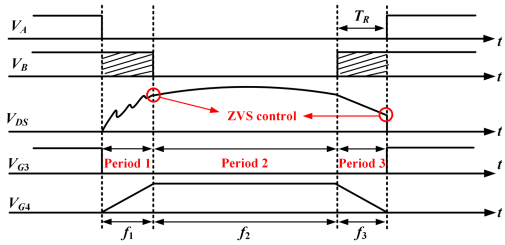


Fig. 12. Detail waveforms of ACF converter.

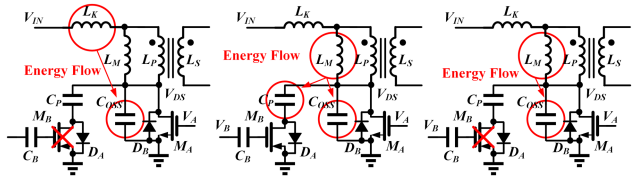


Fig. 13. Energy flow when M_B is turned ON and OFF (period 1 to period 3).

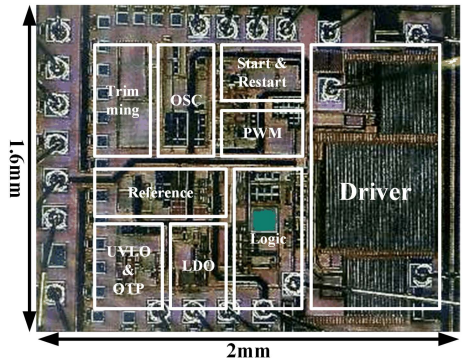


Fig. 14. Photograph of the implemented chip.

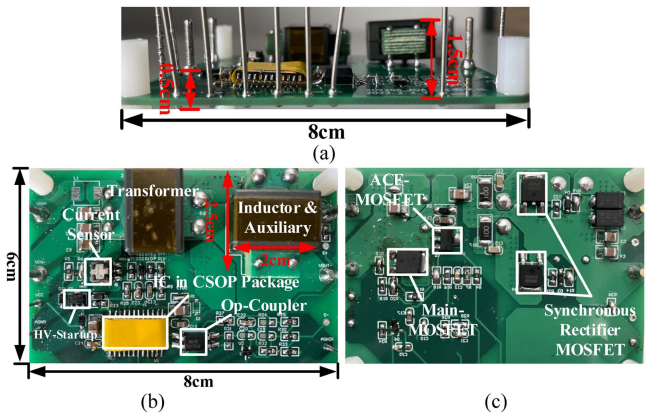


Fig. 15. Photograph of the fabricated PCB. (a) Front view. (b) Vertical view. (c) Bottom view.

the power transistors M_A, M_B will be turned OFF. Therefore, all these protections make the ACF converter system to stop working under abnormal conditions. 2) The second category is the boundary question (marked in blue). When the system works in the boundary state, many extreme problems will be manifested and these problems will be illustrated one by one as follows. When the input voltage is at the high-voltage boundary, the issue about the breakdown of transistors must be considered.

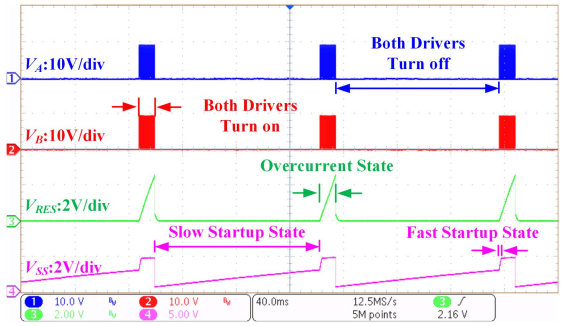


Fig. 16. Measurement waveforms for overcurrent protection and restart of proposed ACF converter.

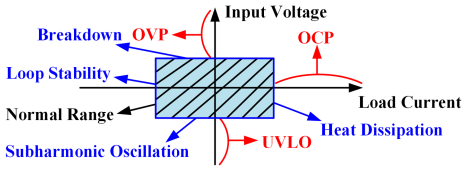


Fig. 17. Limitations shown in the curve of input voltage versus load current.

Thus, the selection of process, parameters about OFF-chip design and component is crucial. When the input voltage is at the low-voltage boundary, the duty cycle will be very large, which is shown in Fig. 23. Large duty cycle will lead to subharmonic oscillation. As a consequence, the slope compensation is needed in IC controller. When the load current is at the large-current boundary, the heat dissipation is a tricky problem. PCB board optimization and additional cooling measures are required. When the load current is at the small-current boundary, large output impedances will result in narrow loop bandwidth, so that the compensator needs to be properly designed.

V. Experimental Results

The proposed ACF converter with completely protection is implemented in the 0.18 μm BCD process. Fig. 14 shows a micrograph of the proposed ACF converter and the area is 1.6 mm $\times$ 2 mm. The view from different angles of the designed PCB is shown in Fig. 15 to evaluate the performance of the proposed ACF converter. And there are some considerations about the layout. For instance, the path from secondary winding to output terminal needs to be covered with a large area of copper to ensure the current capability and heat dissipation. Besides, the path of loop control including the signal of V_{CS}, I_C, I_F, TLV431 and its compensator shown in Fig. 1 in the manuscript needs to be designed as short as possible. The current sensor and op-coupler need to be positioned very close to the IC controller to avoid interference.

Fig. 16 shows the measurement waveforms for overcurrent protection and restart of the proposed ACF converter, which is the same as Fig. 7. When the system is overcurrent, $V_{\rm RES}$ is charged by the sink current. And when $V_{\rm RES}$ is higher than 2.5 V, both V_{SS} and $V_{\rm RES}$ are reset to zero immediately. Then, V_{SS} is charged by a little current first during the slow startup state.

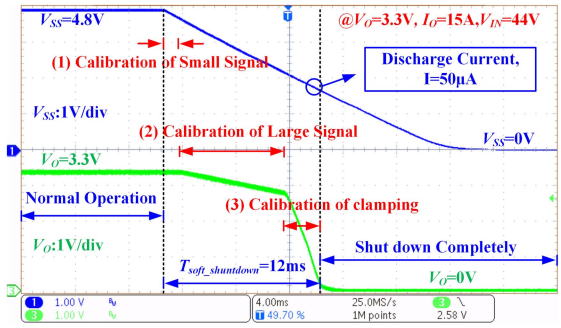


Fig. 18. Measurement waveforms for soft shutdown of proposed ACF converter when system is in an undervoltage state.

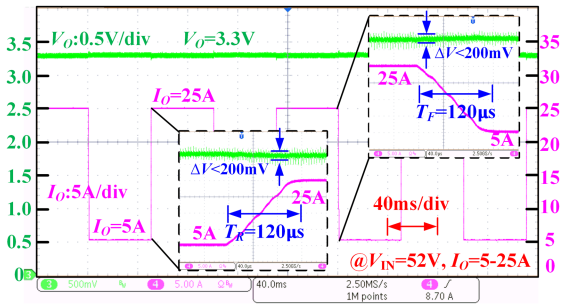


Fig. 19. Measurement waveforms for load step of proposed ACF converter.

When V_{SS} is higher than 2.5 V, it is turned to be charged by a larger current instead of small current and $V_{\rm RES}$ is charged at the same time if the system is overcurrent again. The measurement results show a good performance of overcurrent protection.

Fig. 18 shows the measurement waveforms for the soft shutdown of the proposed ACF converter when system is in an undervoltage state. V_{SS} is discharged with a constant current and output voltage keeps decreasing. And there are three periods during the process. When V_O drops slightly, the loop control is still in the small signal calibration. And then V_O and V_{SS} keeps decreasing but $V_{\rm COMP}$ is still smaller than V_{SS} so that the loop control is in the calibration of large signal. Finally, when $V_{\rm COMP}$ is larger than V_{SS}, $V_{\rm COMP}$ is clamped by V_{SS} and the system is shut down due to the decreasingly smaller duty cycle. The good performance of the function for soft shut down is verified according to measurement results.

Fig. 19 shows the measurement waveforms for load step of the proposed ACF converter. The load current is changed from 5 to 25 A within 120 μs. The overshoot and undershoot are both less than 200 mV and output voltage is very stable at 3.3 V, which demonstrates a good transient response performance and load regulation. The experiment results of ZVS control for ACF converter is shown in Fig. 20 and as is illustrated in Section IV, ZVS control has been realized in ACF MOSFET (M_B) rather than main MOSFET (M_A). To verify the correctness of the derivation, the working waveforms of primary side and secondary side are shown in Fig. 21. When $V_{IN} = 44$ V and $V_O = 3.3$ V, the duty cycle is 45%.

V_A and V_B shown in Fig. 21(a) shows the proper overlap time and the average current of primary winding is 2.5 A when load current is 15 A. The voltage of V_{DS} is 80 V, which is the same

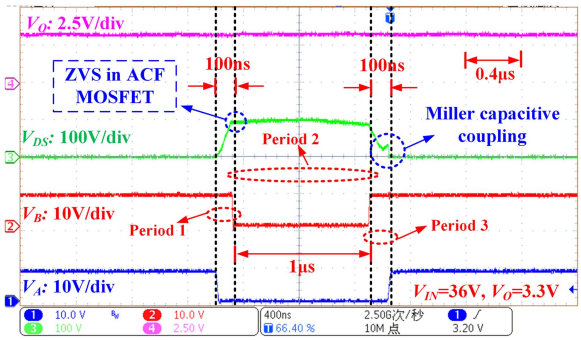


Fig. 20. Experiment results of ZVS control for ACF converter.

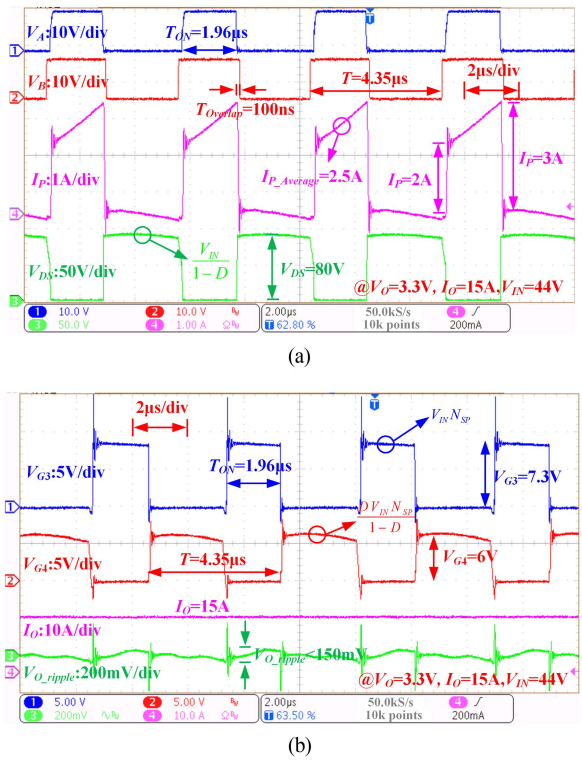


Fig. 21. Measurement waveforms of proposed ACF converter at I_O= 15 A, V_{IN}= 40 V. (a) Waveforms of primary side. (b) Waveforms of secondary side.

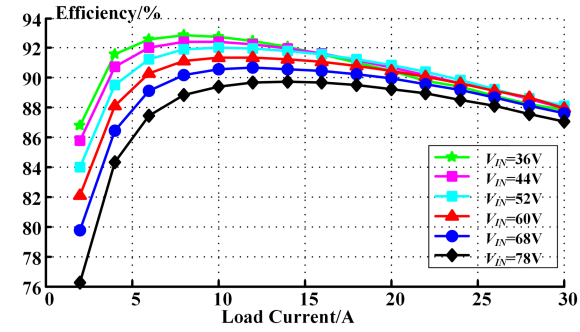


Fig. 22. Measured efficiency versus load current.

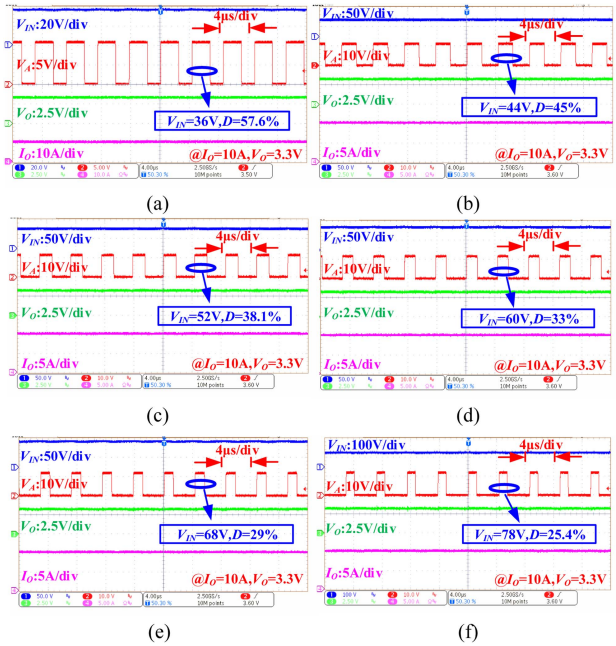


Fig. 23. Measurement waveforms of proposed ACF converter at I_O= 10 A. (a) V_{IN}= 36 V. (b) V_{IN}= 44 V. (c) V_{IN}= 52 V. (d) V_{IN}= 60 V. (e) V_{IN}= 68 V. (f) V_{IN}= 78 V.

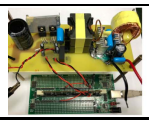
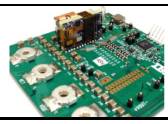
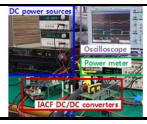
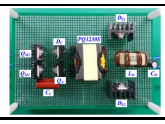
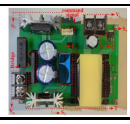
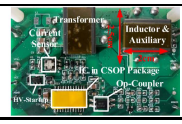
as the expression (6). V_{GS3} and V_{GS4} are shown in Fig. 21(b), which demonstrates the validity of expression (8). Besides, the ripple of the output is 150 mV because of the high working frequency.

The measured efficiency versus load current is shown in Fig. 22. The peak efficiency is 93.0% when V_{IN} = 36 V and I_O = 8 A. And efficiency is larger than 86% when load current is larger than 6 A in all different V_{IN}. As for the light load current, the efficiency is lower because the framework of the secondary side is self-driven synchronous rectifiers. The system may be turned into forced CCM mode and the efficiency is much lower than CCM mode.

Fig. 23 shows the measurement waveforms of proposed ACF converter when I_O = 10 A at different input voltages to verify the rationality of maximum duty cycle. According to the results, it can be concluded that the production of V_{IN} and D is nearly a constant, which can be calculated as (20.736, 19.8, 19.812, 19.8, 19.72, 19.812). Besides, when the system is in the process of very slow startup, the input voltage is changed from low to high level and the V_{SS} level rises faster than the input voltage. According to the expression (4), the circumstance of low input voltage and large conduction time may occur, thus making the voltage of V_{DS} exceeded threshold. The problem can be solved by the circuits of adaptive maximum duty cycle shown in Fig. 11, which is demonstrated in Fig. 23.

Finally, Table IV summarizes the main features of proposed ACF converter in comparison with prior arts. Compared with the previous techniques, the proposed ACF converter provides a chip-level design technique and the four issues mentioned in Section I are all solved perfectly. The whole system is very complete, which including the system and IC controller. The weight and cost can only be determined by three levels (light/medium/heavy) or (low/medium/high) of qualitative analysis according to the system prototype. And the peak efficiency of 93.0% is nearly the same with the previous work. As for

TABLE IV
PROPOSED ACTIVE-CLAMP FORWARD CONVERTER PERFORMANCE COMPARED WITH THE CURRENT STATE-OF-THE-ART

Parameter	TPE 2019 [20]	TPE 2020 [4]	TPE 2020 [3]	TIE 2020 [6]	TIE 2023 [1]	This work
Implementation	System-level	System-level	System-level	System-level	System-level	Chip-level
Technology	/	/	/	/	/	0 18 μm BCD
Chip area (mm^2)	/	/	/	/	/	1.6 mm×2 mm
Total volume (cm^3)	N.A.	4.26(without PCB)	N.A.	47.5+35.5=83	N.A.	24+15=39
Control mode of primary side	ACF in High Side	ACF in Low Side	Interleaved ACF	Double-ended ACF	Three Port	ACF in Low Side
Control mode of secondary side	Diode+Lossless-Snubber	Digital Control+ MOSFET	Digital Control+ MOSFET	Diode	Diode	Self-driven Synchronous Rectification+ MOSFET
Feedback	N.A.	Resister (Nonisolated)	Resister (Nonisolated)	N.A.	N.A.	Op-coupler
Input Voltage(V)	350–400	12/48	36–72	400	10–35 and 45–50	36-78
Output power(W)	480	54	480	400	200	100
Output voltage(V)	48	0.7–1.1	12	12	25/36/48	3.3
Load current(A)	10	60	40	33.33	8/5.6/4.2	30
Turns ratio	62/14	3 or 12	4:2 and 10:2	35:2	2.5	6:1
Output inductor (μH)	213	0.1	10	8	300	2.2
Working frequency (kHz)	65	325	65	75	100	230
Power density (W/cm^3)	/	<12.68	/	4.82	/	2.56
Weight (light/medium/heavy)	heavy	light	heavy	light	medium	light
Cost (low/medium/high)	low	high	high	low	medium	medium
Prototype						
Peak efficiency(%)	94.8%	90.4%	94.5%	92.8%	94.1%	93.0%
Consideration of high voltage startup	N.A.	N.A.	N.A.	N.A.	Self-driven	HV Startup + Auxiliary Winding
Transient response	N.A.	N.A.	N.A.	0.02A/μs 950 mV@3.3–26.6 A	N.A.	0.17 A/μs <200 mV@5–25 A

1. N.A.* stands for not available. 2. Total Volume=PCB Volume + Transformer Volume

the transient response, the proposed ACF converter is much better than the previous work. Because the controller is directly connected in the system by IC controller rather than any other digital or PCBs, the time delay of the whole loop becomes much smaller. The transient ratio is 0.17 A/μs, which is 8.5 times greater than 0.02 A/μs in [6], but the overshoot and undershoot is less than 200 mV, which is much smaller than 950 mV shown in [6]. Besides, a compact volume of 39 cm^3 with high input voltage startup and auxiliary winding power supply has realized reasonable startup and high-power density comparing other works.

VI. CONCLUSION

A chip-level design of the ACF converter with complete protection is proposed and implemented to improve the system performance and compactness for all load range and different input voltages. A 30 A load current with a compact volume of 39 cm^3 has been realized and the peak efficiency is 93.0%. The good performance of transient response for less than 200 mV overshoot and undershoot when the load current is changed from 5 to 25 A within 120 μs has been realized. Through the technique of current sampling and overcurrent counter, the proposed startup and restart controller in the IC design achieves excellent overcurrent protection function. The good stability has been realized by the proposed adaptive maximum duty cycle and slope compensation. With the cooperation with different working states of the system, the IC controller is turned into different working states as well to realize complete protections and all the issues, which are difficult in system-level design mentioned in Section I have been well solved.

REFERENCES

[1] G. Zhou, Q. Tian, and H. Li, "Three-port forward converters with compact structure and extended duty cycle range," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 566–581, Jan. 2023.

[2] H. Bahrami, H. Allahyari, and E. Adib, "A self-driven synchronous rectification ZCS PWM two-switch forward converter with minimum number of components," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 12842–12850, Dec. 2022.

[3] Y. Jeong, J.-D. Park, and G.-W. Moon, "An interleaved active-clamp forward converter modified for reduced primary conduction loss without additional components," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 121–130, Jan. 2020.

[4] X. Zhang, B. Nguyen, A. Ferencz, T. Takken, R. Senger, and P. Coteus, "A 12- or 48-v input, 0.9-v output active-clamp forward converter power block for servers and datacenters," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1721–1731, Feb. 2020.

[5] J.-Y. Lin, P.-J. Liu, and C.-Y. Yang, "A dual-transformer active-clamp forward converter with nonlinear conversion ratio," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4353–4361, Jun. 2016.

[6] M.-H. Kim, S.-H. Lee, B.-S. Lee, J.-Y. Kim, and J.-K. Kim, "Double-ended active-clamp forward converter with low dc offset current of transformer," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1036–1047, Feb. 2020.
[7] H.-S. Youn, J.-I. Baek, and J.-K. Kim, "Interleaved active clamp forward converter with extended operating duty ratio by adopting additional series-connected secondary windings for wide input and high current output applications," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4423–4433, May 2019.
[8] W. Li, L. Fan, Y. Zhao, X. He, D. Xu, and B. Wu, "High-step-up and high-efficiency fuel-cell power generation system with active-clamp flyback–forward converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 599–610, Jan. 2012.
[9] H. Wu and Y. Xing, "Families of forward converters suitable for wide input voltage range applications," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 6006–6017, Nov. 2014.
[10] B.-H. Lee, Y.-D. Kim, M.-Y. Kim, I.-H. Cho, and G.-W. Moon, "Active-clamp forward converter with asymmetric transformer turns for reducing transformer DC offset current," in *Proc. IEEE Ind. Electron. Soc. Conf.*, 2012, pp. 204–209.
[11] P. Kong, S. Wang, F. C. Lee, and Z. Wang, "Reducing common-mode noise in two-switch forward converter," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1522–1533, May 2011.
[12] Q. M. Li, F. C. Lee, and M. M. Jovanovic, "Large-signal transient analysis of forward converter with active-clamp reset," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 15–24, Jan. 2002.
[13] H. Chen, X. Wu, and F. Z. Peng, "Small signal modeling and analysis of interleaved active-clamp forward converter with parallel input and series-parallel output," in *Proc. IEEE Int. Symp. Ind. Electron. Conf.*, 2012, pp. 515–520.
[14] R. Torrico-Bascop and N. Barbi, "A double ZVS-PWM active-clamping forward converter: Analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 16, no. 6, pp. 745–751, Nov. 2001.
[15] B.-S. Lim, H.-J. Kim, and W.-S. Chung, "A self-driven active clamp forward converter using the auxiliary winding of the power transformer," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 51, no. 10, pp. 549–551, Oct. 2004.
[16] T. Qian and B. Lehman, "Dual interleaved active-clamp forward with automatic charge balance regulation for high input voltage application," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 38–44, Jan. 2008.
[17] P. Jang and B.-H. Cho, "Two-switch forward converter with reset winding and an auxiliary active-clamp circuit for a wide input voltage range," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4491–4502, Jun. 2017.
[18] K.-B. Park, G.-W. Moon, and M.-J. Youn, "Two-switch active-clamp forward converter with one clamp diode and delayed turnoff gate signal," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4768–4772, Oct. 2011.
[19] K.-B. Park, C.-E. Kim, G.-W. Moon, and M.-J. Youn, "Three-switch active-clamp forward converter with low switch voltage stress and wide ZVS range for high-input-voltage applications," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 889–898, Apr. 2010.
[20] J.-Y. Lin, S.-Y. Lee, C.-Y. Ting, and F.-C. Syu, "Active-clamp forward converter with lossless-snubber on secondary-side," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7650–7661, Aug. 2019.
[21] W. Qin, N. Yu, Z. Zhou, X. Wu, and J. Zhang, "Active-clamp ZVZCS resonant forward dc transformer (DCX) with load-adaptive on-time control," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10490–10500, Dec. 2018.
[22] W. Fang, X.-D. Liu, and Y.-F. Liu, "A new digital control algorithm for dual-transistor forward converter," *IEEE Trans. Ind. Electron.*, vol. 9, no. 4, pp. 2074–2081, Nov. 2013.
[23] S.-S. Lee, S.-W. Choi, and G.-W. Moon, "High-efficiency active-clamp forward converter with transient current build-up (TCB) ZVS technique," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 310–318, Feb. 2007.
[24] B.-R. Lin, K. Huang, and D. Wang, "Analysis, design, and implementation of an active clamp forward converter with synchronous rectifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 6, pp. 1310–1319, Jun. 2006.
[25] Q. M. Li and F. C. Lee, "Design consideration of the active-clamp forward converter with current mode control during large-signal transient," *IEEE Trans. Power Electron.*, vol. 18, no. 4, pp. 958–965, Jul. 2003.
[26] Y.-K. Lo, T.-S. Kao, and J.-Y. Lin, "Analysis and design of an interleaved active-clamping forward converter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2323–2332, Aug. 2007.
[27] V. Tuomainen and J. Kyyra, "Effect of resonant transition on efficiency of forward converter with active clamp and self-driven SRs," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 315–323, Mar. 2005.

Tianyuan Tang was born in Hubei, China, in 1995. He received the B.S. degree in microelectronics science and engineering from Chongqing University of Posts and Telecommunications, Chongqing, China, in 2018. He is currently working toward the Ph.D. degree in microelectronics science and engineering with the University of Electronic Science and Technology of China, Chengdu, China.

His research interests include analog integrated circuit, dc–dc converter, and isolated power supply.

Ping Luo (Member, IEEE) was born in Xinjiang, China, in 1968. She received the B.S. and M.S. degrees in automation control from Chongqing University, Chongqing, China, in 1990 and 1993, respectively, and the Ph.D. degree in circuit and systems from the University of Electronic Science and Technology of China, Chengdu, China, in 2004.

She is currently a Professor with the University of Electronic Science and Technology of China. Her research interests include dc–dc converter, power management unit, energy harvest IC, and energy management strategies.

Zhuangzhuang Wang was born in Hebei, China, in 1998. He received the B.S. degree in electronics engineering from Hunan University, Changsha, China, in 2022. He is currently working toward the M.S. degree in microelectronics science and engineering with the University of Electronic Science and Technology of China, Chengdu, China.

His research interests include analog integrated circuit and switch power supply.

Chengxin Li was born in Shandong, China, in 2000. He received the B.S. degree in electronics engineering from Harbin Institute of Technology, Weihai, China, in 2022. He is currently working toward the M.S. degree in microelectronics science and engineering with the University of Electronic Science and Technology of China, Chengdu, China.

His research interests include analog integrated circuit and switch power supply.

Bo Zhang (Senior Member, IEEE) received the B.Sc. degree in electronics engineering from the Beijing Institute of Technology, Beijing, China, in 1985, and the M.S. degree in electronics engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 1988.

He is currently a Professor with UESTC. He has authored or coauthored more than 350 publications in peer reviewed journals and international conference. His research interests include power devices and power management technologies.