Constant On/Off-Time Digital Current Control and Design Methods in Three-Level Flying-Capacitor Boost Converters for Fast Transient and Voltage Balancing

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***Abstract*—Constant ON/OFF-time current-mode control (CMC) techniques are useful for wide-duty-ratio operations in multilevel flying-capacitor converters. In this article, event-based constant ON/OFF-time digital CMC architectures are proposed in a three-level flying-capacitor (3L-FC) boost converter, which offers inherent current loop stability, fast transient performance, and active flying-capacitor voltage balancing with stable periodic behavior using one voltage sample per switching cycle. Furthermore, a unified discrete-time (DT) framework is proposed, which is used to derive accurate DT large- and small-signal models. The model accuracy is verified using SIMPLIS switch simulation, and fast-scale stability boundaries are obtained using the root locus plot of the closed-loop poles. A hybrid design approach is presented using continuous-time and DT small-signal models for a balanced tradeoff between simplicity and accuracy. An adaptive ON/OFF-time approach is adopted to regulate the switching frequency and also to retain high load efficiency. A 100-W 12/48-V 3L-FC boost converter prototype is developed in the laboratory. Experimental results are presented to demonstrate superior transient performance with enhanced fast-scale stability boundaries using the proposed architectures.**

***Index Terms*—Adaptive ON-time, boost converter, constant OFF-time, constant ON-time, controller design, current-mode control (CMC), digital control, discrete-time (DT) model, flying capacitor (FC), multilevel, small-signal model, stability analysis.**

I. Introduction

MULTILEVEL flying-capacitor (ML-FC) boost converters remain an attractive solution for high-power-density applications that demand high efficiency at high voltage gain [1], [2], [3], [4], [5], [6]. The use of intermediate flying-capacitor (FC) stages allows reduced device voltage rating, which results in reduced switching loss and smaller output filter size because of a higher effective switching frequency. Thus, for the same ripple specifications, the inductor size in an ML-FC boost converter can be substantially reduced compared to a traditional boost converter. A smaller inductor pushes the right-half-plane (RHP) zero further right side in the complex "s" plane. This results in a higher closed-loop bandwidth (BW) in an ML-FC boost converter; however, there exist many challenges in terms of FC voltage balancing, closed-loop stability, and performance.

Numerous attempts have been made in the past to address some of the above issues [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19]. Phase-shift and phase-disposition pulsewidth modulation techniques were reported in [9] and [10] for FC voltage balancing. However, such open-loop configurations rely on natural balancing, which may not be able to achieve adequate dynamic performance. Voltage-mode control techniques in [12] and [13] attempt to adjust individual duty ratio for balancing the FC voltage; however, such techniques are not sufficient to achieve a higher closed-loop BW in a boost-derived converter, which suffers from the effect due to the RHP zero. A current-mode control (CMC) technique in [14] considers fixed-duty perturbations without using any additional FC voltage balancing loop. However, this technique requires additional circuitry to realize the closed-loop control method, which may introduce other operating modes with increased complexity. A digital current-mode control (DCMC) was applied in a three-level flying-capacitor (3L-FC) buck converter [17], which is also extended into a sensorless approach in [19]. However, such techniques were not extended to 3L-FC boost converters. A DCMC technique under fixed-frequency control was applied in [20] to achieve fast transient response and FC balancing in a 3L-FC boost converter. However, fixed-frequency CMC techniques suffer from inner-loop stability problems for wide-duty-ratio operations and require an external compensating ramp for stability, affecting the controller BW [20], [21], [22].

Variable-frequency control, such as constant ON/OFF-time CMC, offers inherent current-loop stability for a wide-duty-ratio operation [23], [24], which are applied in multilevel boost converters in [25] and [26] and dc–ac applications in [27] for FC voltage balancing. An external precharging circuit is implemented in [25] for soft start-up in a 3L-FC boost converter. Event-based constant ON/OFF-time DCMC techniques

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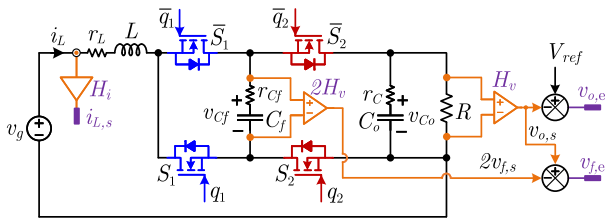

Fig. 1. Schematic of a 3L-FC boost converter with sensing signals.

were applied in traditional boost converters [28], and the effect of the RHP zero was investigated. However, such techniques have not been extended so far in 3L-FC boost converters operating under variable-frequency control. For such converters, suitable modeling and design techniques are not readily available, and also, investigating the impact of sampling delay and RHP zero on closed-loop stability is crucial.

This article proposes a variable-frequency control technique for active balancing of FC voltage and fast transient response in a 3L-FC boost converter shown in Fig. 1. The primary contributions of this work are summarized as follows.

1) Event-based constant ON-time and OFF-time DCMC architectures are proposed in a 3L-FC boost converter taking one voltage sample per switching cycle, thereby reducing computational as well as resource requirements.
2) A discrete-time (DT) framework is developed to analytically derive stability boundary for the closed-loop 3L-FC boost converter. This is a unique contribution for a 3L-FC boost converter under event-based digital control.
3) A hybrid DT controller design framework is developed to highlight the effective design of digital controller using the simplicity of continuous-time (CT) small-signal models and the accuracy of DT small-signal models.
4) The proposed constant ON-time DCMC is also reconfigured to adaptive ON-time pulse frequency modulation (PFM) control under discontinuous conduction mode (DCM) operation for improving light-load efficiency.
5) An experimental comparative study is presented to demonstrate the superiority of the proposed constant ON/OFF-time DCMC over the fixed-frequency counterpart.

The rest of this article is organized as follows. Section II proposes a constant ON/OFF-time DCMC architecture. Section III formulates DT large- and small-signal models. Section IV defines stability boundary and provides controller design guidelines. Section V demonstrates hardware implementation and experimental validation. Finally, Section VI concludes this article.

II. Proposed Event-Based Constant ON/OFF-Time DCMC

Fig. 2(a) shows the schematic of a fixed-frequency DCMC technique, and Fig. 2(b) and (c) shows the schematic of the proposed constant OFF-time DCMC and constant ON-time DCMC architectures, respectively, in a 3L-FC boost converter in Fig. 1. The inductor charging and discharging times are considered as the respective ON and OFF intervals, respectively. The proposed control uses one current feedback loop in analog domain and two voltage feedback loops in digital domain using a time-multiplexed analog-to-digital converter (ADC)—one for the output voltage and the other for the FC voltage. The output voltage controller $G_c(z)$ uses a digital type II compensator to generate the current reference $i_{\rm ref1}$. The FC voltage controller $G_{\rm cf}(z)$ uses a proportional gain and generates a correction factor $i_{\rm cf}$, which along with the first current reference generates the second current reference as $i_{\rm ref2} = i_{\rm ref1} - i_{\rm cf}$. Both $i_{\rm ref1}$ and $i_{\rm ref2}$ are converted into analog current commands using a time-multiplexed digital-to-analog converter (DAC) using a select line $half_1$, as shown in Fig. 2. An analog comparator is used to compare the time-multiplexed analog current reference with the sensed inductor current.

A. Constant Off-Time Digital Peak CMC

Fig. 2(b) shows the constant OFF-time DCMC implementation where the OFF-time is fixed and the ON-time is adjusted by the feedback action. The corresponding timing diagram is shown in Fig. 3. The voltage samples are taken once per switching cycle using an event-based sampling clock $F_{\rm vs}$. The "$reset$" pulses are generated when the sensed inductor current $i_{L,s}$ goes above the control references $i_{\rm ref1}$ and $i_{\rm ref2}$. At the rising edge of $reset$ pulse, a monoshot timer is activated, which generates the constant OFF-time pulse q_c with fixed OFF-time of $T_{\rm off}$, using a global clock $F_{\rm clk}$. At the falling edge of q_c, the "set" pulse is generated. Then, alternate set pulses (set_1, set_2) and reset pulses (rst_1, rst_2) are generated to produce the gate signals q_1 and q_2. The sampling clock $F_{\rm vs}$ is generated during the interval-4, after a time delay of t_s with respect to rst_2 pulse, which is provided to accommodate the ADC conversion and controller computation time.

B. Constant On-Time Digital Valley CMC

In Fig. 2(c), the ON-time under the proposed constant ON-time DCMC is kept fixed, and the OFF-time is adjusted. The relevant timing diagrams are shown in Fig. 3, which shows that "set" pulses are generated when the inductor $i_{L,s}$ goes below the corresponding current references $i_{\rm ref1}$ and $i_{\rm ref2}$. A monoshot timer is activated at each rising edge of "set" pulses, keeping fixed width for q_c as $T_{\rm on}$. At the falling edge of q_c, the "$reset$" pulse is generated. Then, alternate set pulses and reset pulses are selected for generating the gate signals, as shown in Fig. 2(c). The sampling clock $F_{\rm vs}$ is generated during interval-1 after set_2 pulse is generated, with a delay of t_s.

The constant ON-time DCMC offers an inherent fast step-down transient performance [29]. However, the step-up performance suffers for large-step transients, because a minimum OFF-time is enforced. On the other hand, a constant OFF-time DCMC provides a very fast step-up transient performance and suffers in the case of large step-down transients due to a minimum ON-time implementation. The step-up/down performance can be improved if the minimum OFF/ON-time is decreased and/or the value of the ON/OFF-time is adaptively increased [29]. Moreover, a small modification can be made by using a voltage control logic to realize a constant ON-time PFM technique, which can achieve

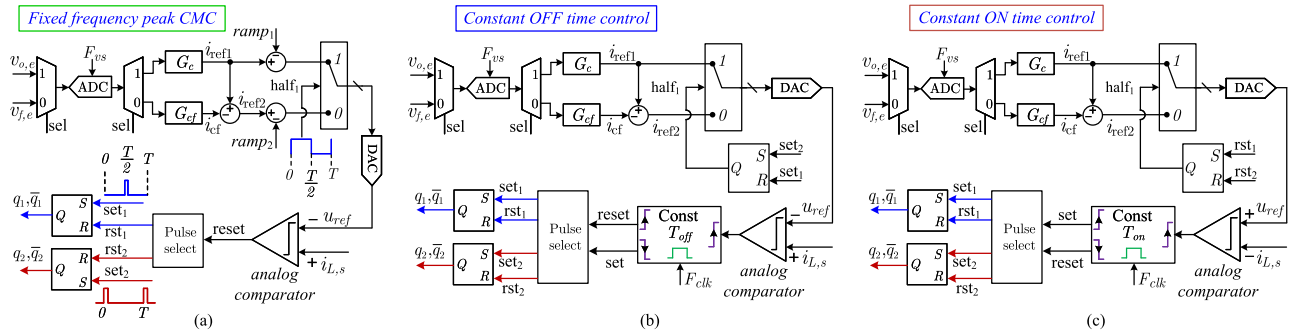

Fig. 2. (a) Schematic of fixed-frequency DCMC. Schematic of the proposed (b) constant OFF-time DCMC and (c) constant ON-time DCMC architectures in a 3L-FC boost converter (shown in Fig. 1).

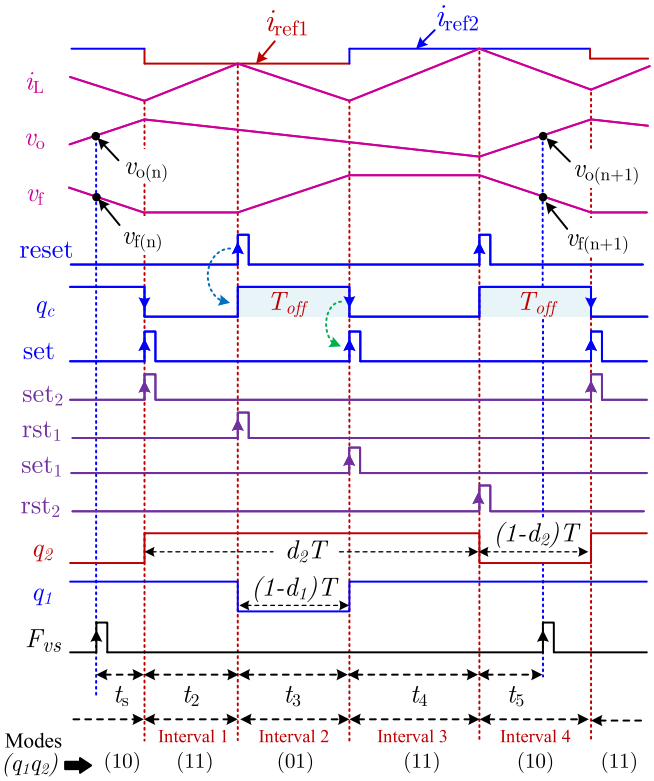

Fig. 3. Timing diagram of constant OFF-time DCMC for $D \geq 0.5$.

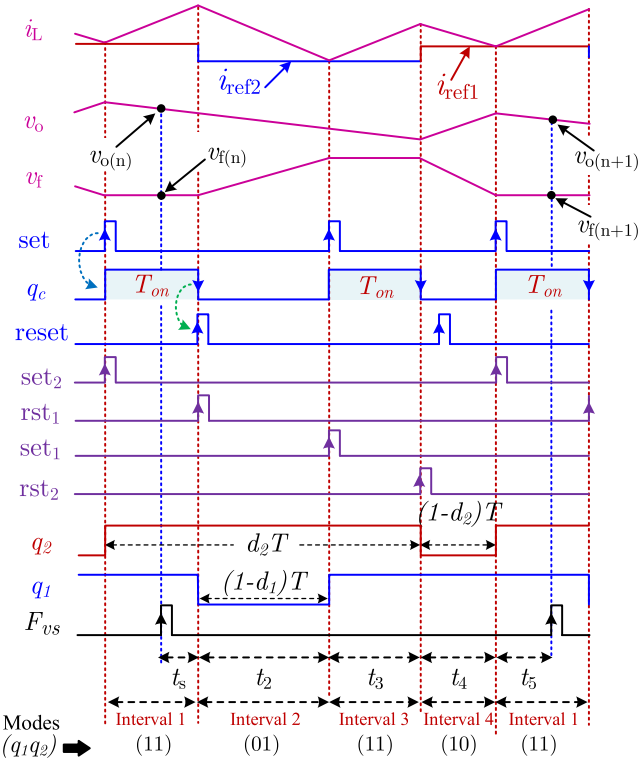

Fig. 4. Timing diagram of constant ON-time DCMC for $D \geq 0.5$.

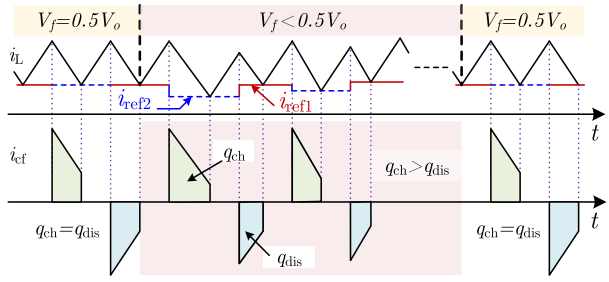

Fig. 5. FC voltage balancing with constant ON-time control scheme.

high light-load efficiency during light-load conditions when the converter essentially operates in DCM.

C. FC Voltage Balancing Technique

To ensure FC voltage balancing, the net charge into the FC is adjusted in each switching cycle. As shown in Fig. 4, for the constant ON-time DCMC, the valley current references are adjusted to directly control the FC charging and discharging periods. Similarly, for the constant OFF-time DCMC (shown in Fig. 3), the peak current references are adjusted to control the net charge going into the FC in each cycle.

Fig. 5 shows the conceptual FC voltage balancing logic under the proposed constant ON-time DCMC method [shown in Fig. 2(c)] in a 3L-FC boost converter. This is accomplished by adjusting the FC charging/discharging intervals using the current reference i_{ref2}, consisting of the correction factor i_{cf}, which is derived from the FC voltage controller $G_{\text{cf}}(z)$.

D. Calculation of Steady-State Switching Frequency

Under constant ON/OFF-time modulation, after balancing the FC voltage, the steady-state switching frequency of the 3L-FC boost converter operating under continuous conduction mode (CCM) can be derived by solving the inductor volt-second balance over a complete switching period [30]. Referring to the timing diagrams in Figs. 3 and 4, the voltage across the inductor can be written under different operating modes in an ideal 3L-FC boost converter as

$$\begin{aligned} &\text{mode 11}: \quad v_L = v_g; \quad \text{mode 01}: \quad v_L = v_g - v_f \\ &\text{mode 10}: \quad v_L = v_g + v_f - v_o. \end{aligned} \tag{1}$$

Taking the steady-state FC voltage as $V_f = V_g/2$, the steady-state switching frequency $f_{\rm sw}$ can be obtained by solving the inductor volt-second balance using (1), which becomes

$$f_{\rm sw} = \frac{V_g}{V_o} \times \frac{1}{T_{\rm off}} = \left(0.5 - \frac{V_g}{V_o}\right) \times \frac{1}{T_{\rm on}}. \tag{2}$$

This shows that for constant timing parameters, i.e., for fixed $T_{\rm on}$ and $T_{\rm off}$, the switching frequency $f_{\rm sw}$ increases (or decreases) with the input voltage under the constant OFF-time (or ON-time) DCMC. However, $f_{\rm sw}$ shows relatively low sensitivity to variations in load current, particularly for smaller MOSFET's ON-state resistance and inductor dc resistance.

III. DT Large- and Small-Signal Model

A generalized DT modeling technique in [31] is extended in this article to derive DT large- and small-signal models in a 3L-FC boost converter under constant ON/OFF-time DCMC by considering practical sampling delays.

A. Derivation of DT Large-Signal Model

Referring to the 3L-FC boost converter in Fig. 1, the state-space model can be written in a compact form as follows:

$$\begin{aligned} \dot{x}(t) &= A_{q_1q_2}x(t) + Bv_{\rm in} \\ v_o &= C_{q_1q_2}x(t);\ v_f = E_{q_1q_2}x(t) \end{aligned} \tag{3}$$

where the vector $x = \begin{bmatrix} x_1 & x_2 & x_3 \end{bmatrix}^T$ and the inductor current, FC voltage, and the output capacitor voltage are the states. The system, input, and output matrices are

$$\begin{aligned} A_{q_1q_2} &= \begin{bmatrix} \frac{p}{L} & \frac{q_1 - q_2}{L} & \frac{-\bar{q}_2\alpha}{L} \\ \frac{q_2 - q_1}{C_f} & 0 & 0 \\ \frac{\bar{q}_2\alpha}{C_o} & 0 & \frac{-\alpha}{RC_o} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \end{bmatrix} \\ C_{q_1q_2} &= \begin{bmatrix} \bar{q}_2\alpha r_C & 0 & \alpha \end{bmatrix} \\ E_{q_1q_2} &= \begin{bmatrix} (q_2 - q_1)r_{Cf} & 1 & 0 \end{bmatrix} \end{aligned} \tag{4}$$

where $p = -(r_L + 2r_{\rm on}) + (\alpha r_C\bar{q}_2) + (r_C(q_1\bar{q}_2 + q_2\bar{q}_1))$ and $\alpha = R/(R + r_C)$. The gate pulses q_1 and q_2 are taken as "1" for the ON-state and "0" for the OFF-state. A generic solution for the state-space model in (3) can be obtained as [31]

$$x(t) = e^{A_{q_1q_2}(t-t_0)}x(t_0) + \Gamma_{q_1q_2}(t - t_0)Bv_{\rm in} \tag{5}$$

where

$$\Gamma_{q_1q_2}(\tau) = \begin{cases} \left(\mathrm{e}^{A_{q_1q_2}(\tau)} - I\right) A_{q_1q_2}^{-1}, & \text{if} A_{q_1q_2} \text{is nonsingular} \\ \sum\limits_{j=1}^{\infty} \frac{A_{q_1q_2}^{j-1}(\tau)^j}{j!}, & \text{if } A_{q_1q_2} \text{ is singular} \end{cases}.$$

Fig. 6 shows the structural changes in mode configurations of the 3L-FC boost converter within two subsequent sampling points under the proposed constant ON/OFF-time DCMC. For the constant ON-time control, the voltage samples are taken at mode "11," and for the constant OFF-time control, at mode "10," considering a sampling delay of t_s. For both the control schemes, a generic DT large-signal model can be derived using (5) with $m = 5$ as follows:

$$\begin{aligned} x_{n+1} = &\left[\left(\sum_{i-1}^{m-1}\left(\prod_{j=0}^{m-i-1} e^{A_{Q_{m-j}}t_{m-j}}\right)\Gamma_{Q_i}(t_i)\right)\right. \\ &\left. + \Gamma_{Q_m}(t_m)\right]Bv_g + \left(\prod_{j=0}^{m-1} e^{A_{Q_{m-j}}t_{m-j}}\right)x_n \end{aligned} \tag{6}$$

where Q_k implies the operating mode (q_1q_2) at the kth transition.

TABLE I
Nominal Power Stage Parameters of the 3L-FC Boost Converter

V_g (V)	V_o (V)	P (W)	L (μH)	C_f (μF)	C_o (μF)	r_L ($m\Omega$)	$r_{\rm on}$ ($m\Omega$)	r_C ($m\Omega$)
12	48	100	10	30	50	2.6	10	5

B. Validation of the DT Large-Signal Model

SIMPLIS switch simulation of an open-loop 3L-FC boost converter is carried out to validate the accuracy of the DT large-signal model defined in (6). The converter is operated with a switching period of 10 μs keeping $T_{\rm on}$ fixed at 2.5 μs for a 12-V input and 60-Ω load resistance. Then, the switching period is changed to 12 μs, keeping the same $T_{\rm on}$. Table I shows the complete converter parameters. The results in Fig. 7 show that the proposed DT model accurately captures the SIMPLIS switch simulation at every sampling instant. Thus, the DT model can be used to carry out fast-scale stability analysis of the closed-loop converter under the proposed control.

C. DT Small-Signal Model and Transfer Functions

The DT small-signal model under constant ON/OFF-time DCMC can be obtained using Taylor series and Jacobian linearization of the DT large-signal model in (6), which can be expressed as

$$\tilde{x}_{n+1} = A_{\rm eq}\tilde{x}_n + B_{\rm eq1}\tilde{t}_{\rm off1} + B_{\rm eq2}\tilde{t}_{\rm off2} \quad (\text{fixed } T_{\rm on}) \tag{7}$$

$$\tilde{x}_{n+1} = A_{\rm eq}\tilde{x}_n + B_{\rm eq1}\tilde{t}_{\rm on1} + B_{\rm eq2}\tilde{t}_{\rm on2} \quad (\text{fixed } T_{\rm off}) \tag{8}$$

where the coefficients are provided in Table II. The perturbed ON/OFF-time intervals can be expressed in terms of control

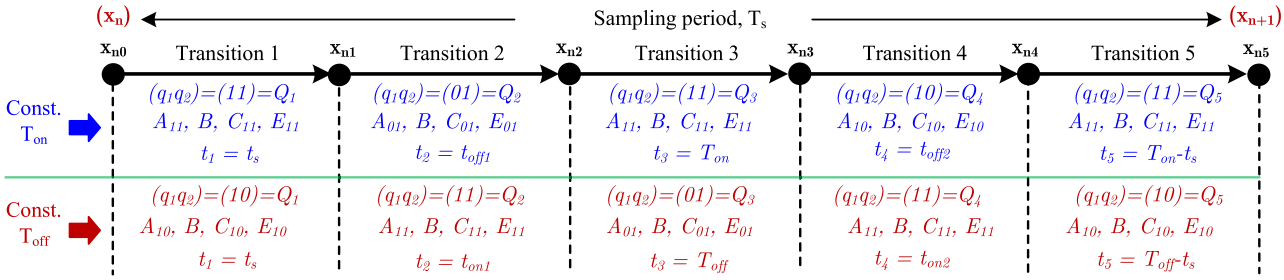

Fig. 6. Periodic evolutions within a sampling period T_s in a 3L-FC boost converter under constant ON/OFF-time control DCMC architectures, where $A_{q_1q_2}$, B, $C_{q_1q_2}$, and $E_{q_1q_2}$ correspond to the system, input, and output matrices given in (4).

TABLE II
SYSTEM MATRIX AND INPUT MATRIX OF THE SMALL-SIGNAL MODELS DEFINED IN (7)–(9)

Co-efficients	constant on-time control	constant off-time control
A_{eq}	$\prod_{j=0}^{m-1} e^{A_{Q_{\text{m-j}}} t_{\text{m-j}}}\Big\vert_{\text{steady state}}$	
B_{eq1}	$\left(\prod_{j=0}^{m-3} e^{A_{Q_{\text{m-j}}} t_{\text{m-j}}}\right) A_{Q_2} e^{A_{Q_2} t_2} \left(e^{A_{Q_1} t_1} x_n + \Gamma_{Q_1}(t_1) B v_g\right) + \left(\prod_{j=0}^{m-2} e^{A_{Q_{\text{m-j}}} t_{\text{m-j}}}\right) B v_g\Big\vert_{\text{steady state}}$	
B_{eq2}	$e^{A_{Q_5} t_5} A_{Q_4} \left(\prod_{j=0}^{m-3} e^{A_{Q_{\text{m-j-1}}} t_{\text{m-j-1}}}\right) \left(e^{A_{Q_1} t_1} x_n + \Gamma_{Q_1}(t_1) B v_g\right) + e^{A_{Q_5} t_5} A_{Q_4} e^{A_{Q_4} t_4} \left(e^{A_{Q_3} t_3} \Gamma_{Q_2}(t_2) + \Gamma_{Q_3}(t_3)\right) B v_g + e^{A_{Q_5} t_5} e^{A_{Q_4} t_4} B v_g\Big\vert_{\text{steady state}}$	
A_m	$A_{\text{eq}} + \frac{B_{\text{eq1}}}{m_2 H_i}\left(H_i[1\,0\,0] + K_{\text{pf}} H_v (C_{Q_1} - 2E_{Q_1}) - k_1 E_{Q_1}\right) + \frac{B_{\text{eq2}}}{m_2 H_i}\left(K_{\text{pf}} H_v (2E_{Q_1} - C_{Q_1}) + k_1 (E_{Q_1} - C_{Q_1})\right)$	$A_{\text{eq}} + \frac{B_{\text{eq1}}}{m_1 H_i}\left(-H_i[1\,0\,0] + k_2 (C_{Q_1} E_{Q_1})\right) + \frac{B_{\text{eq2}}}{m_1 H_i}\left(K_{\text{pf}} H_v (2E_{Q_1} - C_{Q_1}) + k_1 E_{Q_1}\right)$
B_m	$-B_{\text{eq1}}/(m_2 H_i)$	$B_{\text{eq1}}/(m_1 H_i)$

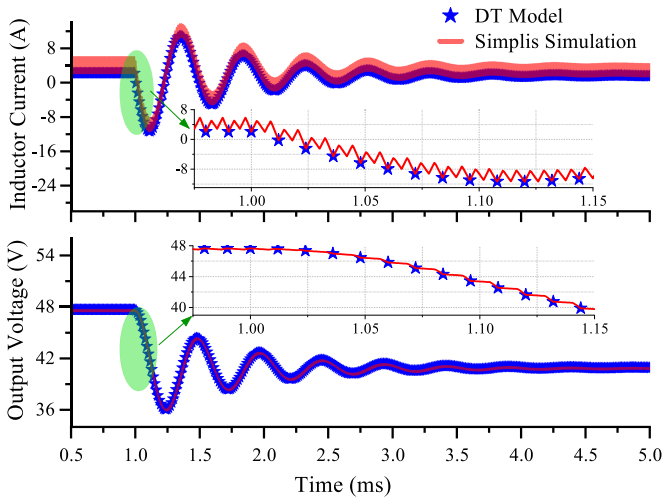

Fig. 7. Validation of the DT large-signal model in (6) of the 3L-FC boost converter using SIMPLIS simulation.

current reference, and the DT small-signal model takes the following form:

$$\tilde{x}_{n+1} = A_m \tilde{x}_n + B_m \tilde{i}_{\text{ref1}} \tag{9}$$

where the coefficients are given in Table II.

The DT control-to-output transfer function (TF) in a 3L-FC boost converter using constant ON/OFF-time control can be written as

$$G_{vc}(z) = \frac{\tilde{v}_o(z)}{\tilde{i}_{\text{ref1}}(z)} = C_{Q_1}(z\mathbf{I} - A_m)^{-1} B_m. \tag{10}$$

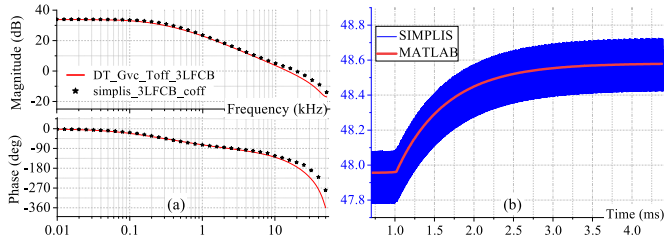

Fig. 8. Validation of DT control-to-output TF using the (a) frequency-domain approach and (b) time-domain approach.

Using the parameters given in Table I, and initially considering a slower FC voltage loop using a smaller proportional gain with $K_{pf} = 0.1$, the control-to-output transfer functions for the individual constant ON/OFF-time DCMC can be obtained from (9) by applying the "z" transformation, which is given as

$$G_{vc,\text{on}}(z) = \frac{1.1821(z^2 - 1.556z + 0.6416)}{(z - 0.9838)(z^2 - 1.348z + 0.4654)}$$
$$G_{vc,\text{off}}(z) = \frac{0.33(z + 1.856)(z - 0.9798)}{(z - 0.9879)(z - 0.9673)(z - 0.01389)}. \tag{11}$$

Fig. 8(a) validates the DT small-signal models using the frequency-domain approach by comparing the bode plot of $G_{vc,\text{off}}(z)$ with that of using SIMPLIS for the 3L-FC boost converter. The figure shows a close agreement between the two plots up to the control BW, which is 8 kHz for this case. The DT small-signal models are also validated using the time-domain

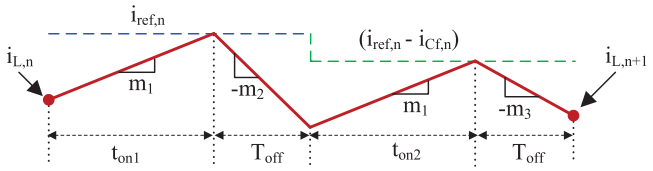

Fig. 9. Inductor current waveform between two successive samples in a 3L-FC boost converter under the proposed constant OFF-time control.

approach by comparing the step response of $G_{vc,\text{off}}(z)$ with that obtained from the switch simulation, as shown in Fig. 8(b).

IV. Stability Analysis and Hybrid Design Method for the Proposed Constant On/Off-Time DCMC

A. Inner Current Loop Stability Analysis

In a 3L-FC boost converter operating under fixed-frequency peak CMC, the inner current loop becomes unstable $\forall D \in \{(0.25, 0.5) \cup (0.75, 1)\}$ and requires external ramp compensation [20]. However, in constant ON/OFF-time DCMC, the inner current loop is inherently stable. From Fig. 9, the relation between two successive inductor current samples under constant OFF-time control can be obtained from the following set of equations:

$$\begin{aligned} i_{L,n} &= i_{\text{ref,n}} - m_1 t_{\text{on1}} \\ i_{\text{ref,n}} &= (i_{\text{ref,n}} - i_{\text{cf,n}}) + m_2 T_{\text{off}} - m_1 t_{\text{on2}} \\ i_{L,n+1} &= (i_{\text{ref,n}} - i_{\text{cf,n}}) - m_3 T_{\text{off}} \\ T &= t_{\text{on1}} + 2T_{\text{off}} + t_{\text{on2}}. \end{aligned} \tag{12}$$

Here, the inductor current slopes are defined as $m_1 = v_g/L$, $m_2 = (v_g - v_f)/L$, and $m_3 = (v_g + v_f - v_o)/L$. After further evaluation of (12), the perturbed inductor current at the $(n+1)$th sample in digital domain can be expressed as

$$\tilde{i}_L(z) = \frac{M_x}{(zI + M_z)} \tilde{i}_{\text{ref}}(z) + \frac{M_y}{(zI + M_z)} \tilde{i}_{\text{cf}}(z) \tag{13}$$

where $M_x = \dfrac{2m_1 + m_2 + m_3}{2m_1 + m_2}$, $M_y = \dfrac{2m_1 + m_1 m_2 + m_3}{2m_1 + m_2}$, and $M_z = m_3/(2m_1 + m_2)$. For the inner current loop to be stable, $|M_z| < 1$, which is always true for all positive values of V_g and V_o. This shows that the inner current loop is inherently stable in the case of constant OFF-time CMC. The same can be derived for constant ON-time CMC.

Fig. 10 shows the SIMPLIS simulation results with inner current loop closed and the outer voltage loop open in a 3L-FC boost converter operating under fixed-frequency peak-CMC and constant OFF-time CMC architectures given in Fig. 2. The FC voltage is made equal to half the output voltage. In the case of fixed-frequency peak CMC, for duty $D > 0.75$, the current loop shows subharmonic instability and becomes stable after ramp compensation. For the same operating conditions, the converter shows stable periodic behavior under constant OFF-time CMC.

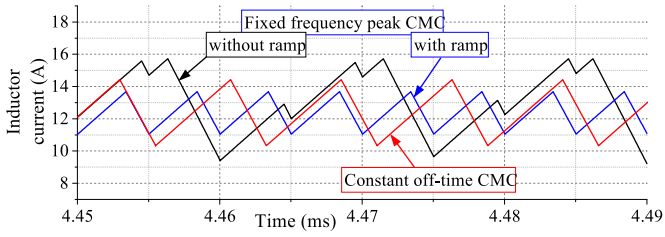

Fig. 10. Inner current loop stability analysis between fixed- and variable-frequency DCMC schemes with $V_{\text{in}} = 8$ V, $V_o = 48$ V, and $R = 24\ \Omega$.

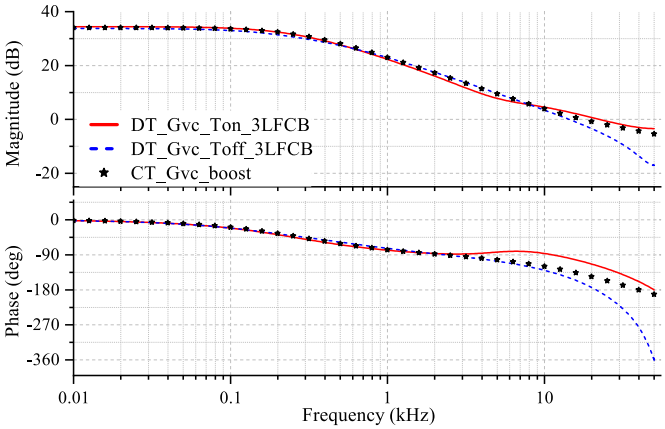

Fig. 11. Comparison of frequency response of control-to-output TFs.

B. CT Small-Signal Model Under CMC

The design process is initiated by using CT small-signal models, which are simple and provide useful design insights in terms of pole/zero of the loop transfer function [23]. In the 3L-FC boost converter, the BW of the FC voltage loop is typically kept much slower than that of the outer voltage feedback and inner current feedback loops. Thus, for the sake of simplicity, the FC dynamics can be ignored, and the control-to-output transfer function of a 3L-FC boost converter under CMC becomes that of a CMC boost converter, which can be approximately written as [23]

$$G_{vc}(s) = k\left(1 + \frac{s}{\omega_z}\right)\left(1 - \frac{s}{\omega_{\text{rhp}}}\right) \Big/ \left(1 + \frac{s}{\omega_p}\right) \tag{14}$$

where

$$k = \frac{RD'}{2H_i}, \omega_{\text{rhp}} = \frac{RD'^2}{L}, \omega_z = \frac{1}{r_C C_o}, \omega_p = \frac{2}{(R + r_C)C_o}.$$

To validate the accuracy, frequency response of the approximate CT model in (14) is compared with that of the accurate DT model in (11) and is shown in Fig. 11. The figure shows that the frequency responses using both the CT and DT models closely match up to one-tenth of the switching frequency. Thus, it is reasonable to initiate design of the digital controller using the simple CT model defined in (14).

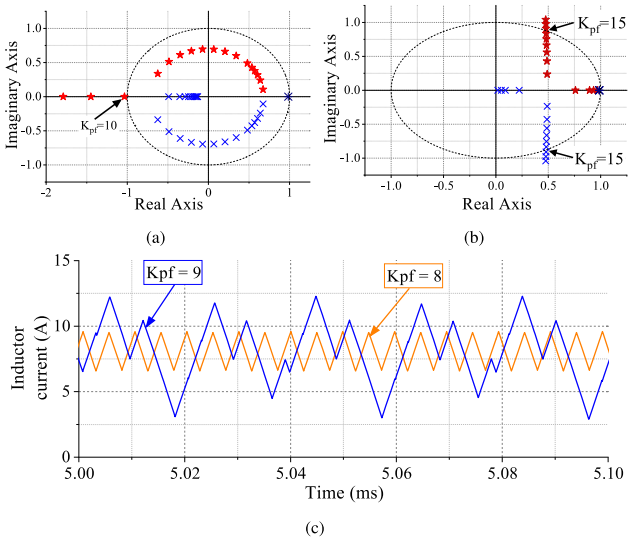

Fig. 12. (a) Root-locus plot for varying FC voltage gain K_{pf} under the proposed constant ON-time DCMC. (b) Fast-scale instability because of using a higher FC voltage gain K_{pf}.

C. Controller Design Using the CT Model

Considering the transfer function in (14), a type-II compensator $G_c(s)$ can be used [23], which takes the form as

$$G_{\text{type}-2}(s) = k_c \left(1 + \frac{s}{\omega_{cz}}\right) \Big/ \left(s\left(1 + \frac{s}{\omega_{cp}}\right)\right). \quad (15)$$

The placement of the poles and zero of the type-II compensator is carried out using the following design steps.

1) Place a zero to cancel the dominant plant pole by making $\omega_{cz} = \omega_p$
2) Place a stable pole at the RHP zero frequency such that $\omega_{cp} = \omega_{\text{rhp}}$
3) Place a pole at origin to achieve zero steady-state error
4) Set the controller gain k_c such that the gain crossover frequency becomes one-third of the RHP zero frequency.

Following the above guidelines, the CT type-II compensator $G_c(s)$ is designed, which is then converted to a DT transfer function $G_c(z)$ using a backward difference formula as follows:

$$G_c(z) = k' \frac{z(z-\alpha)}{(z-1)(z-\beta)} \quad (16)$$

where

$$k' = \frac{k_c T \omega_{cp}(1+\omega_{cz}T)}{\omega_{cz}(1+\omega_{cp}T)}, \quad \alpha = \frac{1}{1+\omega_{cz}T}, \quad \beta = \frac{1}{1+\omega_{cp}T}.$$

D. Closed-Loop Stability Analysis and Controller Retuning

CT models ignore ripple information, which may not be able to capture fast-scale instability of the closed-loop converter.

1) FC Voltage Loop Stability: The closed-loop poles of the 3L-FC boost converter under the proposed constant ON/OFF-time DCMC can be obtained using the DT small-signal model in (10), and the root-locus plots are shown in Fig. 12(a) and (b) for varying FC voltage-loop controller gain K_{pf}. It can be observed

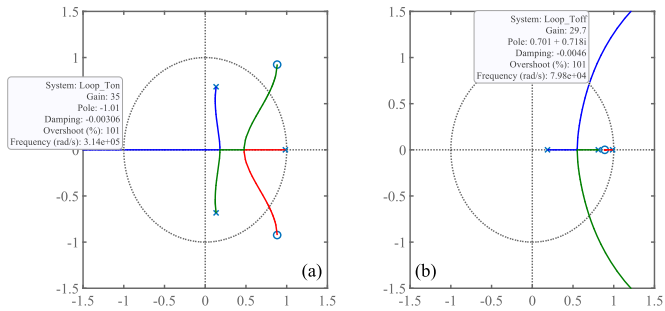

Fig. 13. Root-locus plot for varying controller DC gain in (16) with a sampling delay of 2 μs under (a) constant ON-time DCMC and (b) constant OFF-time DCMC.

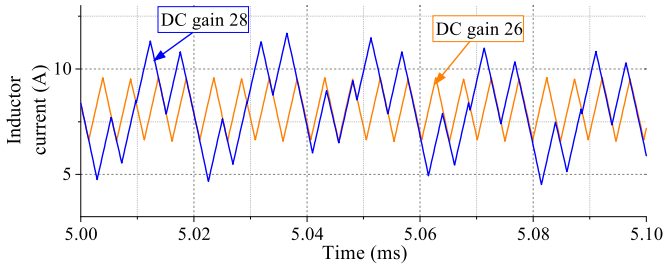

Fig. 14. Fast-scale instability because of higher controller DC gain.

that, in the case of constant ON-time control, one of the closed-loop poles goes out of the unit circle of the complex "z" plane for $K_{pf} > 10$. Similarly, in constant OFF-time control, two of the closed-loop poles go out of the unit circle for $K_{pf} > 15$. The SIMPLIS simulation in Fig. 12(c) depicts that for varying K_{pf} under the proposed constant ON-time DCMC, the closed-loop system is stable for $K_{pf} = 8$, which exhibits fast-scale instability for $K_{pf} = 9$. Also, the stability results are found to be consistent with the analytical predictions using the DT model, whereas the simplified CT model in (14) fails to capture fast-scale instability. The FC voltage controller gain is set to $K_{pf} = 3$.

2) Output Voltage Loop Stability: With $K_{pf} = 3$ and 2 μs sampling delay, the DT control-to-output transfer functions under the proposed constant ON/OFF-time DCMC are obtained using the parameters in Table I as

$$G_{vc,\text{on}}(z) = \frac{1.1845(z^2 - 1.766z + 1.633)}{(z-0.9839)(z^2 - 0.2667z + 0.4847)}$$

$$G_{vc,\text{off}}(z) = \frac{-0.55552(z-2.678)(z-0.8898)}{(z-0.9862)(z-0.8101)(z-0.1869)}. \quad (17)$$

The root-locus plots corresponding to (17) under constant ON/OFF-time DCMC are shown in Fig. 13. The figures show that, under constant OFF-time DCMC, two poles go out of the unit circle of the complex "z" plane when the controller gain exceeds 30. Similarly, for constant ON-time DCMC, one of the poles goes out of the unit circle if the controller gain goes beyond 34. For the constant OFF-time DCMC, the SIMPLIS simulation result in Fig. 14 shows fast-scale instability for a controller dc gain of 28, which is stable for a dc gain of 26. Furthermore, analytical

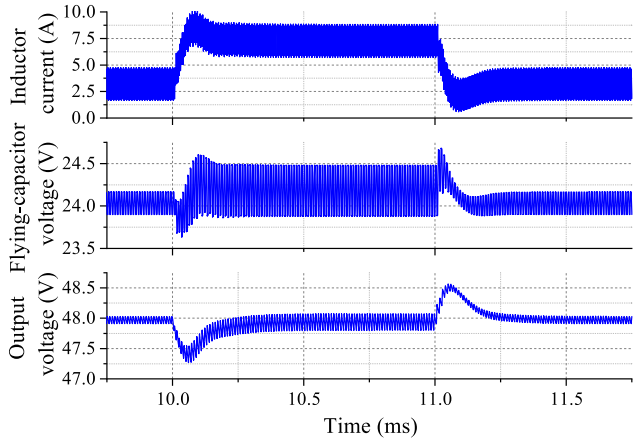

Fig. 15. Load transient response in SIMPLIS simulation for 1-A load step at 48-V output in the 3L-FC boost converter under the proposed DCMC.

stability boundaries for both the constant ON/OFF-time DCMC techniques are consistent with the time-domain SIMPLIS simulation results. Considering the closed-loop stability boundaries from the DT model, the stable type-II compensator gains are obtained using (16) as

$$G_c(z) = 11.5\frac{z(z-0.9524)}{(z-1)(z-0.4011)}. \tag{18}$$

E. Load Transient Simulation Results

Fig. 15 shows the transient performance of the 3L-FC boost converter using the proposed constant OFF-time DCMC for a 1-A step change in load current. In this case, the DT type-II controller in (18) is used along with $K_{\rm pf}$ as 3 using the power stage parameters given in Table I. For both the load step-up and step-down transients, the output voltage is settled within 220 μs with 1.5% voltage undershoot and overshoot with insignificant current overshoot/undershoot. Moreover, the closed-loop system is stable and the FC voltage is balanced. A higher closed-loop BW may be attempted; however, this would lead to a poor phase margin because of the RHP zero effect in a nonminimum phase converter [23].

V. Hardware Implementation and Results

For the experimental validation of the proposed constant ON/OFF-time control architectures, a 100-W 12/48-V hardware prototype of the 3L-FC boost converter is developed using the power-stage parameters given in Table I. A picture of the complete power-stage and controller boards is shown in Fig. 16. The proposed constant ON/OFF-time DCMC architectures are implemented using a field-programmable gate array (FPGA) device.

A. Steady-State Performance

For a nominal output voltage of 48 V, an 8-V input is considered to test the 3L-FC boost converter for high voltage gain with $D > 0.75$, under both the constant ON-time and constant

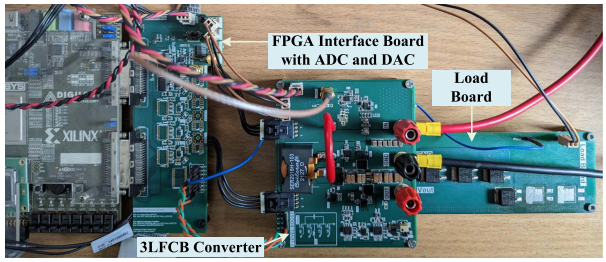

Fig. 16. Experimental hardware setup of the 3L-FC boost converter.

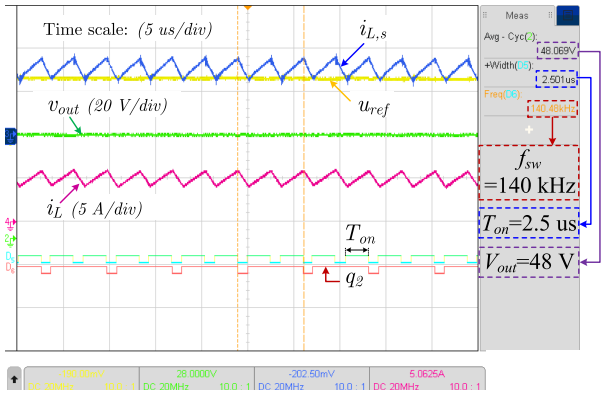

Fig. 17. Experimental result of the 3L-FC boost converter under the constant ON-time DCMC with $v_g = 8$ V, $v_o = 48$ V, and $R = 60\ \Omega$.

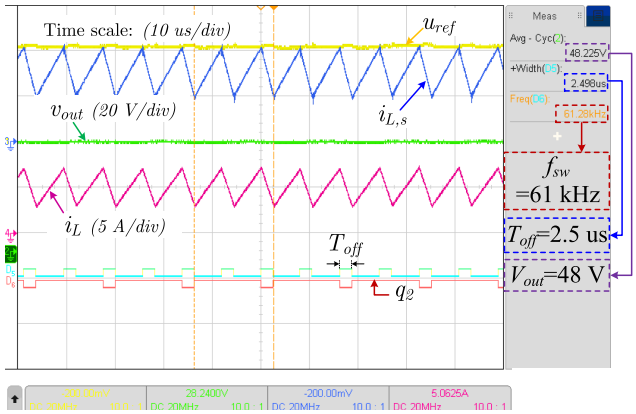

Fig. 18. Experimental result of the 3L-FC boost converter under the constant OFF-time DCMC with $v_g = 8$ V, $v_o = 48$ V, and $R = 60\ \Omega$.

OFF-time DCMC techniques by setting the constant timing parameters $T_{\rm on}$ and $T_{\rm off}$ to 2.5 μs. For both the techniques, the same controller defined in (18) is considered with $K_{pf} = 2$.

Figs. 17 and 18 show stable periodic behavior at steady state under constant ON- and OFF-time DCMC techniques, respectively. If constant ON/OFF-time parameters are kept constant, the switching frequency under both constant ON/OFF-time DCMC techniques varies with the input voltage as per (2) to regulate the output voltage at 48 V. For the constant ON-time DCMC and OFF-time DCMC, the switching frequency is found to be 140 and 61 kHz, respectively, which is consistent with the analytical expression in (2). Thus, for varying input voltage,

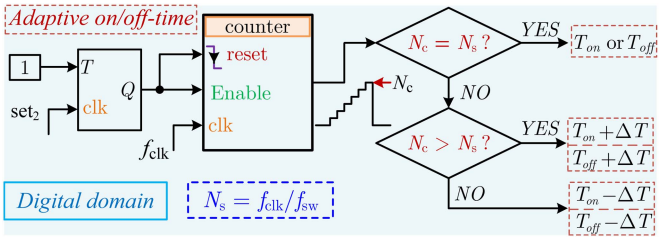

Fig. 19. Schematic of the proposed adaptive ON/OFF-time control logic.

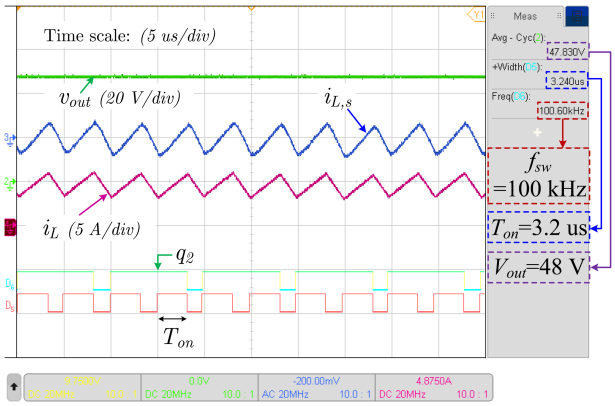

Fig. 20. Experimental result of the 3L-FC boost converter under the proposed adaptive ON-time DCMC with $v_g = 8$ V, $v_o = 48$ V, and $R = 60\ \Omega$.

the constant ON/OFF-time parameters should be adjusted in real time to regulate the switching frequency.

1) Adaptive On/Off-Time Implementation: Fig. 19 shows the schematic of the adaptation logic for constant ON/OFF-time control, which uses the information of the set pulse set_2 in Figs. 3 and 4. Using a counter, a time-to-digital converter logic can be implemented using the desired switching frequency command, which can adjust $T_{\rm on}$ or $T_{\rm off}$ in the runtime to regulate the switching frequency.

For experimental validation, the adaptive ON-time control is implemented keeping the circuit parameters same as the case in Fig. 17, and the steady-state results are shown in Fig. 20. This shows that $T_{\rm on}$ is adjusted to 3.2 μs to regulate the switching frequency at 100 kHz.

2) Light-Load Performance Improvement: Constant ON-time control is popularly used in commercial dc–dc converter products for improving light-load efficiency while operating under DCM, because the switching frequency linearly decreases with the load current [23]. Thus, the proposed constant ON-time DCMC is perfectly suitable to retain high light-load efficiency while operating the 3L-FC boost converter under DCM. A relevant experimental result is shown in Fig. 21, in which a DCM operation is enabled. Under this configuration, when the output error voltage $v_{o,e}$ exceeds the maximum error limit, the MOSFETs S_1 and S_2 are turned ON simultaneously to charge the inductor for a constant ON-time of $T_{\rm on}$. The switch S_1 is then turned OFF. If the FC voltage error exceeds a maximum limit, then S_2 is kept ON for an additional time of $T_{\rm fc}$, operating the converter in mode "01" to charge the FC. Otherwise, S_2 is turned OFF along with S_1, which is the case for most of the

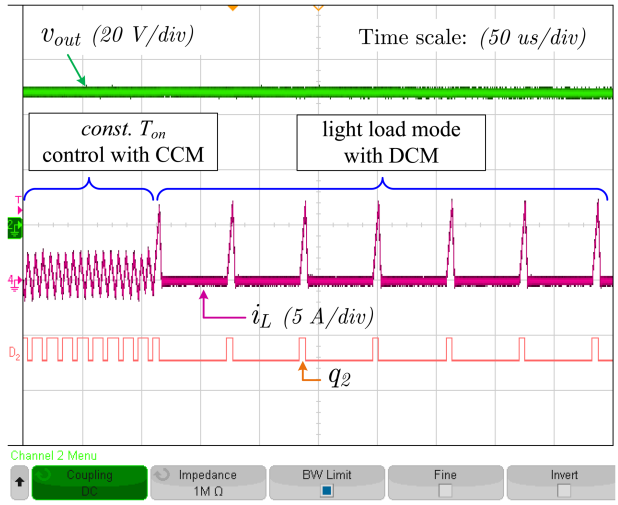

Fig. 21. Light-load operation for $v_g = 15$ V, $v_o = 48$ V, and $R = 300\ \Omega$ under the constant ON-time control with and without enabling DCM.

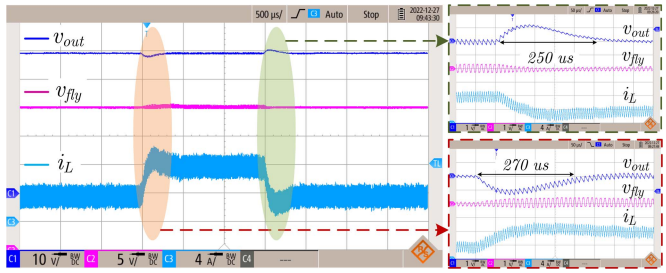

Fig. 22. Load transient response of the 3L-FC boost converter with a 1-A load step size for $v_g = 12$ V and $v_o = 48$ V under the constant ON-time DCMC.

switching cycles due to the slow discharging of the FC voltage under light-load conditions.

In Fig. 21, the load resistance is taken as 300 Ω, and the converter is initially run with the proposed constant ON-time control shown in Fig. 2, keeping $T_{\rm on} = 2.5\ \mu$s at an input voltage of 15 V. Then, the light-load mode with DCM is enabled where $T_{\rm on}$ is set at 5 μs and $T_{\rm fc}$ as 1 μs. For a window of 1 ms, the measured RMS values of the inductor current under CCM and DCM operations using the proposed constant ON-time control are found to be 1.3 and 1.6 A, respectively. However, compared to CCM, the switching frequency under DCM is reduced from 80 to 20 kHz, with S_3 and S_4 being turned OFF completely. Thus, the light-load efficiency of the 3L-FC boost converter can be improved by enabling the DCM operation in the constant ON-time DCMC.

B. Load Transient Performance

Figs. 22 and 23 demonstrate the transient performance of the 3L-FC boost converter using the proposed constant ON-time and OFF-time DCMC techniques, respectively, for a 1-A step change in load current. This results in a nearly identical voltage undershoot/overshoot of 2% and a settling time of 250 μs for load step-up/down transients. Moreover, with the proposed design, the FC voltage is strictly regulated at 24 V for the output voltage

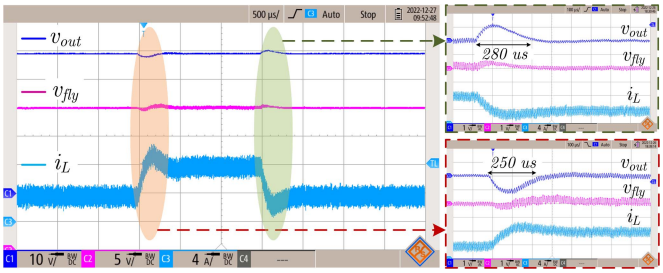

Fig. 23. Load transient response of the 3L-FC boost converter with a 1-A load step size for $v_g = 12$ V and $v_o = 48$ V under the constant OFF-time DCMC.

TABLE III
COMPARISON WITH SIMULATION AND HARDWARE FOR CONSTANT OFF-TIME

Parameter	Simulation (Fig. 15)	Experiment (Fig. 23)
Settling time (μs)	220	250
Overshoot/undershoot (mV)	750	1000

of 48 V. Furthermore, the cycle-by-cycle stability is retained for both the cases even with a 2-μs sampling delay.

A comparative analysis of the constant OFF-time experimental results of Fig. 23 with that of the simulated case study of Fig. 15 is made and is tabulated in Table III. The existing differences can be attributed to capacitor derating effect, unmodeled trace impedances, etc. Nevertheless, simulated and experimental results confirm fast dynamic performance and stable closed-loop behavior of the proposed method.

C. Dynamic Performance Comparison With Fixed-Frequency CMC

The 3L-FC boost converter with fixed-frequency DCMC has restricted closed-loop BW due to reduction in controller dc gain to accommodate sampling delay and/or the use of a compensating ramp to achieve inner loop stability [20]. However, using the proposed constant ON/OFF-time DCMC, the stability boundary is found to be substantially improved, which results in a higher closed-loop BW.

The proposed constant OFF-time control is compared with the fixed-frequency peak CMC technique for a 1-A step-up and step-down load transient case, as shown in Fig. 24. It can be seen that the constant OFF-time control results in a faster settling time with 250 μs during step-up and 280 μs during step-down transients, compared with the fixed-frequency control with 400 μs during step-up and 450 μs during step-down transients. Also, the voltage undershoot/overshoot is reduced, and the overall transient performance is improved by more than 1.5-fold using the proposed technique.

VI. CONCLUSION

In this article, novel event-based constant ON/OFF-time DCMC architectures were proposed in a 3L-FC boost converter, in which output voltage was sampled once per switching cycle for the computation of the digital controllers. A unified

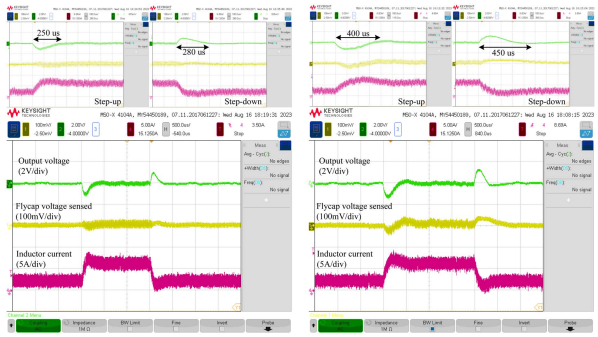

Fig. 24. Comparison of (a) the proposed constant OFF-time design with (b) the fixed-frequency peak CMC for 1-A step-up and step-down load transient case. (a) Proposed constant OFF-time DCMC. (b) Conventional fixed-frequency DCMC.

DT framework was proposed to derive accurate DT large and small-signal models, and the latter was used to derive the analytical stability boundary. A hybrid controller design framework was developed using the simplicity of the CT models and the accuracy of the DT models, which were useful for achieving fast transient performance with stable periodic behavior. A 12-to-48-V 100-W 3L-FC boost converter prototype was developed, and experimental results were presented to demonstrate the usefulness of the proposed techniques. Timing parameters were adaptively varied to regulate the switching frequency. The proposed architectures, along with the hybrid controller design, could improve the transient performance by more than 1.5 times compared with that using the fixed-frequency counterpart. The proposed architectures and the design techniques will be useful in designing high-performance ML-FC boost converters.

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