Characteristic-Based Design of an *LCC* Resonant Converter With a Capacitive Filter

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***Abstract*—The *LCC* resonant converter with a capacitive output filter is a popular topology for variable load applications, although the simultaneous design requirements of wide load range, soft switching, and low conduction loss are not clearly tackled in available design strategies. In this article, the existing time-domain analysis of the converter is extended in a normalized design-oriented fashion. The proposed extension to boundary modes lends itself to the derivation of critical converter characteristics such as the soft switching range. A dimensionless converter and load characteristic-based design algorithm with parameter decoupling is developed to meet the load requirements. The design algorithm reduces the converter rms current while meeting practical requirements of zero-voltage switching and constraints on switching frequency across the load range. The proposed design method is validated using circuit simulations incorporating series dissipative nonidealities and the transformer magnetizing inductance, and also on a 160-W laboratory prototype with switching frequency within the designated limits and $>96\%$ experimental efficiency.**

***Index Terms*—Capacitive filter, resonant converter (RC), time-domain analysis, variable load power supply, zero-voltage switching (ZVS).**

I. Introduction

SOFT-SWITCHED power converters find increasing applications in the domain of high-voltage (HV) dc power supplies [1]. The popularity of these converters is due to their efficiency, compact size, and scope of output regulation. In addition, resonant converter (RC) topologies facilitate the integration of parasitic elements into circuit operation [2].

HV power supplies employ transformers to obtain voltage gain and galvanic isolation. Requirements of turns ratio and insulation for these transformers lead to significant parasitic effects, especially leakage inductance and winding capacitance [1]. While the impact of these parasitic effects could be reduced by using a low turns ratio transformer cascaded with a voltage multiplier stage, a simpler scheme is to absorb them into a resonant network within the converter [3], [4]. RCs are, hence, an attractive choice in such applications [5], [6], [7], [8], [9], [10], [11], [12], [13].

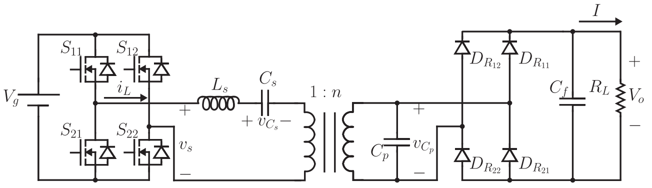

Fig. 1. Power circuit of a full-bridge isolated *LCC*-CF converter.

The *LCC* RC with a capacitive output filter (LCC-CF) [14], given in Fig. 1, has attributes suited to HV applications. The transformer parasitics are modeled as per the IEEE standard model [15]. The structure of the resonant network allows the integration of transformer leakage inductance and stray capacitance parasitics into the series inductor (L_s) and the parallel capacitor (C_p), respectively [5]. The series capacitor (C_s) blocks any dc voltage applied to the transformer [16]. The capacitive filter (C_f) avoids the challenges posed by an HV filter inductor [6], and clamps the voltage across rectifier legs [17]. Consequently, several HV applications of the LCC-CF are reported in the literature [5], [9], [12], [13], [18], [19].

The analysis of the LCC-CF is involved [5], [14] due to the inherent discontinuous conduction of the rectifier. As a result, the resonant circuit waveforms deviate greatly from sinusoids, limiting the applicability of the first-harmonic approximation (FHA) [17]. In addition, the state-plane method lends itself to second-order resonant networks [20] and is not suited to the analysis of the LCC-CF, which comprises a third-order tank.

The time-domain analysis of the LCC-CF is presented in [14]. The steady-state output characteristic is derived by imposing a condition of half-wave symmetry on resonant quantities and solving the resulting equations numerically. Analytical solutions are derived for special operating conditions such as the discontinuous conduction mode (DCM) in the literature [9], [21], [22], [23] but general closed-form expressions are not available. Studies report variations of the analysis of [14] using parameters such as the quality factor of the series *LC* branch [17] or the converter gain at resonance [24].

The preservation of soft switching over the entire operating range is an additional constraint for converter design. Typical HV applications demand converter operation over a wide range

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of output power and output voltage, as reported in studies on X-ray [5], electrostatic precipitator [12], insulation testing [13], microwave [10], and pulsed laser [11] power supplies. Thus, the design of the LCC-CF for an HV application must consider performance over the operating range along with optimized nominal performance. In such designs, zero-voltage switching (ZVS) abates capacitive discharge losses at turn-ON.

The guarantee of soft switching of the LCC-CF is difficult to establish using FHA-based analysis and design methodologies, which remain accurate only under the demanding condition of sinusoidal waveforms. Such methods, although widely discussed in the literature [5], [12], [19], [25], [26], are not suitable for this study. A normalized design methodology based on time-domain analysis is presented in [24]. The method, however, does not include soft switching as a design consideration. Furthermore, a reduced set of design parameters is considered by fixing the value of the series–parallel capacitance ratio a priori. Finally, the design of the converter is for a fixed output voltage, and hence, unsuitable for applications requiring a wide range of output voltages. The design of the LCC-CF converter described in this article addresses these gaps in the literature.

This article proposes a normalized design methodology for a frequency-modulated LCC-CF by extending existing time-domain analysis methods. The method accommodates ranges of frequency, output voltage, and output power variation and ensures ZVS over the entire range of operation. Frequency modulation is selected to avoid the challenges of ensuring ZVS operation of phase-shift-modulated RCs [27]. The major contributions of this work are as follows.

1) The time-domain analysis of [14] is reformulated in a normalized, dimensionless form. This normalization renders the design process invariant for a proposed scaling approach for the converter rating, making the design outcome applicable to a family of scaled designs. In particular, it is shown that the design parameters for the 250-V, 162.5-W scaled prototype presented in this article are also applicable to the target 2.5-kV, 16.25-kW application.
2) The analysis presented in [14] is extended to include the case of unknown switching frequency to accommodate converter design to satisfy the minimum and maximum frequency constraints for variable frequency operation.
3) Boundary modes of operation, crucial to the design of the converter to achieve ZVS over the entire load range, are identified and analyzed.
4) All degrees of freedom provided by the converter circuit parameters are utilized to formulate the novel characteristic-based design strategy for the LCC-CF. In contrast, the time-domain design approaches in the literature operate with reduced sets of design parameters. A method is proposed to decouple design parameters by mapping the LCC-CF characteristics with the load characteristics in the normalized characteristics plane.
5) An rms current minimization framework with ZVS constraints is proposed, which identifies the transformer turns ratio based on load and ZVS constraints. The design method can accommodate a wide load range. This is facilitated by the exact analysis, since RCs exhibit high performance in a narrow range of operation around resonance.
6) The LCC-CF parameters are identified based on the proposed design framework, with additional guidelines to address minimum and maximum switching frequency constraints as well as practical ZVS considerations and transformer nonidealities.

The rest of this article is organized as follows. Existing analysis techniques that show the possibility of additional modeling of the LCC-CF are reviewed and extended in Section II. The converter characteristics obtained from the extended analysis are central to the characteristic-based design procedure developed in Section III. Simulation and experimental results obtained along with efficiency measurements are presented in Section IV. Finally, Section V concludes this article.

TABLE I
DEFINITIONS OF BASE QUANTITIES

Quantity	Base
Voltage	Input voltage, V_g
Impedance	Characteristic impedance, $Z_B = \sqrt{L_s/C_s}$
Time	Series resonant angular period, $\sqrt{L_s C_s}$
Switching frequency	Series resonant frequency, $f_s = 1/(2\pi\sqrt{L_s C_s})$

II. REVIEW AND EXTENSION OF EXISTING ANALYSIS

The power circuit of the LCC-CF is given in Fig. 1. A full-bridge switch network (S_{11}–S_{22}) supplied by a dc voltage source (V_g) excites a resonant tank. The tank comprises an inductor (L_s) and a series capacitor (C_s) coupled to a parallel capacitor (C_p) through a $1:n$ transformer. This network feeds a diode-bridge rectifier ($D_{R_{11}}$–$D_{R_{22}}$) with a filter capacitor (C_f) supplying a resistive load (R_L). The full-bridge excitation (v_s) to the tank is a square wave voltage at switching frequency (f_{sw}). The output voltage (V_o) and current (I) are regulated by varying f_{sw}. The exact time-domain analysis of the converter involves state variables corresponding to the current through the resonant inductor (i_L), and the respective voltages across the series and parallel resonant capacitors (v_{C_s} and v_{C_p}).

A. Normalization of Circuit Quantities and Parameters

The circuit quantities and parameters of Fig. 1 are normalized using the base quantities given in Table I. In particular, the characteristic impedance, Z_B, is used as the impedance base. The quantity, Z_B, is an analytical quantity and does not correspond to a physical impedance in the LCC-CF circuit. To allow the use of unique base quantities, all circuit quantities are referred to the transformer primary side before normalization.

In particular, the time variable (t) is converted into an angle at the series resonant frequency, $\theta = 2\pi f_s t$, as in standard state-plane techniques [28]. This extends the normalization executed in [14] and renders the subsequent analysis and design process dimensionless, and hence, general and scalable [29].

Strict output ripple specifications are integral to power supply applications. Thus, the output filter-load combination is represented as a stiff dc voltage, M. With this simplification, the

TABLE II
DEFINITIONS OF NORMALIZED QUANTITIES AND PARAMETERS

Normalized quantity	Definition
Output voltage, M	V_o/nV_g
Output current, J	nIZ_B/V_g
Switching frequency, F	$f_{\rm sw}/f_s$
Full-bridge excitation, m_s	v_s/V_g
Inductor current, j_L	$i_L Z_B/V_g$
Series capacitor voltage, m_{C_s}	v_{C_s}/V_g
Parallel capacitor voltage, m_{C_p}	v_{C_p}/nV_g
Parallel capacitor, C_p'	n^2C_p/C_s
Load resistance, r_L	$R_L/(n^2 Z_B)$
Series-parallel resonant frequency, γ	$\sqrt{1+C_s/C_p'}$

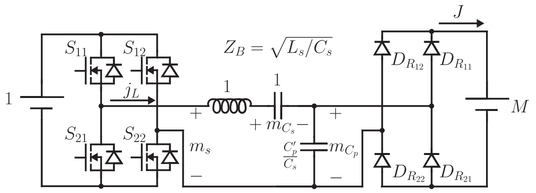


Fig. 2. Normalized equivalent circuit of the LCC-CF converter.

TABLE III
SWITCHING STATES AND PIECEWISE-LTI CIRCUITS OF THE LCC-CF

Piecewise-LTI circuit	Devices in conduction		m_s	m_{C_p}
	Full bridge	Diode bridge		
1a	S_{11}, S_{22}	$D_{R_{12}}$, $D_{R_{21}}$	$+1$	$-M$
2a		–		m_{C_p}
3a		$D_{R_{11}}$, $D_{R_{22}}$		$+M$
1b	S_{12}, S_{21}	$D_{R_{11}}$, $D_{R_{22}}$	-1	$+M$
2b		–		m_{C_p}
3b		$D_{R_{12}}$, $D_{R_{21}}$		$-M$

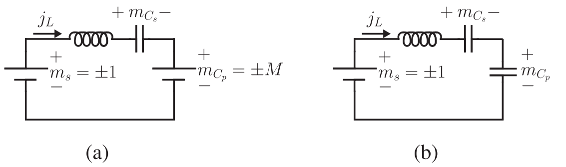


Fig. 3. Piecewise LTI circuits of the LCC-CF. (a) 1a-b, 3a-b, and (b) 2a-b.

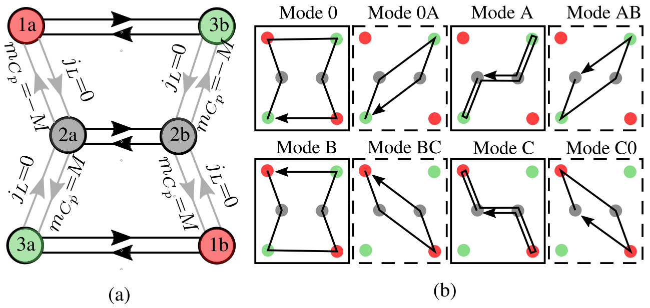


Fig. 4. (a) Transitions between piecewise-LTI circuits of the LCC-CF and corresponding circuit conditions. (b) Principal (solid borders) and boundary (dotted borders) modes of operation of the LCC-CF in terms of this state diagram.

TABLE IV
PROGRESSION OF CIRCUITS FOR THE MODES OF THE LCC-CF

Principal		Boundary	
Mode	Circuit progression	Mode	Circuit progression
0	$3a$-$2a$-$1a$-$3b$-$2b$-$1b$	0A	$3a$-$2a$-$3b$-$2b$
A	$2a$-$3a$-$2a$-$2b$-$3b$-$2b$	AB	$2a$-$3a$-$2b$-$3b$
B	$1a$-$2a$-$3a$-$1b$-$2b$-$3b$	BC	$1a$-$2a$-$1b$-$2b$
C	$2a$-$1a$-$2a$-$2b$-$1b$-$2b$	C0	$2a$-$1a$-$2b$-$1b$

normalized equivalent circuit of the converter is obtained using the qualities listed in Table II and presented in Fig. 2. This normalized circuit is analyzed in the time domain.

B. Piecewise-LTI Circuits and Modes of Operation

The terminology used in the subsequent analysis is as follows. An allowable permutation of "ON" conditions of semiconductor switches is called a *switching state* or simply a *state*. The circuit obtained by suitably replacing switches in a state by open or short circuits is termed as a *piecewise-LTI circuit*. Converter operation with a specific cyclic progression of piecewise-LTI circuits is designated as a *mode* of operation.

The diode bridge has voltage-stiff elements at both its input and output, and its conduction is cut off if the magnitudes of these voltages are unequal. Thus, the diode bridge assumes a so-called "zero" state apart from two conducting states. The full bridge has two possible states in square wave operation. The resulting six possible states of the LCC-CF and the corresponding piecewise linear-time-invariant (LTI) circuits are described in Table III. The dynamic equations for each piecewise-LTI circuit are given in [14] and are not repeated here.

In the conduction states of the diode bridge, the normalized parallel capacitor voltage (m_{C_p}) is clamped to the output voltage ($\pm M$) in piecewise LTI circuits 1a-b and 3a-b, as shown in Fig. 3(a). The circuits 2a-b, shown in Fig. 3(b), are formed during the "zero" state of the diode bridge when the parallel capacitor becomes available for resonance.

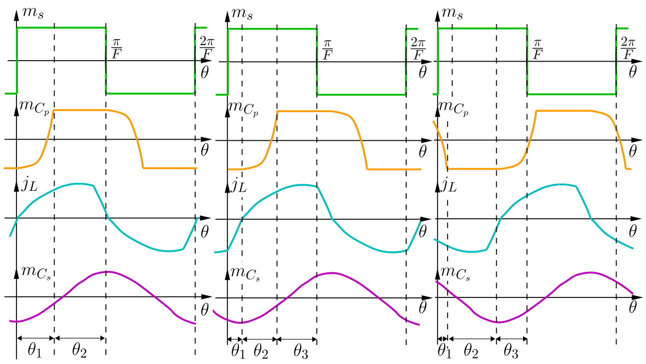
The transitions between the piecewise-LTI circuits occur at the semiconductor device switching instants. The full bridge switches twice per cycle, and the diode bridge switches at instants determined by circuit quantities. The transitions and their governing conditions are summarized in Fig. 4(a). The modes of operation are derived by inspecting these transitions.

The normalized inductor current (j_L), series capacitor voltage (m_{C_s}), and parallel capacitor voltage (m_{C_p}) are ac quantities exhibiting half-cycle symmetry in steady state. In Fig. 4(a), the color code is used to pair half-cycle symmetric piecewise-LTI circuits (e.g., 1a and 1b). The bold and faint arrows denote full-bridge and diode-bridge transitions, respectively.

In steady state, the diode bridge switches twice per half cycle between cut-off and conducting states. If one of these transitions coincides with a full-bridge transition, only two piecewise-LTI circuits occur per half-cycle. However, in general, three piecewise-LTI circuits occur per half cycle. The modes arising from these two cases are termed, respectively, as *boundary* and *principal* modes of the LCC-CF. The circuit transitions for both kinds of modes are illustrated in Fig. 4(b) and summarized in Table IV. Boundary modes 0 A, AB, BC, and

TABLE V
TRANSCENDENTAL EQUATIONS DESCRIBING LCC-CF BOUNDARY (AB) AND PRINCIPAL (B,C) MODES RELEVANT TO THE PROPOSED DESIGN METHOD

Mode	Equations	
AB	$\sin\gamma\theta_1 \cos\left(\frac{\pi}{F}-\theta_1\right)+\gamma\sin\left(\frac{\pi}{F}-\theta_1\right)\cos\gamma\theta_1=0$	(1)
	$M=\frac{\cos(\gamma\,\theta_1)-1}{2\,\gamma^2}-\frac{\cos\left(\theta_1-\frac{\pi}{F}\right)}{2}+\frac{\left(\sin\left(\theta_1-\frac{\pi}{F}\right)-\frac{\sin(\gamma\,\theta_1)}{\gamma}\right)\left(\cos\left(\theta_1-\frac{\pi}{F}\right)+\frac{\cos(\gamma\,\theta_1)-1}{\gamma^2}+1\right)}{2\left(\sin\left(\theta_1-\frac{\pi}{F}\right)+\frac{\sin(\gamma\,\theta_1)}{\gamma}\right)}+\frac{1}{2}$	(2)
	$MJ\left[\sin\left(\frac{\pi}{F}-\theta_1\right)-\frac{\sin\gamma\theta_1}{\gamma}\right]^2-\frac{2F}{\gamma\pi}\left(1-\frac{1}{\gamma^2}\right)\sin\left(\frac{\pi}{F}-\theta_1\right)(1-\cos\gamma\theta_1)\sin\gamma\theta_1\left(1-\cos\left(\frac{\pi}{F}-\theta_1\right)\right)=0$	(3)
B	$M\left(\sin\left(\frac{\pi}{F}-\theta_2\right)-\frac{1}{\gamma}\sin(\gamma\theta_2)\right)-\sin(\frac{\pi}{F}-\theta_1-\theta_2)\left(1-\frac{1}{\gamma^2}\right)(1-\cos(\gamma\theta_2))=0$	(4)
	$M\left(\cos\left(\frac{\pi}{F}-\theta_2\right)+1\right)-(1-\cos(\gamma\theta_2))\left[\left(1-\frac{1}{\gamma^2}\right)\cos(\frac{\pi}{F}-\theta_1-\theta_2)+M\right]=0$	(5)
	$J\left(1-\frac{1}{\gamma^2}\right)(1-\cos\gamma\theta_2)+\frac{2F}{\pi}\left[\left(1-\frac{1}{\gamma^2}\right)(1-\cos\gamma\theta_2)\left(\cos(\frac{\pi}{F}-\theta_1-\theta_2)\right)+M\left(\cos(\frac{\pi}{F}-\theta_2)-1\right)\right]=0$	(6)
C	$\left[1+M+\frac{1}{\gamma^2}(\cos\gamma\theta_1-1)\right]\left[\gamma\sin\theta_2-\sin\gamma\left(\frac{\pi}{F}-\theta_2\right)\right]+\sin\gamma\theta_1\left[\cos\theta_2+1+\frac{1}{\gamma^2}\left(\cos\gamma\left(\frac{\pi}{F}-\theta_2\right)-1\right)\right]=0$	(7)
	$\left[-M+\left(1-\frac{1}{\gamma^2}\right)(\cos\gamma\theta_1-1)\right]\left[\gamma\sin\theta_2-\sin\gamma\left(\frac{\pi}{F}-\theta_2\right)\right]+\left(1-\frac{1}{\gamma^2}\right)\left(\cos\gamma\left(\frac{\pi}{F}-\theta_2\right)-1\right)\sin\gamma\theta_1=0$	(8)
	$J\left(\gamma\sin\theta_2-\sin\gamma\left(\frac{\pi}{F}-\theta_2\right)\right)+\frac{2F}{\pi}\sin\gamma\theta_1(1-\cos\theta_2)=0$	(9)



(a) (b) (c)

Fig. 5. Waveforms of LCC-CF operation in the context of time-domain analysis for (a) boundary mode AB, and principal modes (b) B, and (c) C.

C0 were identified in [14] as intermediates between principal modes, but not analyzed separately. However, the boundary modes are central to the proposed design process and require formulation.

C. Numerical Steady-State Analysis of the LCC-CF

The exact time-domain steady-state analysis of the LCC-CF involves unknown switching instants and initial states. The sinusoidal natural response of the resonant network leads to a system of transcendental equations. The method for their solution outlined in [14] is briefly reviewed as follows.

A set of sample waveforms for the LCC-CF are presented in Fig. 5. The objective of time-domain analysis is the solution of the unknown initial states ($m_{C_p,0}$, $j_{L,0}$, $m_{C_s,0}$) and the unknown interval durations (θ_1, θ_2, θ_3) by imposing implicit and explicit constraints. Half-cycle symmetry of state variables provides three implicit constraints, while diode-bridge switching defines two implicit constraints. The explicit constraint depends on the quantity, such as switching frequency or load, which is a given for the analysis. The solution procedure in [14] uses the switching frequency as the explicit constraint.

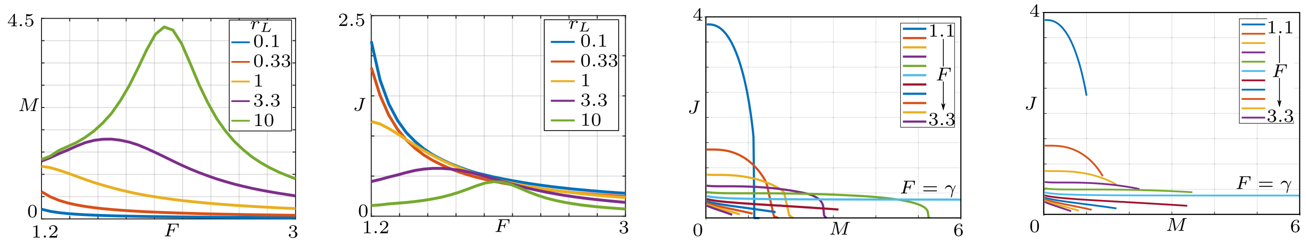
In frequency-modulated converter design exercises, the switching frequency is not known *a priori*. The load is a more suitable constraint in such cases. The choice of constraints decides the numerical formulation and the existing LCC-CF methodology is modified to solve for an unknown switching frequency for a given load condition. The resulting transcendental equations are mode-specific, and the expressions for modes B and C are given in Table V. The remaining principal modes do not exhibit ZVS and are hence not discussed further.

The boundary modes describe soft-switching boundaries in some cases, e.g., mode AB in Fig. 4(b). Defining such boundaries is useful in soft-switched converter design methods, such as that proposed in this article. In the existing framework [14], boundary modes are identified as special cases of the principal modes without dedicated discussion. However, for the present design-oriented approach with an unknown switching frequency, the solution for a boundary mode requires a reformulation of the analysis. The transcendental equations for mode AB are given in Table V. The other boundary modes are not used in the proposed design process.

Based on the foregoing analysis of the LCC-CF, the variations of normalized output voltage and output current with switching frequency, for a set of load resistances, are plotted in Fig. 6(a) and (b), respectively. The design-oriented formulations for the boundary and principal modes, developed in this section, form the basis of the proposed design methodology described next.

III. CHARACTERISTIC-BASED DESIGN

The LCC-CF normalized output current-voltage characteristics presented in Fig. 6(c) are obtained from the transcendental equations described in the preceding section. Each curve is generated at a different normalized switching frequency (F). This



(a) (b) (c) (d)

Fig. 6. Variation with normalized switching frequency, F, for normalized (a) output voltage, M, and (b) output current, J, with the normalized series–parallel resonant frequency parameter, $\gamma = 2.23$, and various values of normalized load resistance, r_L. (c) Normalized output characteristics of the LCC-CF for $\gamma = 2.23$, with F swept from 1.1 to 3.3 for all modes above series resonance (A, B, and C), and (d) considering only ZVS modes (B and C).

TABLE VI
ACTUAL AND SCALED INPUT–OUTPUT RATINGS OF THE LCC-CF CONVERTER

	Actual	Scaled
Input voltage, V_g	600 V	60 V
Output voltage, V_o	830–2500 V	83–250 V
Output power, P_o	1.625–16.25 kW	16.25–162.5 W

quantity is obtained by the normalizing the switching frequency with respect to the series resonant frequency (f_s).

A. Design for ZVS

The LCC-CF characteristics presented in Fig. 6(c) are an ensemble of modes A, B, and C. ZVS operation is ensured by considering only the sections contributed by the ZVS modes.

The primary requirement for ZVS is a negative sign of j_L at the instant, $\theta = 0$, considering the waveforms of Fig. 5. Modes B and C satisfy this condition, as illustrated by the waveforms in Fig. 5(b) and (c), respectively. Thus, the LCC-CF ZVS mode output characteristics shown in Fig. 6(d) are derived from those of Fig. 6(c) by including only modes B and C. These characteristics are used in the subsequent design steps.

B. Considerations to Accommodate the Load Characteristics

A set of LCC-CF converter input and output ratings for a variable-load power supply for an X-ray application is presented in Table VI. For the present discussion, the voltage and power ratings are scaled down by factors of 10X and 100X, respectively. The scaled input and output ratings of the LCC-CF considered for the present discussion are also specified in Table VI. The outcomes of the normalized design procedure are unaffected by this downscaling strategy, as discussed in the Appendix.

The load conditions are specified between limits of output voltage (V_L, V_H) and output power (P_L, P_H), as is typical of a scaled HV power supply, particularly in X-ray applications.

These limits are representable as curves on the normalized output (M–J) plane, described as follows:

$$\frac{\mu_L}{n} \leq M \leq \frac{\mu_H}{n} \qquad \text{where } \mu_{(H/L)} \triangleq V_{(H/L)}/V_g \tag{10}$$

$$\sigma_L Z_B \leq M\, J \leq \sigma_H Z_B \qquad \text{where } \sigma_{(H/L)} \triangleq P_{(H/L)}/V_g^2. \tag{11}$$

The curves are defined by design parameters (n and Z_B) as well as application-dependent parameters ($\mu_H, \mu_L, \sigma_H, \sigma_L$). All possible load conditions are contained within the region bounded by these curves. These curves and the delimited load region ($\mathcal{L}$) on the M–J plane are illustrated in Fig. 7(a).

For the LCC-CF to operate over the entire range of loads, the region $\mathcal{L}$ must be enclosed by the LCC-CF output characteristics. The output characteristics and $\mathcal{L}$ depend on the pairs (f_s, γ) and (n, Z_B) of design parameters, respectively. The proposed formulation thus reduces the LCC-CF design problem to decoupled transformations on a pair of 2-D regions to overlap while satisfying design objectives and constraints.

The design objectives considered here are ZVS over the entire operating range and the minimization of the primary rms current. These objectives correspond to the reduction of switching and conduction losses, respectively. Upper and lower limits on switching frequency constrain the design further.

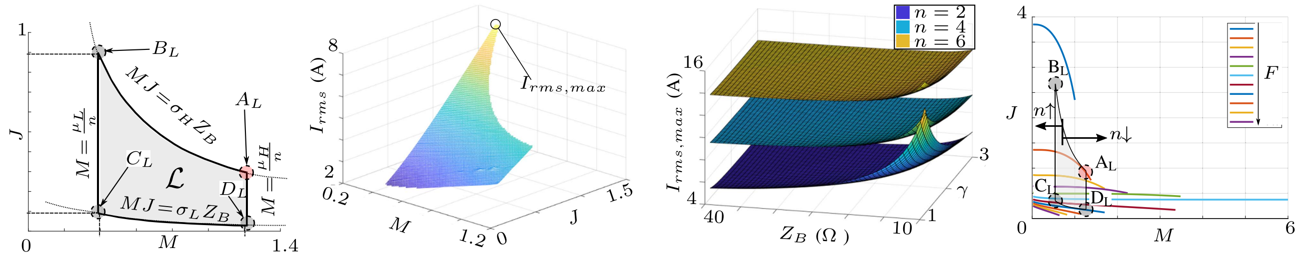
C. Design for Minimum RMS Current

The conduction losses in the LCC-CF occur mainly in the MOSFETs, the inductor, the transformer, and the rectifier diodes. Of these, the diode losses depend on the load condition and are largely insensitive to the secondary side rms current. The remaining conduction losses are influenced directly by the primary-side rms current (I_{rms}), which is identical to the rms inductor current. Thus, the minimization of I_{rms} as a design objective aligns with the minimization of conduction losses.

The range of operating conditions corresponds to a range of I_{rms}. The maximum value ($I_{\text{rms,max}}$) of the rms current corresponds to the maximum conduction loss condition and is hence selected as the quantity to be minimized. The equivalent optimization problem is stated formally as

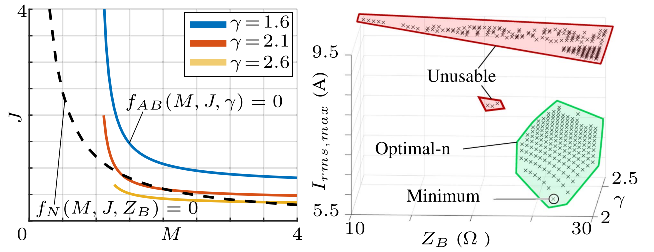
$$(n_o,\, \gamma_o,\, Z_{B_o}) = \underset{n,\gamma,Z_B}{\text{argmin}}\ \max_{\mathcal{L}}(I_{\text{rms}})|\text{ZVS}. \tag{12}$$

In an optimized design with a low circulating ac link current, $I_{\text{rms,max}}$ is expected to occur at the maximum load current condition. This is verified in multiple nonoptimized designs, one of which is illustrated in Fig. 7(b). Thus, the design method aims to



(a) (b) (c) (d)

Fig. 7. (a) Normalized load region defined by output voltage and power limits and (b) variation of primary-side rms current over the entire load region, both for an LCC-CF design with $(n, \gamma, Z_B) = (3.5, 2, 12.9)$. (c) Plot of worst-case rms current illustrating its dependence on the design parameters. (d) Illustration of the effect of turns ratio on a load region fitted inside the ZVS output characteristics.



(a) (b)

Fig. 8. (a) Loci of the ZVS operation boundary ($f_{AB} = 0$) and the nominal operating point ($f_N = 0$). (b) Plot of I_{rms} for designs with various (γ, Z_B) with the selected design minimum indicated. The loci do not intersect in the unusable designs highlighted in red.

minimize the primary-side rms current at the maximum output power and minimum output voltage condition.

The dependence of $I_{\text{rms,max}}$ on the design parameters (n, γ, Z_B) is illustrated in Fig. 7(c) for the ratings of Table VI. The strong effect of n is due to the direct scaling of the load current on the transformer primary side with the turns ratio. Thus, a lower n assists the $I_{\text{rms,max}}$ minimization process.

A lower limit on the turns ratio is imposed by the requirement of overlap between the LCC-CF ZVS characteristic and $\mathcal{L}$, as illustrated in Fig. 7(d). On reducing n beyond this limit, a section of $\mathcal{L}$ (termed the *critical* section) moves out of the ZVS characteristic, violating a design objective. So, the minimum n possible while retaining ZVS is obtained as follows.

D. *Selection of Minimum n*

Owing to the shape of the load region, the critical ZVS condition occurs at the nominal operating point, indicated as A_L and circled in red in Figs. 7(a) and (d). Ensuring ZVS at this nominal point guarantees ZVS for the entire load region. Thus, an LCC-CF design where the nominal point, A_L, is in boundary mode AB achieves ZVS over the entire operating region, with the lowest turns ratio possible for a given (γ, Z_B) pair. This process is shown graphically in Fig. 8(a). The value of n for the design is fixed by the intersection of the locus of the nominal operating point, $f_N = 0$, with the mode-AB characteristic, $f_{AB} = 0$, as indicated in Fig. 8(a). Of these curves, $f_N(\cdot)$ depends on Z_B, while $f_{AB}(\cdot)$ depends on γ.

The curves are derived as follows. Regardless of the choice of n, the operating point A_L satisfies the upper power bound in (11) with an equality relation, yielding $f_N(\cdot)$ as

$$MJ = \sigma_H Z_B \Rightarrow \qquad f_N = MJ - \sigma_H Z_B = 0. \tag{13}$$

The function $f_{AB}(\cdot)$ describes the mode AB characteristic and comprises all points on the $M - J$ plane defined by (1)–(3) for a given value of γ. In practice, these curves are generated for a given γ using the following steps:

1) fix F in (1) and solve for θ_1;
2) substitute F and θ_1 into (2) and (3) and solve for (M, J);
3) update F and repeat step 1.

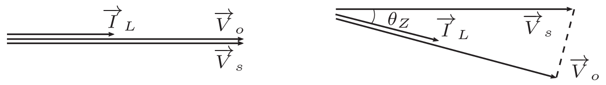
The operation of the critical section of $\mathcal{L}$ at the edge of ZVS in this manner thus yields the minimum value of n feasible in a design for a given (γ, Z_B) pair. Not all (γ, Z_B) pairs lead to an intersection, as evident from Fig. 8(a). For a set of (γ, Z_B) pairs within a range, the minimum n is calculated using the preceding method. The quantity $I_{\text{rms,max}}$ is then evaluated for each partial design (n, Z_B, γ). The design (n_c, Z_{B_c}, γ_c) with the lowest $I_{\text{rms,max}}$ is selected, as illustrated in Fig. 8(b).

E. *Practical Considerations for Ensuring ZVS*

The characteristic-based design method places the nominal operating point at the edge of ZVS. However, to achieve ZVS, a nonzero current is required at the switching instant to (dis)charge the MOSFET drain–source capacitances. The theoretical edge of ZVS represented by mode AB is, therefore, less stringent than the practical ZVS boundary.

To account for this, the nominal condition is designed to operate marginally within mode B, rather than exactly in mode AB. This requires a leftward translation of the load region in Fig. 7(d), and corresponds to a higher turns ratio (n'_c). This quantity is calculated approximately from FHA considerations, rather than exact analysis, to simplify the design procedure.

The full bridge is represented as a sinusoidal ac voltage source $(\overrightarrow{V}_s)$. The resonant tank is modeled as a series reactive element, and the load is considered to be purely resistive with a fictitious ac voltage $(\overrightarrow{V}_o)$ across it. In mode AB, the zero crossings of the full-bridge square wave and the inductor current coincide. In this case, $\overrightarrow{V}_o$ and the ac link current $(\overrightarrow{I}_L)$ phasor coincide in the FHA model as shown in Fig. 9(a). In mode B, both of these phasors lag the input voltage by the ZVS angle θ_Z, as shown



(a) (b)

Fig. 9. FHA phasor diagrams of the LCC-CF for ZVS angle considerations. (a) Mode AB. (b) Mode B.

in Fig. 9(b). The reduction in the output voltage is offset by the increase in turns ratio. This simplistic formulation allows the evaluation of the required turns ratio increment using only the desired minimum ZVS angle as follows:

$$n_c' \cos\theta_Z = n_c \Rightarrow n_c' = n_c \sec\theta_Z. \tag{14}$$

The application of FHA alone is insufficient to obtain ZVS conditions. However, FHA is used in conjunction with exact analysis, in the aforementioned step, to quantify a design modification in a way guided by the exact analysis. The computationally simple relation obtained in (14) justifies the use of FHA in this stage of the design. The effect of the inaccuracy of the ZVS angle obtained through FHA is mitigated by considering a larger value for θ_Z, than is required.

F. Constraints on Switching Frequency

The final design parameter is the series resonant frequency, f_s, which is assigned a value (f_{s_c}) based on the constraints on switching frequency. For instance, frequency-dependent magnetic losses and power semiconductor gate drive capability impose an upper limit ($f_{\text{sw}} \leq f_{\max}$) on switching frequency, while output filter size limits and required control bandwidth impose lower limits ($f_{\min} \leq f_{\text{sw}}$). The ratio $\kappa_f \triangleq f_{\max}/f_{\min}$ measures the allowable range of switching frequency.

The ratio $\kappa_F(n_c, Z_{B_c}, \gamma_c) \triangleq F_{\max}/F_{\min}$ measures the normalized switching frequency range required by the preceding design to cover all load conditions. The condition $\kappa_F > \kappa_f$ indicates that the preceding design violates the frequency constraints. The rms current minimization step is then refined to eliminate all designs with $\kappa_F > \kappa_f$, and the design with the minimum $I_{\text{rms,max}}$ is selected from the remaining designs.

When $\kappa_F \leq \kappa_f$, the frequency constraints are satisfied by the rms current minimization step. The choice of f_{s_c} in this case is not unique; any value may be selected from the range

$$\frac{f_{\min}}{F_{\min}} \leq f_{s_c} \leq \frac{f_{\max}}{F_{\max}}. \tag{15}$$

The complete design flow is illustrated in Fig. 10.

G. Further Design Considerations

The effect of the transformer magnetizing inductance, L_m, is modeled as a branch in parallel with C_p, and offsets the latter to an extent depending on the switching frequency.

This effect is mitigated by augmenting C_p by a value (ΔC_p). The impedance of ΔC_p is selected to cancel out that of L_m at the minimum operating switching frequency ($f_{\text{sw,min}}$), as

$$\Delta C_p = \frac{1}{4\pi^2 f_{\text{sw,min}}^2 L_m}. \tag{16}$$

The mitigation of the effect of L_m instead of its use as an additional parameter in the proposed design avoids an additional magnetic component and/or involved transformer design. This approach further preserves the third-order nature of the state equations used in the main design flow, and refines the accuracy of the design to meet the target performance.

H. Comparison With Design Methods in the Literature

The main advantages of the proposed characteristic-based design method presented in this article are established in comparison to design strategies in the literature, in Table VII.

The simplicity of the FHA technique allows the tackling of relatively wide load ranges in [5] and [12]. However, this trades off with the difficulty of achieving ZVS. Methods based on the DCM of the resonant current in the LCC-CF [9], [21], [22] employ closed-form expressions available for this mode. However, the requirement of DCM limits the availability of this method to tackle load variation. The time-domain techniques employed in [14] and [24] overcome this difficulty and ensure ZVS over the operating range. However, the relative complexity of the time-domain analysis is prohibitive to the minimization of rms current over the complete space of design parameters. Thus, the design algorithms are executed with a reduced set of design parameters in [14] and [24]. Further, the preceding design strategies lack an explicit minimization of rms current; in [12], total loss is minimized employing a genetic algorithm, which does not provide adequate insights into LCC-CF operation, and hence, has limited generalizability. The proposed design method addresses the ZVS challenge by employing exact time-domain analysis. In addition, the normalized analysis and the characteristic-based rms current minimization could readily be extended to other applications.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The proposed characteristic-based design procedure is executed for the load requirements and the design constraints given in Tables VI and VIII, respectively.

The imposed frequency constraint is $\kappa_f = 250/90 = 2.78$. The initial execution of the partial design yields a required frequency spread of $\kappa_F = 2.19 < \kappa_f$. Hence, no modification of the initial design space is necessary. The parameter f_s is selected using (15), such that the lowest operating frequency corresponds to the lower limit in Table VIII. The raw design outcome, the consequent circuit parameters, and the parameters realized in the prototype are tabulated in Table IX. The fabricated prototype is shown in Fig. 11. Values of circuit nonidealities, measured or obtained from datasheets, are tabulated in Table X. These nonidealities are included in the circuit simulations.

The simulated and experimental waveforms at the limits of operation are presented in Fig. 12. The operating point B_L exhibits the highest rms inductor current, as evident from Fig. 12(b). The temporal instants of the transition of the full-bridge voltage, v_s,

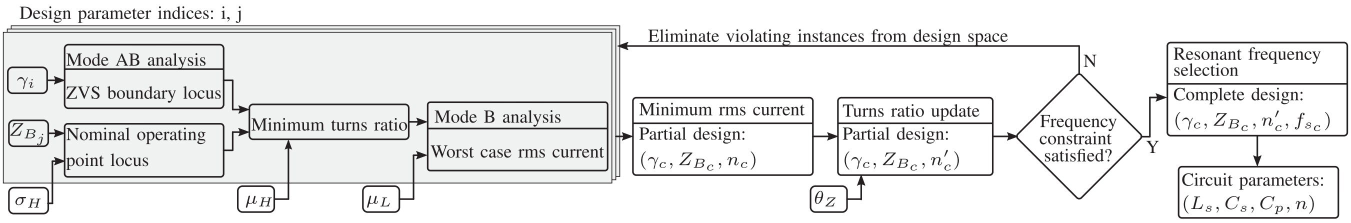
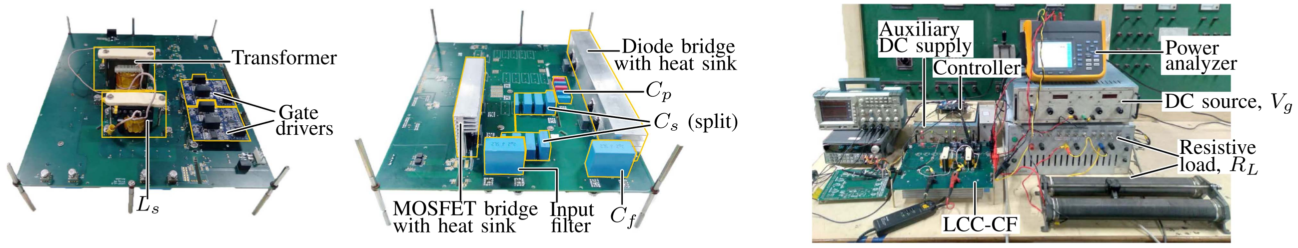


Fig. 10. Flowchart of the proposed characteristic-based design procedure.

TABLE VII
METHODOLOGICAL COMPARISON OF THE PROPOSED CHARACTERISTIC-BASED DESIGN WITH ALGORITHMS IN THE LITERATURE

Method	Modulation	Voltage range	Power range	Analysis strategy	Degrees of design freedom	Design optimization	ZVS
Ref. [5]	Hybrid	3X	100X	FHA	4 (L_s, C_s, C_p, n)	No	No
Ref. [9]	Constant on time	1X	1X	Time-domain (DCM)	3 (L_s, C_s, n)	No	No
Ref. [12]	Hybrid	10X	10X	FHA	4 (L_s, C_s, C_p, n)	Yes	No
Ref. [14]	PFM	1X	8.5X	Time-domain	3 $(L_s, C_s, C_p, n = 1)$	No	Yes
Ref. [21]	Constant on time	1X	1X	Time-domain (DCM)	2 (C_s, n)	No	No
Ref. [22]	Constant on time	1X	1X	Time-domain (DCM)	4 (L_s, C_s, C_p, n)	No	No
Ref. [24]	PFM	1X	6X	Time-domain	2 $(L_s, C_p, C_s = C_p, n = 1)$	No	Yes
Ref. [26]	PFM	1.2X	5X	FHA	3 (C_p, C_s, n)	No	No
Proposed	PFM	3X	10X	Time-domain	4 (L_s, C_s, C_p, n)	Yes	Yes



(a) (b) (c)

Fig. 11. (a) Top side, and (b) bottom side of the fabricated 162.5 W LCC-CF laboratory prototype. (c) Experimental setup.

TABLE VIII
CONSTRAINTS FOR THE CHARACTERISTIC-BASED DESIGN PROCEDURE

Lower limit on switching frequency, f_{min}	90 kHz
Upper limit on switching frequency, f_{max}	250 kHz
Worst-case ZVS angle, θ_Z	18°

TABLE IX
OUTCOME OF THE CHARACTERISTIC-BASED DESIGN PROCEDURE

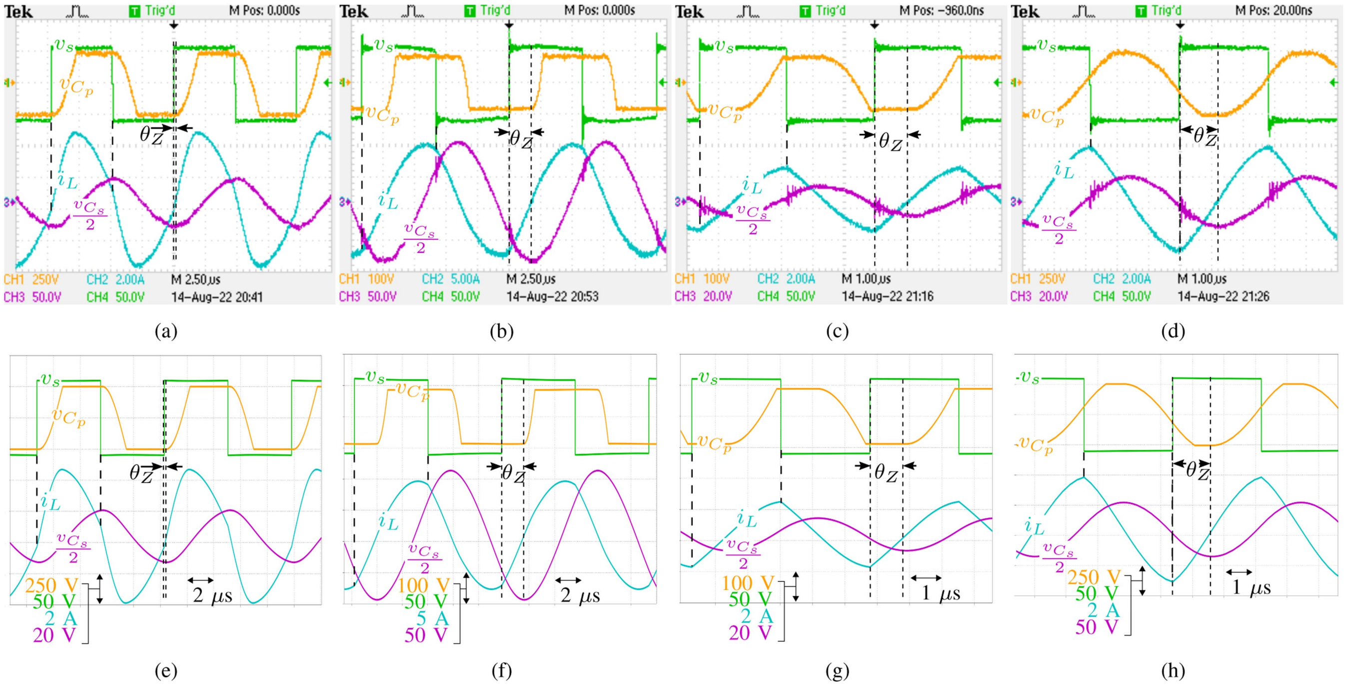
Design	γ_c	Z_{B_c} (Ω)	n'_c	f_{s_c} (kHz)
	2.04	26.9	2.73	76.6
Circuit parameters	L_s (μH)	C_s (nF)	n'_c	C_p (nF)
	55.8	77.3	2.73	3.28
Realized parameters	L_s (μH)	C_s (nF)	n'_c	$C_p + \Delta C_p$ (nF)
	56.3	78.0	2.72	3.85

TABLE X
MEASURED AND DATASHEET NONIDEALITIES OF THE LCC-CF PROTOTYPE

Tx. LV-side magnetizing inductance[1]	769 μH
Tx. LV-side leakage inductance[1]	2.46 μH
Tx. HV-side capacitance	$<$ 10 pF
Tx. LV-side winding resistance[1]	67 mΩ
Inductor series resistance[1]	80 mΩ
D_{ij} diode drop	4 V
$D_{R_{ij}}$ diode drop	1.8 V
MOSFET on resistance, R_{on}	72 mΩ

[1] Measured at 100 kHz.

and the zero crossing of the inductor current, i_L, are marked with dotted lines. The angle of separation between these instants indicates the ZVS angle, θ_Z. Clearly, $\theta_Z > 0$ at each operating point, which signifies successful ZVS realization. The characteristic-based design places the nominal operating point close to the edge of ZVS, leading to a low ZVS angle for the operating point A_L, shown in Fig. 12(a). As the load condition deviates from the nominal, the ZVS angle increases. Each of the remaining operating points shown in Fig. 12 corresponds to a substantially different load voltage and/or power, and hence exhibits a larger ZVS angle. Thus, as the output voltage and power deviate from the nominal value, the ZVS of the switches is achieved by a greater margin. The circuit quantities, including θ_Z, corresponding to these operating points are compared with the analytical values in Tables XI and XII along with an additional operating point within $\mathcal{L}$. The simulation and experimental results mutually agree with small deviations from analysis due to the ideality assumption.



(a) (b) (c) (d)

(e) (f) (g) (h)

Fig. 12. LCC-CF operating waveforms over the load range considering the operating points A_L, B_L, C_L, and D_L. Experiments at (a) $V_o = 250$ V, $P_o = 162.5$ W, (b) $V_o = 83$ V, $P_o = 162.5$ W, (c) $V_o = 83$ V, $P_o = 16.25$ W, and (d) $V_o = 250$ V, $P_o = 16.25$ W. Simulations at (e) $V_o = 250$ V, $P_o = 162.5$ W, (f) $V_o = 83$ V, $P_o = 162.5$ W, (g) $V_o = 83$ V, $P_o = 16.25$ W, and (h) $V_o = 250$ V, $P_o = 16.25$ W. For each operating point, the ZVS condition is indicated in terms of the ZVS lag angle, θ_z.

TABLE XI

COMPARISON OF ANALYTICAL (AN.), SIMULATED (SIM.), AND EXPERIMENTAL (EXP.) OUTPUT QUANTITIES AND EFFICIENCY, AND RESPECTIVE ERRORS (ERR.) WITH RESPECT TO EXPERIMENT, AT THE FOUR EXTREME AND ONE INTERIOR OPERATING POINTS (O.P.) OF THE LCC-CF

O.P.	P_o					V_o					η (%)		
	An. (W)	Err. (%)	Sim. (W)	Err. (%)	Exp. (W)	An. (V)	Err. (%)	Sim. (V)	Err. (%)	Exp. (V)	Sim.	Err.	Exp.
$\mathrm{A_L}$	162.5	0.6	160	0.9	161.5	250	0.1	248.1	0.9	250.3	96.96	0.6	96.33
$\mathrm{B_L}$	162.5	0.1	163.2	0.3	162.7	83	0.4	83.2	0.6	82.7	90.07	1.4	88.82
$\mathrm{C_L}$	16.25	0.5	16.13	1.2	16.33	83	0.1	82.7	0.2	82.9	92.70	3.2	89.79
$\mathrm{D_L}$	16.25	0.7	16.3	0.4	16.37	250	0.3	250.5	0.1	250.8	87.63	9.4	80.08
$\mathrm{E_L}$	89.5	1.6	89.5	1.6	91	166.5	1.6	166.6	1.5	169.2	96.24	1.1	95.20

TABLE XII

COMPARISON OF ANALYTICAL (AN.), SIMULATED (SIM.), AND EXPERIMENTAL (EXP.) STEADY-STATE QUANTITIES, AND RESPECTIVE ERRORS (ERR.) WITH RESPECT TO EXPERIMENT, AT THE FOUR EXTREME AND ONE INTERIOR OPERATING POINTS OF THE LCC-CF

O.P.	f_{sw}					θ_Z (^{o})					$i_{L,\mathrm{rms}}$				
	An. (kHz)	Err. (%)	Sim. (kHz)	Err. (%)	Exp. (kHz)	An.	Err.	Sim.	Err.	Exp.	An. (A)	Err. (%)	Sim. (A)	Err. (%)	Exp. (A)
$\mathrm{A_L}$	113.0	9.6	105.0	1.8	103.1	11.7	6.9	6.4	1.6	4.8	3.04	1.0	3.05	1.3	3.01
$\mathrm{B_L}$	90.0	5.0	86.2	0.6	85.7	58.7	6.3	54.6	2.2	52.4	6.21	0.6	6.24	0.2	6.25
$\mathrm{C_L}$	197.5	9.6	183.7	1.9	180.2	75.6	9.4	74.7	8.5	66.2	1.27	1.6	1.33	3.1	1.29
$\mathrm{D_L}$	193.4	9.6	177.9	0.8	176.4	80.0	4.4	80.7	5.1	75.6	2.15	0.9	2.26	4.2	2.17
$\mathrm{E_L}$	133.0	8.0	126.3	2.5	123.2	46.2	4.5	45.0	3.3	41.7	2.48	0.8	2.53	1.2	2.50

The analytically predicted loss components, as well as the analytical breakdown of the experimental power loss, are presented in Fig. 13. The analytical estimates of power loss are obtained using analytical values of the state variables along with measured or datasheet values of nonidealities. The total power loss is measured using a Fluke 6004+ power analyzer. The conduction loss is calculated using device nonidealities obtained from the datasheet, and series resistances of the inductor and the transformer measured using an N4L PSM3750 frequency response analyzer. Experimentally measured currents and voltages are used to calculate the conduction loss and the MOSFET turn-OFF losses from standard formulae [30]. Core losses are computed by substituting the peak flux densities, obtained from the design of the magnetics, into the Steinmetz relation [31].

At relatively high power, corresponding to the operating points A_L, B_L, and E_L defined in Fig. 7(a), the ohmic losses in the semiconductor devices and the magnetics constitute the dominant form of power loss. This validates the minimization of

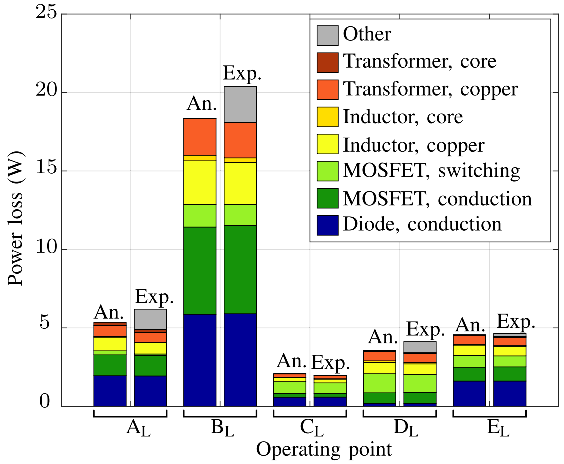


Fig. 13. Analytically predicted loss components (An.) and detailed analytical breakdown of the experimental losses (Exp.) of the LCC-CF for the various operating points.

TABLE XIII
Comparison of the Peak Experimental (Exp.) and Simulated (Sim.) Efficiency of the Proposed Design With Design Approaches in the Literature

Method	Peak efficiency (%)		Output condition	
	Exp.	Sim.	Voltage (V)	Power (W)
Ref. [5]	92.0	-	150k	65k
Ref. [21]	93.68	-	31k	22.9k
Ref. [9]	91.0	-	60k	5k
Ref. [22]	90.15	-	7k	2k
Ref. [26]	-	96.8	220	500
Proposed	96.33	96.96	250	162.5

the rms current as a design objective. The higher proportion of frequency-dependent losses at the low-power operating points, C_L and D_L, is expected due to the relatively high frequency of operation of these points, as given in Table XII. The design exhibits low power loss over a wide range of output voltage and power, with a $> 80\%$ experimental efficiency (η) even with 10% of nominal load at nominal voltage. A deviation from analytical values of switching frequency is required to overcome losses in nonidealities. The worst-case analytical, simulated, and experimental ZVS angles deviate from the design value used in the method outlined in Section III-E, although ZVS is still preserved across all operating points.

The lack of clear quantification of operating efficiency for a number of LCC-CF designs in the literature [5], [12], [14], [24] hinders a direct comparison of their efficiency with that of the proposed design method. Efficiency figures noted from the literature are presented in Table XIII. Across these designs, the operating conditions span more than one order of magnitude for both output voltage and power. The comparative evaluation of efficiency figures for these designs presents challenges, owing to their distinct power and voltage levels. While a fair comparison of efficiency requires comparable voltage and power levels, the obtained efficiency figures are on par with designs in the literature, especially with [26], which considers a comparable voltage and power rating.

The presented results are obtained for a downscaled converter. The interested reader is referred to discussions of high-power designs of the LCC-CF in the literature for a detailed treatment of application-specific challenges of transformer design, insulation, and construction [5], [12], and thermal management [12].

V. CONCLUSION

The concerns regarding the design of RCs with wide output voltage and/or load range are addressed in this article, for the LCC-CF topology. Previous normalization frameworks are systematized and existing steady-state time-domain analysis techniques are extended to cover boundary modes, showing their relevance to boundaries of soft switching. Design-oriented methods for the numerical solution of these modes are outlined. A method of designing the converter subject to load requirements and constraints is proposed and validated in nonideal simulation and experiments for a 250-V, 162.5-W LCC-CF prototype with 10X and 3X variations in output power and output voltage, respectively. A peak experimental efficiency of 96.33% and a maximum error of less than 4.2% between experimental and simulated rms current, demonstrate the efficacy of the design. The step-by-step discussion of the design procedure and related analysis are significant resources for the design of this converter, considering soft switching (ZVS) and minimization of conduction loss over a wide converter output voltage and load range.

APPENDIX

The proposed design method is validated on a prototype whose power and voltage levels are scaled down from the actual ratings entailed by the variable load application. In this context, the scale factor (χ) is defined as the ratio of a scaled physical quantity to the actual physical quantity. The scale factors for voltage (χ_V) and power (χ_P), used in this article, are equal to 0.1 and 0.01, respectively. Thus, the scaling of the prototype in this article satisfies the relation given by

$$\chi_V^2 = \chi_P. \tag{17}$$

The outputs of the proposed characteristic-based design algorithm depend only on the design inputs. Thus, the design outcomes are different in the actual and scaled cases only if the two cases have different design inputs. The design inputs to the algorithm described in Section III are the parameters, μ_L, μ_H, σ_L, σ_H, $f_{\min}$, $f_{\max}$, and θ_Z.

The parameters, μ_H, μ_L, and θ_Z, are dimensionless, and hence, invariant under scaling. The frequency limits, $f_{\min}$ and $f_{\max}$, are not directly affected by the scaling of the voltage and power levels, and are, therefore, assumed to be independent of scaling. The design inputs, σ_L and σ_H, possess dimensions of impedance. The scale factor (χ_Z) for impedance is related to the scale factors for voltage and power, as

$$\chi_Z = \chi_V^2 / \chi_P. \tag{18}$$

If the scaling is performed in a way such that (17) is satisfied, the actual and scaled values are the same for any quantity with the dimension of impedance, i.e., $\chi_Z = 1$. Thus, for the power and voltage scaling presented in this article, impedance-like quantities are identical in the actual and scaled designs. The design inputs, σ_L and σ_H, are also the same.

Thus, the outcomes of the proposed design method, i.e., n, L_s, C_s, and C_p, and other circuit parameters, remain identical for both the actual and scaled designs corresponding to the respective ratings given in Table VI.

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