An Impedance-Source-Based Soft-Switched High Step-Up DC–DC Converter With an Active Clamp

Saeed Habibi, *Graduate Student Member, IEEE*, Ramin Rahimi, *Member, IEEE*, Mehdi Ferdowsi, *Senior Member, IEEE*, and Pourya Shamsi, *Senior Member, IEEE*

***Abstract*—This article proposes a high step-up dc–dc converter based on a trans-inverse impedance-source structure, in which the voltage gain of the converter is increased by using a lower number of turns ratio of the coupled inductors (CI) windings. The proposed converter achieves a very high voltage gain and a very low voltage stress on the switches. An active clamp is incorporated into the topology of the proposed converter, helping to absorb the energy of the leakage inductances of the CI, and to recycle that energy to the output of the converter to further increase the voltage gain. Furthermore, the active clamp is used to realize soft turn ON for the main switch of the converter. Additionally, the clamp switch also turns ON under zero voltage switching condition. Apart from the soft turn ON of the switches of the proposed converter, the diodes of the converter also turn OFF with a minimized reverse recovery power loss because of the controlled current falling rate of these diodes with the leakage inductance of the CI. The operation principle, steady-state analysis, and comparison are presented in this article. Also, the analysis is verified using a 200 W, and 20 V to 400 V experimental setup.**

***Index Terms*—Active clamp, coupled inductor, dc–dc converter, high step-up, impedance source.**

I. Introduction

DUE to the adverse climate effects resulting from fossil fuel use, the expansion of renewable energy is inevitable. Because of the intermittent nature of renewable energy resources such as photovoltaic (PV) and wind, energy storage systems using fuel cells and batteries are required for the successful transition from fossil fuels to clean energy. Among renewable energy resources, PV energy generation has gained popularity in the recent decade [1], [2]. Due to the relatively low voltage of the PV panels (typically less than 50 V), a dc–dc converter with a high voltage conversion ratio is required to connect PV panels to a dc-bus of a grid-connected inverter or a dc microgrid (e.g., 380 V, 400 V, or higher voltage levels) [3], [4]. A similar situation exists for the fuel cell energy storage systems [5], making high conversion ratio dc–dc converters essential for moving toward clean energy generation, and storage. For these types of applications, the conventional boost converter is not suitable because it has limited voltage gain and high losses occur when operating at extreme duty cycles [6].

Different voltage boosting techniques such as switched-capacitor (SC), voltage multiplier (VM) cells, switched-inductor (SI), and coupled inductors (CI) have been integrated into the basic step-up converters to achieve a high voltage conversion ratio [7], [8]. The integration of SC and VM cells to step-up converters provides a high voltage at the output of the converter. However, these cells only add a static gain to the converters. Therefore, for a higher voltage at the output, a greater number of cells is required [9]. Integrating SI cells into the basic converters provides higher voltage gain than converters based on SC and VM cells, but because of the high number of magnetic cores, the power density of these converters is low [10].

The combination of the CI with other voltage boosting techniques helped to derive converters that achieve a high voltage conversion ratio at a medium or low duty cycle. Another advantage of these converters is the low voltage stress on the power switch, which reduces the switching power loss [11]. Also, in these converters, lower voltage ratings are required for the power switch, leading to the selection of a MOSFET with lower $R_{DS(\,\mathrm{ON})}$, and lower conduction loss. However, these topologies require a high number of turns ratio to achieve a very high voltage gain, resulting in large magnetic components with considerable leakage inductances [12], [13]. Handling the stored energy in these large leakage inductances becomes challenging at the turn OFF instances of the power switch; therefore, passive and active snubbers are used to prevent voltage spikes on the power switches and recycle that energy to further increase the voltage gain of the converter [13].

Unlike the conventional CI-based high step-up dc–dc converters, in which the voltage gain increases by using a higher number of turns ratio for the CI, some impedance-source-based converters achieve higher voltage gain by using a lower number of turns ratio for the CI. Based on this concept, a trans-inverse converter was presented in [14]. This converter can achieve a high voltage gain at a low duty cycle, but the major drawback of this converter is that the duty cycle range of the converter is limited, and it depends on the turn ratio of the CI. Two improved trans-inverse converters are presented in [14] and [15], in which the duty cycle range is extended. However, insufficient voltage gain and hard switching of their power switch are major drawbacks of these converters. The converters in [14] and [15] use two-winding CIs in their structure. Recently, improved

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The authors are with the Department of Electrical and Computer Engineering, Missouri University of Science and Technology, Rolla, MO 65409 USA (e-mail: s.habibi@mst.edu; r.rahimi@mst.edu; ferdowsi@mst.edu; shamsip@mst.edu).

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trans-inverse converters with three-winding CIs are presented in [16], [17], and [18]. These converters use the trans-inverse structure along with the voltage multiplier cells to increase the voltage gain of the converter. With the help of quasi-resonance operation in these converters, zero current turn ON is achieved for the power switch.

Another category of impedance-source-based converters that has a similar operating principle to the trans-inverse structure is Y-source high step-up dc–dc converters [19], [20]. However, Y-source converters have three-winding CIs. The third winding in the Y-source converters is used to further increase the voltage gain of the converters. Y-source converters usually have high voltage stress on the power switch [21]. However, by shifting the power switch to the input side and integrating VM cells into the Y-source converters, high-performance converters are derived [22], [23], [24], [25]. Converters in [22], [23], and [24] utilize a passive clamp to absorb the energy of the leakage inductance of the CI and the converter in [25] uses an active clamp. A major drawback of the converters in [22] and [24] is the lack of soft switching for the main power switch of these converters. Also, the converter in [24] has a limited duty cycle range ($0 < D < 0.5$), resulting in a steep voltage gain curve. Another converter that uses a Y-source connection in its structure is presented in [26]. Although this converter has high voltage gain and zero voltage turn ON for the power switches, it has a high ripple input current, which may degrade the lifetime of PV panels and fuel cell stacks [14], limiting the applications of this converter.

Impedance source converters using passive and active clamps have been proposed in the literature [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29]. Compared to the active clamps, passive clamps have a simple structure and may have slightly higher power loss. Moreover, in some of the impedance source-based high step-up converters, the parasitic capacitance of the clamp diode, when it is OFF, might form an unwanted resonance loop in the circuit [16].

Considering the advantages and disadvantages of different topologies, an impedance-source-based high step-up dc–dc converter is proposed in this article. The characteristics of the proposed converter and contributions of this article are as follows.

1) The proposed converter uses a three-winding CI, in which two windings are used to achieve the trans-inverse structure and the third one is utilized to further increase the voltage gain of the converter and keep the voltage stress on the power switch low.
2) The proposed converter uses an active clamp circuit to absorb the leakage inductance energy during the turn OFF instances of the main power switch. The active clamp helps to achieve zero voltage switching (ZVS) for the main power switch, and the body diode of the main switch helps to achieve ZVS for the clamp switch.
3) The proposed converter has higher flexibility in design. That is the output voltage on the converter can be controlled by three parameters: the duty cycle of the main switch, the difference in the number of turns of the secondary and primary windings, and the turn ratio of the tertiary to primary windings.

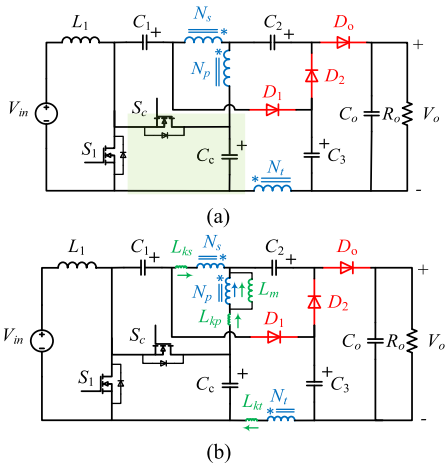

Fig. 1. Proposed high step-up DC–DC converter and its equivalent circuit. (a) Proposed converter. (b) Equivalent circuit.

4) The clamp capacitor voltage is controlled only by the duty cycle. Therefore, the voltage stress on the main and auxiliary power switches, which are equal to the voltage of the clamp circuit, can be set to be very low voltage while the converter provides a very high voltage gain.
5) The low voltage stress on the power switches helps to minimize the switching and conduction losses in the power switches.
6) The diodes used in this topology turn OFF with a minimized reverse recovery loss, which is the result of controlling the falling rate of the diode current by the leakage inductances of the CI. These desired characteristics make the proposed converter a suitable candidate for PV to dc microgrid and PV to ac grid applications.

The rest of this article is organized as follows. The topology of the proposed converter is presented in Section II. The operation principle and the steady-state analysis of the proposed converter are carried out in Section III. A comparison study between the proposed converter and the existing converters is provided in Section IV. The design considerations of the proposed converter and the experimental results of the converter are included in Sections V and VI, respectively. Finally, Section VII concludes this article.

II. Proposed High Step-Up DC–DC Converter

The proposed converter is shown in Fig. 1(a). The proposed converter has a three-winding CI, three diodes (D_1, D_2, and D_o), five capacitors (C_c, C_1, C_2, C_3, and C_o), one main switch (S_1), and one auxiliary switch (S_c) for the active clamp circuit. S_c along with C_c form the active clamp for the main switch. The clamp circuit (S_c and C_c) is highlighted in Fig. 1(a). The equivalent circuit of the proposed converter is shown in Fig. 1(b). In the equivalent circuit, the CI is replaced by a three-winding ideal transformer. A parallel inductance is added to the primary winding of the transformer as the magnetizing inductance (L_m). Three series inductances (L_{kp}, L_{ks}, and L_{kt}) acting as the leakage inductance of each winding are added to the equivalent circuit

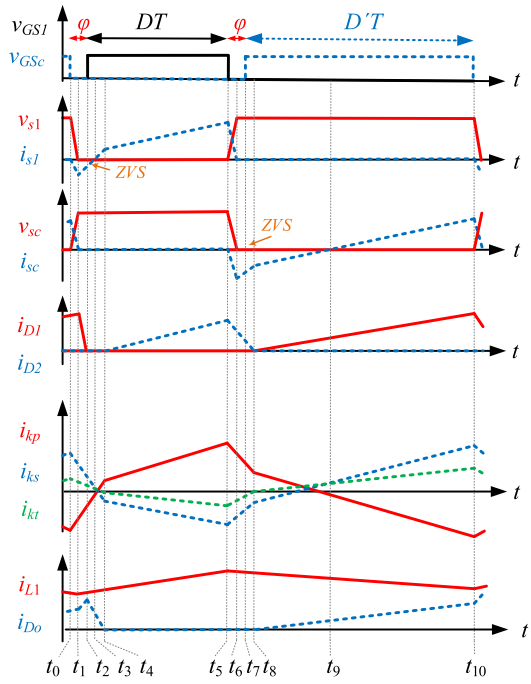

Fig. 2. Ideal key waveforms of the proposed converter.

model. The turns ratio between the secondary to the primary winding is denoted by $n_{21} = N_s/N_p$ and the turns ratio between the tertiary to the primary winding is denoted by $n_{31} = N_t/N_p$, and the magnetizing reference is shown by "$*$".

III. Operation Principle and Steady-State Analysis of the Proposed Converter

The proposed converter has two power switches that turn ON complementary with a time delay between the gate signals. The gate-source signals (v_{GS1} and v_{GSc}) are shown in Fig. 2. The duty cycle of the gate signals of the main and clamp switches are D and D', respectively. After each gate signal, there is a time delay of φ that is required for soft switching realization. The voltage and current waveforms of the power switches along with the current waveforms of the diodes and CI windings are shown in Fig. 2. Based on this figure, there are ten operating modes for the proposed converter. These operating modes are discussed in the following. Three assumptions are used to develop the steady-state analysis for this converter as follows:

1) the converter operates in the continuous conduction mode;
2) the capacitors are large enough to keep the voltage constant during a switching cycle;
3) the parasitic elements of the components are ignored except for the leakage inductance of the CI.

A. Operating Modes

Mode 1 ($t_0 < t < t_1$): Prior to this mode, the clamp switch (S_c) was ON, and at $t = t_0$, S_c turns OFF by the gate signal. The parasitic capacitance of S_c (C_{Sc}) starts to charge and the capacitance of S_1 (C_{S1}) starts to discharge until the voltage on C_{S1} reaches almost zero. Then, the body diode of S_1 turns ON and the circuit moves to the next mode. The circuit configuration of this mode is shown in Fig. 3(a).

Mode 2 ($t_1 < t < t_2$): During this mode, both power switches are OFF. At the beginning of this mode ($t = t_1$), the body diode of S_1 starts to conduct, which makes the voltage on S_1 equal to zero. At the end of this mode, diode D_1 turns OFF. The current equation for D_1 is presented in (1), showing that the falling rate of the diode is controlled by the leakage inductances of the CI, which minimizes the reverse recovery power loss for the diode D_1. The circuit configuration of this mode is shown in Fig. 3(b)

$$i_{D_1}(t) = i_{D_1}(t_0) + \left(\frac{V_o + V_{C_1} - V_{C_2} - V_{C_3} - V_{C_c} - V_{L_m}}{L_{kp}} + \frac{V_{C_1} - V_{C_3} + n_{31} V_{L_m}}{L_{kt}} + \frac{V_{C_2} + V_{C_3} - V_o + n_{21} V_{L_m}}{L_{ks}} \right) \times (t - t_0) \tag{1}$$

Mode 3 ($t_2 < t < t_3$): Prior to this mode, the body diode of S_1 was conducting, and at $t = t_2$ the gate signal of S_1 (v_{GS1}) changes from low to high and turns S_1 ON. Therefore, S_1 turns ON under ZVS condition. The circuit configuration of this mode is shown in Fig. 3(c). The circuit stays in this mode until the current direction changes and the body diode of S_1 stops conducting.

Mode 4 ($t_3 < t < t_4$): During this mode, S_1 and D_o are conducting. The circuit stays in this mode until D_o current reaches zero. The current equation for D_o is presented in (2), and as the current equation shows, the falling rate of D_o is controlled by L_{kt} inductance, minimizing the reverse recovery loss

$$i_{D_o}(t) = i_{D_o}(t_3) + \frac{V_{C_2} + V_{C_c} - V_o - (n_{31} + 1) V_{L_m} - V_{L_{kp}}}{L_{kt}} (t - t_3). \tag{2}$$

Mode 5 ($t_4 < t < t_5$): At $t = t_4$ the current in the tertiary winding reaches zero, and then it flows in the opposite direction. Consequently, D_o turns OFF, and D_2 turns ON. In this mode, the input and the magnetizing inductors are energized. The voltage equations in this mode are presented in (3). The circuit configuration of this mode is shown in Fig. 3(e). The circuit stays in this mode until S_1 is turned OFF by the gate signal

$$\begin{cases} V_{L_1} = V_{in} \\ (1 - n_{21}) V_{L_m} + V_{kp} + V_{ks} = V_{C_c} - V_{C_1} \\ (1 + n_{31}) V_{L_m} + V_{kp} - V_{kt} = V_{C_2} + V_{C_c} - V_{C_3}. \end{cases} \tag{3}$$

Mode 6 ($t_5 < t < t_6$): At $t = t_5$ switch S_1 turns OFF with the gate signal command and C_{S1} and C_{Sc} start to charge and discharge, respectively. The voltage on S_c drops to zero and then, the body diode of S_c starts to conduct. The circuit configuration of this mode is shown in Fig. 3(f).

Mode 7 ($t_6 < t < t_7$): At the beginning of this mode, the body diode of the S_c starts to conduct. During this mode, the gate signals of both switches are OFF. The equivalent circuit of this mode is shown in Fig. 3(g).

Mode 8 ($t_7 < t < t_8$): At $t = t_7$ the power switch of the clamp circuit (S_c) turns ON with the gate signal, and because the body diode of this switch was already conducting, the switch turns

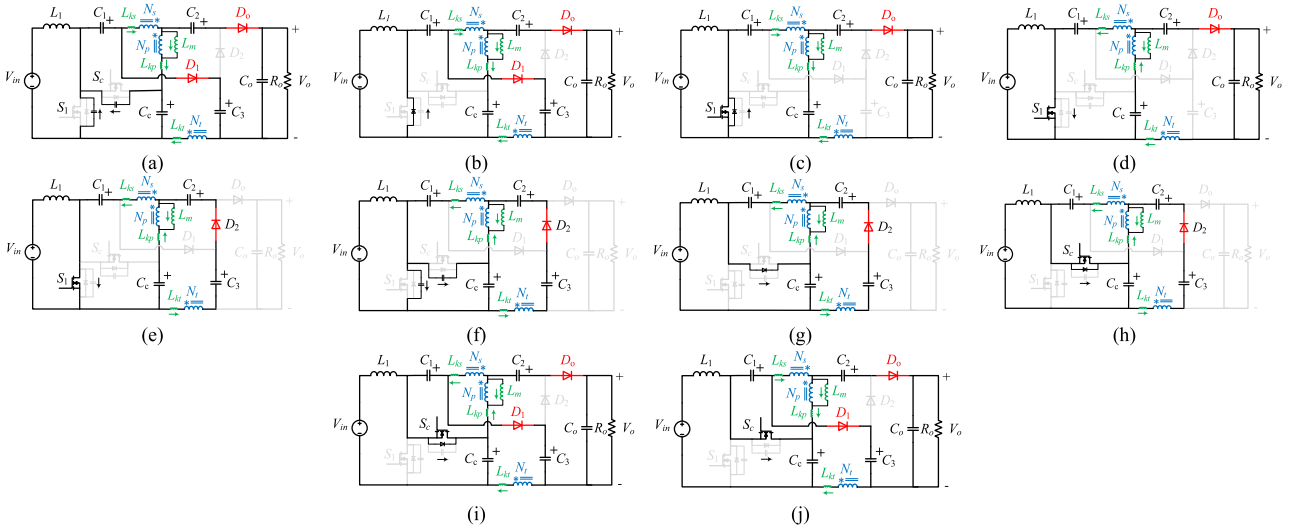

Fig. 3. Operating modes of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8. (i) Mode 9. (j) Mode 10.

ON at ZVS condition. The circuit configuration of this mode is shown in Fig. 3(h). The circuit stays in this mode until D_2 stops conducting. The current equation for D_2 is presented in (4), showing that the falling rate of the diode current is controlled with L_{kt}

$$i_{D_2}(t) = i_{D_2}(t_6) + \frac{V_{C_3} - V_{C_2} - V_{C_c} + (1+n_{31})V_{L_m} + V_{L_{kp}}}{L_{kt}}(t - t_6). \tag{4}$$

Mode 9 ($t_8 < t < t_9$): At $t = t_8$ the current of the tertiary winding reaches zero and starts to conduct in the opposite direction, therefore, D_2 turns OFF, and D_1 and D_o turn ON. During this mode, the input and magnetizing inductors are discharged. The voltage equation of these inductors is presented in (5). The circuit stays in this mode until the body diode of S_c stops conducting. The circuit configuration of this mode is shown in Fig. 3(i)

$$\begin{cases} V_{L_1} = V_{in} - V_{C_c} \\ (1-n_{21})V_{L_m} + V_{kp} + V_{ks} = -V_{C_1} \\ n_{31}V_{L_m} + V_{kt} = V_{C_1} + V_{C_c} - V_{C_3} \\ (1+n_{31})V_{L_m} + V_{kt} - V_{kp} = V_{C_2} + V_{C_c} - V_o. \end{cases} \tag{5}$$

Mode 10 ($t_9 < t < t_{10}$): This mode is similar to Mode 9 except for the current direction of S_c. The voltage equations of this mode and Mode 9 are identical, as presented in (5). The circuit configuration for this mode is shown in Fig. 3(j), and the circuit stays in this mode until S_c is turned OFF by the gate signal.

The operating modes of the proposed converter are described in this section. The voltage equations that are required to derive the steady-state analysis are also presented in (3) and (5).

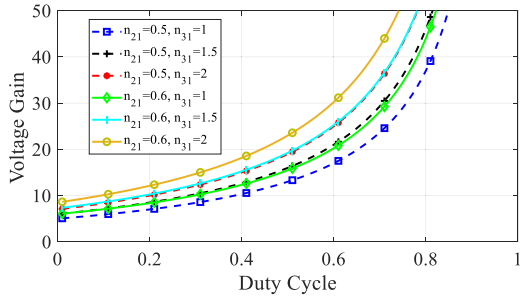

Fig. 4. Voltage gain of the proposed converter for different combinations of n_{21} and n_{31}.

B. Voltage Gain

Among the ten operating modes of the proposed converter, modes 1, 2, 3, 4, 6, 7, and 8 have very short durations compared to the durations of modes 5, 9, and 10. That is because modes 1, 2, 3, 4, 6, 7, and 8 are considered transitional modes, and modes 5, 9, and 10 are considered dominant modes. By ignoring the voltage drop on the leakage inductances and using the voltage equations of the dominant modes, and then applying the volt-second balance principle, the voltage of the capacitors is found in (6).

Using the voltage of the capacitors, the ideal voltage gain of the converter is found and presented in (7). Also, the voltage gain of the converter for different combinations of n_{21} and n_{31} is plotted in Fig. 4. As can be seen from Fig. 4, even with a very low turns ratio for the CI ($n_{21} = 0.5$ and $n_{31} = 1$), a high voltage gain such as 20 can be achieved in medium duty cycles ($D < 0.7$) with this converter

$$\begin{cases} V_{C_c} = \frac{1}{1-D} V_{\text{in}} \\ V_{C_1} = \frac{D}{1-D} V_{\text{in}} \\ V_{C_2} = \frac{1+n_{31}-n_{21}D}{(1-n_{21})(1-D)} V_{\text{in}} \\ V_{C_3} = \frac{(1-n_{21})(1+D)+n_{31}D}{(1-n_{21})(1-D)} V_{\text{in}} \end{cases} \tag{6}$$

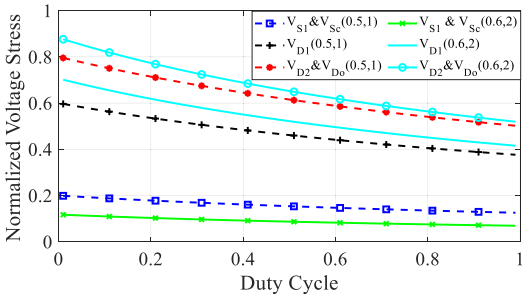

Fig. 5. Normalized voltage stress on the semiconductor devices for two different combinations of (n_{21}, n_{31}).

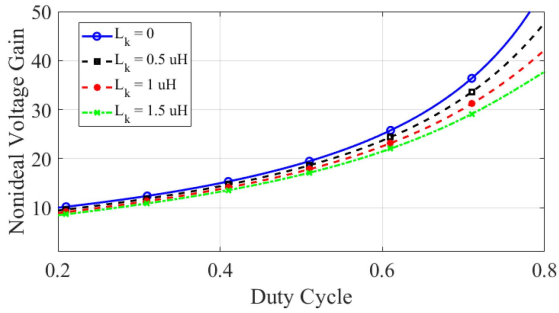

Fig. 6. Nonideal voltage gain of the converter for different values of leakage inductances.

$$G = \frac{V_o}{V_{\text{in}}} = \frac{1+(1+n_{31}-n_{21})(1+D)}{(1-n_{21})(1-D)}. \tag{7}$$

D. Voltage Stress Across Semiconductor Devices

The voltage stress on both power switches is equal to the voltage of C_c. The normalized voltage stress of the switches to the output voltage is presented in (8). The maximum voltage stress on D_1, D_2, and D_o occur in Mode 3, Mode 6, and Mode 3, respectively. Using the voltage of the capacitors in (6), the normalized voltage stress on the diodes to the output voltage is found in (9). The voltage stress on the semiconductor devices for two different combinations of (n_{21}, n_{31}) are illustrated in Fig. 5. As depicted in Fig. 5, the power switches have a very low voltage stress throughout the duty cycle range. By increasing the turns ratio of the CI from ($n_{21} = 0.5$ and $n_{31} = 1$) to ($n_{21} = 0.6$ and $n_{31} = 2$), the normalized voltage stress on the power switches becomes even smaller. However, this change slightly increases the normalized voltage stress on the diodes

$$\frac{V_{S_1}}{V_o} = \frac{V_{S_c}}{V_o} = \frac{1-n_{21}}{1+(1+n_{31}-n_{21})(1+D)}. \tag{8}$$

E. Current Stress on Semiconductor Devices

By conducting the average current analysis on this topology, the average current stresses on the semiconductor components, the average current in the windings and magnetizing inductance of the CI are found in (10)

$$\begin{cases} \frac{V_{D_1}}{V_o} = \frac{1+n_{31}-n_{21}}{1+(1+n_{31}-n_{21})(1+D)} \\ \frac{V_{D_2}}{V_o} = \frac{1+n_{31}}{1+(1+n_{31}-n_{21})(1+D)} \\ \frac{V_{D_o}}{V_o} = \frac{1+n_{31}}{1+(1+n_{31}-n_{21})(1+D)}. \end{cases} \tag{9}$$

F. Voltage Gain Drop Due to the Leakage Inductance of the CI

In Section III-B, the ideal voltage gain of the proposed converter was derived by ignoring the leakage inductances voltage drop. However, there are always leakage inductances associated with the CI windings. By assuming a negligible current ripple for the magnetizing inductance of the CI, the nonideal voltage gain ($\breve{G}$) of the proposed converter is found in (11). The parameter X is defined in (12), which is a linear combination of the leakage inductances. By assuming $n_{21} = 0.5$ and $n_{31} = 2$, the output resistance (R_o) equal to 800 Ω, and the switching frequency (f_{sw}) of 50 kHz, the nonideal voltage gain of the proposed converter is plotted for different values of the leakage inductances in Fig. 6. In this figure, the leakage inductance of the CI windings assumed to be equal

$$\begin{cases} \frac{I_{D_1}}{I_o} = \frac{I_{D_2}}{I_o} = \frac{I_{D_o}}{I_o} = \frac{I_{S_C}}{I_o} = 1 \\ \frac{I_{L_{kp}}}{I_o} = \frac{I_{L_{ks}}}{I_o} = \frac{I_{L_{kt}}}{I_o} = 1 \\ \frac{I_{N_p}}{I_o} = n_{21} - n_{31} \\ \frac{I_m}{I_o} = 1 - n_{21} + n_{31} \\ \frac{I_{S_1}}{I_o} = \frac{1+m+(2-2n+m)D}{(1-n)(1-D)} \end{cases} \tag{10}$$

$$\breve{G} = \frac{1+(1+n_{31}-n_{21})(1+D)}{(1-n_{21})(1-D)\left(1+\frac{2f_{sw}}{DR_o}X\right)} \tag{11}$$

$$X = \frac{(n_{21}+(1+D)n_{31})(n_{21}+2n_{31})}{(1-n_{21})^2(1-D)^2} L_{kp} + \frac{(1+(1+D)n_{31})(1+2n_{31})}{(1-n_{21})^2(1-D)^2} L_{ks} + \frac{2(1+D)}{1-D} L_{kt}. \tag{12}$$

IV. Comparison With Existing Converters

To develop a comparison between the proposed converter and other existing converters, different parameters such as voltage gain, component count, voltage stress on the power switch, maximum voltage stress on the diode, input current ripple, and soft switching characteristics of converters are considered.

To establish a comprehensive and fair illustrative comparison, the total number of turns ratio for CI windings in the converters listed in Table I is assumed to be 2.5. The denominators of the voltage gain equations for certain converters in Table I comprise two components: The first part, expressed in the general form of (1-n) or (n-1), depends on the difference of the CI windings number of turns, and the second part is (1-D). In the following, the authors have explored various combinations of numbers for

TABLE I
COMPARISON OF THE PROPOSED CONVERTER WITH EXISTING CONVERTERS

Converter	Voltage gain (V_o/V_{in})	Component count		Normalized voltage stress on power switch	Maximum normalized voltage stress on diodes	Input current ripple	Soft switching of the main power switch
		S/L/C/D/CL$^{(NW)}$	Total				
Proposed	$\frac{1+(1+n_{31}-n_{21})(1+D)}{(1-n_{21})(1-D)}$	2/1/5/3/1$^{(3)}$	12	$\frac{(1-n_{21})}{1+(1+n_{31}-n_{21})(1+D)}$	$\frac{1+n_{31}}{1+(1+n_{31}-n_{21})(1+D)}$	Low	ZVS-Turn ON
[16]	$\frac{2+D+n_{31}(2-D)-n_{21}}{(1-n_{21})(1-D)}$	1/1/6/5/1$^{(3)}$	14	$\frac{1-n_{21}}{2+D+n_{31}(2-D)-n_{21}}$	$\frac{1+n_{31}}{2+D+n_{31}(2-D)-n_{21}}$	Low	ZCS-Turn ON
[17]	$\frac{1+2n_{31}-n_{21}}{(n_{31}-n_{21})(1-D)}$	1/1/5/4/1$^{(3)}$	12	$\frac{n_{31}-n_{21}}{1+2n_{31}-n_{21}}$	$\frac{1+n_{31}}{1+2n_{31}-n_{21}}$	Low	ZCS-Turn ON
[18]	$\frac{2+n_{21}(2-D)-n_{31}(1+D)}{(1-n_{31})(1-D)}$	1/1/5/4/1$^{(3)}$	12	$\frac{1-n_{31}}{2+n_{21}(2-D)-n_{31}(1+D)}$	$\frac{1-n_{31}+n_{21}}{2+n_{21}(2-D)-n_{31}(1+D)}$	Low	ZCS-Turn ON
[22]	$\frac{1+n_{21}+D}{(1-n_{31})(1-D)}$	1/1/5/4/1$^{(3)}$	12	$\frac{1-n_{31}}{1+n_{21}+D}$	$\frac{1+n_{21}}{1+n_{21}+D}$	Low	-
[23]	$\frac{2+D+(n_{31}-n_{21})}{(1-n_{21})(1-D)}$	1/1/5/4/1$^{(3)}$	12	$\frac{1-n_{21}}{2+D+(n_{31}-n_{21})}$	$\frac{1+n_{31}}{2+D+(n_{31}-n_{21})}$	Low	ZCS-Turn ON
[25]	$\frac{2+n_{21}-n_{31}}{(1-n_{31})(1-D)}$	2/1/4/2/1$^{(3)}$	10	$\frac{1-n_{31}}{2+n_{21}-n_{31}}$	$\frac{1+n_{21}}{2+n_{21}-n_{31}}$	Low	ZVS-Turn ON
[26]	$\frac{2(1+n_{21}+n_{21}D)}{1-D}$	2/0/5/3/2$^{(2)}$	13	$\frac{1}{2(1+n_{21}+n_{21}D)}$	$\frac{1+n_{21}}{2(1+n_{21}+n_{21}D)}$	High	ZVS-Turn ON
[27]	$\frac{2+n_{31}-n_{21}}{(1-n_{21})(1-D)}$	2/1/4/2/1$^{(3)}$	10	$\frac{1-n_{21}}{2+n_{31}-n_{21}}$	$\frac{1+n_{31}}{2+n_{31}-n_{21}}$	Low	ZVS-Turn ON
[28]	$\frac{1+(n_{21}+1)D}{1-D}$	1/1/3/2/1$^{(2)}$	8	$\frac{1}{1+(n_{21}+1)D}$	$\frac{n_{21}+1}{1+(n_{21}+1)D}$	Low	-
[29]	$\frac{1+n_{21}+n_{31}+D}{(1-D)n_{21}}$	1/1/5/4/1$^{(3)}$	12	$\frac{n_{21}}{1+n_{21}+n_{31}+D}$	$\frac{1+n_{31}}{1+n_{21}+n_{31}+D}$	Low	-

n_{21} and n_{31} to ensure that the first part of the denominators is equal to 0.4 for all converters, thereby confirming a fair and meaningful comparison. Therefore, for the proposed converter and converters in [16], [23], and [27], the turn ratios are $n_{21} = 0.6$ and $n_{31} = 1.9$. For converters in [18], [22], and [25], the turn ratios are $n_{31} = 0.6$ and $n_{21} = 1.9$. For the converter in [17], $n_{21} = 1.05$ and $n_{31} = 1.45$, for the converters in [26] and [28] with a two winding CI, $n_{21} = 2.5$, and for the converter in [29], $n_{21} = 0.4$ and $n_{31} = 2.1$ is used. Using these numbers for the turns ratio of CIs, the voltage gain of these converters is plotted in Fig. 7(a). The normalized voltage gain to the total component count is also plotted in Fig. 7(b). Considering Fig. 7(a), the proposed converter has a higher voltage gain than other competitors except for the converter in [16] within $D < 0.6$ and [18] for $D < 0.4$. However, by taking the total number of components into account [see Fig. 7(b)], the proposed converter has higher voltage gain than these two converters for $D > 0.4$, which accounts for the majority of the proper operation region of these converters. The comparison of the normalized voltage stress on the power switch and the maximum normalized maximum voltage stress on diodes are plotted in Fig. 8(a) and (b), respectively. Considering these two figures, the proposed converter has lower voltage stress compared to the other converters for the duty cycle range of $D > 0.4$, except for the converter in [16], which has higher number of components than the proposed converter. Similarly, the proposed converter has a good performance considering the maximum voltage stress on diodes. The only converter that has lower voltage stress on the diode is the converter in [27]. However, this converter has a greater component count and a high input current ripple.

The total component count of the proposed converter is only greater than the converters in [25], [27], and [28]. However, these converters have lower voltage gain and high voltage stress on the semiconductors. Also, the proposed converter provides a low ripple input current and soft turn ON for the main and clamp power switches. Considering these factors, it can be concluded that the proposed converter has obvious advantages over the existing converters, and it is a suitable candidate for renewable energy applications.

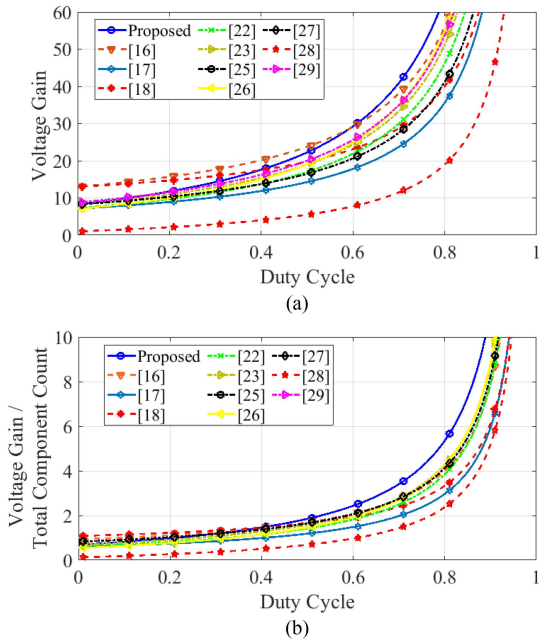

Fig. 7. Voltage gain comparison. (a) Voltage gain of the proposed converter and existing converters. (b) Normalized voltage gain comparison.

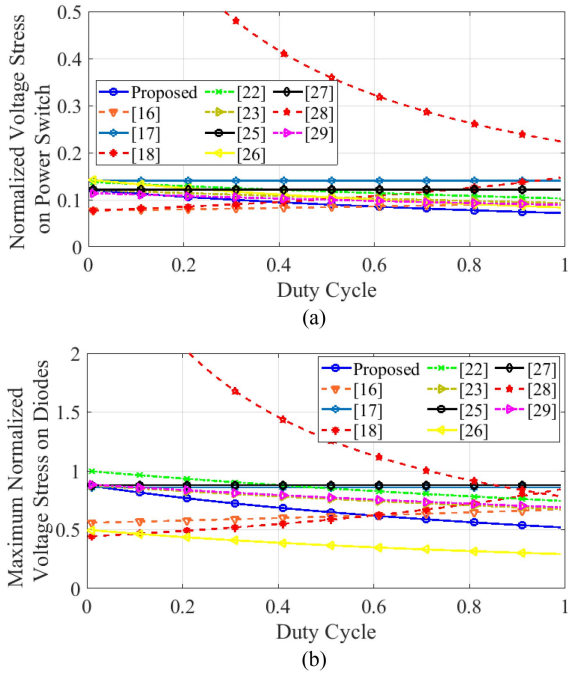

Fig. 8. Comparison of, (a) normalized voltage stress on power switch, (b) normalized maximum voltage stress on diodes.

TABLE II
COMPARISON OF EXPERIMENTAL SETUP PARAMETERS

Converter	V_{in} (V)	V_o (V)	P_o (W)	f_{sw} (kHz)	η (%)	Normalized input current ripple ($\frac{\Delta I_{in}}{I_{in}}$)
Proposed	20	400	200	50	94	$\frac{R_o}{f_{sw}L_1}\frac{(1-n_{21})G+n_{21}-2-n_{31}}{G^2((1-n_{21})G+1+n_{31}-n_{21}}$
[16]	25	400	400	60	93.5	$\frac{R_o}{f_{sw}L_1}\frac{(1-n_{21})G+n_{21}-2-2n_{31}}{G^2((1-n_{21})G+1-n_{31})}$
[17]	20	200	160	50	96.6	$\frac{R_o}{f_{sw}L_1}\frac{(n_{31}-n_{21})G+n_{21}-1-2n_{31}}{G^3(n_{31}-n_{21})}$
[18]	20	250	200	nr	94.4	$\frac{R_o}{f_{sw}L_1}\frac{(1-n_{31})G-2n_{21}-2+n_{31}}{G^2((1-n_{31})G-n_{21}-n_{31})}$
[22]	28	380	200	50	94.9	$\frac{R_o}{f_{sw}L_1}\frac{(n_{31}-1)G+n_{21}+1}{G^2((n_{31}-1)G-1)}$
[23]	20	250	200	60	94.8	$\frac{R_o}{f_{sw}L_1}\frac{(n_{21}-1)G+n_{31}-n_{21}+2}{G^2((n_{21}-1)G-1)}$
[25]	28	380	200	100	95.8	$\frac{R_o}{f_{sw}L_1}\frac{(n_{31}-1)G-n_{31}+n_{21}+2}{G^2((n_{31}-1)G)}$
[26]	22	400	500	50	95.11	-
[27]	25	400	200	50	95.2	$\frac{R_o}{f_{sw}L_1}\frac{(n_{21}-1)G+n_{31}-n_{21}+2}{G^2((n_{21}-1)G)}$
[28]	20	200	200	100	93.8	$\frac{R_o}{f_{sw}L_1}\frac{G-1}{G^2(G+n_{21}+1)}$
[29]	28.5	400	200	50	94.1	$\frac{R_o}{f_{sw}L_1}\frac{Gn_{21}-n_{21}-n_{31}-1}{G^2(Gn_{21}1)}$

The experimental setup parameters such as the input voltage, output voltage, frequency, and efficiency along with the normalized input current ripple are presented in Table II for the compared converters. Based on Table II, the proposed converter achieves a high efficiency of %94 at a higher voltage conversion ratio than other converters. Also, the normalized input current ripple is plotted for the converters in Table II in Fig. 9. As can

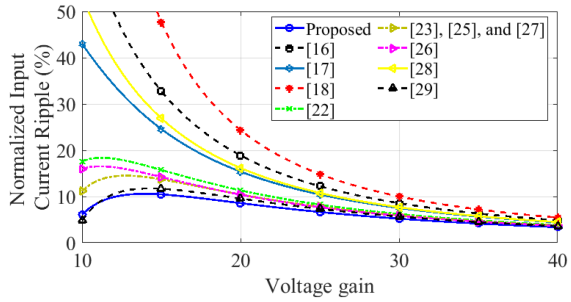

Fig. 9. Comparison of normalized input current ripple versus voltage gain.

be seen from Fig. 9, the proposed converter has the lowest normalized input current ripple. For the plots, the following parameters are assumed: $R_o = 800\ \Omega$, $f_{sw} = 50$ kHz, and $L_1 = 200$ uH.

V. DESIGN CONSIDERATIONS

In this section, design guidelines for the proper operation of the proposed converter and soft switching realization of the switches are presented.

A. Passive Components

Most renewable applications such as PV energy generation require a low input ripple for the high step-up dc–dc converters. Therefore, by considering $\alpha\%$ ripple for the input current, the minimum value for the input inductor is found in

$$L_1 \geq \frac{(1-n_{21})^2 (1-D) R_o}{f_{sw} (\alpha\%) (1+(1+n_{31}-n_{21})(1+D))^2}. \quad (13)$$

Similarly, by assuming $\beta\%$ ripple for the magnetizing inductance, the required value for the magnetizing inductance is found in (14) Also, to keep i_{Lm} positive during a switching cycle, L_m must be larger than the critical value ($L_{m,c}$) in (15)

$$L_m \geq \frac{(1+(1+n_{31}-n_{21})(1+D))(1+D) R_o D}{fsw (\beta\%) (1+n_{31}-n_{21})(1-n_{21})(1-D)} \quad (14)$$

$$L_{m,c} = \frac{D(1-D) R_o}{2f_{sw}(1+n_{31}-n_{21})(1+(1+n_{31}-n_{21})(1+D))}. \quad (15)$$

By considering that the maximum voltage stress on the power switch and the maximum input voltage are $V_{S(\max)}$ and $V_{\text{in}(\max)}$, the relationship between the turns ratio of the CI and voltage gain of the converter can be found in

$$\frac{G(1-n_{21})-(2+n_{31}-n_{21})}{G(1-n_{21})+(1+n_{31}-n_{21})} < 1 - \frac{V_{\text{in}(\max)}}{V_{S(\max)}}. \quad (16)$$

To find the minimum required capacitance value, the average current passing through the capacitors during Mode 5 is used. For each capacitor, the allowable voltage ripple is assumed to be $\gamma\%$ of its nominal voltage. The capacitor value requirements

for the proposed converter are found in

$$\begin{cases} C_c \geq \frac{(1+(1+n_{31}-n_{21})(1+D))((1+n_{31})(1+D)-nD-1+n)}{f_{sw}(\gamma\%)R_o(1-n_{21})^2} \\ C_1 \geq \frac{(1+(1+n_{31}-n_{21})(1+D))((1+n_{31})(1+D)-nD)}{f_{sw}(\gamma\%)R_o(1-n_{21})^2 D} \\ C_2 \geq \frac{1+(1+n_{31}-n_{21})(1+D)}{f_{sw}(\gamma\%)R_o(1+n_{31}-n_{21}D)} \\ C_3 \geq \frac{1+(1+n_{31}-n_{21})(1+D)}{f_{sw}(\gamma\%)R_o((1-n_{21})(1+D)+n_{31}D)} \\ C_o \geq \frac{D}{f_{sw}(\gamma\%)R_o}. \end{cases} \quad (17)$$

B. Soft Switching

To achieve soft switching for the power switches, the required conditions are investigated in this section. Switch S_1 is turned ON under ZVS condition if the current passing through S_c is positive at $t = t_{10}$. This means that at $t = t_{10}$, the current entering the L_1-C_1 node (i_{Sc}) should be positive to help discharge and charge C_{Sc} and C_{S1}, respectively. The mathematical expression for this statement is presented in (18). By using the parametric current values in (18) and (19) is achieved. Equation (19) shows that the $i_{Sc}(t_{10})$ is positive for any given value for L_m

$$i_{S_c}\ (t_{10}) = -i_{L_1}\ (t_{10}) + i_{D_1}\ (t_{10}) + i_{L_{k_s}}\ (t_{10}) > 0 \quad (18)$$

$$\frac{1+2n_{31}}{(1-D)\,(1-n)} I_o + \frac{V_{\text{in}} D}{2 f_{sw}} \left(\frac{1}{L_1} + \frac{1}{(1-n_{21})^2 L_m} \right) > 0. \quad (19)$$

A similar condition can be examined for switch S_c at $t = t_5$. At this time, the current of S_1 must be positive to achieve soft switching for S_c. Considering that at Mode 5, $i_{S1}(t_5) = i_{L1}(t_5)$ - i_{Lks} (t_5), and $i_{L1}(t_5)$ is a positive and i_{Lks} (t_5) is a negative value, it can be concluded that $i_{S1}(t_5)$ is always positive and the soft switching condition for S_c is consistently satisfied.

To make sure that the antiparallel diode of S_1 turns ON at $t = t_1$, the energy stored in the equivalent leakage inductance of the circuit should be larger than the energy required to charge and discharge C_{Sc} and C_{S1}, respectively [30]. This statement is presented as a mathematical expression in (20). In (20), C_{S1} and C_{Sc} are the parasitic capacitances of the switch S_1 and S_c, respectively. L_{keq} is the equivalent leakage inductance seen from the terminals of the S_1 and S_c, and I_{keq} is the current of L_{keq} during Mode 1. Mode 1 is very short, and during this mode, the voltage of capacitors (C_c, C_1, C_2, C_3, and C_o) are constant. Similarly, the current of the input and the magnetizing indicators are also constant. This means that the capacitors and inductors can be modeled as voltage and current sources in the circuit configuration of Mode 1. To find the Thevenin impedance of the circuit in this mode, the current and voltage sources can be modeled as open and short circuit, respectively. Applying this procedure to the circuit configuration of Mode 1, the equivalent circuit is found in Fig. 10(a). The equivalent leakage inductance value is found in (21). Considering (20) and (21), the relationship between the equivalent leakage inductance, switch capacitances, and the output current is found in (23). The soft switching region is plotted in Fig. 10(b), showing that a very small leakage inductance is required to achieve soft switching at the rated

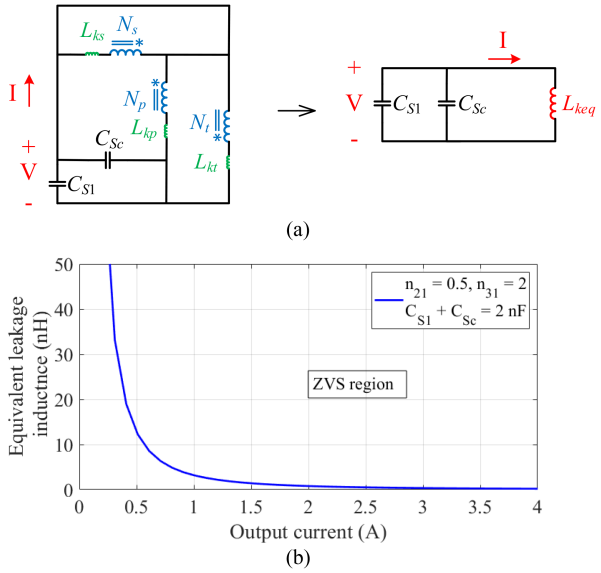

Fig. 10. (a) Equivalent circuit of mode 1. (b) Equivalent leakage inductance versus the output load.

power of the converter

$$\frac{1}{2} L_{k_{eq}} \left(I_{k_{eq}}\right)^2 > \frac{1}{2} \left(C_{S_1} + C_{S_c}\right) V_{C_c}^2 \quad (20)$$

$$L_{k_{eq}} = \frac{L_{k_p}\left(n_{21}^2 L_{k_t} + n_{31}^2 L_{k_s}\right) + L_{k_s} L_{k_t}}{\left(1+n_{31}\right)^2 L_{k_s} + n_{21}^2 \left(L_{k_t} + L_{k_p}\right)} \quad (21)$$

$$K = (1 + 2n_{31} + (1 + n_{31} - n_{21}) \times \left(\frac{\alpha\%}{2} (1+D) + \frac{\beta\%}{2} (1-D) \right) + \frac{\alpha\%}{2} \right) \quad (22)$$

$$L_{k_{eq}} \geq \frac{\left(C_{S_1} + C_{S_c}\right) V_{\text{in}}^2 (1-n_{21})^2}{K^2 I_o^2}. \quad (23)$$

Another condition for soft switching is the appropriate time delay between the gate signals. The time delay between the gate signals of S_c and S_1 was defined as φ in Fig. 2. The minimum time delay (φ_{min}) is found based on the required time to fully discharge C_{S1} and charge C_{Sc}, and it is presented in (24). The maximum time delay (φ_{max}) is calculated using the conduction time of the antiparallel diode of the switch S_1 and its equation is as presented in (25). By using a time delay between φ_{min} and φ_{max}, proper timing for the gate signals can be found for the soft switching operation

$$\varphi_{\text{min}} = \frac{V_{\text{in}} (1-n_{21}) \left(C_{S_1} + C_{S_c}\right)}{K I_o} \quad (24)$$

$$\varphi_{\text{max}} = \frac{K \left((n_{21}+n_{31})^2 L_{k_p} + (1+n_{31})^2 L_{k_s} + (1-n_{21})^2 L_{k_t} \right) I_o}{(1-n_{21})\,(1+n_{31})^2\, V_{\text{in}}}. \quad (25)$$

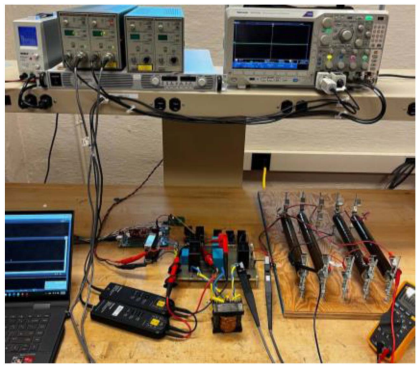

Fig. 11. Experimental setup.

TABLE III
EXPERIMENTAL SETUP PARAMETERS

Input voltage (V_{in})	20 V
Output voltage (V_o)	400 V
Power (P)	200 W
Switching frequency (f_{sw})	50 kHz
Duty cycle (D)	0.56
Switch (S_1 and S_c)	FDH055N15A $R_{DS(ON)}$ = 4.8 $m\Omega$, t_{off} =92 ns, $C_{DS} \cong$ 0.7 nF
CI	ETD 59/31/22 n_{21} = 0.5, n_{31}=2, L_m = 248 μH L_{kp}= 1.56 μH, L_{ks}= 0.39 μH, and L_{kt}= 6 μH R_p = 9.2 $m\Omega$, R_s = 6.8 $m\Omega$, and R_t = 24.5 $m\Omega$
Input inductor (L_1)	81 μH R_{L1} = 17 $m\Omega$
Diodes (D_1, D_2, and D_o)	C3D100060 V_{F0} = 0.72 V, r_D = 0.05 Ω
Capacitors	C_c = 60 μF, ESR_{Cc} = 4.1 $m\Omega$ C_1 = 60 μF, ESR_{C1} = 4.1 $m\Omega$ C_2 = 20 μF, ESR_{C2} = 3.3 $m\Omega$ C_3 = 20 μF, ESR_{C3} = 3.3 $m\Omega$ C_o = 20 μF, ESR_{Co} = 3.3 $m\Omega$

VI. EXPERIMENTAL RESULTS

To validate the steady-state analysis of the proposed converter, a 200 W experimental setup is developed. The experimental setup is shown in Fig. 11, the proposed converter can operate in a wide range of input voltage, but 20 V is selected for the input voltage of the setup, and the output voltage is 400 V. The switching frequency of the converter is 50 kHz. The turns ratio of the CI is $n_{21} = 0.5$ and $n_{31} = 2$ with the magnetizing inductance of 248 μH. The experimental setup parameters and the parasitic elements associated with the circuit components are listed in Table III.

The experimental results of the proposed converter are shown in Fig. 12. Fig. 12(a) displays the gate-source signal, voltage, and current waveforms of switch S_1. The voltage stress on S_1 is very low (almost 45 V), and this switch turns ON under ZVS condition. A zoomed version of the voltage and current waveforms of S_1 is presented in Fig. 12(b). As shown in Fig. 12(b), first, the voltage on S_1 drops, then the antiparallel diode of S_1 starts to conduct. When V_{GS1} starts to rise from low to high, the voltage on S_1 is zero, and this switch is turned ON with a zero voltage. The gate source signal, voltage, and current waveforms of switch S_c are shown in Fig. 12(c). Similar to S_1, S_c also has a very low voltage stress, and it also turns ON under ZVS condition. A zoomed version of Fig. 12(c) is shown in Fig. 12(d), and as it can be seen from Fig. 12(d), V_{GSc} was applied when the body diode of S_c was conducting, therefore, S_c turns ON under ZVS condition.

The current waveforms of the diodes are presented in Fig. 12(e), showing a good agreement with the ideal key waveforms in Fig. 2. Fig. 12(e) reveals that the reverse recovery power loss is minimized for the diodes using the leakage inductance of the CI. The current waveforms of the CI windings are shown in Fig. 12(f). These waveforms are in alignment with the ideal key waveforms. The voltage waveforms of diodes are shown in Fig. 12(g), and the voltage of capacitors are displayed in Fig. 12(h). These voltage values are very close to the expected values found using the steady-state analysis of the circuit. The current and voltage waveforms of input and output terminals are shown in Fig. 12(i). As is obvious from Fig. 12(i), the input ripple of the proposed converter is low, which makes this converter ideal for renewable energy applications.

The inherent stability of the proposed converter is tested under load change. As presented in Fig. 13, the load of the proposed converter in the experimental setup is changed from 200 W to 150 W and vice versa.

The proposed converter is tested at different power levels to measure the converter efficiency at the voltage conversion ratio of 20. For the efficiency measurement purpose, the input voltage was 20 V, and the output voltage was 400 V. As can be seen from Fig. 14, the experimental efficiency of the proposed converter is approximately 94% at rated power. The theoretical efficiency of the converter also is calculated using the simulation data. Based on Fig. 14, the theoretical efficiency is relatively accurate because it has almost 1% error at the rated power.

VII. LOSS ANALYSIS

For calculating the power loss in the semiconductor devices of the proposed converter, the root mean square (rms) currents of the power switches and diodes are required. The rms current of the semiconductor components are calculated in (26) is shown at the top of the next to next page. The average currents of the semiconductor currents are also presented in (10). Using the rms and average current of the power switches, the power loss in the power switches is calculated in (28). In (28), $P_{s,cond}$ is the conduction power loss and $P_{s,\ SW}$ is the switching power, $R_{DS(\mathrm{ON})}$ is the ON-state resistance of the power switch, and $t_{f(\mathrm{off})}$ is fall time of the power switch. The power loss of the diodes is found by using (30), in which V_{F0} is the forward voltage of the diode and r_D is the resistance of the diode. The parasitic elements of the circuit components are presented in Table III.

The power loss of the magnetic components is divided into two parts: 1) the copper loss of the windings (P_{cu}) and 2) the core loss (P_{core}). By using the rms current of the windings in (30) and the resistance of the windings from Table III, the copper loss of the magnetic components is found in (32). Also, the core loss of the magnetic cores can be found using $P_{\mathrm{core}_{CI}}$ in (32). The

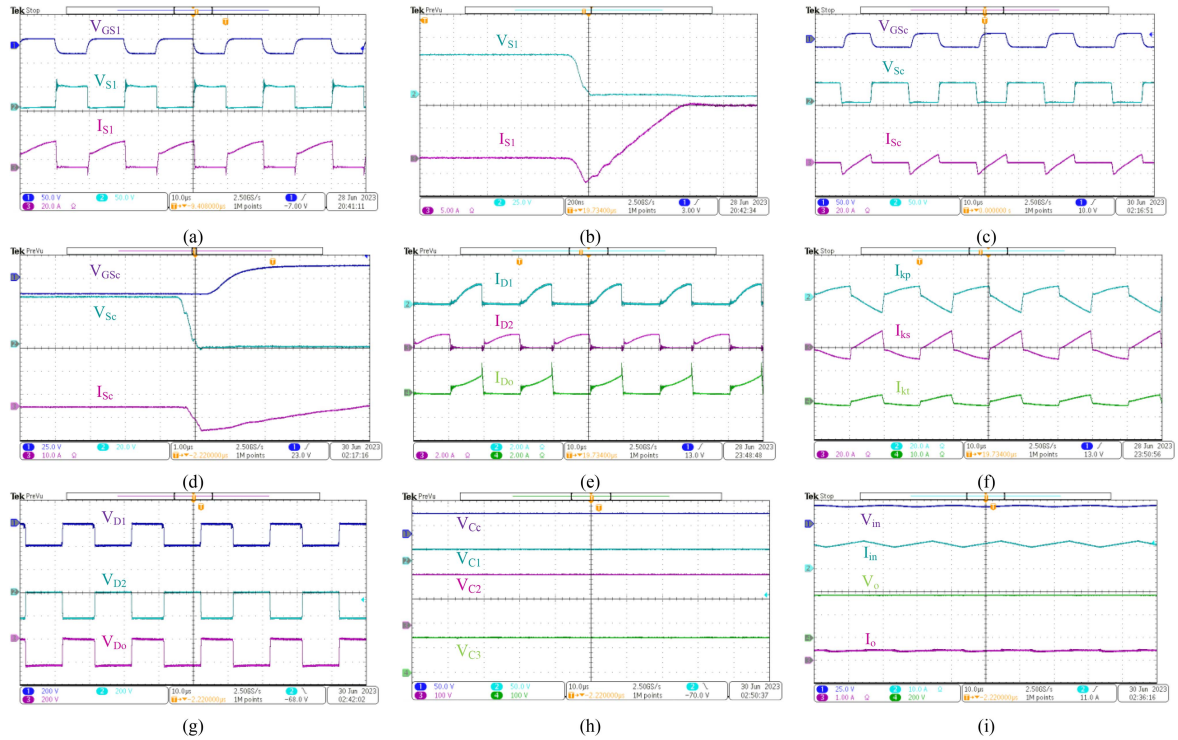

Fig. 12. Experimental results. (a) Gate signal (V_{GS1}), voltage (V_{S1}), and current (I_{S1}) waveforms of S_1. (b) V_{S1} and I_{S1} at turn ON instance. (c) Gate signal (V_{GSc}), voltage (V_{Sc}), and current (I_{Sc}) waveforms of S_c. (d) V_{GSc}, V_{Sc}, and I_{Sc} at turn ON instance. (e) Current waveforms of diodes. (f) Current waveforms of the CI windings. (g) Voltage waveforms of the didoes. (h) Voltage of the capacitors. (i) Input and output voltage and current waveforms.

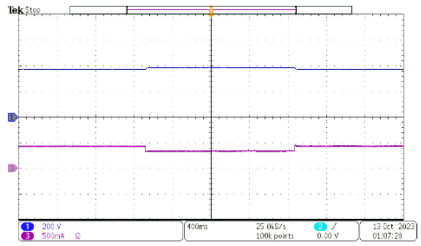

Fig. 13. Response of the output voltage (CH1) to step change in load current (CH3).

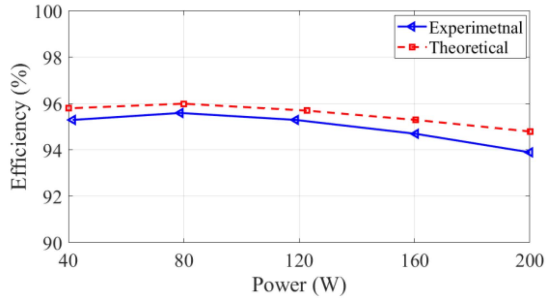

Fig. 14. Efficiency of the proposed converter versus power.

parameters in this equation can be found using the manufacture data sheet. Similarly, the input inductor's power loss can be found using (33). The power loss on the capacitors is found using (34). The effective series resistance (ESR) is presented

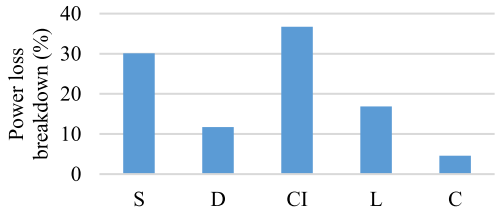

Fig. 15. Loss breakdown of the proposed converter at the rated power.

in Table III

$$\begin{cases} P_{S,cond} = R_{DS(\text{on})}\left(I^2_{S_1(\text{rms})} + I^2_{S_c(\text{rms})}\right) \\ P_{S,SW} = \frac{1}{2} V_s f_{sw} t_{f(\text{off})}\left(I_{S_1} + i_{sc}\left(t_{10}\right)\right) \\ P_S = P_{S,cond} + P_{S,SW} \end{cases} \tag{28}$$

$$i_{sc}\left(t_{10}\right) = \frac{\left(2 + n_{31} - n_{21}\right)\left(1 + n_{21} + \left(1 - n_{21}\right) D\right)}{\left(1 - n_{21}\right)\left(1 - D\right)} \tag{29}$$

$$P_D = V_{F0}\, I_D + r_D I^2_{D(\text{rms})} \tag{30}$$

$$\begin{cases} I_{kp}\ (\text{rms}) = \frac{I_o}{\sqrt{3}(1-n_{21})} \sqrt{\left(\frac{2n_{31}-(1+n_{31}-n_{21})D}{D}\right)^2 + \left(\frac{4n_{31}-(1+n_{31}-n_{21})(1-D)}{1-D}\right)^2} \\ I_{ks}\ (\text{rms}) = \frac{I_o}{\sqrt{3}(1-n_{21})} \sqrt{\left(\frac{2+2n_{31}-(1+n_{31}-n_{21})D}{D}\right)^2 + \left(\frac{4+4n_{31}-(1+n_{31}-n_{21})(1-D)}{1-D}\right)^2} \\ I_{kt}\ (\text{rms}) = 2I_o\sqrt{\frac{1+3D}{3D(1-D)}} \end{cases} \tag{31}$$

$$\begin{cases} I_{D_1(\text{rms})} = I_{D_o(\text{rms})} = \frac{2I_o}{\sqrt{3(1-D)}} \\ I_{D_2(\text{rms})} = \frac{2I_o}{\sqrt{3D}} \\ I_{S_1(\text{rms})} = \frac{1+n_{31}+(2-2n_{21}+n_{31})\sqrt{D}}{(1-n_{21})(1-D)}\ I_o \\ I_{S_c(\text{rms})} = \frac{\sqrt{\begin{array}{c}((2+n_{31}-n_{21})(1+n_{21}+(1-n_{21})D))^2\left(1-D-\frac{\Delta t}{T}\right)+ \\ (1+2n_{31}+2(1+n_{31}-n_{21})(1-D))^2\frac{\Delta t}{T}\end{array}}}{(1-n_{21})(1-D)\sqrt{3}}\ I_o \end{cases} \tag{26}$$

$$\Delta t = \frac{(2(1-n_{21})+(2+n_{31}-n_{21})(1+n_{21}+(1-n_{21})D))(1-D)T}{1+2n_{31}+2(1+n_{31}-n_{21})(1-D)+(2+n_{31}-n_{21})(1+n_{21}+(1-n_{21})D)} \tag{27}$$

$$\begin{cases} P_{cu_{CI}} = R_p\ I^2_{Lkp(\text{rms})} + R_s I^2_{Lks(\text{rms})} + R_t I^2_{Lkt(\text{rms})} \\ P_{\text{core}_{CI}} = K(f)^{\alpha}\left(\frac{\Delta B_{CI}}{2}\right)^{\beta} \\ P_{CI} = P_{cu_{CI}} + P_{\text{core}_{CI}} \end{cases} \tag{32}$$

$$\begin{cases} P_{L_1} = R_{L_1}\ I^2_{L_1(\text{rms})} + P_{\text{Core}_{L_1}} \\ P_{\text{core}_{L1}} = K(f)^{\alpha}\left(\frac{\Delta B_{L_1}}{2}\right)^{\beta} \end{cases} \tag{33}$$

$$P_C = \sum_{i=1}^{N_C} P_{C_i} = \sum_{i=1}^{N_C} \text{ESR}_{C_i} I^2_{C_i(\text{rms})}\ . \tag{34}$$

Using the loss analysis, the loss breakdown of the proposed converter at rated voltage and power is calculated and presented in Fig. 15 As can be seen in Fig. 15, the majority of the power loss is associated with power switches and the CI.

VIII. Conclusion

An impedance-source-based high step-up dc–dc converter was proposed in this article. The proposed topology uses a trans-inverse structure combined with voltage multiplier cells and an active clamp method to achieve a high voltage gain. The proposed converter provides a high voltage conversion ratio with a very low voltage stress on the power switches. Also, both of the power switches turn ON under the ZVS condition, leading to lower switching power loss and a high efficiency in the converter. Additionally, because of the controlled falling rate of the diode currents, their reverse recovery power loss was eliminated, further improving the efficiency of the converter. This article covered the steady-state analysis, comparison with existing converters, the detailed design guidelines to achieve soft-switching, and experimental results. The experimental results showed that the proposed converter achieves an efficiency of almost 94% at the rated power for the conversion ratio of 20. The proposed converter has been proven to be an ideal candidate for renewable energy applications.

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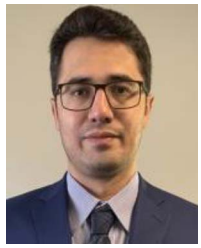
Saeed Habibi (Graduate Student Member, IEEE) received the B.S. degree from K. N. Toosi University of Technology, Tehran, Iran, in 2015, and the M.S. degree (*with focus on power electronics*) from the University of Tehran, Tehran, Iran, in 2018. He is currently working toward the Ph.D. degree with the Department of Electrical and Computer Engineering, Missouri University of Science and Technology (formerly UMR), Rolla, MO, USA, all in electrical engineering.

His research interests are power electronics, electric vehicles, direct current distribution systems, renewable energies, and energy storage systems.



Ramin Rahimi (Member, IEEE) received the B.Sc. degree in electrical engineering from the University of Tabriz, Tabriz, Iran, in 2013, the M.Sc. degree in electrical engineering from the University of Tehran, Tehran, Iran, in 2016, and the Ph.D. degree in electrical engineering from the Missouri University of Science and Technology (formerly UMR), Rolla, MO, USA, in 2022.

He is currently a Lead Electrical Engineer with Eaton Corporation, Raleigh, NC, USA. His research interests include power electronics, renewable energies, electrical vehicles, switching power supplies, and design and implementation of power converters.

Mehdi Ferdowsi (Senior Member, IEEE) received the B.S. degree in electronics from the University of Tehran, Tehran, Iran, in 1996, the M.S. degree in electronics from Sharif University of Technology, Tehran, Iran, in 1999, and the Ph.D. degree in electrical engineering from the Illinois Institute of Technology, Chicago, in 2004.

He was the faculty with the Missouri University of Science and Technology (formerly UMR), Rolla, MO, USA, in 2004, where he is currently a Professor with the Department of Electrical and Computer Engineering. His research interests include power electronics, energy storage, smart grid, vehicular technology, and wide bandgap devices.

Dr. Ferdowsi was a recipient of a National Science Foundation CAREER Award in 2007. He is an Associate Editor of IEEE TRANSACTIONS ON POWER ELECTRONICS. Since 2004, he has been successful in securing more than $5 million in funding—his individual share. The published results of his scholarly activities include 2 book chapters and more than 140 archival journals and conference proceedings. He has graduated more than 30 M.Sc. and Ph.D. students. He was the recipient of several Outstanding Teaching Awards and Recognitions from Missouri S&T, Missouri S&T's Faculty Excellence Award in 2017, he and his students was the recipient of best paper award at the IEEE Vehicle Power and Propulsion Conference in 2008, and a best poster award at the IEEE International Conference on Renewable Energy Research and Applications in 2014.

Pourya Shamsi (Senior Member, IEEE) received the B.Sc. degree from the University of Tehran, Tehran, Iran, in 2007, and the Ph.D. degree from The University of Texas at Dallas, Richardson, TX, USA, in 2012, both in electrical engineering.

He is currently the Woodard Associate Professor of Electrical Engineering with Missouri University of Science and Technology (formerly UMR), Rolla, MO, USA. His research interests include power electronics, microgrids, wide bandgap devices, MV inverters, and motor drives.