An Adaptive Synchronous Driving Phase Control Method of GaN-Based Full-Bridge 6.78-MHz WPTS

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***Abstract*—The GaN-based active rectifiers have the potential to improve the efficiency of the several megahertz wireless power transfer system (WPTS). The full-bridge active rectifier can eliminate extra dc–dc converters for output regulation with less voltage stress than resonant rectifiers, such as Class E, Φ rectifiers. However, the lack of the synchronous phase control method is the core challenge for full-bridge active rectifier in 6.78-MHz WPTSs. Meanwhile, the increasing switching losses and reverse conduction losses of the gallium nitride high electron mobility transistors are the main constraints on the efficiency of the system. This article proposes an adaptive synchronous driving phase control (ASDPC) method of the GaN-based full-bridge rectifiers in 6.78-MHz WPTS. With the proposed method, the full-bridge rectifier can obtain the maximum output power in the critical zero voltage switching operation over a wide load range. A 50-W 6.78-MHz WPTS is built to verify the effectiveness and stability of the proposed ASDPC method. The dc–dc efficiency is improved in the wide load range of 8–50 Ω (11.8–54.57 W) and reaches 87.18% at $P_o = 44.9$ W. Compared to the system without ASDPC, the efficiency can be improved by 5.2% at light load and 3.1% at heavy load.**

***Index Terms*—6.78-MHz wireless power transfer system (WPTS), dynamic dead time control (DDTC), full-bridge rectifier, synchronous phase control, zero voltage switching (ZVS).**

I. Introduction

THE megahertz (MHz) wireless power transfer system (WPTS) is considered to be a promising technology in applications such as consumer electronics, drones, and unmanned vehicles [1], [2], [3], [4]. The increasing operating frequency brings lightweight coils and compact converters to the WPTS [5], [6]. The emerging wide bandgap devices provide the possibility for WPTSs to operate at 6.78 MHz or higher frequencies in the Industrial Scientific Medical band. The operating frequency is determined to be 6.78 MHz conventionally, considering the performance of the power electronic device, the complexity of coils, and the difficulty of control. In several MHz scenarios, the gallium nitride high electron mobility transistors (GaN HEMTs) stand out for their compact size and fast switching speed. However, the inherent parasitic capacitance of the GaN HEMTs and the parasitic parameters of the printed circuit board (PCB) still result in considerable switching loss and hard-switching ringing [7], [8], [9]. Thus, the significance of the soft switching and the reliability are highlighted in MHz WPTS.

It is known that, in the 6.78-MHz WPTS, zero voltage switching (ZVS) operations of switches over a wide load range are absolutely necessary. The resonant rectifiers have attracted widespread attention because of their excellent performances in soft switching [10], [11], [12], [13]. The impedance matching networks cascaded have been thoroughly investigated to maintain the ZVS operation in a wide load range [14], [15], [16]. In the low-voltage situations, resonant rectifiers are prominent thanks to their high efficiency and convenience in control. However, the large voltage/current stress forces users to choose GaN HEMTs with higher withstand voltage, which limits the improvement of the power density. The bridge topology stands out for the low voltage/current stress and simplicity. The passive rectifier is widely applied in the 6.78-MHz WPTS. However, the parasitic capacitance of diodes not only results in considerable switching loss but also affects the frequency characteristics of the resonant network [17]. The active bridge rectifier is essential on account of the high efficiency and the power angle regulation.

The synchronization method is the primary challenge in the bridge rectifier. The methods in [18], [19], and [20] are applicable to full-bridge rectifiers fabricated in 0.35 μm CMOS while the output power and overall efficiency are very limited. A zero-crossing current sensing scheme is proposed in [21] for synchronous phase control of the 6.78-MHz full-bridge rectifier. With a delicate design, the current sensing signal and the current phase are 180° out of phase. However, the method poses the risk of synchronization failure with frequency and phase oscillation. A synchronization with higher robustness is proposed in [22], with an improved current sampling method. However, the dynamic performance of the method is restricted by AD sampling and serial peripheral interface (SPI) communication speed between the controller and the digital control oscillator. Wu et al. [23] propose an accurate synchronization method

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without zero crossing detection at 85 kHz. The power factor of the rectifier is calculated with the fundamental component of the resonant current and the driving signals. Unfortunately, the method is not suitable at MHz because of the inevitable propagation delay. Accurate propagation delay compensation is the necessary component of synchronization [24].

ZVS operation over a wide load range is another issue. An additional *LC* branch is introduced to the bridge rectifier connected at the midpoints [21], [22], [25], [26]. The additional *LC* branch provides the current for charging and discharging the parasitic capacitance of the switches during the dead time. Nevertheless, the ZVS operation depends on the dead time and dc voltage of the rectifier. The *LC* parameters are usually calculated under the worst operating conditions to ensure the ZVS operation over the whole load range. Even if the ZVS operation is achieved, there is still a negligible reverse conduction loss. Tebianian et al. [26] proposed a dynamic dead time control (DDTC) method for the inverter with additional *LC* branches. Although the reverse conduction loss is reduced, the additional *LC* branch will introduce extra losses and potential high-frequency resonant point. Therefore, it is meaningful and beneficial to ensure the critical ZVS operation over a wide load range without additional *LC* branches. To avoid sensitivity to the system parameters, the reverse conduction should be detected quickly and reliably. In high-frequency dc–dc converters, the reverse conduction detection by sampling the drain–source voltage is widely adopted [27], [28], [29], [30]. However, the dead time regulation of the rectifier has not been investigated.

Aiming at the above problems, an adaptive synchronous driving phase control (ASDPC) method is proposed in this article. The hardware implementations are validated with low-cost commercial devices. Compared to conventional synchronous phase control methods, the full-bridge rectifier achieves critical ZVS operation without additional *LC* branches. With the proposed method, the output power of the system can be increased reliably in the low-voltage/current stress scenarios.

The rest of this article is organized as follows. Section II derives the condition of ZVS operation and the optimal operating curve (OOC) from fundamental harmonic equivalent (FHA) and the time domain model. Section III illustrates the structure of the proposed ASDPC method. The serial control with the DDTC outer loop–synchronous driving phase control (SDPC) inner loop is thoroughly analyzed. Section IV presents the experimental results to prove the validity of the proposed control method. Finally, Section V concludes the article.

II. ZVS Operation Condition and the OOC

A. Basic Analysis From FHA and Time Domain Model

The schematic and the FHA model of an S–S type WPTS are shown in Fig. 1, where L_1, L_2, R_1, R_2, and M are self-inductance, equivalent series resistance, and mutual inductance of the coils, respectively. C_1 and C_2 are the capacitors of the series–series type compensation topology. Q_1–Q_4 and S_1–S_4 are GaN HEMTs in the inverter and the rectifier. R_L is the load resistance and Z_{eq} is the input impedance of the rectifier. V_1 is the input dc voltage of source and V_o is the output dc voltage of the WPTS. i_{L1} is

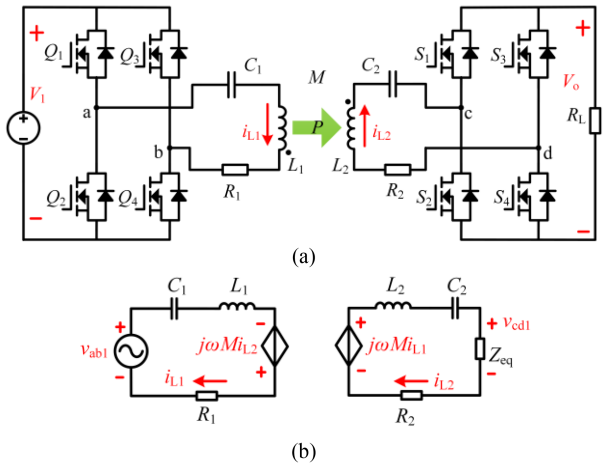

Fig. 1. (a) Schematic and (b) equivalent circuit of an S–S type WPTS.

the current in the primary coil, whereas i_{L2} is the current in the secondary coil. v_{gs1}–v_{gs4} are the gate–source voltages of S_1–S_4. a, b, c, and d are midpoints of bridges in the inverter and the rectifier. T and ω are the operating frequency and the operating angular frequency, respectively

$$\omega^2 = \frac{1}{L_1 C_1} = \frac{1}{L_2 C_2}. \tag{1}$$

v_{ab1} and v_{cd1} are the fundamental harmonic component of v_{ab} and v_{cd}. When the operating frequency meets (1) with R_1 and R_2 are neglected, the rms value of i_{L1} and i_{L2}, I_{L1} and I_{L2}, can be obtained as

$$\begin{cases} \dot{I}_{L1} = -\frac{v_{ab1}}{\omega^2 M^2} \cdot Z_{eq} \\ \dot{I}_{L2} = j \cdot \frac{v_{ab1}}{\omega M} \end{cases}. \tag{2}$$

In (2), the constant current characteristic of the SS topology is verified that i_{L2} is load independent. Hence, when ω, M, V_1, and the duty cycle of the inverter are constant, the secondary resonant network can be considered as a constant current source. Both primary and secondary networks are in resonance at the operating frequency when Z_{eq} is purely resistive. However, it is necessary to introduce a certain power angle to achieve the ZVS operation of the inverter and rectifier where typical waveforms are shown in Fig. 2. φ_1 and φ_2 are the power angles of the inverter and the rectifier, respectively. DT_1 and DT_2 are the dead times of the inverter and the rectifier, respectively. t_0 and t_1 are the starting time and the ending time of the dead time interval, respectively. The power angle φ_1 is inductively reflected by the reactive secondary power angle φ_2. With R_1 and R_2 neglected, $\varphi_1 = \varphi_2$ establishes.

On one hand, the power angle of the rectifier should be minimized for the maximum output power. To make it more intuitive, the power in each area is marked by the blocks in different colors. P_{area1} and P_{area4} are the power during the dead time. P_{area2} and P_{area3} are the power during the on time. It is obvious that P_{area1} and P_{area2} are positive, whereas P_{area3} and P_{area4} are negative. P_{area1} and P_{area4} are the necessary reactive power to achieve the ZVS operation where $P_{area1} + P_{area4} = 0$.

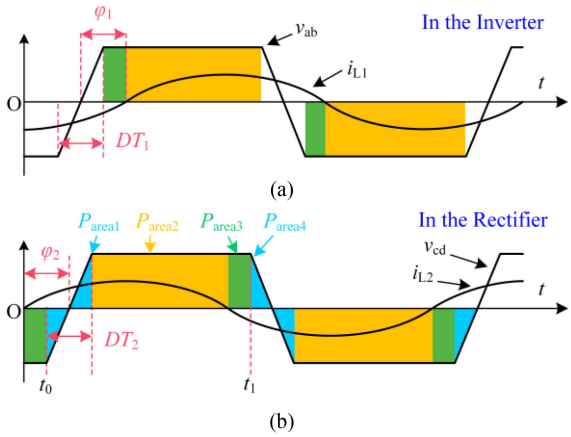

Fig. 2. Typical waveforms of (a) the inverter and (b) the rectifier.

The output power depends on P_{area2} and P_{area3}, where P_{area3} is the additional reactive power. Hence, t_0 should be decreased to reduce P_{area3}.

On the other hand, the critical ZVS operation should be realized to reduce the switching losses. The losses of GaN HEMTs consist of the on-time loss, overlapped loss, and the reverse conduction loss. The on-time loss depends on the current and the drain–source on resistance of the device. The overlapped loss depends on the ZVS operation, which can be categorized into three types: the partial ZVS operation, the post ZVS operation, and the critical ZVS operation. The v_{ds} is higher than 0 when $v_{\text{gs}} = 1$ in the partial ZVS operation. The v_{ds} is lower than 0 when $v_{\text{gs}} = 1$ in the post ZVS operation. The v_{ds} is 0 when $v_{\text{gs}} = 1$ in the critical ZVS operation. The overlapped loss exists only in the partial ZVS operation, whereas the reverse conduction loss exists only in the post ZVS operation. Thus, DT_2 is supposed to be controlled to the optimal value over the wide load range. The condition of the ZVS operation of the rectifier is

$$Q_{\text{ZVS}} = \int_{t_0}^{t_0+DT_2} i_{\text{L2}} \sin(\omega t)\text{d}t \geq Q_{\text{oss}} = \sum Q_{\text{ossn}} \tag{3}$$

where the dead time starting time t_0 can be obtained by

$$t_0 = \frac{\varphi_2}{\omega} - \frac{DT_2}{2}. \tag{4}$$

Q_{ZVS} is the charge quantity of i_{L2} within the dead time. Q_{ossn} is the output charge of the switch n. Q_{ossn} is a positively correlated nonlinear function of v_{ds}, which can be obtained by integrating over v_{ds} and C_{ossn}, as shown in Fig. 3. In the full-bridge rectifier, v_{ds} is equal to the output voltage V_{o}, which can be calculated by

$$V_{\text{o}} = \frac{1}{\frac{T}{2}} \int_{t_0+DT_2}^{t_1} R_{\text{L}} \cdot i_{\text{L2}} \sin(\omega t)\text{d}t \tag{5}$$

where the dead time ending time t_1 can be obtained by

$$t_1 = t_0 + \frac{T}{2}. \tag{6}$$

According to Fig. 3 and (3)–(6), the changes in φ_2 and DT_2 result in the variations of Q_{zvs} and Q_{oss}, as shown in Fig. 4.

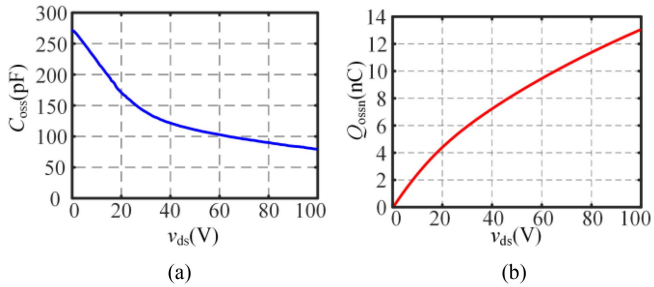

Fig. 3. (a) C_{oss} and (b) Q_{ossn} of EPC2007C versus v_{ds} [32].

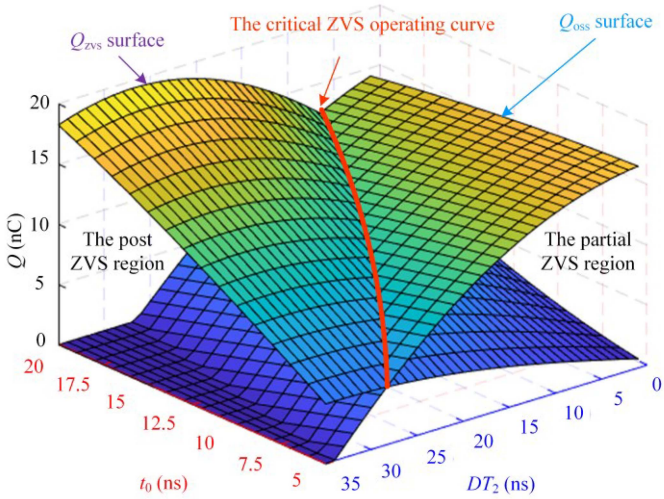

Fig. 4. Operating curve in the critical ZVS operation.

It is noted that i_{L2} is normalized to 1 A and R_{L} is 30 Ω. The intersection of Q_{zvs} and Q_{oss} surfaces is the critical ZVS operating curve at a certain R_{L}. Due to deviation in parasitic parameters and the propagation delay, the driving phase angle δ is considered as the control target, rather than the power angle φ_2. The driving phase angle δ can be obtained by

$$\delta = \varphi_2 + \frac{DT_2}{2}. \tag{7}$$

On the critical ZVS operating curve, δ of various loads versus DT_2 is shown in Fig. 5. As the load gradually increases, its post ZVS region shrinks and the partial ZVS region grows. In order to obtain the maximum output power under the critical ZVS operation, the rectifier is supposed to run at the optimal operating point where δ is the minimum. Thus, the OOC under various loads can be obtained, as shown by the red dashed line in Fig. 5. From the OOC, the reference of δ can be set as

$$\delta_{\text{ref}} = \omega \cdot DT_2 + \omega \cdot T_{\text{ZVS}} = \omega \cdot DT_2 + \theta_{\text{ZVS}}. \tag{8}$$

θ_{zvs} is the margin reserved to stabilize the system from three disturbances, which are the edge jitter, the quantization error from the digital PI controller, and the frequency difference from system clocks in both sides, respectively. T_{zvs} is determined to be one system clock cycle (2.5 ns).

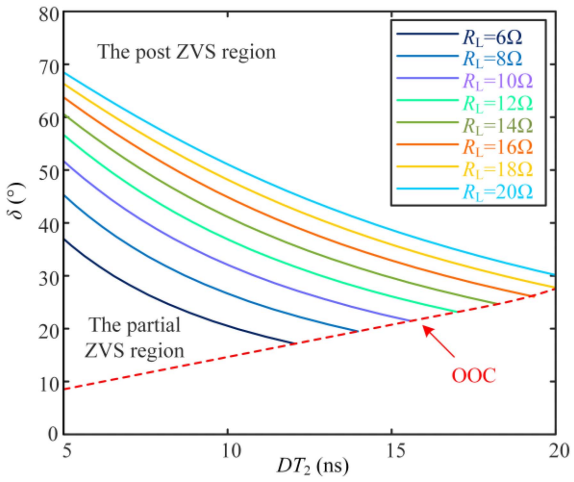

Fig. 5. Driving phase of the critical ZVS operating curve at various load.

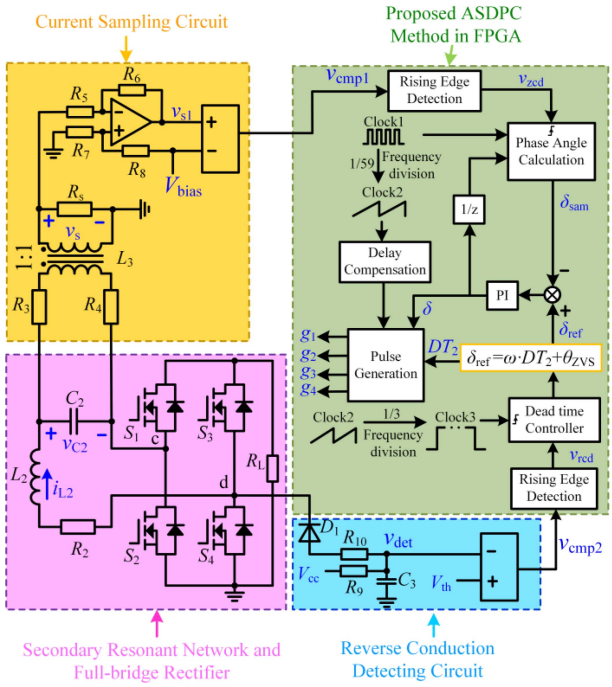

Fig. 6. Control block diagram of the proposed ASDPC method.

III. Proposed ASDPC Method

An ASDPC method is proposed in this section. The control block diagram is depicted in Fig. 6. The main hardware implementation circuit and related control strategy are shown in the green block. The secondary resonant network and the full-bridge rectifier are shown in the purple block. The positive zero crossing point of i_{L2} is obtained by the current sampling circuit in the yellow block. The reverse conduction detecting (RCD) circuit is shown in the blue block.

A. Current Sampling Circuit

The coupled inductor (L_3) is connected in parallel with the resonant capacitor (C_2) through two current-limiting resistors (R_3 and R_4). A shunt resistor (R_s) is located in the secondary side of the coupled inductor. The coupling coefficient of L_3 is more than 0.99. The resistance of R_3 and R_4 are large enough that the influence of the current sampling circuit on the secondary compensation network is suppressed. In this way, i_{L2} is indirectly sampled via the voltage of the resonant capacitor (v_{C2}), which lags behind i_{L2} by 90°. Meanwhile, the voltage of the shunt resistor (v_s) is 90° ahead of v_{C2} under conditions where the input impedance is much larger than the $1/\omega C_2$. Therefore, v_s remains in phase with i_{L2}. v_{s1} is obtained by adding a dc bias (V_{bias}) to v_s in the signal processing circuit where R_5, R_6, R_7, R_8 are equal. Finally, v_{s1} is compared with V_{bias} by the comparator. The rising edge of the comparator output signal (v_{cmp1}) represents the zero crossing point of i_{L2}.

B. Structure of the Proposed ASDPC Control

The system clock (Clock1) counts at 400 MHz. Clock2 is the carrier clock, obtained from Clock1 through 59 frequency division. The phase angle calculation takes Clock1 as its clock, and calculates the driving phase angle (δ_{sam}) to update driving pulses (g_1–g_4). When the secondary controller starts operating, the phase of Clock2 is taken as the reference. The counter cnt1 counts from 1 to 59. Once the secondary current positively crosses zero, the output of the comparator (v_{cmp1}) will change from low to high. The rising edge of v_{cmp1} is detected as the trigger signal for the phase angle calculation. If $v_{zcd} = 1$, the instantaneous value of the system clock counter (cnt_1) will be recorded, which represents the phase of the i_{L2}. The voltage phase (v_{pha}) is provided by the output of the unit delay. Thus, δ_{sam} can be calculated as

$$\delta_{ref} = v_{pha} - cnt_1 + t_{delay} \tag{9}$$

where t_{delay} is the whole propagation delay. The calculated driving phase angle (δ_{sam}) is compared with the reference (δ_{ref}), which is calculated by DT_2 from the dead time controller. Next, the driving phase angle error is sent to the digital PI controller. The output of the digital PI controller (δ) is used for pulse generation and recorded for the phase angle calculation in the next cycle. The 6.78-MHz digital sawtooth carrier wave is generated by Clock2. With the δ, DT_2, and the carrier after the delay compensation, four drive signals are obtained.

It is worth noting that the frequency deviation effect is prominent in 6.78-MHz WPTS. There are two reasons: one is that the system frequency of the primary controller and the secondary controller are not large enough; the other is the parameter deviation of components at 6.78 MHz. Thus, the rising edge of the v_{cmp1} and v_{cmp2} may occur at any time, missing the rising edge of Clock1. To suppress the frequency deviation effect, the rising edge detection module composed of a D trigger aligns the rising edges uniformly. The edge jitter can be controlled within 2.5 ns.

C. Delay Compensation

The whole propagation delay is the sum of input delay and output delay, which needs to be accurately calculated and compensated. The input delay is

$$t_{\text{delay\_in}} = t_{\text{cs}} + t_{\text{pro}} + t_{\text{cmp}}. \tag{10}$$

t_{cs} is the delay caused by the phase shift of the current sampling circuit. Wang et al. [31] illustrate the amplitude-frequency and phase-frequency characteristics of v_{s} with simplified circuit. To obtain the more accurate propagation delay, the leakage inductance of the coupled inductor and the shunt resistor are considered here. The function of v_{s} to i_{L2} is derived as

$$v_{\text{s}} = \frac{R_{\text{s}} \cdot sL_{\text{m}}}{(R_{\text{s}} + sL_{\text{m}}) \cdot \left[1 + \left(R + sL_{\text{s}} + \frac{R_{\text{s}} \cdot sL_{\text{m}}}{R_{\text{s}} + sL_{\text{m}}}\right) \cdot sC_2\right]} \cdot i_{\text{L2}} \tag{11}$$

$$t_{\text{cs}} = \arctan\left\{\frac{\omega^2 \left(R_{\text{s}}L_{\text{s}} + RL_{\text{m}} + R_{\text{s}}L_{\text{m}}\right) C_2 - R_{\text{s}}}{\omega \left(RR_{\text{s}}C_2 + L_{\text{m}}\right) - \omega^3 L_{\text{m}}L_{\text{s}}C_2}\right\} \cdot \frac{T}{2\pi} \tag{12}$$

where R is the sum of R_3 and R_4, and L_{m} and L_{s} are the magnetizing inductance and leakage inductance of the coupled inductor, respectively.

The phase delay at 6.78 MHz can be calculated by substituting the circuit parameters into (11). t_{pro} is the propagation delay of the operational amplifier and the comparator, found in the datasheets. t_{cmp} is the delay from the hysteresis voltage of comparator, calculated by

$$t_{\text{cmp}} = \frac{\arcsin\left(\frac{V_{\text{hys}}}{V_{\text{s1}}}\right)}{\omega} \tag{13}$$

where V_{hys} is the hysteresis voltage and V_{s1} is the amplitude of v_{s1}.

The increase in R_3 and R_4 will reduce t_{cs}, but the attenuated gain of v_{s} will increase t_{cmp}. Therefore, the gain, the overall input delay, and input impedance are taken into account to set a proper value of the current-limiting resistor, which is 100 kΩ here.

The driving signals of the top GaN HEMTs are based on the midpoint voltage, which is floating to the ground. Generally, the driver ICs are divided into the half-bridge driver, the low-side drivers, and the isolated gate drivers. The isolated drivers are not suitable for MHz scenarios due to the low switching frequency. The half-bridge driver has the advantage of high integration. However, the driving signal of the top GaN HEMT has an additional level shift module compared to that of the low GaN HEMT. This results in a larger propagation delay of the top driving signal than the low driving signal. The low-side driver has the advantage of a high peak current and a stable propagation delay. Therefore, the low-side driver is adopted in the proposed system. Both the top driving signal and low driving signal are obtained from field-programmable gate array (FPGA) through digital isolation ICs. The bootstrap circuit is used to achieve isolated power supply.

Therefore, the output delay is

$$t_{\text{delay\_out}} = t_{\text{FPGA}} + t_{\text{iso}} + t_{\text{drv}}. \tag{14}$$

t_{FPGA} is the delay due to the logical operation in FPGA. There exists a delay of two system clock in the rising edge detection. t_{iso} and t_{drv} are the propagation delay of the digital isolator and the low-side driver, respectively. The delay compensation can be realized by shifting the resulting carrier an interval obtained by (10)–(14).

D. Dynamic Dead Time Control

Generally, v_{gs} is the only variable to turn ON or OFF the GaN HEMTs. However, when the GaN HEMTs is charged to the source-drain voltage exceeding reverse conduction threshold ($V_{\text{gd\_th}}$) within the dead time ($v_{\text{gs}} = 0$), the GaN HEMTs will conduct reversely. Owing to the symmetry of the device, $V_{\text{gd\_th}}$ is approximately the same as the gate threshold ($V_{\text{gs\_th}}$). Even with the ZVS operation, such a large source-drain forward voltage still leads to significant reverse conduction loss at 6.78 MHz, deteriorating the system efficiency.

To reduce the reverse conduction loss, the DDTC is realized in the proposed method to achieve the critical ZVS operation. The RCD circuit is composed of a diode, pull-up resistors, a filter capacitor, a voltage reference, and a comparator, as depicted in Fig. 6.

The cathode of the diode is connected to the midpoint d, and the anode is connected to V_{cc} through pull-up resistors, R_9 and R_{10}. The reverse conduction is detected by comparing the RCD voltage (v_{det}) and the preset threshold (V_{th}). When the midpoint voltage (v_{d}) is higher than V_{cc} minus the diode forward voltage drop (V_{diode}), the diode D_1 turns OFF, that is, v_{det} equals V_{cc}. When v_{d} is lower than the V_{cc} – V_{diode}, the diode D_1 turns ON. The v_{det} can be represented as

$$v_{\text{det}} = \frac{R_{10}}{R_9 + R_{10}} \cdot V_{\text{cc}} + \frac{R_9}{R_9 + R_{10}} \cdot \left(v_{\text{d}} + V_{\text{diode}}\right). \tag{15}$$

A low-pass filter composed of the filter capacitor and voltage divider resistors can avoid interference from hard-switch ringing. The value of the capacitor and V_{th} is a tradeoff of the dynamic of RCD and filter bandwidth. The cutoff frequency is determined to be 31 MHz to suppress the effect on the RCD circuit.

The output of the comparator (v_{cmp2}) is fed into the DDTC module through the rising edge detection module. The DDTC module is triggered by Clock3. If $v_{\text{rcd}} = 1$, the DT_2 will be decreased; If $v_{\text{rcd}} = 0$, the DT_2 will be increased. The Clock3 is obtained by Clock1 through 3 frequency division, weighing the stability and response speed of DDTC. The conventional DDTC has been widely applied in GaN-based converters [27], [28], [29], [30]. However, the key problem of the DDTC in the 6.78-MHz WPTS is the relationship between the synchronous phase control and DDTC. It is difficult to ensure the stability and effectiveness of the system if the two control loops operate in parallel. A serial control structure with the DDTC outer loop–SDPC inner loop is adopted in the ASDPC method. The logic diagram is depicted in Fig. 7.

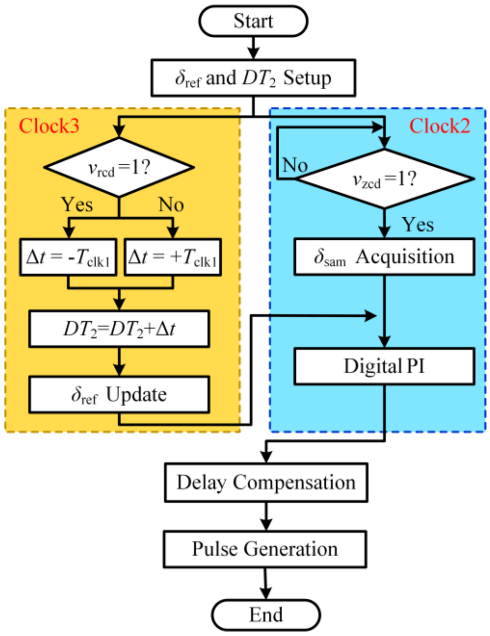

Fig. 7. Logic diagram of the proposed serial control structure.

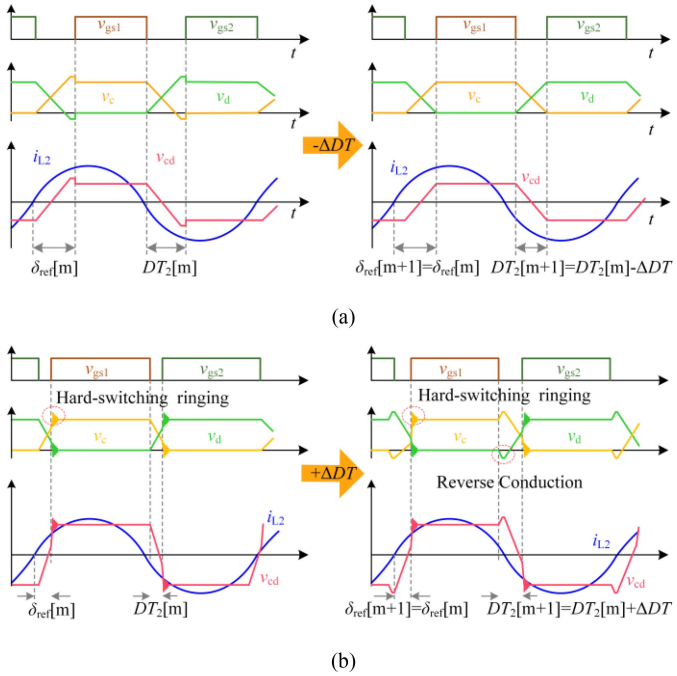

Fig. 8. Parallel control structure of SDPC loop and DDTC loop. (a) Post ZVS operation. (b) Partial ZVS operation.

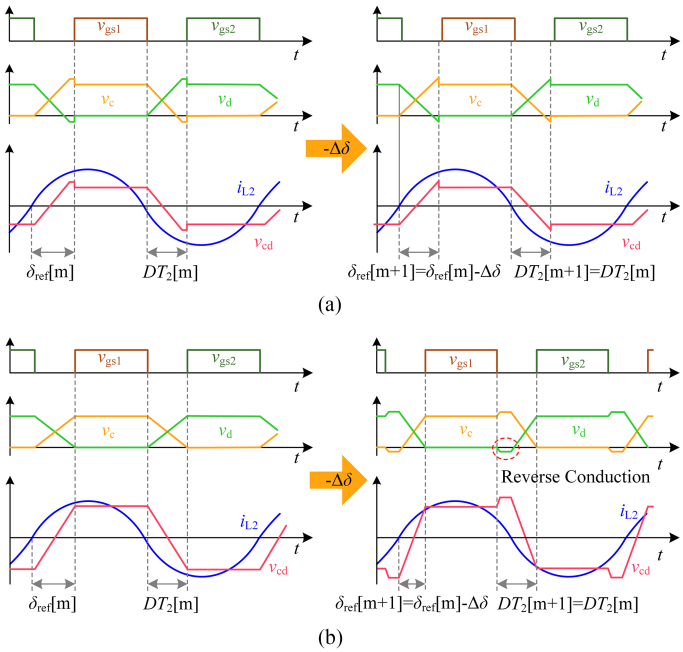

Fig. 9. Single-state control with RCD. (a) Post ZVS operation. (b) Bug caused by the decreasing driving phase and the fixed dead time.

The optimal driving phase and dead time at rated operating conditions are first calculated by substituting the parameters and rated output power into the OOC. Then, the DDTC outer loop regulates the dead time once $v_{\rm rcd}$ is captured. The driving phase reference is calculated and fed to the SDPC inner loop. The driving phase is adjusted at the operating frequency of Clock2. Finally, the driving pulses are generated with the controlled driving phase and dead time.

Compared to the serial control structure, there are also two cases: the parallel control structure and the single-stage control with RCD. Case I is that the DDTC loop operates in parallel with the SDPC loop, as shown in Fig. 8. In Fig. 8(a), the rectifier is in the post ZVS operation at the cycle $[m]$ with $v_{\rm rcd} = 1$. The SDPC loop controls the driving phase to the reference, whereas the DDTC loop decreases the DT_2. Although the rectifier achieves the critical ZVS operation in the cycle $[m+1]$, the excessive driving phase introduces the extra reactive power component, sacrificing the maximum output power of the rectifier. In Fig. 8(b), the rectifier is in the partial ZVS at cycle $[m]$ with $v_{\rm rcd} = 0$. The dead time will be increased while the driving pulse is stabilized at the fixed reference. In cycle $[m+1]$, the reduced on-time causes the reverse conduction to occur in the positive power part. Thus, the dead time is controlled to decrease with $v_{\rm rcd} = 1$. The DDTC loop is in the contradiction where the hard switching is still not eliminated.

Case II is that of a single-stage control with the critical ZVS operation as the target where $v_{\rm rcd}$ is detected as the reference of the driving phase control loop, as shown in Fig. 9. In Fig. 9(a), the rectifier runs in post ZVS operation under the light load. Since the dead time remains constant, the reverse conduction still occurs even if the driving phase decreases until equal to the dead time in cycle $[m+1]$. This situation indicates that fixed dead time is not suitable to the wide load range. If the driving phase continues to decrease at the light load or the phase disturbance is disturbed due to the frequency jitter during the critical ZVS operation, the reverse conduction will occur since $v_{\rm gs1}$ or $v_{\rm gs2}$ sets to zero in advance, as shown in Fig. 9(b). The phase control loop will further decrease the driving phase with $v_{\rm rcd} = 1$, forming positive feedback of the driving phase wrongly. The bug deteriorates the stability of the system and even leads to the phase control failure.

The proposed serial control of DDTC outer loop–SDPC inner loop can achieve the critical ZVS operation with the minimum reactive component. On one hand, the rectifier is in the partial

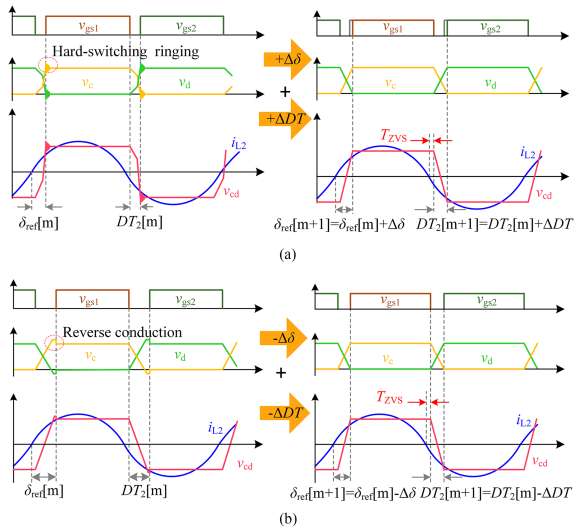

Fig. 10. Proposed serial control structure of DDTC outer loop–SDPC inner loop. (a) Partial ZVS operation. (b) Post ZVS operation.

ZVS operation at cycle $[m]$ with $v_{\mathrm{rcd}} = 0$, as shown in Fig. 10(a). DDTC and SDPC will increase the dead time and driving phase, respectively. The rectifier achieves the critical ZVS operation in the cycle $[m + 1]$, introducing an additional power angle of θ_{zvs}. On the other hand, the rectifier is in post ZVS operation at cycle m with $v_{\mathrm{rcd}} = 1$, as shown in Fig. 10(b). Correspondingly, DDTC and SDPC will decrease the dead time and driving phase, respectively. With the constant θ_{zvs}, the rectifier achieves the critical ZVS operation similarly.

E. Timing Sequence Diagram of the ASDPC Method

The proposed synchronization control method will be illustrated in detail with the timing diagram shown in Fig. 11. In the proposed method, in order to maintain the symmetry of the two bridges, s_1 and s_4 are the same, and so are s_2 and s_3. Thus, the logic of s_3 and s_4 is no longer described here. The rising and falling edges of the driving pulses are defined A and B, respectively, where subscripts represent the corresponding driving pulses.

In the cycle $[n]$, when the rising edge of the v_{cmp1} occurs ($v_{\mathrm{zcd}} = 1$), the instantaneous value of the system clock (Clock1) is recorded as $cnt_1[n]$. With $cnt_1[n]$ and the $\delta[n–1]$ from the unit delay module, $\delta_{\mathrm{sam}}[n]$ can be calculated. Then, the $\delta[n]$ can be obtained based on $\delta_{\mathrm{ref}}[n]$. After delay compensation, $B_1[n]$ is updated by $\delta[n]$. $A_2[n]$ and $B_2[n]$ are then calculated through a dead time $DT_2[n]$ and a half operating cycle $T/2$. Finally, $A_1[n]$ is obtained by $DT_2[n]$ and $B_2[n]$.

Since the v_{det} keeps higher than V_{th}, v_{rmp2} remains low. Therefore, both δ_{ref} and DT_2 are increased in the cycle $[m + 1]$. It can be seen that δ_{ref} and DT_2 are updated in the negative half wave of i_{L2}, between $t[n]$ and $t[n + 1]$, which guarantees that the two control loops do not interfere with each other. In the cycle $[n + 1]$, the $cnt_1[n + 1]$ is updated at $t[n + 1]$. With the new $\delta_{\mathrm{ref}}[n + 1]$ ($= \delta_{\mathrm{ref}}[m + 1]$) and $DT_2[n + 1]$ ($= DT_2[m + 1]$), the $B_1[n + 1]$, $A_2[n + 1]$, $B_2[n + 1]$ and $A_1[n + 1]$ are updated in the same way. Whenever a synchronous signal is generated, the system always controls B_1 of the current cycle to slightly lag the i_{L2} by T_{zvs} in the negative zero crossing point. By using the half beat control, the propagation delay can be accurately compensated. The system is highly robust.

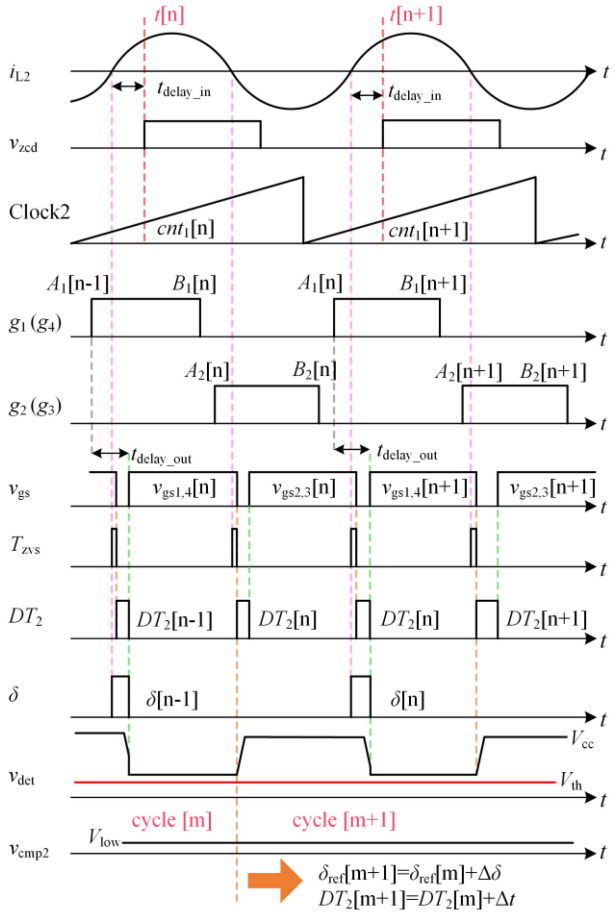

Fig. 11. Timing sequence diagram of the ASDPC method.

TABLE I
CIRCUIT PARAMETERS OF THE PROPOSED WPTS

Symbol	Description	Value
L_1	Primary resonant inductor	3.05 μH
C_1	Primary resonant capacitor	178 pF
R_1	Primary ESR of resonant network	0.4 Ω
L_2	Secondary resonant inductor	3.06 μH
C_2	Secondary resonant capacitor	176 pF
R_2	Secondary ESR of resonant network	0.4 Ω
M	Mutual inductance of L_1 and L_2	0.32 μH
f	Operating frequency	6.78 MHz
R_{dson}	Drain-source on resistance of GaN HEMTs	0.024 Ω
V_{sd}	Reverse conduction voltage of GaN HEMTs	2.1 V
R_{L}	Load resistor	8−50 Ω
d	Face to face distance of coils	4.5 cm
k	Coupling coefficient	0.105

IV. EXPERIMENTAL VERIFICATION

A. Experimental Platform Setup

To verify the proposed ASDPC method, a 50-W GaN-based full-bridge 6.78-MHz WPTS is built as shown in Fig. 12. The specific circuit parameters and key devices used are listed in Tables I and II.

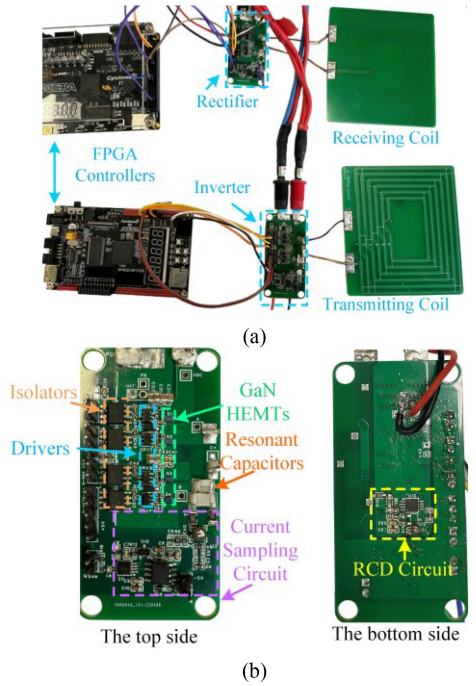

Fig. 12. Prototype of the 50-W GaN-based full-bridge 6.78-MHz WPTS. (a) Overview of the prototype. (b) Detailed view of the rectifier.

TABLE II
KEY COMPONENTS PARAMETERS OF THE PROPOSED WPTS

Component	Parameters
GaN HEMT	EPC2007C
Driver	LM5114
Comparator	ADCMP602
Controller	EP4CE10F17C8
Operational amplifier	AD8055
Isolator	ADuM121N
Coupled inductor	LPD5030-103
Diode for RCD	RF01vm2sfh

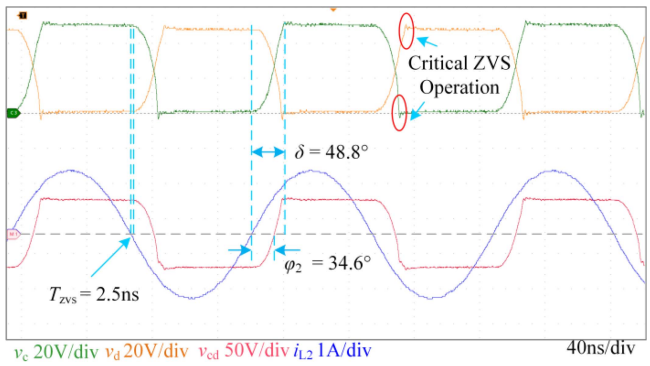

Fig. 13. Steady waveforms at the rate operating condition.

The circuit boards of the inverters and rectifiers are well-designed to optimize the parasitic parameters. The coils are single-sided PCB coils with same dimensions of 10 cm × 8 cm.

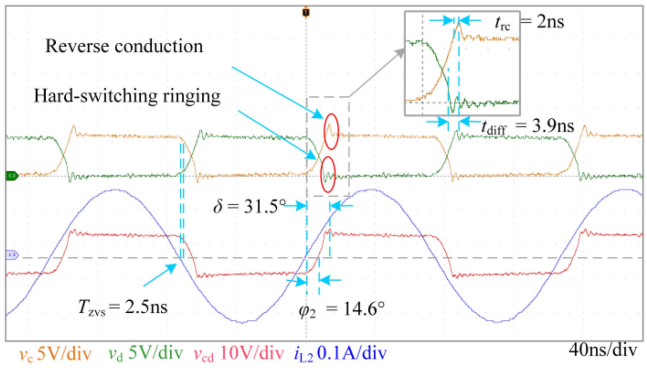

Fig. 14. Steady waveforms at the limit operating condition.

B. Steady-State Verification

Fig. 13 illustrates the steady-state waveforms at the rated operating condition where V_{dc} is 40 V, R_L is 40 Ω. P_o is 44.9 W, P_{in} is 51.5 W, and dc–dc efficiency is 87.18%. The green curve is the voltage at the midpoint c (v_c), the yellow curve is the voltage at the midpoint d (v_d), the pink curve is the input voltage of the rectifier (v_{cd}), and the blue curve is the secondary current (i_{L2}). As can be seen, the rectifier achieves the critical ZVS operation without reverse conduction and hard-switching ringing. The power angle φ_2 is 34.6°, δ is 48.8° and T_{zvs} is 2.5 ns. Hence, the effectiveness of the method is proved by the waveform in the rated operation case.

Fig. 14 shows the steady-state waveforms at the limit operating condition with low output power where V_{dc} is 5 V, R_L is 40 Ω. P_o is 0.63 W, P_{in} is 0.79 W, and dc–dc efficiency is 79.7%. The yellow curve is the voltage at the midpoint c (v_c), the green curve is the voltage at the midpoint d (v_d), the pink curve is the input voltage of the rectifier (v_{cd}), and the blue curve is the secondary current (i_{L2}). The power angle φ_2 is 14.6°, δ is 31.5° and T_{zvs} remains 2.5 ns. As the output power decreases, the driving phase and dead time decrease adaptively. Since the current is captured through the voltage of the resonant capacitor, the SDPC loop can still be triggered stably at a limit operation. The serial control structure also helps to improve the stability of the system. With the proposed ASDPC method, the system can operate in the critical ZVS operation stably even at low output power.

As can be seen, both post ZVS operation and partial ZVS operation are present in the rectifier. The reason is the asymmetry of the bridges caused by the difference in parasitic inductance of the power and drive loops of the two bridges. The difference in the driving loop parasitic inductances and the input capacitance of the GaN HEMTs can lead to variability in the switch turn-ON speed. Therefore, the turn-ON process of the top switch is slower than that of the low switch. The discharging process is also faster than the charging process. Although the low switch has experienced some of the hard-switch ringing, v_{rcd} is triggered to 1 due to the slower turn-ON process of the top switch. Thus, the dead time will not be increased. The hysteresis time between the two switches turn ON is measured to 3.9 ns.

Under this limit operating condition, the output voltage is smaller. Hence, the required Q_{oss} is smaller. The effect of the

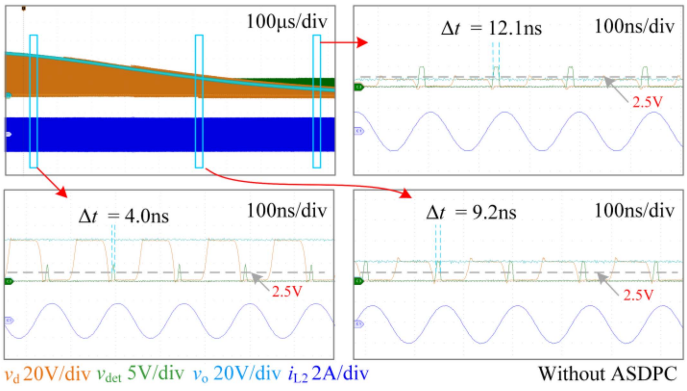

Fig. 15. Dynamic waveforms of the system without ASDPC method.

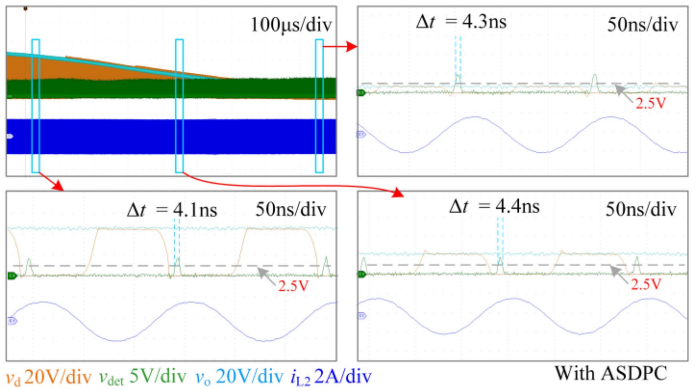

Fig. 16. Dynamic waveforms of the system with ASDPC method.

hysteresis time is more obvious consequently. As the output power increases, its effect on the critical ZVS operation diminishes. The reverse conduction interval ($t_{\rm rc}$) is 2 ns, which is lower than the $T_{\rm clk1}$ (= 2.5 ns). The minor impact on efficiency and output power is acceptable. In summary, the stability and effectiveness of the proposed method are demonstrated.

C. Dynamic Verification

A dynamic experiment was set up to verify the dynamic characteristic of the proposed ASDPC. The system was running stably at the rated operating condition ($V_{\rm dc} = 40$ V, $R_{\rm L} = 40\ \Omega$. $P_{\rm o} = 44.9$ W) before the load changed. It is noted that the system without ASDPC operates in the fixed dead time and driving phase reference.

The dynamic waveforms without DDTC are shown in Fig. 15 when the load is changed from 40 to 8 Ω. The waveforms at 10, 530, and 880 μs after load change are shown in detail. The yellow curve is the voltage at the midpoint d ($v_{\rm d}$), the green curve is the voltage at the "+" terminal of the comparator ($v_{\rm det}$), the light blue curve is the rectifier output voltage ($V_{\rm o}$), and the blue curve is the resonant current ($i_{\rm L2}$). The comparator is at TTL level where the threshold is 2.5 V. The post ZVS operation occurs in the system without DDTC when the load is changed to the light load. The time when $v_{\rm det}$ is high is increased from 4.0 to 12.1 ns. This indicates a significant increase of the reverse conduction time. When the system resumes stable at 8 Ω, $P_{\rm o}$ is 10.6 W, $P_{\rm in}$ is 13.94 W, and dc–dc efficiency is 76.2%.

The dynamic waveforms with ASDPC are shown in Fig. 16 when the load is changed from 40 to 8 Ω. The waveforms at 10, 480, and 885 μs after load change are shown in detail. With the ASDPC, the time when $v_{\rm det}$ is high is almost constant (≈ 4 ns). The critical ZVS operation is maintained during the load change. The results verify the stability and the fast response speed of the proposed method when the load changes. When the system resumes stable at 8 Ω, $P_{\rm o}$ is 11.8 W, $P_{\rm in}$ is 14.5W, and dc–dc efficiency is 81.4%. The output power and the efficiency are increased by reducing the excess reverse conduction and the additional reactive power components.

Fig. 17 illustrates the output power and the dc–dc efficiency of the system with/without ASDPC over a wide load range. To avoid unfair comparisons, both systems have been stable at the rated operating condition with the critical ZVS operation.

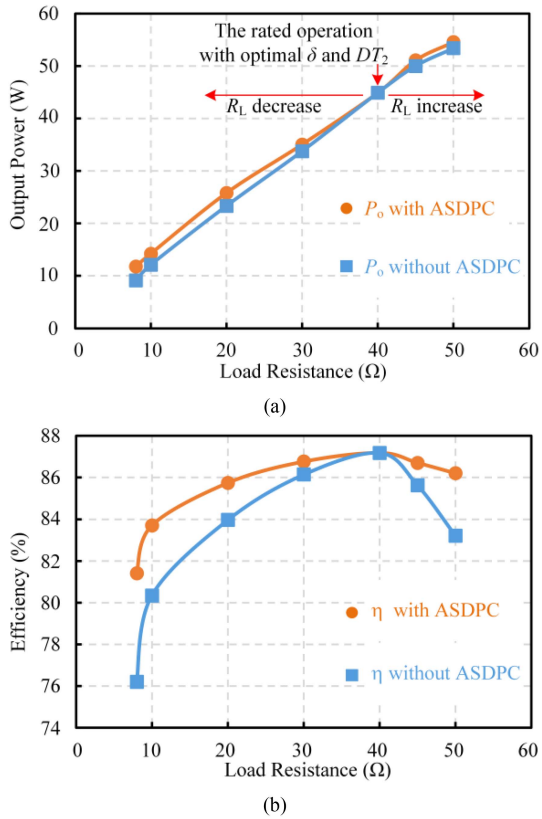

Fig. 17. (a) Output power and (b) DC–DC efficiency of the WPTS with/without proposed ASDPC method over the wide load range.

After varying the load resistance, their output power and dc–dc efficiency are collected for comparison. In this way, the system is in post ZVS operation when $R_{\rm L} < 40\ \Omega$, whereas in partial ZVS operation when $R_{\rm L} > 40\ \Omega$. From the results, it is clear that even though the system achieves ZVS operation, the reverse conduction loss due to the post ZVS operation and the excessive reactive power angle do reduce the output power and efficiency. Although the partial ZVS operation reduced some of the hard-switching loss, it is still significant in 6.78 MHz at heavy load. The system with the proposed ASDPC obtains a maximum efficiency of 87.18% at $P_{\rm o} = 44.9$ W when $R_{\rm L} = 40\ \Omega$. Compared to the system without ASDPC, the efficiency can be improved by 5.2% at light load and 3.1% at heavy load.

V. Conclusion

This article proposed an ASDPC for the full-bridge 6.78-MHz WPTS. First, the conditions to achieve the critical ZVS operation in full-bridge rectifier are derived from the FHA model and the time domain model. The OOC with the maximum output power and the critical ZVS operation can be obtained. Second, an ASDPC method is illustrated to keep the rectifier operating on the OOC. The positive zero crossing point of the secondary resonant current is detected as the synchronous signal to control the driving phase angle, where the delay is precisely calculated and compensated. Then, the structure of the DDTC outer loop–SDPC inner loop serial control strategy is analyzed in detail. Finally, a 50-W GaN-based full-bridge 6.78-MHz WPTS is built. The steady-state and dynamic experimental results verify the effectiveness and stability of the proposed method. The proposed ASDPC method enables full-bridge active rectifier to achieve the critical ZVS operation and the maximum output power over the wide load range. The system obtains a maximum efficiency of 87.18% at $P_{\mathrm{o}} = 44.9$ W. Compared to the system without ASDPC, the efficiency can be improved by 5.2% at light load and 3.1% at heavy load.

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