An Accurate and Intelligent Approach to Predicting the Power Device Fatigue Failure Process

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***Abstract*—It is significant to study power device package fatigue failure as it seriously affects the reliability of power systems. Nevertheless, the research of the power device failure process is insufficient. In this article, an accurate and intelligent approach is proposed to predict the power device fatigue failure process with multiple fatigue sampling method (MFSM) and minimal component unit method (MCUM). The MFSM is proposed to accurately build the power device lifetime model. It is accomplished through the multiple sampling fatigue morphology evolution process of solder layers combined with the fatigue parameter. Morphology evolution is detected by scanning acoustic microscope technology under an accelerated lifetime test. The fatigue parameter is obtained through finite-element analysis (FEA) by establishing each sampling geometry model. Then, the lifetime model is determined by their same failure area fraction (F_s). In particular, digital image processing is applied to describe solder layer shapes in detail, which is also the key to building a real FEA geometry model. The MCUM is utilized to complete the prediction of failure process, where solder layers are divided into minimal units and the FEA solution and location information of each unit are known. Based on the lifetime model, the failure area can be determined and the fatigue failure process can be finished intelligently by cosimulation. The proposed method is accurate and intelligent enough in predicting the failure of solder layers, which is more helpful for planned device management.**

***Index Terms*—Digital image processing (DIP), failure area fraction, fatigue failure process, lifetime model, minimal component unit method (MCUM), multiple fatigue sampling method (MFSM).**

I. Introduction

NOWADAYS, power electronic systems have been widely used in many fields, such as aerospace, industrial automation, transportation, and renewable energy power generation, which require high reliability [1], [2], [3]. As the core part of power electronic systems, power semiconductor devices are one of the most fragile components [4]. According to reports, power electronic device failures account for more than 30% of power electronic system failures [5]. The failure modes can generally be separated into two categories: chip related and packaging related. Chip-related failures can directly cause the device to become inoperable. Packaging-related failures can be further divided into bonding wire failure and solder layer failure. They both have a fatigue process. By studying the process, the lifetime can be obtained. And it will be helpful to achieve planned equipment maintenance to avoid catastrophic failures. Especially, the solder layer lifetime model and fatigue failure process are studied in this article.

The existing lifetime model can be divided into empirical model and physical model [6], [7]. The advantage of empirical model is that its form is relatively simple, and its parameters can be extracted through accelerated lifetime test (ALT) data without considering the specific physical structure and material characteristics of the power device. Temperature fluctuation is an important factor that is first considered [8]. Due to the less factors considered, the results are not accurate enough. The Norris–Landzberg model takes into account the frequency of cycles based on the Coffin–Manson model [9]. In addition to frequency, other factors also affect the fatigue failure process. The Bayerer model [10] considers medium temperature, heating time t_{on}, the load current *I*, the bonding wire diameter *D*, and the device block voltage *V*. Although the prediction accuracy has improved, the Bayerer model depends on a large number of acceleration test results under different operating conditions, which takes a lot of time and cost. Therefore, some physical models were proposed to reflect the physical nature of fatigue failure and establish the relationship between failure physical mechanism and lifetime. They can be divided into three major categories, which are stress-based, strain-based, and energy-based. The Basquin equation is used to describe fatigue failures caused by stress change [11]. The Engelmaier model highlights the impact of strain [12]. The energy-based model [13], which is called strain–stress energy, takes into account both stress and strain. During the application of physical models, finite-element analysis (FEA) is an essential tool for obtaining critical stress or strain. By combining physical models with FEA, the lifetime of the power device under different operating conditions can be accurately predicted, thus the health status of the device can be effectively monitored.

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However, there are still some problems in the application of physical lifetime models currently. On the one hand, the lifetime model is difficult to calibrate from the point of view of material properties. Pang et al. [14] measured derived solder alloy mechanical properties from the bulk specimen tensile test and lap shear solder joint tests specimen. Kim et al. [15] evaluated the microstructures and tensile properties of three typical solder alloys under three different cooling conditions. Samavatian et al. [16] considered the plastic strain and creep strain during the solder fatigue failure. But few physical lifetime models are applied to lifetime prediction. On the other hand, it is difficult to establish the real shape of the solder layer in FEA [17], [18], [19]. It has been found that voids will appear inevitably in the device solder layers, not only in semiconductor devices production [20], [21] but also during fatigue failure. Tran et al. [22] built a detailed 3-D electrothermal model of the solder layer containing ideal circular void to suggest a method for optimizing void thresholding from multiphysical viewpoint. Surendar et al. [23] established circular voids in the solder geometry model to analyze how the number of thermal cycles would affect the mechanical properties and thermal conductivity of porous solder. Hu et al. [24] studied the slow fatigue failure process in the presence of initial defects that are represented as ideal triangles and circles in FEA under thermal stress cycles. Huang et al. [25] established the FEA geometry of the real solder layer in one fatigue state to study the failure mechanism of the die-attach. Nevertheless, there is a lack of an effective method to describe the different fatigue states of the solder layer and the whole fatigue failure process has not been studied.

The purpose of this article is to solve the aforementioned problems so as to more accurately and intelligently predict the fatigue process of solder layers. An accurate method named multiple fatigue sampling method (MFSM) is proposed to study the lifetime model, and digital image processing (DIP) is applied to establish a real FEA model. After these, the minimal component unit method (MCUM) is used to intelligently predict the whole fatigue failure process of the power device with cosimulation based on the lifetime model. In this way, the fatigue failure of the power device can be obtained by advanced simulation technology and the critical fault can be predicted under various working condition, which significantly reduces device development costs.

The rest of this article is organized as follows. In Section II, DIP means is introduced. The fatigue power device needs to be detected through the scanning acoustic microscope (SAM) technique first to get the morphology of solder layers in the form of an image. Then, the location information of the solder layers is identified by various DIP intelligent algorithms, and the outline drawn by them will be displayed. They are also used to map the process of fatigue change and to establish the exact FEA model. In Section III, the details of the MFSM are revealed. As a way to accelerate fatigue failure, a power cycling (PC) test is done to acquire the whole morphology evolution, and fatigue characteristics are measured by online monitoring. During this procedure, a constant period is set for sampling. Meanwhile, the corresponding FEA verified by transient thermal resistance is established to obtain the fatigue parameters. The lifetime model is determined by failure area fraction (F_s) combining morphology evolution and fatigue parameter. In Section IV, more detail of the MCUM is shown to predict intelligently the solder layer fatigue process and characteristic change through the cosimulation of MATLAB and COMSOL. The brand-new IGBT device in a different work condition is done to validate the aforementioned lifetime model and prediction method. Finally, Section V concludes this article.

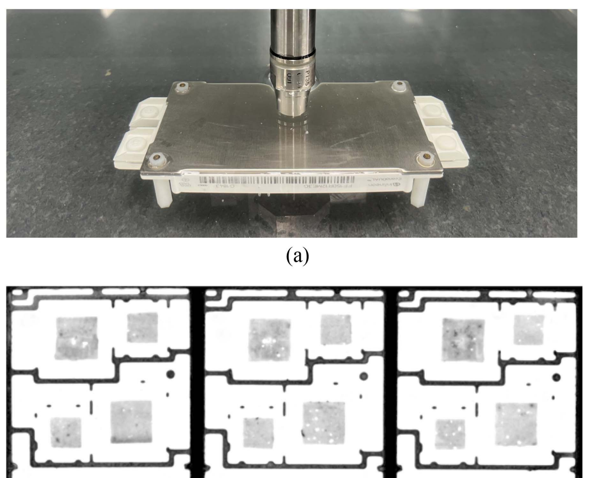


Fig. 1. Observation of the solder layers. (a) SAM scans solder layers of the module. (b) Scanned image of solder layers.

II. Location Information Acquirement of Solder Layer Morphology

The SAM technique and DIP means are used to get the irregular solder layer morphology. They are, respectively, applied for solder layer observation and identification.

A. Observation of the Solder Layers

At present, two main techniques of detecting semiconductor devices are X-ray tools and SAM [26], and their effectivities have been proved by destructive cross-sectional techniques [26].

The technique of observing solder layers used in this article is SAM, as shown in Fig. 1(a). SAM is a nondestructive testing equipment that uses ultrasonic waves to image microscopic objects. The acoustic image produced by SAM is entirely caused by variations on the surface or inside the material. Because ultrasonic waves propagate differently in copper and solder and cannot propagate in air, which is the state of voids, the real shapes of solder layers can be reflected. The device used in the experimental process is FF150R12ME3G and one of scanned results of solder layers under chips is shown in Fig. 1(b). In this figure, the gray square area is the solder and the white in the gray are voids. It can be seen that the boundaries of the solder and voids are fairly clear, which provides the possibility of identifying the solder and voids.

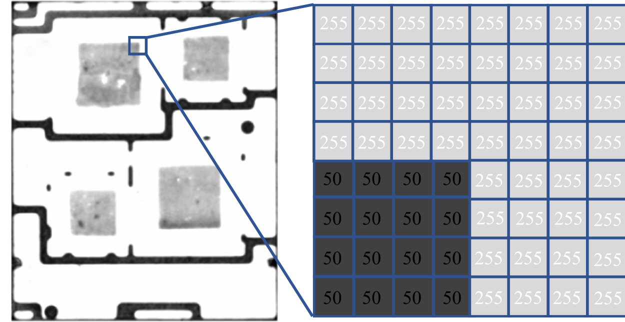


Fig. 2. Digital array format in DIP of the partial image after grayscale processing.

B. Identification of the Solder Layers

To get accurate location information of the solder layer from the SAM images, what is the digital image needs to be considered. Generally, an image is defined as a 2-D function, $F(x,y)$, where x and y are spatial coordinates, and the amplitude of F at any pair of coordinates (x,y) is called the intensity of the image at that point. When x,y, and amplitude values of F are finite, it is a digital image. The type of images used in this article is 8-bit color format. It has 256 different shades of colors in it and commonly known as grayscale image. In this format, 0 stands for black, 255 stands for white and other intermediate values stands for different shades of gray. The local digital array of the solder layer image is shown in Fig. 2, where the boundaries of solder and voids in the digital array are as obvious as the image.

DIP means are applied to automatically identify the location information of solder and voids. In fact, DIP is the process of calculating the digital array, in which computer algorithms are used to get enhanced image and extract the useful information. In this article, only solder layers under IGBTs are processed and the whole results are shown in Fig. 3. The red contour boundaries in Fig. 3(e) are the final processing result composed of the coordinates identified by DIP, which can be built directly in FEA geometry to accomplish the real solder layer geometry model. It can be seen that recognized coordinates can truly reflect the shape of solder layers. The application principle and the process are introduced as follows, which can be divided into three parts, namely convolution filtering, nonlinear reinforcement, and contour detection.

The purpose of convolution filtering is to remove the noises in the digital image generated by SAM when detecting the device. Its working principle is shown in Fig. 4(a) and the digital image result is shown in Fig. 3(b). The kernel performs convolution operation with the input image array in turn and each value in the result array is a weighted average of itself and others in the surrounding field. Gaussian convolution kernel is selected in this article, which can increase the weight value of the center point, and reduce the points away from the center. So, the effects of isolated value, which is the way of the noises exist can be reduced. By preprocessing in this way, interference can be eliminated.

Nonlinear reinforcement algorithms are the key part of identification, which are used to recognize the boundaries of the solder and voids. Different from the convolution filtering, it is to traverse and numerically calculate each value of the image array. And there are two steps, enhancing the grayscale difference and binarizing. The enhancement algorithm is Gamma transform, its application result of different value is shown in Fig. 4(b). In this figure, it can be seen that when $\gamma > 1$, the gap between small numbers and larger numbers will be bigger. Corresponding to the solder layer, the distinction of the solder and voids in digital array will increase after using this transform, as shown in Fig. 3(c) and this will get a better result for the next step. Binarization is to convert the image to black and white, which means there are only

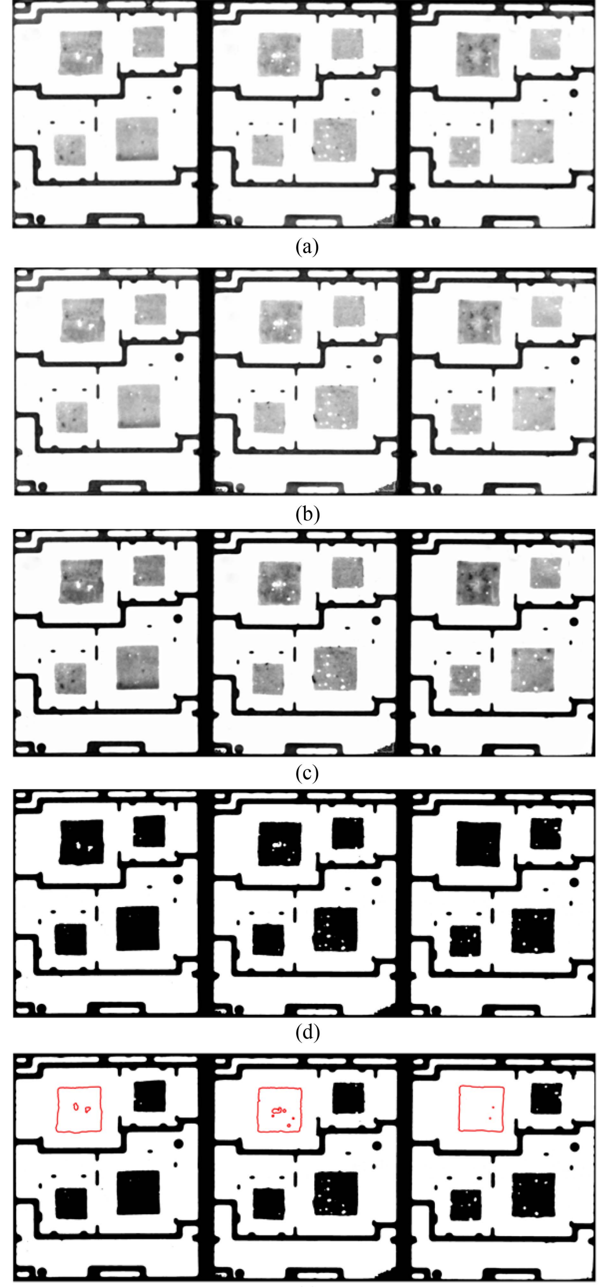
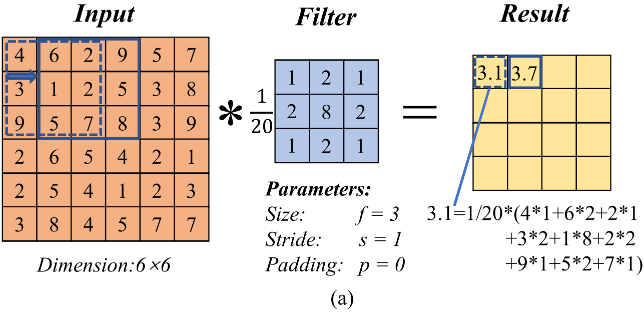


Fig. 3. Results in DIP. (a) Digital image. (b) Convolution filtering. (c) and (d) Nonlinear reinforcement. (e) Contour detection.



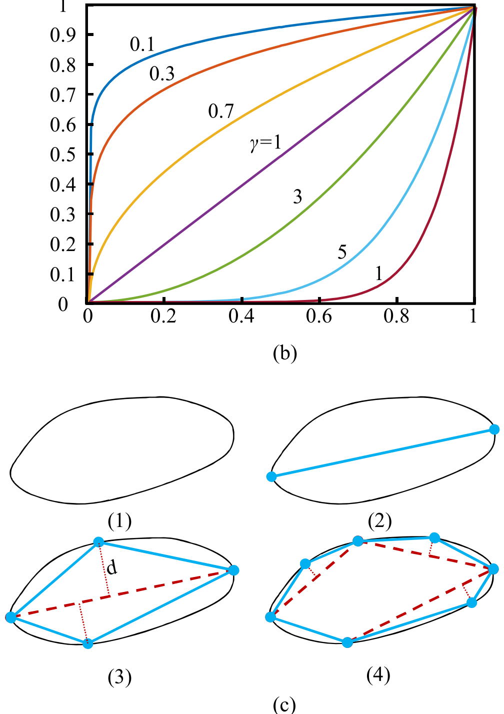


Fig. 4. Principles in the DIP. (a) Convolution filtering. (b) Nonlinear reinforcement. (c) Contour detection.

two values in the digital image array. The realization method is to determine a threshold value to distinguish the solder and voids. When the matrix value is bigger than the threshold, it is white, otherwise it is black. After this step, shapes of solder layers are determined as shown in Fig. 3(d).

The last step in DIP is to identify solder layer shapes by location coordinates based on the binarized image. To get more accurate FEA results, the quality of meshing must be ensured. Considering that the smallest unit shape of mesh division is a triangle, it is better to fit solder layers into the polygon, which can greatly improve the efficiency and accuracy of modeling and solution. The principle of fitting is shown in Fig. 4(c), where the void is randomly shaped, and a polygon approaches it infinitely. Its core idea is to determine the two farthest points in the void boundary first, then selecting points in the boundary with the longest distance to every edge of the polygon until the distance of the whole points is less than the set threshold, which determines the fitting precision. After fitting, coordinates of the polygon are known, and they can be built in the FEA geometry model.

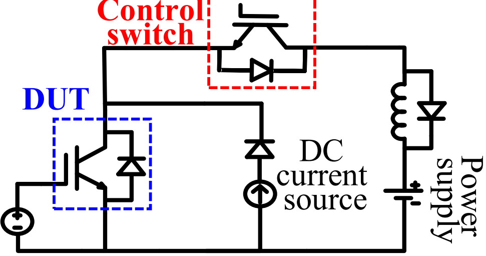


Fig. 5. PC test circuit diagram.

Only three solder layers of the device are identified as shown in Fig. 3(e), as the center of this article is to study solder layers under IGBT.

As aforementioned, whether the power device is new or in the fatigue state, the solder layer can be identified and the real FEA geometry model can be established.

III. Determination of the Solder Layer Lifetime Model

To explore the solder layer lifetime model, the sampling method named MFSM is proposed in this part. First, the PC test is done in this part to get the morphology evolution. And fatigue parameters of each sampling are calculated by FEA based on the PC test. Then, the lifetime model is determined through F_s.

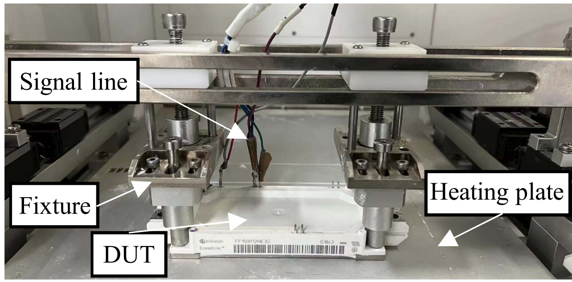
A. PC Test

The PC test is a major way to investigate the reliability of power electronic devices [27], [28]. The circuit diagram is shown in Fig. 5. The device under test in this article is FF150R12ME3G and the dc PC test is done to fatigue the solder layers. In order to know the fatigue state of the device, many characteristics are monitored online, such as junction temperature T_j, the collector–emitter voltage $V_{\rm ce}$, $R_{\rm th\cdot jc}$, etc.

T_j is a significant parameter during the solder fatigue failure. The saturation voltage drop ($V_{\rm cesat}$) of the device at low current as a thermal sensitive electrical parameter is measured to calculate the T_j in this article. Before measuring the T_j by $V_{\rm cesat}$, the temperature coefficient calibration (TCC) test has been carried out, as shown in Fig. 6(a). The device is placed in a closed equipment and heated by a heating plate, whose temperature is considered equal to the case temperature ($T_{\rm c}$). When the temperature of the heating plate reaches the set value, it will remain constant. At this time, the device as a whole has reached a thermally stable state, which means the T_j is the same as T_c. Then, $V_{\rm cesat}$ is tested through the measuring lines. A total of eight temperature values were set in this article and the temperature characteristic curve obtained by the TCC test is shown in Fig. 7(a), which has good linearity and sensitivity, where the slope of the fitted line is –2.37 mV/°C and the intercept is 0.663 V. Once the relationship of $V_{\rm ce}$ and T_j is obtained, the T_j can be calculated online, which can be expressed as

$$V_{\rm CE} = -0.00237 \cdot T_j + 0.663. \quad (1)$$

The PC test is shown in Fig. 6(b). Different from the TCC test, thick copper wires are connected to the terminals of the device,



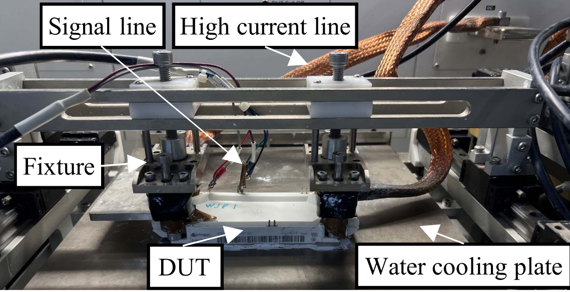


Fig. 6. (a) TCC test. (b) PC test.

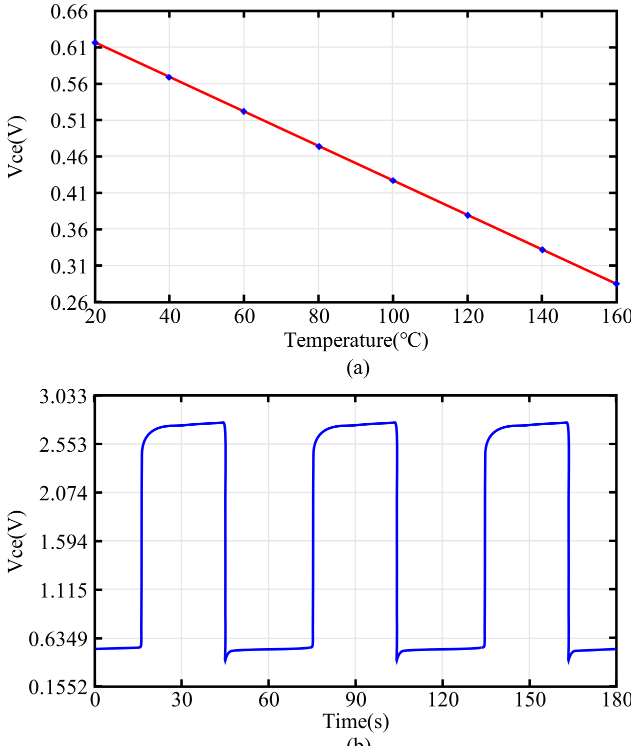


Fig. 7. Results of (a) TCC test and (b) PC test.

and a large current set as 180 A passes through the IGBT. The device is fixed to the water-cooling plate using a clamp, and the water temperature is set to 20 °C. In order to accelerate the fatigue of solders, the period is set to 1 min, and the high current passes half of the time. The V_{ce} results of the PC test for several cycles are shown in Fig. 7(b), and it is worth noting that it will change as the solder layers fatigue and voids expand. It is known

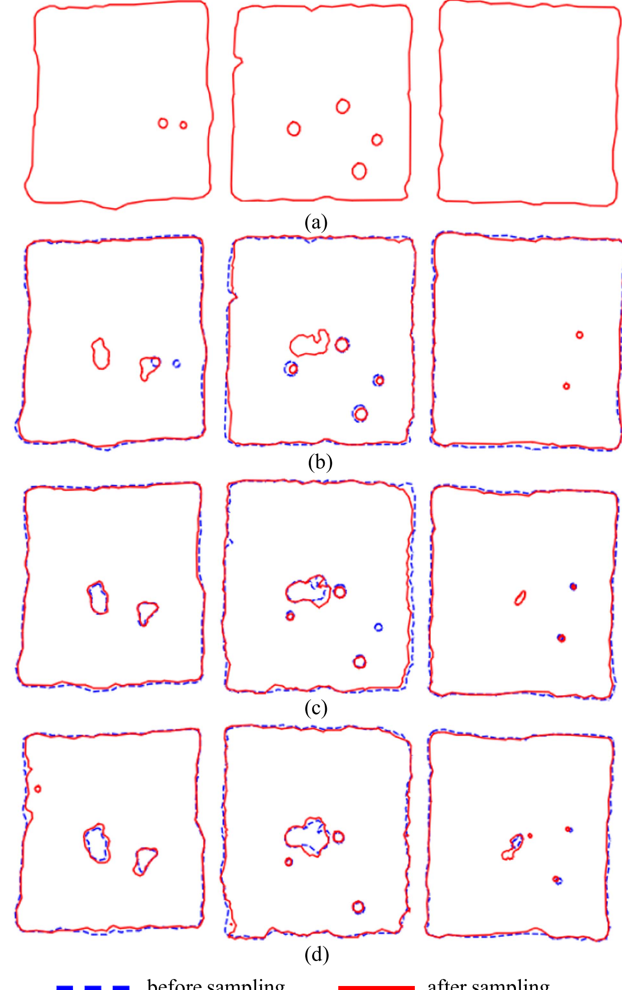
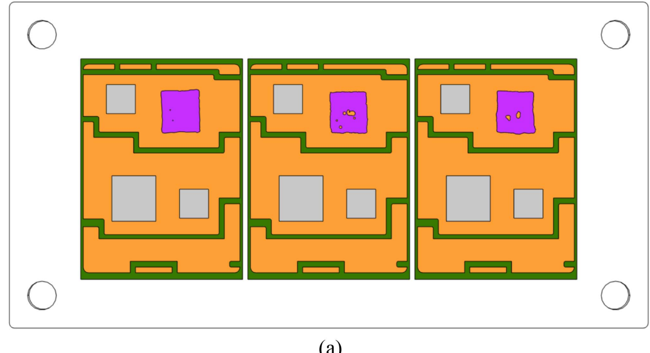


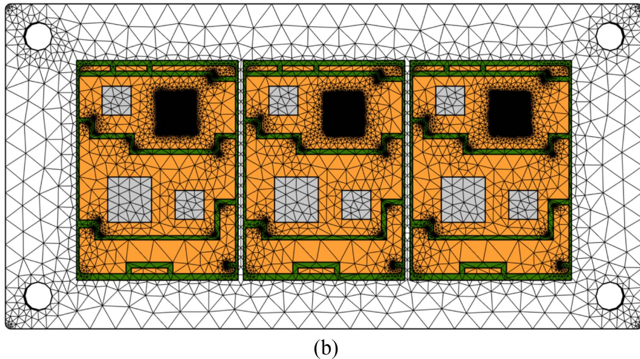
Fig. 8. Sampling results (a) original, (b) first sampling, (c) second sampling, and (d) third sampling.

that ΔT_j is the biggest factor affecting fatigue failure. Therefore ΔT_j in this article is raised as high as possible, which reaches over 100 °C.

There are a total of 75 thousand cycles done in this article when thermal resistance increases by 20%, which means the power device has completely failed. In the whole process, the device is sampled four times. And since the initial sampling device is brand new, it is called zeroth sampling. The sampling after the PC test is called the first, second, and third sampling. Therefore, there are four states of solder layers that are applied to determine the lifetime model. The morphology evolution of solder layers is shown in Fig. 8, which is described through DIP, where the blue dotted line represents the solder layer shapes before sampling, and red solid line represents after sampling. It can be found that the fatigue failure area is always in the center of the solder layers and around the outer boundaries. Especially, it is random of the failure area location when voids first exist in the solder center. This situation is not observed first [29], it has a lot to do with individual differences. It is also worth noting that some of the small voids disappear and some voids become smaller after the PC test, this is because the stress and strain



(a)



(b)

Fig. 9. (a) Geometry and (b) meshes of the FEA model.

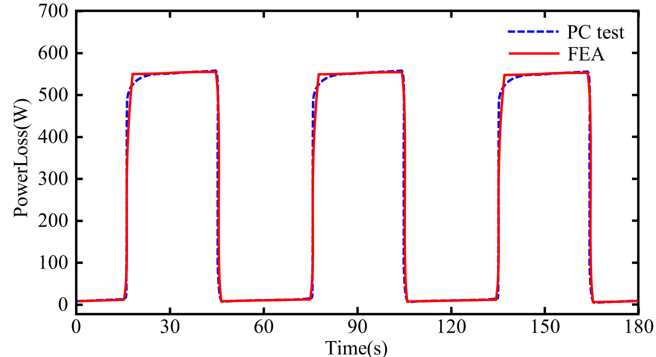


Fig. 10. Power loss curves of the PC test and FEA.

TABLE I
MAJOR MATERIAL PROPERTIES AND THICKNESS OF THE DEVICE

Layers	Materials	ρ (kg/m^3)	k (W/(m·°C))	C_p (J(kg·°C))	Thickness (mm)
Chip	Si	2330	$k_{si}(T)$	$C_{p\text{-}si}(T)$	0.12
Solder	SnAgCu	7404	64	232	0.1
DBC copper	Cu	8700	400	385	0.3
Ceramics	Al_2O_3	3900	27	776	0.635
Baseplate	Cu	8700	400	385	3

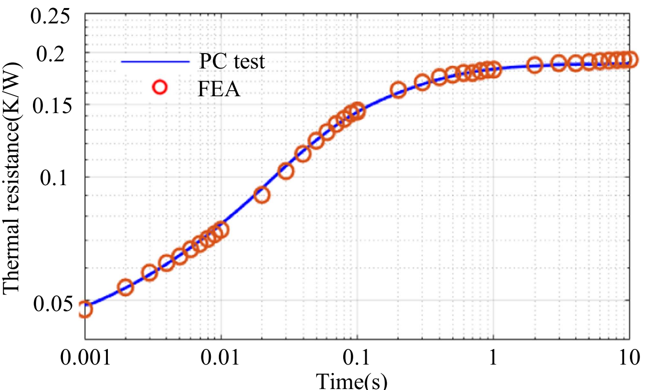


Fig. 11. Transient thermal resistance obtained from the PC test and FEA.

around them are influenced by their void radius [24], and in the fatigue process, the solder will deform. Also, it is why after PC test, some void areas are filled with the solder again and the void shape changes too much.

B. Thermomechanical Physics Model of FEA

FEA is one of the most commonly used methods for analyzing the thermomechanical behavior of devices during fatigue. The FEA tool used in this article is COMSOL Multiphysics, which has already been a widely recognized commercial FEA software. There is a feature of COMSOL that is its modeling process can be controlled by MATLAB codes. With this, FEA can be finished automatically including establishing the geometry, setting up thermomechanical physics, boundary condition, and so on.

The geometry model is automatically established by program control. According to the coordinates identified by DIP mentioned before, the shapes and sizes of the solder layers are known, and one of the fatigue states in FEA is shown in Fig. 9(a). It can be seen that through the control of the algorithm, FEA geometry can restore the shape of the device, no matter how complex it is. In particular, the mesh of the device in FEA is shown in Fig. 9(b), where units of the solder layer mesh are very small, which means higher quality and more accurate solutions.

By means of online monitoring, the boundary conditions of the thermomechanical physics model are kept consistent with the PC test. They include the IGBT power loss, as shown in Fig. 10, the convection coefficient of water cooling, four fixed corners of the substrate held on by the fixture, and so on. And major material properties and thickness of the device in FEA are shown in Table I.

Anand's viscoelastic material model [30] is used to simulate the creep process of solders, as it explains physical phenomena such as strain rate, strain hardening, crystalline structure, and evolution.

Thermal resistance is an important indicator for evaluating the fatigue failure of the solder layer. Typically, a module is considered failed when the thermal resistance exceeds the initial 20%. Therefore, the FEA model is validated through the transient thermal resistance as shown in Fig. 11.

The FEA strain results obtained by establishing the geometry model before sampling are shown in Fig. 12. It can be found that the bigger strain values are concentrated at the boundaries, and fatigue failure at the boundaries has also been observed in the PC test. The failure area obtained by both are consistent.

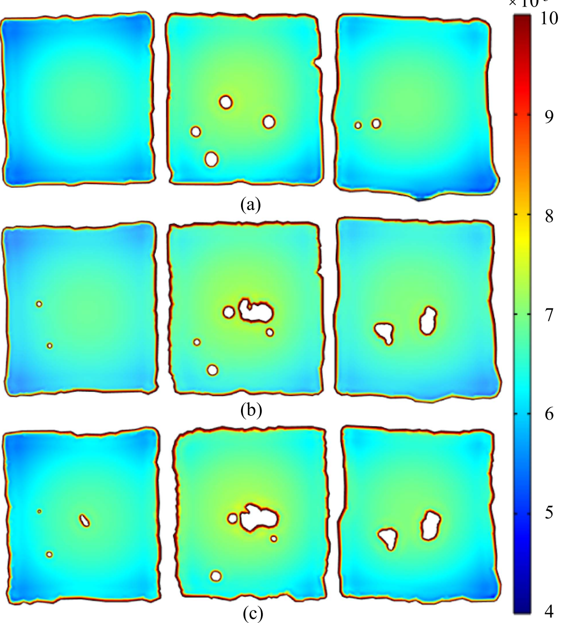


Fig. 12. Solder layer strain results of FEA before sampling. (a) First sampling. (b) Second sampling. (c) Third sampling.

C. Lifetime Model of the Solder Fatigue Failure

The procedures of fatigue failure lifetime modeling consist of four primary steps [31].

1) A theoretical or constitutive equation forms the basis for modeling, which can be defined or chosen. Appropriate assumptions need to be made in constructing the constitutive equation.
2) The constitutive equation is translated into an FEA program and a model created. The FEA program calculates the predicted stress–strain values for the system under study and returns stress values for the simulated conditions.
3) The FEA results are used to create a model predicting the number of cycles to failure, N_f.
4) The model or results must be tested and verified using thermal cycling data.

These four steps describe the general process where fatigue modeling is developed, implemented, and verified. Anand's constitutive model and FEA software COMSOL have been introduced, which correspond to the first two steps. And the third and fourth steps are as follows.

In the third step, a model needs to be created. The lifetime model is the basis of predicting the N_f of the solder layer. As mentioned before, the lifetime model can be divided into many categories. In order to reflect the microscopic principle of the solder layer fatigue, the strain-based lifetime model is applied in this article and it comes in many forms one of which is shown as follows:

$$N_f = C_1(\Delta\varepsilon_p)^{-C_2} \tag{2}$$

where N_f is the solder lifetime, $\Delta\varepsilon_p$ is fatigue parameter strain change per cycle, and C_1 and C_2 are constant related to the solder material. It can be concluded that it is a monotone function between N_f and $\Delta\varepsilon_p$ in terms of the lifetime model expression. In other words, the N_f of the solder depends on the amount of $\Delta\varepsilon_p$. Actually, in the production of power devices, the material and reflow process are the same, so the N_f of solder layers is theoretically equal. The reason why some areas, such as the solder around and in the mid of solder layers observed in Fig. 8, first experienced fatigue failure is that their strain changes $\Delta\varepsilon_p$ are bigger than the others. There must be a threshold $\varepsilon_{\mathrm{th}}$, and when the accumulated strain reaches it, the solder fatigue failure occurs, which means that when the value of $\varepsilon_{\mathrm{th}}$ is determined, the lifetime model can be obtained. With this model, when the solder layer fails, it can be determined, and the fatigue process can be predicted. A particular sampling method is proposed to complete the lifetime model in the fourth step.

Procedures of the sampling method named MFSM are shown in Fig. 13. It is the combination of morphology evolution and fatigue parameter. On the one hand, the ALT is performed multiple times to get the complete morphology fatigue evolution of solder layers. Before and after the ALT of every constant cycle numbers, which is to keep N_f of the failure area the same, the morphology of solder layers will be detected by SAM technology. Meanwhile, morphology evolution and fatigue area can be obtained by DIP. On the other hand, the fatigue parameter is calculated by FEA. The geometry model before sampling is built, and then, the same boundary conditions, including power loss and N_f consistent with ALT measured by online monitoring, are set. Through the operation of multiphysics simulation, the fatigue parameter strain distribution, which is needed for the lifetime model in this article, can be known. According to the FEA results as shown in Fig. 12, the function between the failure area and the strain is also monotonous, which has a monotone relationship with N_f. Therefore, the failure area can be used as an intermediate variable to determine the quantitative relationship between N_f and $\varepsilon_{\mathrm{th}}$. Basically, a failure area can be obtained by a fixed number of PC test cycles in every sampling, and this failure area can also be obtained by a strain value in FEA. The same failure area calculated by the PC test and FEA can determine the relationship of cycle numbers corresponding to N_f and strain corresponding to $\varepsilon_{\mathrm{th}}$.

Considering the different size of each solder layer and the uncertainty of fatigue failure morphology, the failure area fraction (F_{s}) is chosen as the intermediate quantity. It is calculated by dividing the fatigue area of each sample by the original area of the solder layer. By calculation, keeping the fraction obtained from each sampling consistent with the one determined by the FEA, when the $\varepsilon_{\mathrm{th}}$ of solder layers reaches 0.0085, the solder fatigue failure occurs. In this way, the F_{s} results obtained by PC tests and lifetime model are shown in Fig. 14, where blue, black, and red curves represent the solder layers on the left, mid, and right sides of the power device, respectively. There are nine sets of data here consisting of three samples and three solder layers. It can be seen that F_{s} of the mid solder layers is bigger than the other two. It is because of the thermal coupling. It can also be seen in Fig. 12 that the strain caused by thermal stress in the mid is bigger than others.

When the lifetime model is finished, the process and characteristic parameters during the solder fatigue failure can be predicted as shown in Fig. 13.

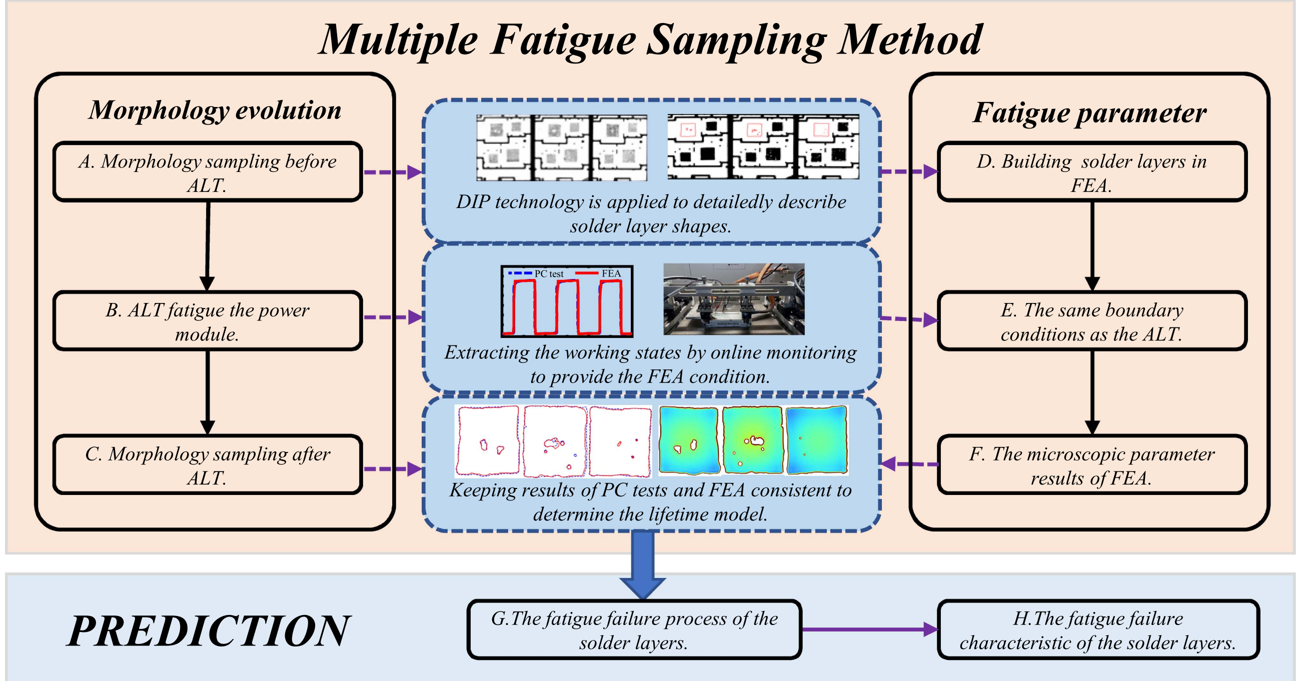


Fig. 13. Multiple fatigue sampling method of determining the lifetime model and prediction of the solder layer fatigue process.

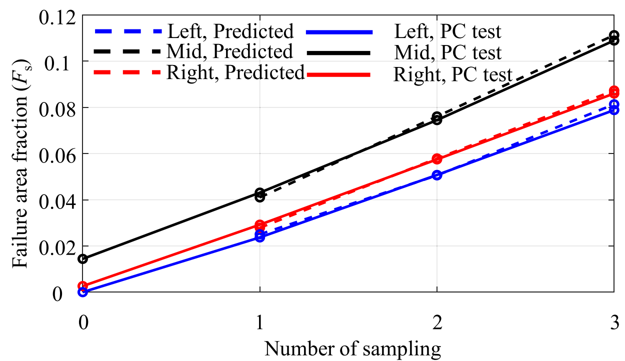


Fig. 14. Failure area fraction curves calculated by the PC test and the lifetime model.

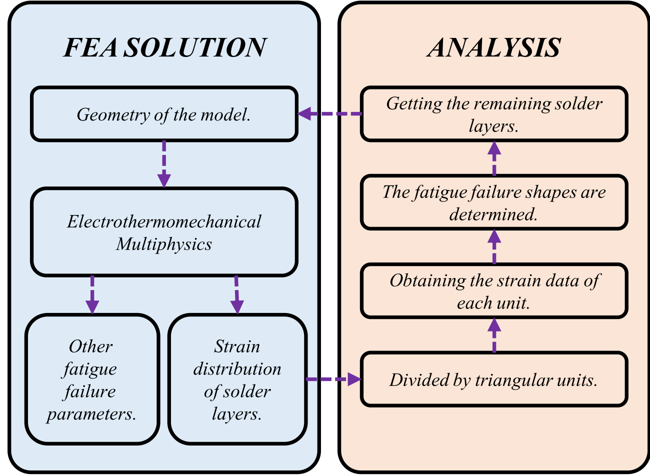


Fig. 15. Process of predicting the fatigue properties using the MCUM.

IV. Prediction of Process and Characteristic Parameters During the Solder Fatigue Failure

To intelligently predict the fatigue properties, the new dividing method named MCUM based on FEA and lifetime model is proposed in this part. It is all completed automatically by MATLAB and COMSOL cosimulation. There are two compositions, including the calculation of FEA and the numerical analysis of the solution, as shown in Fig. 15. This technique can not only effectively predict the fatigue failure process by determining the solder failure shapes but also predict the characteristic parameters of the device by FEA.

A. Introduction of the Evaluation Technique

The evaluation technique is done iteratively to reflect the real fatigue process. And every iteration consists of five steps as shown in Fig. 15. In the first step, the geometry including the void of the device is established. In the second step, the fatigue failure parameters including the strain distribution in solder layers are obtained by calculating FEA. In the third step, the solder layers are divided into minimal triangular units by the MCUM, where the fatigue strain data, which the lifetime model requires, can be read. In the fourth step, according to aforementioned lifetime model and fatigue strain data, the shapes of failure solder are determined. Finally, the remaining solder layers without failure can be known. They are then built in the FEA model again and the next iteration will begin. The part of FEA solution has been introduced before, and the analysis part and MCUM will be introduced.

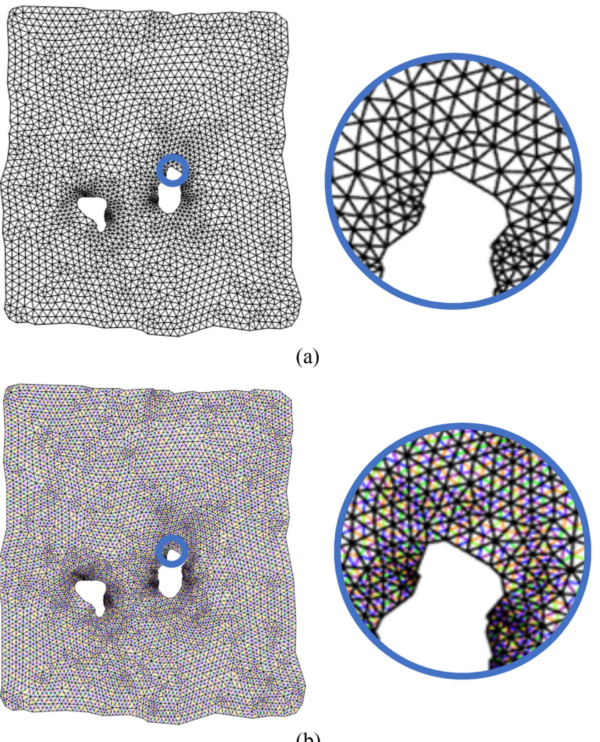


Fig. 16. (a) Mesh of the solder layer during FEA and (b) result divided with minimal units when reading strain distribution.

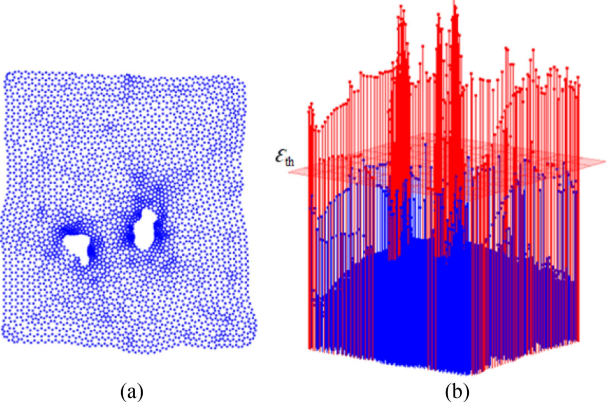


Fig. 17. Obtaining the failure zone of the solder layer. (a) Point distribution map. (b) Lifetime model judgment.

The idea of dividing the solder layers into minimal units is in accordance with the principle of the solder fatigue failure and FEA. In the process of solder layers fatigue failure, it changes gradually. Even in the same solder layer, the fatigue degree is different. When the fatigue reaches the failure limit, the solder disappears. Therefore, it is necessary to take into account the fatigue situation of each location to predict the solder layer evolution. And the MCUM is proposed to solve the need by dividing the solder layer into minimal units and judging the failure degree of these minimal units to determine the failure of the solder layer. It is like a picture is made up of a lot of pixels, a solder layer is made up of a lot of minimal units. As long as this minimal unit is small enough, it can meet the needs of the failure process. Of course, the position of the minimal unit cannot be random, as it must satisfy the principle of FEA mesh to ensure the accuracy. According to the FEA modeling process, mesh division is needed first to construct the overall matrix before calculation. The quality of the mesh is directly related to the accuracy of the solution. In Fig. 16(a), the mesh of the solder layer in FEA is shown. For FEA solution, it is accurate enough, but it is not enough to study the solder fatigue evolution. As the calculated results on the mesh nodes are the most accurate, the method of continuing the division of the original mesh as the minimal unit was adopted. In Fig. 16(b), triangles of the quarter mesh size are used to divide the solder layer. Since the division still follows the laws of FEA meshes, the fatigue data of minimal component can also be read in MATLAB. Of course, the smaller the minimal unit, the more accurate the strain data obtained from the FEA solution, but it will bring more computation. In order to meet the high precision, the one ninth of a mesh size triangular unit is selected in this article.

The strain data of each minimal unit are obtained with the help of the intelligent algorithm. The strain extraction distribution of one solder layer after 25 000 cycles is shown in Fig. 17. It is made up of about 42 thousand minimal units in actual operation, and just one in nine is shown in Fig. 17(a). In this figure, enough points are taken from the places of concern. In Fig. 17(b), the magnitude of strain is more intuitively represented by the use of height, which is drawn using the point distribution in Fig. 17(a). According to the ε_{th} provided by the lifetime model, the part above the strain threshold drawn in red is deemed to be a failure and the area below is a healthy area, which will still exist in the next iteration. When these are determined, what next to do is how to build the new solder layer geometry model in order to start the next iteration.

The way of building a new geometry model is by removing the failed solder from the original. It is practically finished in COMSOL by setting up the minimal units of the failure area, and the difference from the original shape is predicted. In Fig. 18, three fatigue failure conditions, including void boundary, solder layer boundary, and solder layer center, which will occur during the fatigue process, are shown, where the red areas are the failure minimal unites and the predicted shapes are the new geometry model of the next iteration. While the geometry model is completed, the next iteration will begin until the power device fails completely.

As far, a complete iteration is finished as shown in Fig. 15. By this technique, the whole process of the solder layer fatigue failure process can be simulated by COMSOL and MATLAB. Meanwhile, as calculation processes are done by FEA, the characteristic quantity of interest, such as T_j as long as can be obtained in FEA, will be predicted.

B. Prediction of the Fatigue Process and Characteristic Parameter

Following the MCUM, the predicted fatigue failure processes of solder layers are introduced. As mentioned before, the position is random when the voids first appear in the solder layer.

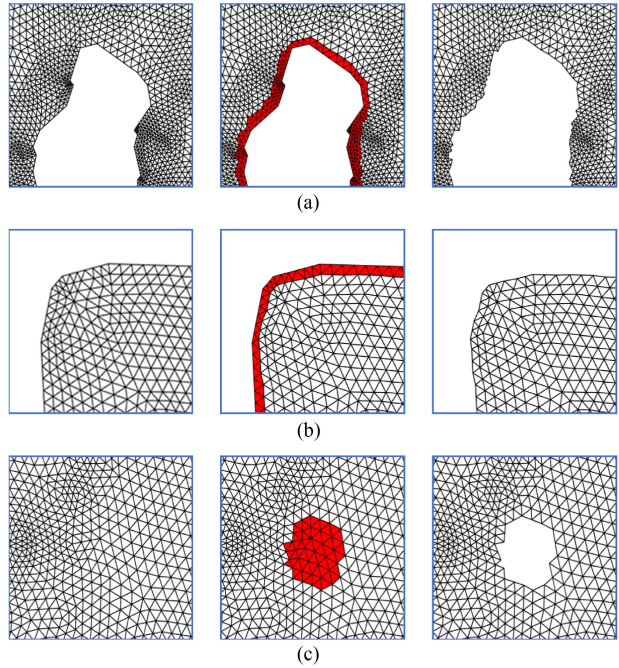


Fig. 18. Original, determination of the failure area, and predicted process of three possible conditions. (a) Void boundary. (b) Solder layer boundary. (c) Solder layer center.

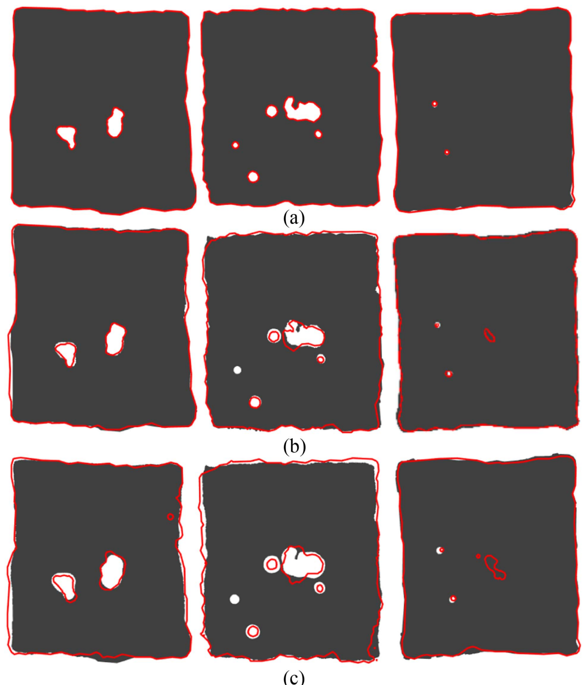


Fig. 19. Solder layer shapes of the predicted fatigue process are shown in gray and sampling shapes including (a) first sampling, (b) second sampling, and (c) third sampling are shown in red curves.

Therefore, the first sampling solder layer shapes are used as the initial geometry of the predicted in order to be compared with sampling shapes as shown in Fig. 19. In this figure, the predicted solder layer shapes are shown in gray and sampling shapes of the PC test are shown in red curves. It can be seen

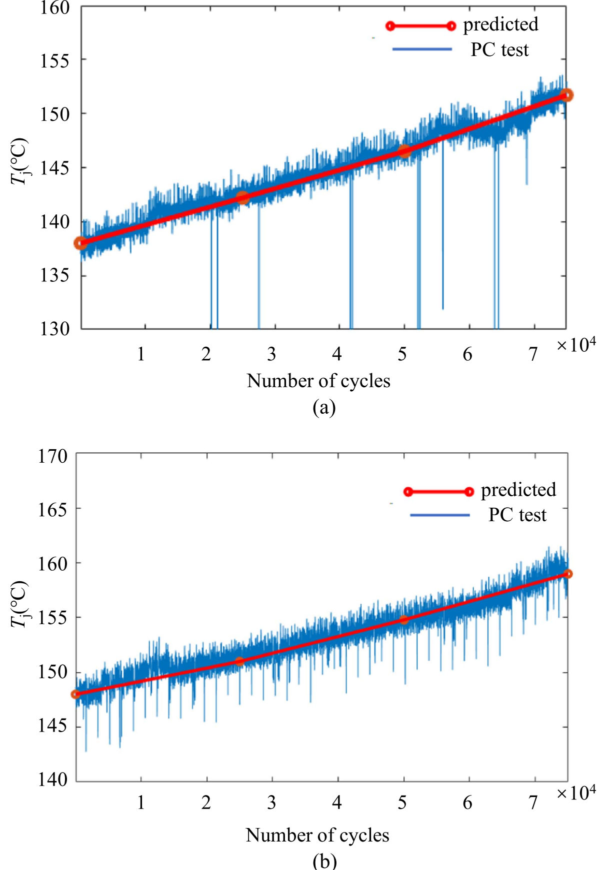


Fig. 20. T_j results of the PC test. (a) 180 A,1 min. (b) 200 A, 2 min and predicted.

that the predicated solder layer shapes are almost identical to the sample ones, and as F_s is concerned, they are almost the same. In Fig. 19(b) and (c), it can be clearly seen that the failure speed of the solder layers is accelerating, and the growth rate of the void area is also getting faster and faster. This is consistent with the previous research that the failure rate of power devices becomes faster and faster at the late stage of fatigue failure.

T_j is predicted on the basis of the predicted fatigue process. In order to be persuasive, two different working conditions, the current and the period, 180 A, 1 min and 200 A, 2 mins of the PC test are carried out. As shown in Fig. 20, the results of the PC test shown in blue and the predicted shown in red are basically a match. Considering that the first time the position of voids first appearing in the solder layer center is random, the failure ratio of the solder layer boundaries and center is set to be the same as the previous PC test and the location of the central void is set as the geometric center in the process of making this prediction.

V. Conclusion

This article proposes an accurate and intelligent approach to predicting an IGBT fatigue failure process and characteristic parameters. Intelligent algorithm DIP is applied to obtain the precise morphology shapes of the solder layers during the PC test, which are used to build a real FEA geometry model and

describe the F_s. The lifetime model is determined by the morphology evolution of the PC test and the fatigue parameter of the MFSM. The F_s of each solder layer is used as the inspection standard, and the data obtained by PC test and FEA verify the correctness of the model. Finally, the fatigue failure process of solder layers and characteristic parameters are predicted using the MCUM. PC tests under different working conditions are carried out in order to verify the correctness of the proposed method. Through the research in this article, the fatigue failure of the device is expressed more intuitively. The fatigue state of the solder layer can be predicted based on the working conditions of the device, thereby controlling and optimizing the long-term service performance of the power device. Also, the method in this article can consider the impact of voids on the thermal path of the device during electrothermal coupling analysis.

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