A Simplified Implementation With Improved Dynamic Performance of PWM Plus Phase-Shift Control for Four-Switch Buck–Boost Converter

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***Abstract*—The four-switch buck–boost converter possesses features that enable both voltage step-up and step-down, and positive output voltage. This converter has gained widespread popularity in applications that require a wide input voltage range. By utilizing pulsewidth modulation (PWM) plus phase-shift control, all power switches can achieve zero-voltage-switching across the entire input voltage and load range. Additionally, this control scheme minimizes ripple and rms value of the inductor current, thereby achieving high efficiency. This article aims to simplify the implementation of PWM plus phase-shift control and enhance the dynamic performance by approximating the phase-shift duty cycle. A 420-W prototype is fabricated and tested in the laboratory for verification.**

***Index Terms*—Four-switch buck–boost (FSBB) converter, pulsewidth modulation (PWM) plus phase-shift control, zero-voltage-switching (ZVS).**

I. Introduction

NONISOLATED dc–dc converters with voltage step-up and step-down capability are usually adopted in the applications where the output voltage is within the input voltage range. Basic converters with such capability include the buck–boost, Cuk, Zeta, and SEPIC converters. The buck–boost and Cuk converters output a negative voltage, which is not suitable for applications where a positive voltage is required. The Zeta and SEPIC converters output a positive voltage, however, they require more passive components. Furthermore, the power devices in all the aforementioned converters sustain a high voltage, which is the sum of the input voltage and output voltage. Comparatively, the two-switch buck–boost converter provides positive output voltage, low voltage stress, and fewer passive components, and has been widely used in distributed power supplies [1], [2], [3], electric vehicles [4], [5], and photovoltaic power supplies [6], [7]. To improve the efficiency, the two diodes can be replaced by two MOSFETS, and thus, a four-switch buck–boost (FSBB) converter is obtained, as shown in Fig. 1, where Q_1–Q_4 are the power switches, D_1–D_4 and C_1–C_4 are the antiparallel diodes and the output capacitors of Q_1–Q_4, respectively, L_c is the inductor, C_f is the output filter capacitor, and R_{Ld} is the load resistance.

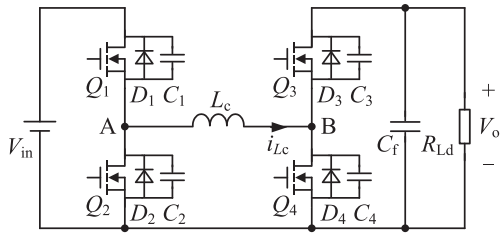

Fig. 1. Topology of the four-switch buck–boost converter.

Various control schemes have been proposed for the FSBB converter, which can be divided into three types: 1) single-mode control [8], 2) two-mode control [9], [10], [11], [12], [13], [14], and 3) quadrilateral current control [15], [16], [17], [18], [19], [20].

For the single-mode control, Q_1 and Q_4 are switched at the same time, however, the inductor current ripple is quite large. For the two-mode control, when the input voltage is higher than the output voltage, the FSBB converter operates in buck mode with Q_3 turned ON and Q_4 turned OFF; and when the input voltage is lower than the output voltage, the FSBB converter operates in boost mode with Q_1 turned ON and Q_2 turned OFF. As a result, the inductor current ripple is minimized, leading to reduced switching and conduction losses. However, Q_1 and Q_4 are hard-switched, limiting the switching frequency to the low range.

In recent years, the wide bandgap (WBG) power devices such as GaN and SiC have developed rapidly, which could be operated at a relatively high switching frequency. Although the turn-OFF loss of the WBG power devices is quite small, the turn-ON loss is still large [21]. So, it is necessary to realize zero-voltage-switching (ZVS) for the WBG power switches.

For the two-mode control, by intentionally reducing the inductor to allow a negative inductor current flow, ZVS can be achieved for all the switches [14]. However, the inductor current ripple remains unchanged over the full load range, and the light-load efficiency is low. Besides, when the input voltage is near the output voltage, the inductor current ripple becomes very small and the inductor current cannot reverse, thus causing ZVS

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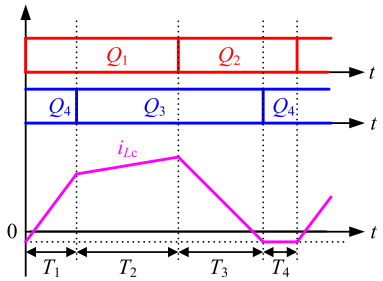

Fig. 2. Quadrilateral current control scheme.

to fail. The quadrilateral current control [15] achieves ZVS for all the power switches, and keeps the negative inductor current at a fixed value, as shown in Fig. 2. In [16], Q_2 and Q_3 are turned OFF simultaneously for avoiding circulating current due to the conduction of Q_2 and Q_4. However, the switching frequency increases as the load decreases, leading to a large loss at light load. A pulsewidth modulation (PWM) plus phase-shift control has been proposed previously [17], which regulates the duty cycles of Q_1 and Q_4, denoted by D_{y1} and D_{y2}, respectively, and the phase-shift duty cycle corresponding to phase-shift between the turn-ON instants of Q_1 and Q_3, denoted by D_θ. With this control scheme, the switching frequency is constant, and the inductor current ripple and rms value are minimized. Since there are three control variables (D_{y1}, D_{y2}, and D_θ), the implementation of the control circuit is relatively complex. By minimizing the rms value of the inductor current, which is derived in [18], a control scheme involving the three control variables can be derived. Similarly, a control scheme can be derived, on the basis of minimizing the loss [19]. Also, the effect of the switching sequence on the rms value of the inductor current and ZVS has been revealed from the physical viewpoint, and the optimal operating modes as well as the corresponding control method are given [20]. Essentially, the optimal operating modes obtained in [20] are the same as those in [17], [18], and [19].

In [17], [18], and [19], the PWM plus phase-shift control scheme is implemented with a lookup table, requiring significant storage resource for achieving adequate control accuracy. In [20], the implementation of the control scheme does not require a lookup table and storage resource. However, a phase-shift duty cycle closed-loop of low corner frequency is used, resulting in a slow response when the load or the input voltage changes, which has been analyzed in [22], and it is not acceptable in certain situations, such as pulsed power supplies [23] and voltage regulator modules [24]. Besides, in [20], failure to achieve ZVS of the power switches during transient seriously affects the performance and reliability of the WBG power devices [25].

In this article, the implementation of the PWM plus phase-shift control proposed in [20] is simplified, eliminating the phase-shift duty cycle closed-loop. As a result, the dynamic performance is greatly improved, and all the power switches can realize ZVS during the transients.

The rest of this article is organized as follows. The operating principle of the FSBB converter with PWM plus phase-shift control is briefly introduced in Section II. In Section III, the expression of the phase-shift duty cycle is derived and approximated. In Section IV, the implementation of the control scheme with the approximate phase-shift duty cycle is given. In Section V, a 420-W prototype of the FSBB converter is fabricated and tested to verify the proposed control scheme. Finally, Section VI concludes this article.

II. Operating Principle of the FSBB Converter With PWM Plus Phase-Shift Control

The operating principle of the FSBB converter with the PWM plus phase-shift control has been presented in detail in [20], and it is briefly introduced in this section.

A. Relationship of the Input and Output Voltages

At steady state, the relationship between the input and output voltages of the FSBB converter is [20]

$$\frac{V_o}{V_{in}} = \frac{D_{y1}}{1 - D_{y2}}. \tag{1}$$

B. ZVS Conditions

Assuming that the four power switches are identical and their output capacitance is C_{oss}, the minimum current for realizing ZVS for all the power switches during the dead time t_{dead} is

$$I_{ZVS} = 2C_{oss}V_{in\_max}/t_{dead}. \tag{2}$$

To achieve ZVS for all the power switches, the inductor current i_{Lc} should be lower than $-I_{ZVS}$ before Q_2 and Q_3 are turned OFF and be larger than I_{ZVS} before Q_1 and Q_4 are turned OFF.

C. Optimal Operating Modes

Fig. 3 shows the key waveforms of the optimal operating modes of the FSBB converter to ensure the minimum ripple and rms value of inductor current [20].

At heavy load, the FSBB converter works in pseudocritical continuous current mode (PCRM), as shown in Fig. 3(a), where, Q_2 and Q_3 are turned off concurrently when i_{Lc} decays to $-I_{ZVS}$. The values of i_{Lc} at points P and Q, denoted by I_P and I_Q, respectively, are larger than I_{ZVS}.

As the load decreases, the segment PQ is translated downward. When I_P ($V_{in} > V_o$) or I_Q ($V_{in} < V_o$) decays to I_{ZVS}, Q_4 or Q_1 is turned OFF immediately, and the critical load current is defined as I_G. When the load further decreases, the FSBB converter works in pseudodiscontinuous current mode (PDCM), as shown in Fig. 3(b) and (c), where Q_3 will be turned OFF before the end of the switching period, and Q_2 and Q_4 will conduct and i_{Lc} is kept at $-I_{ZVS}$.

III. Approximation of the Phase-Shift Duty Cycle

A. Theoretical Expression of Phase-Shift Duty Cycle

To guarantee the optimal operation of the FSBB converter, D_{y1}, D_{y2}, and D_θ should be properly regulated.

As shown in Fig. 3, CLK1 and CLK2 are the clock signals corresponding to the turn-ON instants of Q_1 and Q_3, respectively.

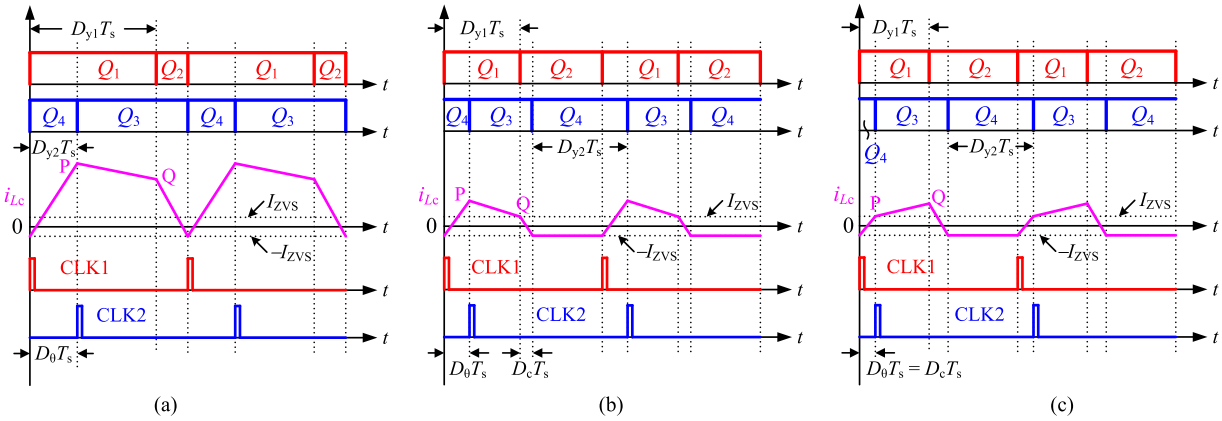

Fig. 3. Key waveforms of the optimal operating modes of the FSBB converter. (a) PCRM. (b) PDCM when $V_{\rm in} < V_{\rm o}$. (c) PDCM when $V_{\rm in} > V_{\rm o}$.

CLK1 is defined as the start of each switching period. The ratio of the phase-shift of the two clock signals to the switching period $T_{\rm s}$ represents the phase-shift duty cycle D_θ, whose expression under different operating modes is derived below.

According to Fig. 3, $I_{\rm P}$ and $I_{\rm Q}$ can be expressed as

$$I_{\rm P} = -I_{\rm ZVS} + \frac{V_{\rm in}}{L_{\rm c}} D_\theta T_{\rm s} \tag{3}$$

$$I_{\rm Q} = \begin{cases} -I_{\rm ZVS} + \frac{V_{\rm o}}{L_{\rm c}}(1 - D_{\rm y1})T_{\rm s} & \text{(PCRM)} \\ -I_{\rm ZVS} + \frac{V_{\rm o}}{L_{\rm c}}(D_\theta + 1 - D_{\rm y1} - D_{\rm y2})T_{\rm s} & \text{(PDCM).} \end{cases} \tag{4}$$

As seen from Fig. 3(b) and (c), under PDCM, $I_{\rm Q} = I_{\rm ZVS}$ when $V_{\rm in} < V_{\rm o}$, and $I_{\rm P} = I_{\rm ZVS}$ when $V_{\rm in} > V_{\rm o}$. According to (3) and (4), the expression of D_θ under PDCM can be obtained as

$$D_{\theta\_\rm PDCM} = \begin{cases} \frac{2L_{\rm c}I_{\rm ZVS}}{V_{\rm o}T_{\rm s}} + D_{\rm y1} + D_{\rm y2} - 1 & V_{\rm in} < V_{\rm o} \\ \frac{2L_{\rm c}I_{\rm ZVS}}{V_{\rm in}T_{\rm s}} & V_{\rm in} \geq V_{\rm o}. \end{cases} \tag{5}$$

According to (1), (5) can be rewritten as

$$D_{\theta\_\rm PDCM} = \begin{cases} \frac{2L_{\rm c}I_{\rm ZVS}}{V_{\rm o}T_{\rm s}} + \frac{V_{\rm o}-V_{\rm in}}{V_{\rm o}} D_{\rm y1} & V_{\rm in} < V_{\rm o} \\ \frac{2L_{\rm c}I_{\rm ZVS}}{V_{\rm in}T_{\rm s}} & V_{\rm in} \geq V_{\rm o}. \end{cases} \tag{6}$$

As shown in Fig 3(a), under PCRM, Q_2 and Q_3 are turned OFF at the same time, giving

$$D_{\theta\_\rm PCRM} = D_{\rm y2}. \tag{7}$$

As seen from Fig. 1, i_{Lc} flows into the load when Q_3 conducts, and the output current $I_{\rm o}$ under PCRM can be obtained as

$$I_{\rm o} = \frac{I_{\rm P} + I_{\rm Q}}{2}(D_{\rm y1} - D_{\theta\_\rm PCRM}) + \frac{I_{\rm Q} - I_{\rm ZVS}}{2}(1 - D_{\rm y1}). \tag{8}$$

Putting (3) and the first expression in (4) into (8), and combining with (1) and (7), the expression of $D_{\theta\_\rm PCRM}$ can be derived, as given in (9) shown at the bottom of the next page. As seen, there are two solutions for $D_{\theta\_\rm PCRM}$. According to (3), the larger D_θ is, the larger $I_{\rm P}$ is. In order to reduce the inductor current ripple, a smaller $D_{\theta\_\rm PCRM}$ is preferred. So, the sign "$\pm$" before the root is chosen as "$-$".

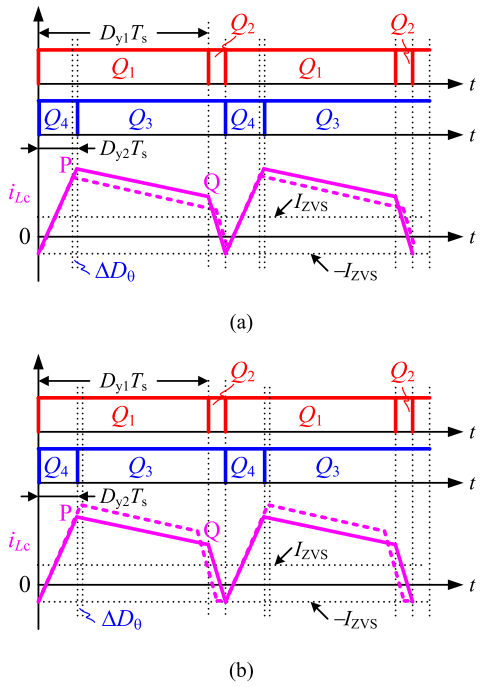

Fig. 4. Waveforms of i_{Lc} when the approximate $D_{\theta\_\rm PCRM}$ is (a) smaller; (b) larger.

Letting the smaller solution of (9) be equal to (6), and combining with (1), the critical load current $I_{\rm G}$ is obtained as (10), which is shown at the bottom of the next page.

B. Approximation of Phase-Shift Duty Cycle

The expression of $D_{\theta\_\rm PCRM}$ given in (9) will be approximated for ease of application. Moreover, its effect on the inductor current waveform is analyzed.

If the approximate $D_{\theta\_\rm PCRM}$ is smaller than the theoretical one, as shown in Fig. 4(a), $D_{\rm y2}$ also reduces since it equals to $D_{\theta\_\rm PCRM}$. According to (1), $D_{\rm y1}$ will increase accordingly to keep the output voltage unchanged. Thus, i_{Lc} cannot decay to $-I_{\rm ZVS}$ at the end of the switch period. As a result, Q_1 and Q_4 will lose ZVS.

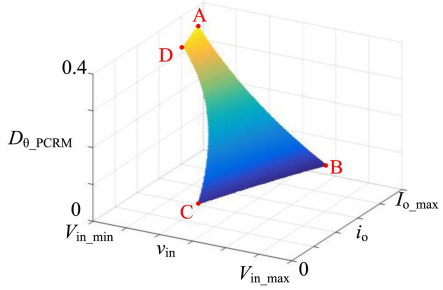

Fig. 5. Surface of D_{θ_PCRM} as the functions of the input voltage and output current.

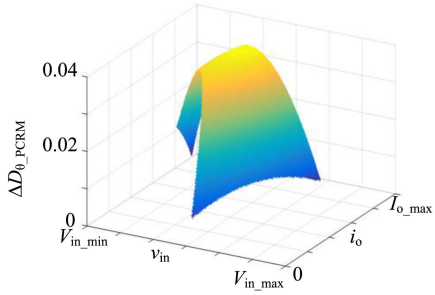

Fig. 6. Surface of ΔD_{θ_PCRM} as the functions of the input voltage and output current.

If the approximate D_{θ_PCRM} is larger than the theoretical one, as shown in Fig. 4(b), D_{y2} also increases. According to (1), D_{y1} will reduce. This will make i_{Lc} decay to $-I_{ZVS}$ before the end of the switching cycle, and Q_1 and Q_4 can realize ZVS.

Therefore, to achieve ZVS for all the power switches, the approximate D_{θ_PCRM} needs to be larger than the theoretical one.

When the output voltage V_o, inductor L_c, switching period T_s and I_{ZVS} required for ZVS are determined, D_{θ_PCRM} is a function of input voltage v_{in} and output current i_o. Using Taylor's series expansion, and reserving only the first derivative item, (9) can be approximated as

$$\begin{aligned} & D_{\theta\_PCRM\_appr}(v_{in}, i_o) \\ = \; & D_{\theta\_PCRM}(V_{in\_0}, I_{o\_0}) + \left.\frac{\partial D_{\theta\_PCRM}}{\partial v_{in}}\right|_{(V_{in\_0}, I_{o\_0})} (v_{in} - V_{in\_0}) \\ & + \left.\frac{\partial D_{\theta\_PCRM}}{\partial i_o}\right|_{(V_{in\_0}, I_{o\_0})} (i_o - I_{o\_0}) \\ = \; & \left.\frac{\partial D_{\theta\_PCRM}}{\partial v_{in}}\right|_{(V_{in\_0}, I_{o\_0})} v_{in} + \left.\frac{\partial D_{\theta\_PCRM}}{\partial i_o}\right|_{(V_{in\_0}, I_{o\_0})} i_o \\ & + D_{\theta\_PCRM}(V_{in\_0}, I_{o\_0}) \\ & - \left.\frac{\partial D_{\theta\_PCRM}}{\partial v_{in}}\right|_{(V_{in\_0}, I_{o\_0})} V_{in\_0} - \left.\frac{\partial D_{\theta\_PCRM}}{\partial i_o}\right|_{(V_{in\_0}, I_{o\_0})} I_{o\_0}. \end{aligned} \tag{11}$$

The accuracy of (11) to fit (9) strongly depends on the Taylor expansion point (V_{in_0}, I_{o_0}). For the sake of simplicity, (11) can be rewritten as

$$D_{\theta\_PCRM\_appr}(v_{in}, i_o) = a v_{in} + b i_o + c. \tag{12}$$

By substituting the parameters given in Table II in Section V into (9), the surface of theoretical D_{θ_PCRM} can be drawn, as shown in Fig. 5. The surface boundary points are A(V_{in_min}, I_{o_max}), B(V_{bond}, I_{o_max}), C(V_o, $I_G(V_o)$), and D(V_{in_min}, $I_G(V_{in\_min})$), where V_{bond} corresponds to $I_G = I_{o\_max}$. As seen from Fig. 5, the surface is concave. So, to ensure $D_{\theta\_PCRM\_appr}$ is always greater than or equal to the theoretical D_{θ_PCRM}, it is only required to make $D_{\theta\_PCRM\_appr}$ equal to the theoretical D_{θ_PCRM} at points A, B, and C, i.e.,

$$\begin{aligned} & D_{\theta\_PCRM\_appr}(\mathrm{J}) \\ & = D_{\theta\_PCRM}(\mathrm{J}) \ (\mathrm{J} = \mathrm{A}, \mathrm{B}, \mathrm{C}). \end{aligned} \tag{13}$$

Substitution of the parameters given in Table II into (13), yields

$$60a + 5b + c = 0.39 \tag{14}$$

$$84a + 1.34b + c = 0.074 \tag{15}$$

$$100a + 5b + c = 0.07. \tag{16}$$

By solving (14)–(16), we have $a = -0.008$, $b = 0.034$, and $c = 0.7$. Thus, $D_{\theta\_PCRM\_appr}$ is expressed as

$$D_{\theta\_PCRM\_appr} = -0.008 v_{in} + 0.034 i_o + 0.7. \tag{17}$$

The fitting error of the phase-shift duty cycle under PCRM is

$$\begin{aligned} \Delta D_{\theta\_PCRM}(v_{in}, i_o) = & D_{\theta\_PCRM\_appr}(v_{in}, i_o) \\ & - D_{\theta\_PCRM}(v_{in}, i_o). \end{aligned} \tag{18}$$

Substituting (17) and (9) into (18), the surface of ΔD_{θ_PCRM} can be drawn, as shown in Fig. 6. As seen, the fitting error is small and greater than zero over the entire input voltage and load range, which means that $D_{\theta\_PCRM\_appr}$ is always larger than the theoretical D_{θ_PCRM}, guaranteeing ZVS for all the power switches.

Since $D_{\theta\_PCRM\_appr}$ is larger than the theoretical D_{θ_PCRM}, the inductor current ripple is increased, as shown in Fig. 4(b).

$$D_{\theta\_PCRM} = D_{y2\_PCRM} = \frac{\left(\frac{V_o}{V_{in}}\right)^2 + \frac{L_c I_{ZVS}}{V_{in} T_s} \pm \sqrt{\left(\frac{V_o + V_{in}}{V_{in}} - \frac{L_c I_{ZVS}}{V_{in} T_s}\right)^2 - \left[\left(\frac{V_o}{V_{in}}\right)^2 + \frac{V_o}{V_{in}} + 1\right]\left(\frac{2 L_c I_o}{V_{in} T_s} + 1\right)}}{\left(\frac{V_o}{V_{in}}\right)^2 + \frac{V_o}{V_{in}} + 1} \tag{9}$$

$$I_G = \begin{cases} \frac{V_{in}\left(2V_{in}^2 - V_o^2\right) I_{ZVS}}{V_o^3} - \frac{2V_{in}^2 (V_{in} + V_o) L_c I_{ZVS}^2}{V_o^4 T_s} + \frac{V_{in}^2 (V_o - V_{in}) T_s}{2 V_o^2 L_c} & V_{in} < V_o \\ \frac{(2V_o - V_{in}) I_{ZVS}}{V_{in}} - \frac{2(V_{in} + V_o) V_o L_c I_{ZVS}^2}{V_{in}^3 T_s} + \frac{V_o (V_{in} - V_o) T_s}{2 V_{in} L_c} & V_{in} \geq V_o \end{cases} \tag{10}$$

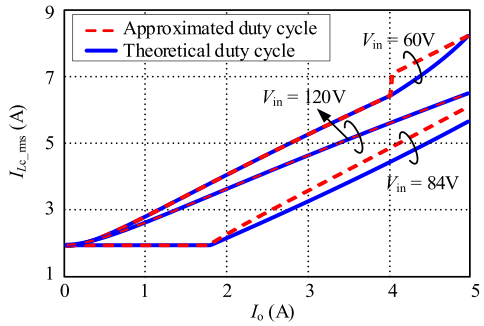

Fig. 7. Curves of the rms value of inductor current with the theoretical and approximated phase-shift duty cycles.

The rms value of inductor current I_{Lc_rms} is expressed as

$$I_{Lc\_rms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_{Lc}^2 dt}$$

$$= \frac{1}{\sqrt{3}}\sqrt{\begin{array}{l} D_\theta\left(I_{ZVS}^2 - I_P I_{ZVS} - I_P I_Q - I_Q I_{ZVS}\right) \\ +D_{y1}\left(I_P^2 + I_P I_Q + I_Q I_{ZVS} - I_{ZVS}^2\right) \\ -D_{y2}\left(I_Q^2 - I_Q I_{ZVS}\right) + I_{ZVS}^2 + I_Q^2 - I_Q I_{ZVS} \end{array}} \quad (19)$$

where I_P and I_Q are given in (3) and (4), respectively.

According to (19), the curves of I_{Lc_rms} with the theoretical and approximated D_{θ_PCRM} are depicted, as shown in Fig. 7. As seen, since only D_{θ_PCRM} is approximated, I_{Lc_rms} increases under PCRM, and it remains unchanged under PDCM. However, the increased I_{Lc_rms} is negligible due to the small fitting error.

Compared with the implementation of the PWM plus phase-shift control scheme given in [20], the approximate D_{θ_PCRM} changes with the load current and input voltage in real time, and the phase-shift duty cycle closed-loop and the filter with low cutoff frequency are no longer needed. Since D_{θ_PCRM} is equal to D_{y2}, which has a direct effect on the regulation of the output voltage according to (1), the real-time change of D_{θ_PCRM} will greatly improve the dynamic performance of the FSBB converter and maintain ZVS during the transient when the input voltage and output current are abruptly changed.

IV. Implementation of PWM Plus Phase-Shift Control With Approximate Phase-Shift Duty Cycle

With the approximate D_{θ_PCRM}, the implementation of the PWM plus phase-shift control is given in Fig. 8, which includes subcircuits A, B, and C.

A. Output Voltage Regulation Circuit

Subcircuit A is used to regulate the output voltage. The sensed output voltage v_{os} is compared with the voltage reference V_{o_ref}, and the error is sent to the output voltage regulator, which consists of amplifier EA1 and its periphery circuits. The output of the output voltage regulator v_{eaout} is compared with the saw-tooth carrier v_{saw} via comparator Comp1, whose output is sent to RS trigger 1 together with clock signal CLK1 to generate the drive signals of Q_1 and Q_2. Here, v_{saw} is synchronized with CLK1.

B. Valley Current Control Circuit

Subcircuit B is used to generate the drive signals of Q_3 and Q_4. The inductor current i_{Lc} is compared with $-I_{ZVS}$, and once i_{Lc} decays to $-I_{ZVS}$, comparator Comp2 outputs a high level, and then the OR gate outputs a high level, which resets the output Q of RS trigger 2 to turn OFF Q_3. Note that, CLK1 is intentionally included here to make Q_3 be turned OFF when Q_2 is turned OFF in the case i_{Lc} has not decayed to $-I_{ZVS}$ at the end of the switching period. The turn-ON instant of Q_3 (i.e., the turn-OFF instant of Q_4) is determined by CLK2, which is generated by the phase-shift generation circuit.

C. Phase-Shift Generation Circuit

Subcircuit C is the phase-shift generation circuit, which generates CLK2. The expressions of the phase-shift duty cycle under PCRM and PDCM have been obtained in Section III, and the specific implementation is given here.

As shown in Fig. 3(b) and (c), when the FSBB converter is operated under PDCM, the duty cycle corresponding to the interval when i_{Lc} changes between I_{ZVS} and $-I_{ZVS}$ is defined as D_c, which is expressed as

$$D_c = \begin{cases} \frac{2L_c I_{ZVS}}{V_o T_s} & V_{in} < V_o \\ \frac{2L_c I_{ZVS}}{V_{in} T_s} & V_{in} \geq V_o \end{cases}. \quad (20)$$

As seen from (20), when $V_{in} > V_o$, D_c is related to V_{in}, and it is smaller than D_c when $V_{in} < V_o$. To ensure i_{Lc} decays from I_{ZVS} to $-I_{ZVS}$ when $V_{in} < V_o$ or increases from $-I_{ZVS}$ to I_{ZVS} when $V_{in} > V_o$, D_c should satisfy

$$D_{c\_max} = \frac{2L_c I_{ZVS}}{V_o T_s}. \quad (21)$$

According to (6), (20), and (21), the modulation signal V_{θ_PDCM} for obtaining D_{θ_PDCM} can be expressed as

$$V_{\theta\_PDCM} = \begin{cases} D_{c\_max}V_M + \frac{V_o - V_{in}}{V_o} D_{y1} V_M & V_{in} < V_o \\ D_{c\_max}V_M & V_{in} > V_o \end{cases} \quad (22)$$

where V_M is the amplitude of v_{saw}.

As seen from subcircuit A in Fig. 8, v_{eaout} is equal to $D_{y1}V_M$. By substituting it into (22), we have

$$V_{\theta\_PDCM} = \begin{cases} D_{c\_max}V_M + \frac{V_o - V_{in}}{V_o} v_{eaout} & V_{in} < V_o \\ D_{c\_max}V_M & V_{in} > V_o. \end{cases} \quad (23)$$

In Fig. 8, V_{θ_PDCM} is implemented by a subtracter (consists of amplifier EA3 and its peripheral circuits), a multiplier, and adder1 (consists of amplifier EA4 and its peripheral circuits). The subtracter outputs $v_{os} - v_{ins}$, and the multiplier outputs $[(v_{os} - v_{ins})/v_{os}]\ v_{eaout}$, which is equal to $[(V_o - V_{in}) / V_o] \cdot v_{eaout}$ when the sampling gains of V_{in} and V_o are set same. Note that if $V_{in} > V_o$, the output of the subtracter is negative, and diode D_1 conducts to clamp the input y of the multiplier to zero. Thus, the multiplier outputs zero and the adder 1 outputs $D_{c\_max}V_M$.

When the FSBB converter operates under PCRM, as shown in Fig. 3(a), according to (17), the corresponding modulation

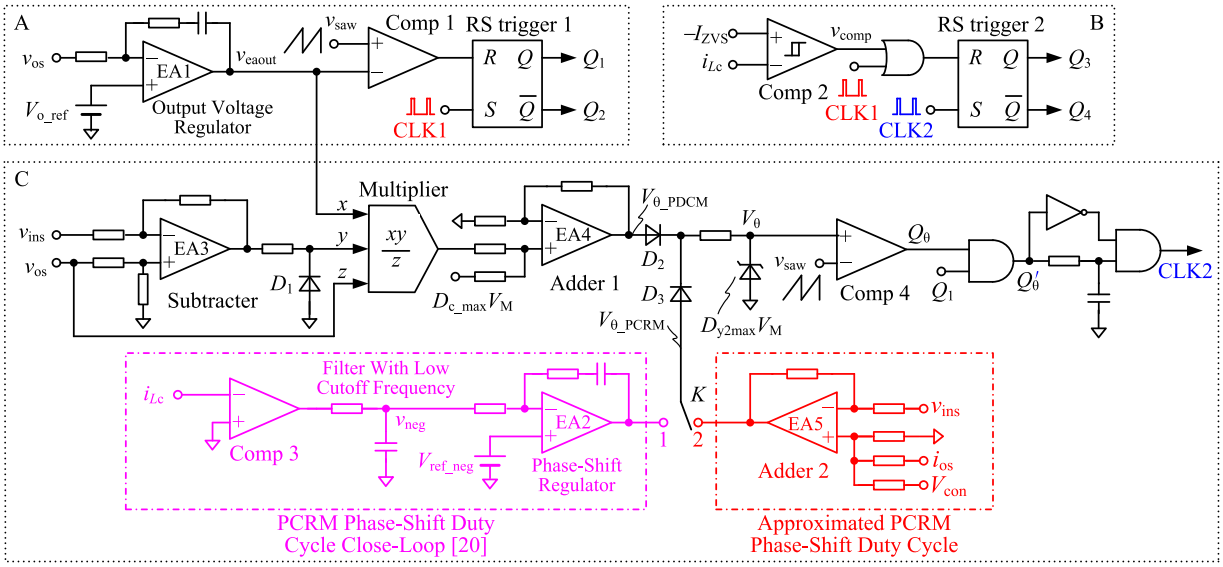

Fig. 8. Circuit implementation of the simplified PWM plus phase-shift control with approximated phase-shift duty cycle.

TABLE I
COMPARISON OF QUADRILATERAL CURRENT CONTROL METHODS

Paper	[16]	[17],[18],[19]	[20]	This paper
Switching Frequency	Variable	Constant	Constant	Constant
Lookup Table	No	Yes	No	No
Dynamic Response	Medium	Medium	Slow	Fast
ZVS During Transient	No	No	No	Yes

signal V_{θ_PCRM} can be expressed as

$$V_{\theta\_PCRM} = (-0.008v_{in}+0.034i_o+0.7)V_M. \quad (24)$$

V_{θ_PCRM} is implemented by adder2, which consists of amplifier EA5 and its peripheral circuits, as shown in subcircuit C within the right-side dash-dotted box. The sensed input voltage v_{ins}, the sensed output current i_{os} and the bias voltage $V_{con} = 0.7\ V_m$ are added with the coefficients according to (24) through amplifier EA5 to obtain V_{θ_PCRM}. For comparison, the PCRM phase-shift duty cycle closed-loop proposed in [20] is also given in subcircuit C within the left-side dash-dotted box. As seen, with the approximate D_{θ_PCRM}, the implementation is quite simple, and the closed-loop for D_{θ_PCRM} and the filter (consists of a *RC* filter with low cutoff frequency) can be removed. Furthermore, D_{θ_PCRM} is calculated in real time, which will lead to fast dynamic performance when the input voltage and output current are abruptly changed.

The larger one of V_{θ_PCRM} and V_{θ_PDCM} is sent to Comp4, and compared with v_{saw} to generate Q_θ. Then, Q_θ and Q_1 are sent to the AND gate for ensuring Q_4 to be turned OFF no later than Q_1, and the output of the AND gate is sent to the phase-shift clock generating circuit, which is composed of a NOT gate, an AND gate and a *RC* integral circuit. The phase-shift clock generation circuit is essentially a mono-clock generation circuit triggered by the falling edge of Q'_θ, in which the *RC* integral circuit is used to determine the pulse width of the generated clock signal CLK2. Note that, the rising edge of CLK2 correspond to the falling edge of Q'_θ.

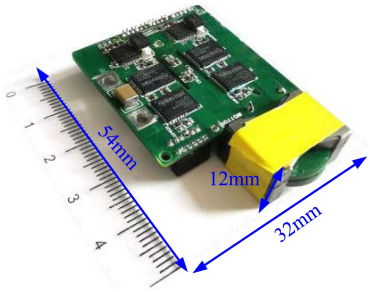

Fig. 9. Prototype of the FSBB converter.

TABLE II
KEY PARAMETERS OF THE PROTOTYPE

Parameter	Value	Parameter	Value
Switching Frequency f_s	500 kHz	Input Voltage V_{in}	60~120 V
Inductor L_c	3 μH	Output Voltage V_o	84 V
Output Capacitor C_f	100 μF	Output Current I_o	5 A

Note that subcircuits A and C can also be implemented with digital control for more flexibility, while subcircuit B cannot be realized by a pure digital controller due to the real-time comparison. Thus, the proposed method can be realized by the commercial analog-digital hybrid controller, such as UCD3138.

D. Comparison of Quadrilateral Current Control Methods

In order to show the advantages of the proposed control method, Table I provides the comparison of the state-of-the-art

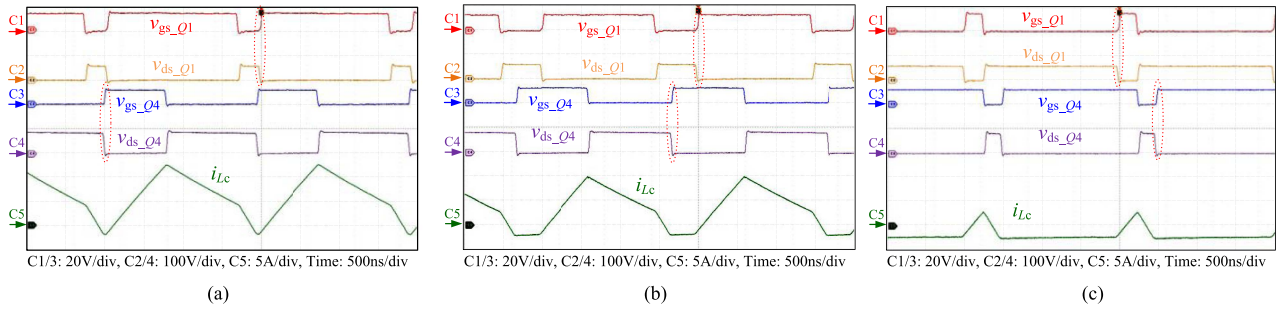

Fig. 10. Steady-state waveforms when $V_{\rm in} = 60$ V. (a) Full load. (b) Half load. (c) No load.

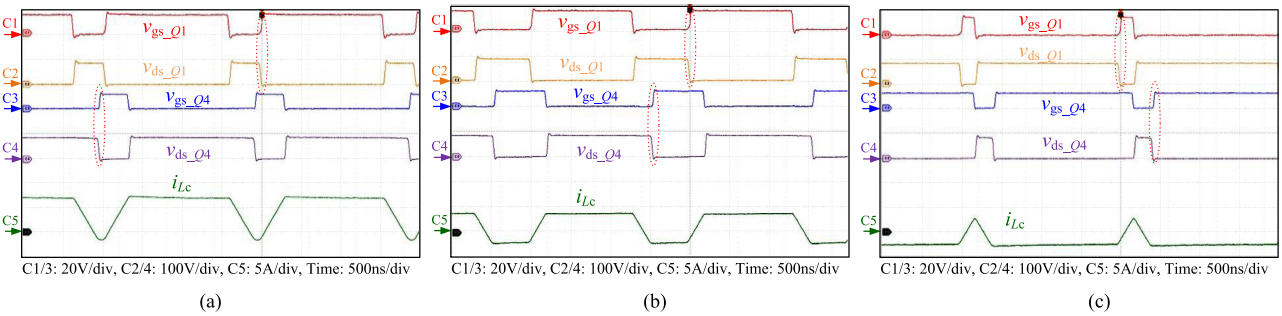

Fig. 11. Steady-state waveforms when $V_{\rm in} = 84$ V. (a) Full load. (b) Half load. (c) No load.

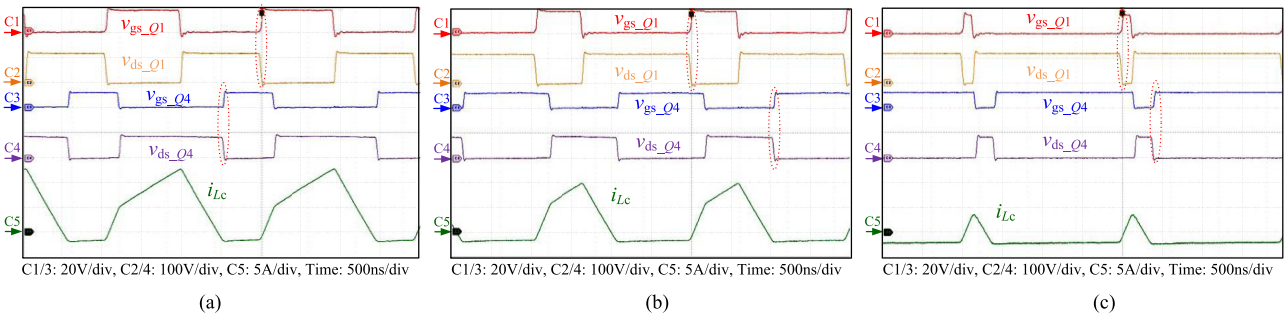

Fig. 12. Steady-state waveforms when $V_{\rm in} = 120$ V. (a) Full load. (b) Half load. (c) No load.

quadrilateral current control with the proposed one. As shown, the proposed control method has the following benefits.

1) The implementation is simplified because it does not require a lookup table or complex phase-shift duty cycle closed-loop.
2) The dynamic performance is greatly improved when the loads or the input voltage step changes, which is necessary in some situations such as the pulsed power supplies and voltage regulator modules.
3) The ZVS for all the power switches during transient is ensured, improving the reliability of the WBG power devices.

V. Experimental Verification

In order to verify the effectiveness of the simplified PWM plus phase-shift control, a 420-W prototype with 500-kHz switching frequency is fabricated in the lab, as shown in Fig. 9. The key parameters of the prototype are listed in Table II.

The Navitas GaN HEMTS (NV6128) are chosen as the power switches to achieve high efficiency. A PQ20.5 ferrite core and two PCB windings connected in series are used for the inductor to achieve high power density.

Figs. 10 to 12 show the steady-state experimental waveforms of the FSBB converter at different loads under $V_{\rm in} = 60$ V, 84 V, and 120 V, respectively, in which, $v_{\rm ds\_Q1}$ and $v_{\rm ds\_Q4}$ are the drain-source voltages of Q_1 and Q_4, respectively. As seen, $v_{\rm ds\_Q1}$ and $v_{\rm ds\_Q4}$ reduce to zero before Q_1 and Q_4 are turned ON, respectively. Thus, Q_1 and Q_4 realize ZVS. Likewise, Q_2 and Q_3 also realize ZVS.

Fig. 13(a) and (b) shows the dynamic experimental waveforms when the output current is stepped between 10% and 90% full-load under $V_{\rm in} = 84$ V using the original control method [20] and the simplified control method proposed in this article, respectively, in which, V_θ is the modulation signal for D_θ. As seen, with the approximate phase-shift duty cycle, the FSBB converter has a faster dynamic response with smaller overshoot

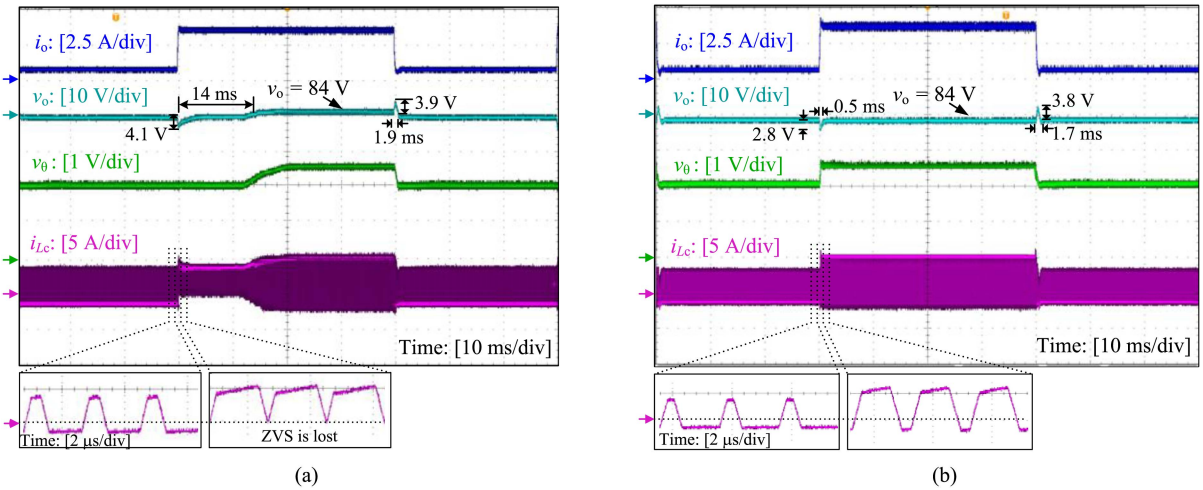

Fig. 13. Transient waveforms when the load is stepped between 10% and 90% full-load with $V_{\rm in}$ = 84 V using (a) original control method [20] and (b) proposed simplified control method.

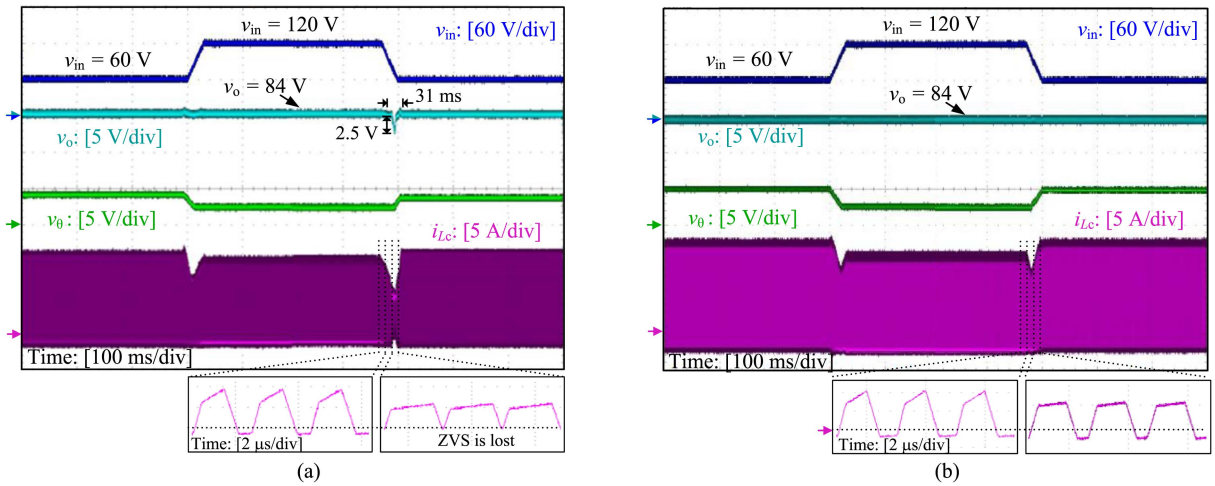

Fig. 14. Transient waveforms when the input voltage is stepped between 60 V and 120 V under full-load using (a) original control method [20] and (b) proposed simplified control method.

and undershoot of $v_{\rm o}$ and shorter recovery time. Besides, according to the analysis in Section III, when the load steps to 90% full-load, the FSBB converter works under PCRM. As shown in Fig. 13(a), with the original control method [20], V_θ cannot respond quickly with the load current due to the low corner frequency and the setting time of the low-pass filter in the closed-loop for $D_{\theta\_\rm PCRM}$. This causes the phase shift duty cycle to be smaller than the required theoretical value during the transient, and the inductor current cannot decay to $-I_{\rm ZVS}$ and ZVS is lost until the regulation of $D_{\theta\_\rm PCRM}$ is completed. When the load steps to 10% full-load, the FSBB converter works under PDCM, and V_θ decreases slowly but is larger than the required theoretical value. Thus, ZVS is maintained. As shown in Fig. 13(b), with the simplified control method, V_θ changes with the load current in real time, the phase shift duty cycle is always larger than the required theoretical value, and the inductor current can still decay to $-I_{\rm ZVS}$ during the transient, ensuring ZVS for all the power switches.

Fig. 14(a) and (b) shows the dynamic experimental waveforms when the input voltage $v_{\rm in}$ is stepped between 60 V and 120 V under full load with original control method [20] and the simplified control method proposed in this article, respectively. As seen, with the approximate phase-shift duty cycle, the FSBB converter also has a faster dynamic response with smaller overshoot and undershoot of $v_{\rm o}$ and shorter recovery time. Meanwhile, when $v_{\rm in}$ step to 60 V from 120 V, the FSBB converter switches to PCRM from PDCM. As shown in Fig. 14(a), with the original control method [20], ZVS is lost due to the slow response of $D_{\theta\_\rm PCRM}$. As shown in Fig. 14(b), with the proposed control method, V_θ changes with the input voltage in real time, and the inductor current still decay to $-I_{\rm ZVS}$, ensuring ZVS during the transient.

Fig. 15 shows the measured efficiencies of the FSBB converter under different load and input voltage with the original control method [20] and the simplified control method, respectively. As seen, at light load, the FSBB converter works in PDCM, so the

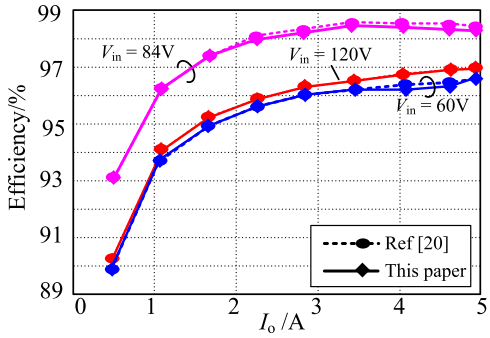

Fig. 15. Comparison of the measured efficiencies between the original control method [20] and the proposed simplified control method.

efficiency of the converter with the simplified control method is unchanged. With the load increasing, the converter operates under PCRM, then the efficiency slightly reduces for the little increased I_{Lc_rms}, and its maximum drop value is 0.1%, being negligible. Note that, the two efficiency curves at $V_{in} = 120$ V of both the control schemes proposed in [20] and this article coincide since the converter always works under PDCM, which corresponds to Fig. 7. The peak efficiency of the prototype is 98.5% when $V_{in} = 84$ V. Moreover, the full-load efficiency at different input voltages is higher than 96.7%.

VI. Conclusion

In this article, a simplified control method for PWM plus phase-shift is proposed for the four-switch buck–boost converter, where the phase-shift duty cycle under PCRM is approximated. Compared with the previous schemes, which require a lookup table or complex closed-loop control of the PCRM phase-shift duty cycle, the proposed control scheme simplifies the implementation. The dynamic performance is greatly improved at the expense of a slight degradation of efficiency, and at the same time zero-voltage-switching for all the power switches is maintained during the transient. A 420-W prototype is fabricated and tested in the lab, and the experimental results are provided to verify the effectiveness of the proposed simplified control method.

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