

A Novel Rectifier-Less Synchronous Electric Charge Extraction and Inversion Interface Circuit for PE Energy Harvesters

Zhidong Chen¹, Yinshui Xia¹, Ge Shi¹, Xiudeng Wang¹, Huakang Xia¹, and Yidie Ye¹, *Member, IEEE*

Abstract—A novel rectifier-less synchronous electric charge extraction and inversion (ReL-SECEI) interface circuit for Piezoelectric energy harvesters is proposed in this article. At the peak voltages of the Piezoelectric Transducer (PZT), a portion of electric charges is inverted on the clamped capacitance C_D , so that the PZT is automatically regulated at a higher output voltage state to improve extracted energy from the PZT. In addition, the self-powered implementation of the ReL-SECEI circuit is presented. It reduces the number of components by optimizing the positive and negative synchronous switches. The rectifier-less and simplified designs reduce the internal power loss and, hence, improve the energy harvesting efficiency. The ReL-SECEI circuit is verified by the experiment, the harvested power is load-dependent and the peak output power is obtained with the optimum load, which reaches 4.2 times that of the standard energy harvesting circuit.

Index Terms—Charge inversion, energy harvesting, piezoelectric (PE), piezoelectric transducer (PZT), rectifier less.

I. INTRODUCTION

IN GENERAL, batteries need to be implanted in the wireless sensor networks (WSN) nodes to provide a continuous and reliable electric energy supply, while regular battery replacement is inevitable. Since there are various forms of ambient energy, such as wind energy, vibration energy, thermal energy, and so

on [1], WSN nodes can be self-sufficient by integrating an energy harvester and converting the ambient energy into electrical energy [2], [3].

The energy harvester using Piezoelectric Transducers (PZTs) is one of the energy harvesting techniques and can convert Piezoelectric (PE) energy into electrical energy [4], [5], [6]. However, the PZT outputs the alternating current (ac) voltage while direct current (dc) power supply is required in the WSN nodes. Usually, the interface circuit is essential to achieve energy transfer from a PZT to the energy storage, and then a dc supply can be obtained to power these ubiquitous WSN nodes. The simplest one is called the standard energy harvesting (SEH) circuit, which is composed of a diode rectifier bridge and a filter capacitor. The SEH circuit has its limitations in terms of energy harvesting efficiency, rendering it suitable only for strongly-coupled PZT [7].

A variety of nonlinear interface circuits were proposed to achieve higher energy harvesting efficiency, such as parallel-synchronized switch harvesting on inductor (P-SSHI) [8] and series-synchronized switch harvesting on inductor (S-SSHI) [9]. The SSHI techniques employ the LC oscillation to reverse the PE voltage quickly at the peak voltage points during $1/2$ th of the LC oscillation period ($t_{SSHI} = 0.5T_{LC}$) and it has been demonstrated that the peak output power ratio between a high-quality SSHI and the ideal SEH can reach 8 times [10], [11], [12]. However, these SSHI designs are load-dependent and their ultimate performance is only achieved with the optimal load. Thus, the double SSH by Lallart et al. [13] and the enhanced SSH by Shen et al. [14] interface circuits were proposed to reduce the load dependency and a wider operating range is achieved with the extra regulation circuits. Chen et al. [15], Long et al. [16], and Xia et al. [17] adopted multi-input S-SSHI and P-SSHI circuits, respectively, to enhance harvested power. These multi-input interface circuits can harvest energy from multiple PZTs simultaneously; however, the load-dependent drawbacks still exist. SSH on capacitors (SSHC) is another technique that the OFF-chip inductor is replaced by the switched-capacitor and can be fully integrated [18], [19], [20].

To address the load-dependent drawback, the applications of the maximum power point tracking (MPPT) technique in SSHI were studied. Fang et al. [21] associated the S-SSHI circuit with a continuous MPPT technique named fractional normal-operation voltage. Precharged energy is essential to power the active

Manuscript received 22 August 2023; revised 1 November 2023; accepted 21 December 2023. Date of publication 25 December 2023; date of current version 26 January 2024. This work was supported in part by the National Natural Science Foundation of China under Grants 62131010, U22A2013, 61971389, 62271275, and 62334006, in part by the Natural Science Foundation of Zhejiang Province under Grants LZ20F010006, LY21F010006, and LR22F010001, in part by the Natural Science Foundation of Ningbo under Grants 2021J181 and 2023J122, and in part by the Scientific Research Fund of Zhejiang Provincial Education Department under Grant Y202250275. Recommended for publication by Associate Editor M. Vitelli. (*Corresponding author: Zhidong Chen.*)

Zhidong Chen is with the College of Information and Intelligence Engineering, Zhejiang Wanli University, Ningbo 315100, China, and also with the Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo 315211, China (e-mail: 1701082016@nbu.edu.cn).

Yinshui Xia, Xiudeng Wang, Huakang Xia, and Yidie Ye are with the Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo 315211, China (e-mail: xiayinshui@nbu.edu.cn; 1611082572@nbu.edu.cn; xiahuakang@nbu.edu.cn; yeyidie@nbu.edu.cn).

Ge Shi is with the College of Mechanical and Electrical Engineering, China Jiliang University, Hangzhou 310018, China (e-mail: shige@cjlu.edu.cn).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TPEL.2023.3346872>.

Digital Object Identifier 10.1109/TPEL.2023.3346872

devices before the MPPT starts. Wang et al. [22] introduced a self-powered MPPT controller implemented with passive components for the SSHI interface circuit. Nonetheless, the voltage drops of the passive components restrict the MPPT efficiency with low input voltage. Yue et al. [23] proposed a duty-cycle-based MPPT algorithm for P-SSHI circuit to maximize output power. However, an integrated analog computer is required to calculate the MPP.

The synchronous electric charge extraction (SECE) technique by Lefeuvre et al. [24] is the first interface circuit that can eliminate the power load dependency (or at least weakly dependent). First, all the energy stored on the PE clamped capacitance C_p is transferred to an inductor L in 1/4th of the LC oscillation period ($t_{SECE} = 0.25T_{LC}$); second, the energy on inductor L is released to the final storage through the freewheeling diode. Several improved interface circuits were proposed based on the basic SECE topology, such as the self-powered optimized SECE by Wu et al. [25], the self-powered SECE with low phase-lag by Shi et al. [26], the SECE with residual charge inversion by Dini et al. [27] and the synchronous inversion and charge extraction interface by Cheng et al. [28]. Furthermore, Romani et al. [29] and Dini et al. [30] employed SECE-based circuits for multi-input PZTs with a single inductor configuration to harvest more energy. Wang et al. [31] introduced a multi-input SECE circuit based on buck structure for PE energy harvesting.

Since nonsinusoidal vibrations are typically encountered in the environment, interface circuits under different vibration modes were carried out. Costanzo and Vitelli [32] introduced a nonlinear dynamic maximum power transfer control algorithm in the case of nonsinusoidal vibrations. The performances of SECE and S-SSHI interface circuits under variable mechanical excitation was studied [33]. Costanzo et al. [34] proposed a self-powered power optimizer under nonsinusoidal vibrations to enhance the power harvesting capability, which is implemented by a switch-mode circuit and behaves like a negative capacitance. Dalin and Hasan [35] presented a self-powered SECE circuit, which has low phase lag and is only suitable for low-frequency pressure-type PE energy harvesting.

Usually, a rectifier bridge is employed in these interface circuits to provide ac–dc conversions, such as the diode rectifier bridge and negative voltage converter. The rectifier bridges only work when the PZT voltage exceeds the threshold voltage and causes lots of energy loss. Especially, when the output of the PZT is weak, the energy consumed by the rectifier bridges may even exceed the energy harvested by the load. As a solution to this issue, Cai and Manoli [36] proposed an interface circuit based on the autonomous conjugate impedance matching method, which removes the rectifier bridge so that energy loss can be reduced. Du et al. [37] proposed an efficient SSHI interface circuit, which increases the input range of the PZT. Although the abovementioned solutions improve the energy harvesting efficiency with low voltage, extra control circuits are required and the complexity of the circuit is increased. Shareef et al. [38] proposed a multi-input rectifier-less ac–dc interface circuit. However, it suffers from drawbacks in inefficient switching and complicated gate drive so a high circuit loss exists.

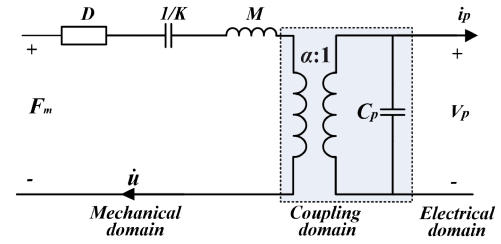


Fig. 1. Equivalent circuit model of a PZT.

In this article, a novel rectifier-less synchronous electric charge extraction and inversion (ReL-SECEI) interface circuit is proposed and the self-powered implementation of the ReL-SECEI circuit is presented. The proposed ReL-SECEI circuit extracts the partial electric charges and inverts the remainder on the clamped capacitance C_p of PZT to achieve improved output power. In addition, the self-powered and rectifier-less designs reduce the internal power loss and, hence, improve the energy harvesting efficiency. The inversion voltage of the ReL-SECEI circuit is significantly related to the output voltage, so that the harvested power is load-dependent and there is an optimum output voltage when the harvested power reaches the peak. The drawback can be addressed by employing MPPT techniques.

The rest of this article is organized as follows. In Section II, the circuit topology of the SECE and the proposed Rel-SECEI are introduced, respectively. In Section III, the self-powered implementation of the Rel-SECEI circuit is described. In Section IV, the experimental work is provided. Finally, Section V concludes this article.

II. SECE AND ReL-SECEI TOPOLOGY

A. Equivalent Circuit Model

The equivalent model of the PZT is an electromechanical coupling system, as shown in Fig. 1. It can be equivalent to a transformer-based circuit, which consists of mechanical domain, coupling domain, and electrical domain. The governing equations are given by [8]

$$M \ddot{u} = F_m - Ku - D\dot{u} - \alpha V_p \quad (1)$$

$$i_p = \alpha \dot{u} - C_p \dot{V}_p \quad (2)$$

where F_m , M , D , K , and C_p are the external mechanical vibration force, modal mass, damper, global equivalent stiffness, and PE clamped capacitance, respectively. α and u are the PE force-voltage factor and vibration displacement in the mechanical domain. V_p and i_p are the output PE voltage and current, respectively.

B. SECE Circuit

The SECE is a typical interface circuit for PE energy harvesting. Fig. 2(a) shows the typical SECE circuit, which is composed of a PZT, a diode bridge rectifier, a switch S , an inductor L , a diode D , and an output capacitor C_r . At the peak of the PZT voltage, energy on C_p is first extracted to the inductor L and the

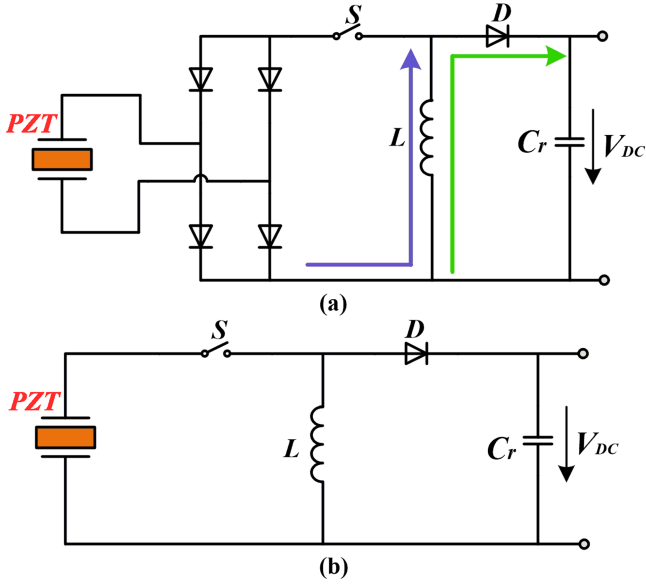


Fig. 2. Topological structure of (a) SECE; (b) proposed ReL-SECEI.

PZT voltage drops from the peak to 0. Then, energy is transferred from L into the output capacitor C_r . The energy that can be harvested is computed in [27].

$$E_h = 2C_p V_{P0}^2 (1 - 2\gamma)^2 e^{-\pi/(\omega_{01}\tau)} \quad (3)$$

where $\tau = 2L/r$ with L and r assumed to be the inductor value and the resistance of the inductor. γ and ω_{01} can be obtained in

$$\gamma = \frac{V_\gamma}{V_{P0}} \quad \omega_{01} = \sqrt[3]{LC_p} \quad (4)$$

where V_γ and V_{P0} are the threshold voltage of the diode bridge rectifier and the open-circuit voltage of the PZT, respectively.

From (3) and (4), it can be seen that the diode rectifier bridge causes a portion of energy loss. As the open circuit voltage V_{P0} decreases, the energy loss caused by the diode rectifier bridge increases. And when V_{P0} is small ($V_{P0} < 2V_\gamma$), the SECE circuit cannot harvest energy from the PZT anymore. Hence, if the diode rectifier bridge can be removed, the energy that can be harvested will increase.

C. ReL-SECEI Circuit

The topological structure of the proposed ReL-SECEI circuit is shown in Fig. 2(b). In contrast to the SECE circuit, the ReL-SECEI removes the diode bridge rectifier by optimizing the energy harvesting method. Fig. 3(a) and (b) shows the energy harvesting model in the positive half cycle and in the negative half cycle, respectively. The ReL-SECEI divides the energy harvesting operation into two parts, charges inversion and charges extraction, to achieve efficient energy harvesting. In addition, it can be seen that the LC resonant loop in the ReL-SECEI circuit has no extra energy-consuming components, which contributes to the more efficient LC resonance.

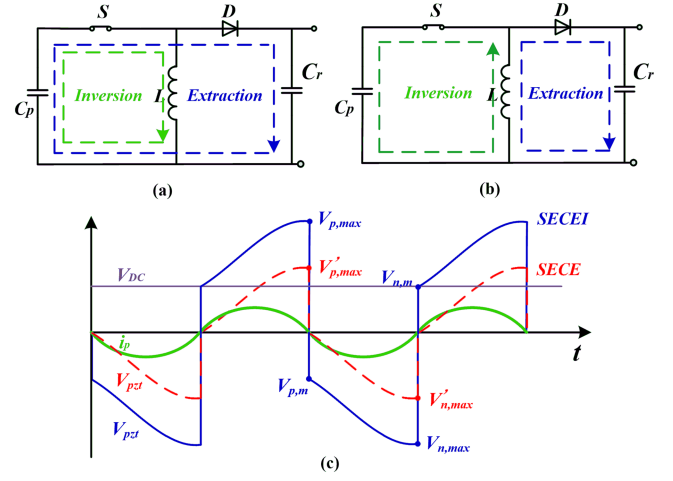


Fig. 3. Energy harvesting models and waveforms. (a) Energy harvesting model in the positive half cycle. (b) Energy harvesting model in the negative half cycle. (c) Waveforms of the ReL-SECEI and SECE.

Fig. 3(c) shows the working voltage waveforms of the PZT in the ReL-SECEI and SECE circuits. As illustrated, the ReL-SECEI and SECE do the energy harvesting operation at the same time. The SECE extracts the whole charges of the PZT while the ReL-SECEI extracts the partial electric charges and inverts the others so that the working voltage of the ReL-SECEI is significantly higher than that of the SECE. Its detailed working principle is described as follows.

Define t_p and t_n as the duration time of the LC resonant loop in the positive half cycle and in the negative half cycle, respectively. The inversion factor λ_p and λ_n in the positive and negative half cycle can be expressed as

$$\begin{cases} \lambda_p = e^{-\omega t_p/2Q} \\ \lambda_n = e^{-\omega t_n/2Q} \end{cases} \quad (5)$$

In the positive half cycle, the PZT voltage $V_{pzt} > 0$. The switch S is turned ON when V_{pzt} reaches its peak, and the peak voltage can be expressed in

$$V_{p,max} = V_{n,m} + 2\frac{\alpha U_M}{C_p} \quad (6)$$

where $V_{n,m}$ is the inversion voltage of the previous negative half cycle.

First, the energy on C_p is extracted to the load with the loop of the capacitors C_p , C_r , the switch S and the diode D . When the PZT voltage V_{pzt} drops to the output voltage V_{dc} , the diode D cuts off and the charges extraction stages finishes. Then, the switch S is still turned ON and the capacitors C_p and the inductor L form an LC resonant loop. Since t_p is equal to $1/2 LC$ resonance period ($t_p = 0.5T_{LC}$), the residual electric charges are inverted on C_p . The extracted energy and the inverted voltage in the positive half cycle can be obtained, respectively, as follows:

$$E_{e,p} = \frac{1}{2} C_p (V_{p,max}^2 - V_{dc}^2) \quad (7)$$

$$V_{p,m} = \lambda_p \cdot V_{dc} \quad (8)$$

In the negative half cycle, $V_{pzt} < 0$, the energy harvesting process can also be divided into two parts: 1) charges inversion and 2) charges extraction stages, as shown in Fig. 3(b). The peak voltage $V_{n,max}$ in the negative half cycle can be expressed in

$$V_{n,max} = V_{p,m} + 2 \frac{\alpha u_M}{C_p} \quad (9)$$

where $V_{p,m}$ is the inversion voltage of the previous positive half cycle.

Then, switch S is turned ON, and the capacitor C_p and the inductor L form an LC resonant loop. After $0.25T_{LC}$, the energy on C_p is transferred to inductor L , V_{pzt} drops from the peak value $V_{n,max}$ to 0, and inductor current increases from 0 to the peak. Switch S remains in the conductive state and inductor L starts to charge C_p inversely. At the same time, diode D is cut off since the voltage across inductor L is less than V_{dc} . The PZT voltage V_{pzt} and inductor current I_L can be defined as

$$V_{pzt}(t) = V_{n,max} \cos(\omega t) e^{-\omega t/2Q} \quad (10)$$

$$I_L(t) = \sqrt{\frac{C_p}{L}} V_{n,max} \sin(\omega t) e^{-\omega t/2Q}. \quad (11)$$

When the voltage at the ends of the inductor exceeds V_{dc} , diode D is conducted, and the residual energy on L begins to charge output capacitor C_r through D . Hence, t_n is larger than $0.25T_{LC}$, and the inductor charges the C_p inversely to a certain negative voltage $-V_{n,m}$ as shown in Fig. 3(c).

The extracted energy and inverted voltage in the negative half cycle can be obtained, respectively, as follows:

$$E_{e,n} = \frac{1}{2} C_p (V_{n,max}^2 \lambda_n^2 - V_{dc}^2) \quad (12)$$

$$V_{n,m} = V_{dc}. \quad (13)$$

t_n is the duration time of LC resonant loop and can be expressed as

$$\cos(\omega t_n) e^{-\omega t_n/2Q} = \frac{V_{dc}}{V_{n,max}}. \quad (14)$$

The range value of t_n is given in

$$\frac{\pi}{2} < \omega t_n < \pi. \quad (15)$$

According to the working principle of the ReL-SECEI, the harvested energy is transferred to the output capacitor in one cycle can be expressed as

$$E = E_{e,p} + E_{e,n}. \quad (16)$$

The corresponding harvested output power is finally given by (17) shown at the bottom of the this page

It can be seen that there is an optimal output voltage when the harvested output power reaches its peak value, and the optimal

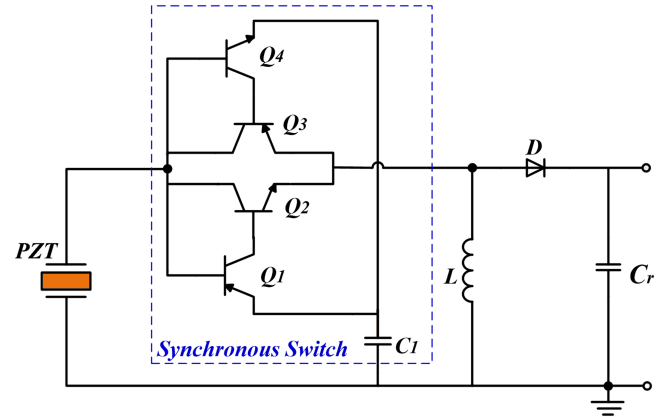


Fig. 4. Self-powered ReL-SECEI circuit.

TABLE I
COMPONENTS REQUIRED IN THE CIRCUITS

	TPEL [12]	TPEL [39]	TPEL [15]	TIE [40]	This work
Transistors	4	4	8	4	4
MOSFETs	0	0	0	1	0
Capacitor	2	2	2	1	1
Inductor	1	1	1	2	1
Diodes	4	12	0	3	1
Resistors	0	4	0	0	0

load voltage and the peak output power can be obtained

$$V_{dc,opt} = \frac{2\alpha u_M}{C_p} \frac{1 + \lambda_p \lambda_n^2}{1 - \lambda_p^2 \lambda_n^2} \quad (18)$$

$$P_{out,max} = 2f \frac{\alpha^2 u_M^2}{C_p} \left[(1 + \lambda_n^2) + \frac{(1 + \lambda_p \lambda_n^2)^2}{1 - \lambda_p^2 \lambda_n^2} \right]. \quad (19)$$

When the output voltage deviates from the optimal value, the output power reduces. The integration of the MPPT controller can make the proposed circuit output the maximum power. In addition, it should be pointed out that the peak output power described in (18) is the energy that theoretically can be harvested. In other words, it is electrical energy that the PZT converts from mechanical energy. If an interface circuit is connected, since parts of energy are consumed, the optimal load voltage and the peak output power will reduce.

III. IMPLEMENTATION OF THE ReL-SECEI

Fig. 4 shows the implementation of the self-powered ReL-SECEI circuit. Except for the output capacitor C_r and the interfaced PZT, only a synchronous switch, an inductor and a diode are required. And the synchronous switch consists of four transistors (Q_1 , Q_2 , Q_3 , and Q_4) and a small detecting capacitor C_1 . The components required in each self-powered circuit are shown in Table I, it can be found that the proposed

$$P_{out} = \frac{1}{2} f C_p (V_{p,max}^2 + V_{n,max}^2) e^{-\omega t_m/Q} - 2V_{dc}^2 = 2f C_p \left[\frac{\alpha^2 u_M^2}{C_p^2} (1 + \lambda_n^2) + \frac{\alpha u_M}{C_p} V_{dc} (1 + \lambda_p \lambda_n^2) - \frac{1}{4} V_{dc}^2 (1 - \lambda_p^2 \lambda_n^2) \right]. \quad (17)$$

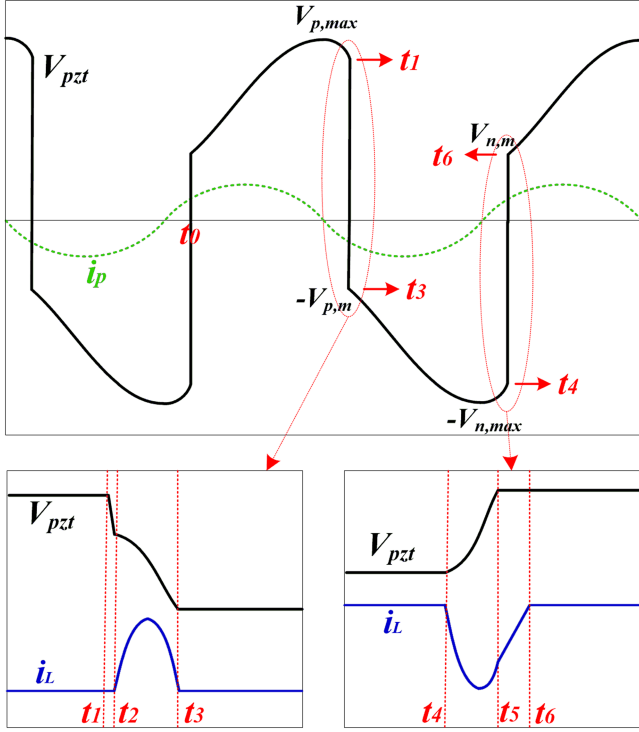


Fig. 5. Typical waveforms of the self-powered ReL-SECEI circuit.

ReL-SECEI circuit uses fewer components than other interface circuits proposed previously.

Take one working cycle period t_0 – t_6 for discussion. The typical waveforms of the self-powered ReL-SECEI circuit are shown in Fig. 5. Fig. 6 shows the detailed working principle in positive half-cycle natural charging time (t_0 – t_1), positive half-cycle extraction and inversion time (t_1 – t_3), negative half-cycle natural charging time (t_3 – t_4), and negative half-cycle inversion and extraction time (t_4 – t_6).

A. Positive Half-Cycle Natural Charging (t_0 – t_1)

In this period, the equivalent current source i_p charges C_p of PZT and C_1 , as shown in Fig. 6(a), while the working voltage V_{pzt} of the PZT increases and the waveform of V_{pzt} is shown in Fig. 5. When V_{pzt} reaches its peak value, it can be expressed as

$$V_{p,max} = V_{n,m} + \frac{2\alpha u_M}{C_p + C_1}. \quad (20)$$

Due to the detecting capacitor C_1 , the peak voltage on C_p reduces and causes energy loss. If the value of C_1 increases, the energy transferred on C_p decreases since the C_1 and C_p are connected in parallel in the natural charging state. The energy loss caused by C_1 can be expressed as

$$E_{p,loss1} = \frac{1}{2}C_p \left(V_{n,m} + \frac{2\alpha u_M}{C_p} \right)^2 - \frac{1}{2}C_p \left(V_{n,m} + \frac{2\alpha u_M}{C_p + C_1} \right)^2. \quad (21)$$

Although the energy loss can be decreased by reducing the value of C_1 , small C_1 may cause the following restrictions: the ON-resistance of the switching transistor in the synchronous switch is large and the energy on C_p will not be fully extracted.

Hence, C_1 should meet the following condition:

$$C_1 > \frac{1}{\beta} C_p. \quad (22)$$

C_1 is related to the dc gain β of the transistors in the synchronous switch and C_p . It should be noted that an appropriate value should be chosen for C_1 in the synchronous switch.

At the same time, the voltage on C_1 also reaches its maximum value after charging by i_p

$$V_{C1,max} = V_{n,m} + \frac{2I_p}{\omega \cdot (C_p + C_1)} - V_{BE} \quad (23)$$

where V_{BE} stands for the transistor threshold voltage.

Starting from the peak point, i_p begins to reverse and V_{pzt} decreases. However, the voltage on C_1 remains unchanged because the charges stored on C_1 cannot be released. At time t_1 , V_{pzt} drops to $V_{p,max} - 2V_{BE}$, so that transistors Q_1 and Q_2 are turned ON. The phase lag θ between the peak voltage point and the switching operation can be calculated as in

$$\theta = \cos^{-1} \left(\frac{V_{p,max} - 2V_{BE}}{V_{p,max}} \right). \quad (24)$$

B. Positive Half-Cycle Extraction and Inversion Time (t_1 – t_3)

At instant t_1 , C_p and C_r constitute the first loop with the conduction of Q_2 and D , so that the energy stored on C_p is transferred to C_r , as shown in Fig. 6(b). And the voltage V_{pzt} drops quickly (time t_1 – t_2), as shown in Fig. 5.

At time t_2 , the energy extraction process stops since the voltage V_{pzt} is lower than $V_{dc} + V_D + V_{CE(sat)}$ and the diode D is cut off. $V_{CE(sat)}$ and V_D stand for the saturated conduction voltage and the conduction voltage drop, respectively. During this period, the main energy loss is caused by diode D and the transistor Q_2

$$E_{p,loss2} = \int (V_{CE(sat)} + V_D) \cdot I(t) dt. \quad (25)$$

From another perspective, the extraction efficiency in this process can be expressed as

$$\eta_{p,e} = \frac{V_{dc}}{V_{CE(sat)} + V_D + V_{dc}}. \quad (26)$$

From (26), it can be found that extraction efficiency can be maintained at a high level when the output voltage is high. And most of the energy will be consumed if the output voltage is low.

At instant t_2 , L and C_p constitute the second loop with the conduction of Q_2 so that the residual energy stored on C_p is transferred to L , as shown in Fig. 6(b). After $1/2 LC$ resonant period, C_p is charged reversely, causing the voltage V_{pzt} inverts $-V_{p,m}$. The main energy loss in the LC loop is caused by the transistor Q_2 and the inductor L and can be expressed as

$$E_{p,loss3} = \int_0^{\pi\sqrt{LC}} (V_{CE(sat)} \cdot i_L + r \cdot i_L^2) dt \quad (27)$$

where i_L and r stand for the current of the inductor and the equivalent resistance of the inductor L , respectively.

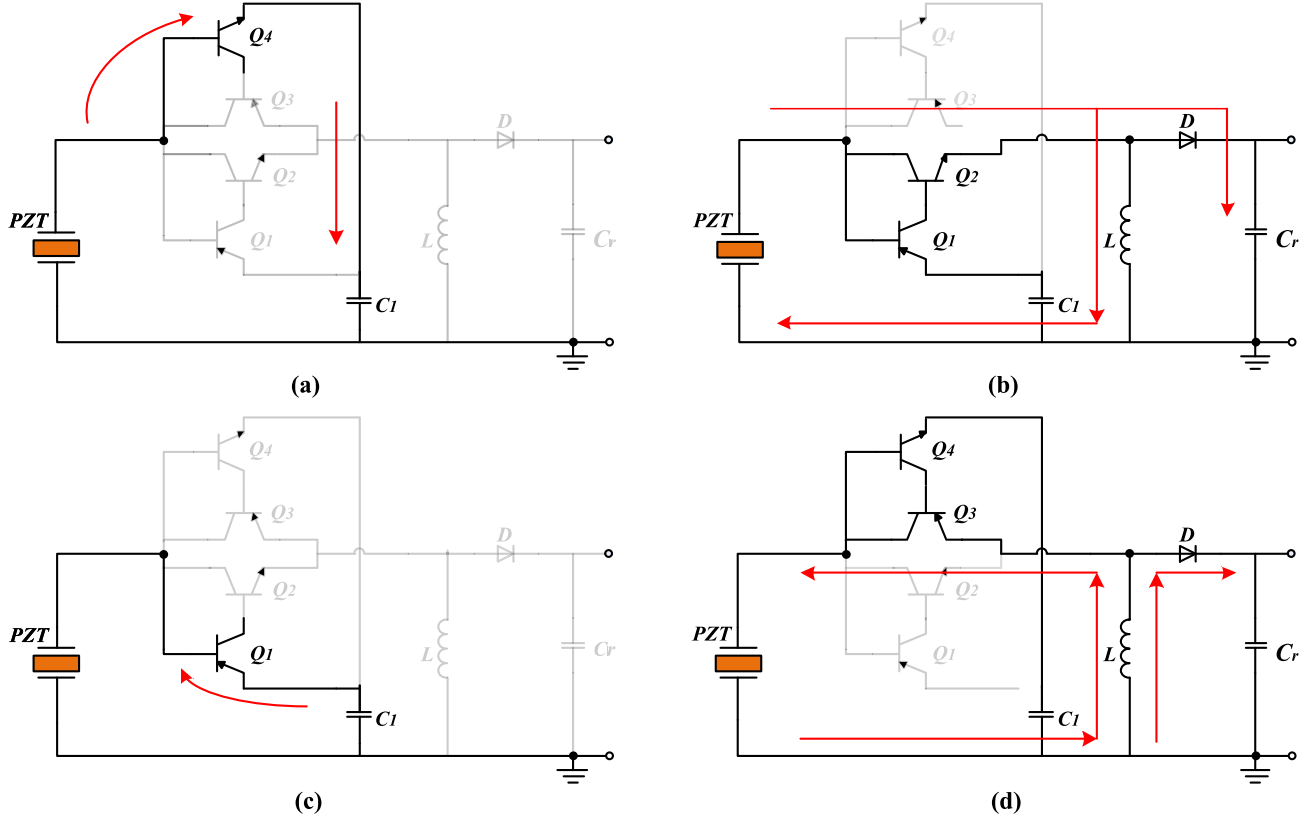


Fig. 6. Four phases within one cycle. (a) Positive half-cycle natural charging (t_0-t_1). (b) Positive half-cycle extraction and inversion (t_1-t_3). (c) Negative half-cycle natural charging (t_3-t_4). (d) Negative half-cycle inversion and extraction (t_4-t_6).

For the inversion process, from time t_1 to t_2 , the inversion voltage $V_{p,m}$ can be obtained as

$$V_{p,m} + V_{CE(sat)} = (V_{dc} + V_D + V_{CE(sat)}) \cdot \lambda_p. \quad (28)$$

C. Negative Half-Cycle Natural Charging Time(t_3-t_4)

In this period, it works the same as the positive half-cycle natural charging time. i_p also charges C_p and C_1 , as shown in Fig. 6(c).

D. Negative Half-Cycle Inversion and Extraction Time(t_4-t_6)

At time t_4 , V_{pzt} drops to $V_{n,max} - 2V_{BE}$ and then Q_3 and Q_4 are turned ON. Then L and C_p constitute the LC oscillation circuit with the conduction of Q_3 so that the energy on C_p is transferred to L , as shown in Fig. 6(d). When the conduction time of Q_3 is larger than $0.25T_{LC}$, the inductor charges C_p inversely to a certain negative voltage, as shown in Fig. 5.

At time t_5 , the inductor voltage exceeds $V_{dc} + V_D$ and the diode D is conducted. The charges inversion process stops and the generated energy loss can be expressed as

$$E_{n,loss1} = \int (V_{CE(sat)} \cdot i_L + r \cdot i_L^2) dt. \quad (29)$$

Then, the residual energy on L begins to charge C_r through D . During this period, the main energy loss can be obtained in

$$E_{n,loss1} = \int (V_D \cdot i_L + r \cdot i_L^2) dt. \quad (30)$$

From (29) and (30), it can be seen that the main energy loss is caused by the diode D , the transistor, and the inductor. The components with low threshold voltage and the inductor with high-quality factors can reduce energy loss. However, the higher quality factor means a larger inductor volume, which limits its application in micro WSN nodes.

IV. EXPERIMENTAL WORK

A. Experimental Setup

The experimental platform is set up to verify the above theoretical analysis, which is composed of the PZT, a signal generator, an oscilloscope, a power amplifier, a bench multimeter, a shaking table and the tested interface circuits, as shown in Fig. 7. The PZT from Mide Technologies, with 190 nF corresponding internal capacitance, is fixed on the shaking table, and the shaking table is excited by the power amplifier and signal generator. Three tested circuit fabricated by the discrete components based on ReL-SECEI, SECE, and S-SSHI is shown in Figs. 4, 8(a) and (b), respectively. Three different inductors, 2.2 mH with 16 Ω internal resistance, 4.7 mH with 20 Ω internal resistance and 50 mH with 100 Ω internal resistance, are adopted to test the energy harvesting performance of the circuits. A 4.7 nF capacitance is used as C_1 while an electrolytic capacitor with a 10 μ F capacitance value is used as C_r . Two PNP transistors and two NPN transistors use the components 2N3906 and 2N3904, respectively. The diode uses the component 1N4148.

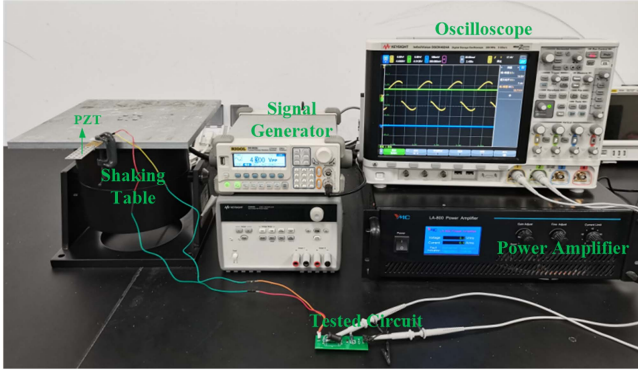


Fig. 7. Experimental setup.

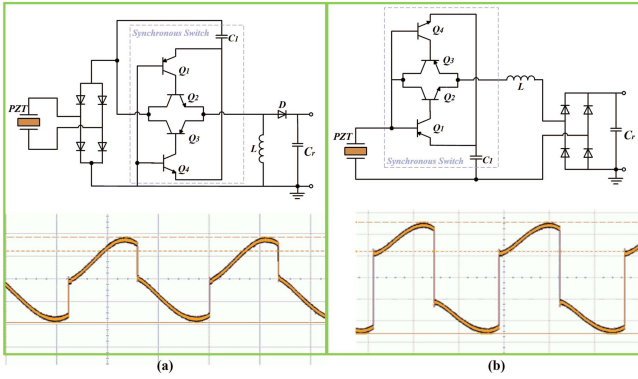


Fig. 8. Circuits and waveforms of (a) SECE and (b) S-SHI.

The signal generator is adjusted to make the PZT work near its resonance frequency of 19 Hz and the open circuit voltage of the PZT, $V_{oc} = 3$ V. The PZT is interfaced in the input end of the proposed Re-SECEI circuit while a 100 k Ω load resistor is connected to the output end. Fig. 9 shows the measured voltage V_{pzt} , output voltage V_{dc} , and inductor current i_L waveforms in the experiment, in which there is an enlarged view of the rising and falling edges. The falling edge means the charges extraction and inversion in the positive half-cycle, while the rising edge means the charges inversion and extraction in the negative half-cycle. The falling edge can be divided into two stages: 1) the charges extraction stage from time t_1 to t_2 and 2) the inversion stage from time t_2 to t_3 , as shown in Fig. 9. And the rising edge can also be divided into two stages: 1) the charges inversion stage from time t_4 to t_5 and 2) the charges extraction stage from time t_5 to t_6 . It can be seen that the captured waveforms in the experiment are consistent with the waveforms in the analysis, as shown in Fig. 5, which verifies the feasibility of the proposed circuit.

Fig. 10 shows the simulated and experimental output power curves of the proposed ReL-SECEI versus the different output voltage V_{dc} under sinusoidal vibrations. The simulated output power in the figure is simulated by the LTspice platform based on the model of Fig. 1. The detailed parameters for simulations are given in Table II. The experimental output power is obtained under the sinusoidal vibrations, as shown in Fig. 11(a). It can be seen that there is an optimal output voltage in the proposed circuit under the fixed vibration amplitudes. The output power

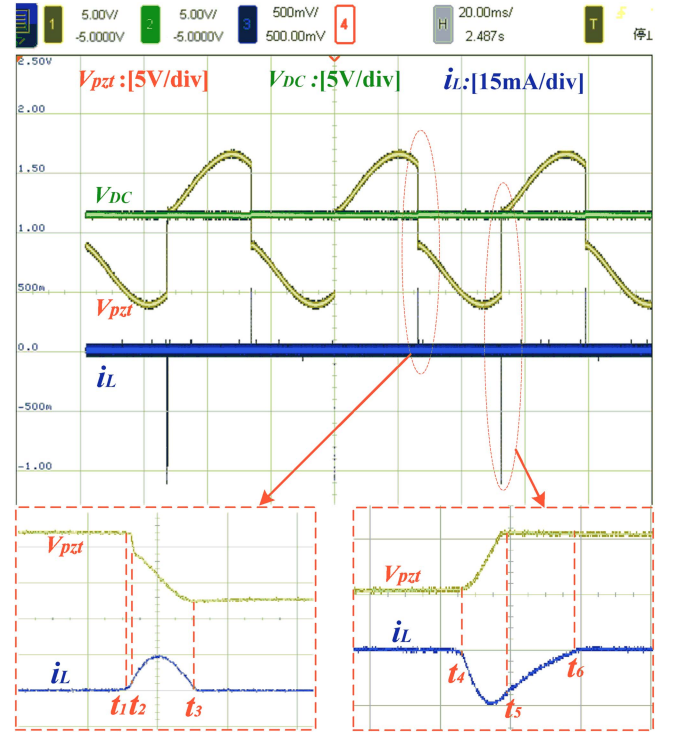
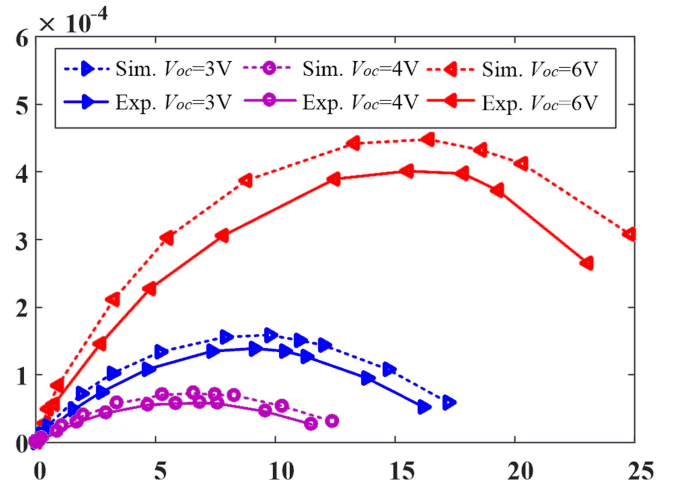


Fig. 9. Captured waveforms in the experiment.

Fig. 10. Simulated and experimental output power versus V_{dc} under different vibration amplitudes.TABLE II
PARAMETERS FOR SIMULATIONS

Parameters	values
Mass, M	0.02 kg
Damping coefficient, D	0.03 N·s/m
Spring stiffness, K	284.745 N/m
PE clamped capacitance, C_p	190 nF
Natural Frequency, f_n	19 Hz
PE force-voltage factor, α	0.0002 N/V
Equivalent voltage source, V_s	0.021 V

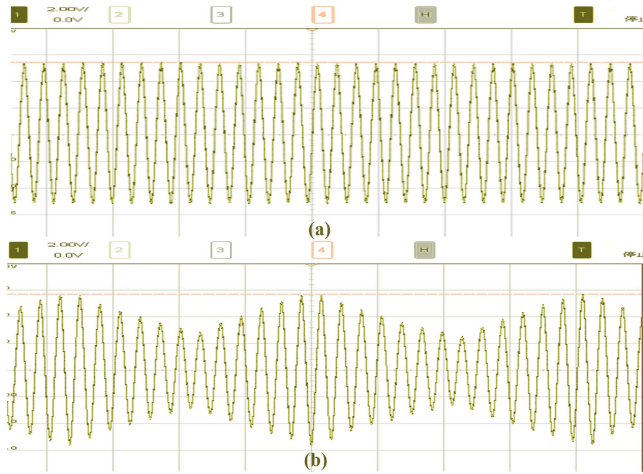


Fig. 11. Output of the PZT under. (a) Sinusoidal vibrations. (b) Intermittent vibration.

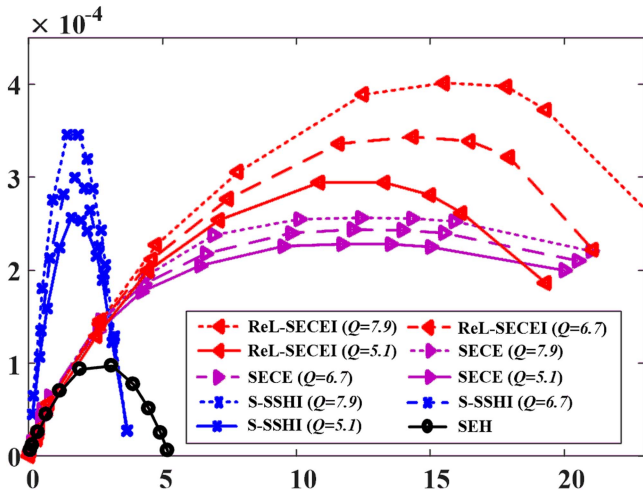


Fig. 12. (a) Measured peak output power under different excitation frequencies f . (b) Measured output power versus V_{dc} under nonsinusoidal vibration.

decreases as the output voltage V_{dc} deviates from its optimal value, which is consistent with the previous analysis. The inversion voltage of the ReL-SECEI circuit is significantly related to the output voltage, so that the harvested power is load-dependent and there is an optimum output voltage when the harvested power reaches the peak. The drawback can be addressed by employing MPPT techniques and the high output power can be maintained.

Fig. 12 shows the experimental output power of the ReL-SECEI, S-SSHI, SECE, and the SEH versus the different output voltage V_{dc} under sinusoidal vibrations ($V_{oc} = 6$ V). The ReL-SECEI, S-SSHI, and SECE are implemented by the same synchronous switch, inductor, and energy-storage capacitor. In addition, the components used in the experiment also remained consistent. Three different inductors, 2.2 mH (16 Ω), 4.7 mH (20 Ω), and 50 mH (100 Ω) were adopted to test the performance of the ReL-SECEI, S-SSHI, and SECE. The electrical quality factor is 6.7 (2.2 mH), 7.9 (4.7 mH), and 5.1 (50 mH), respectively. The tested circuits adopt the inductors with different quality factors and the output power changes. Although the value of

50 mH is the highest, the electrical quality factor is lowest. It can be seen that the ReL-SECEI, S-SSHI, and SECE has the worst performance when the inductor with 50 mH is adopted. An inductor with a high-quality factor will reduce the energy loss and improve the output power. The influence of the inductor on ReL-SECEI, S-SSHI, and SECE is related to the inductance value and influenced by the internal resistance. However, the inductor with a high-quality factor will increase its volume and limit its application in micro WSN nodes.

Among them, the ReL-SECEI and the S-SSHI are influenced evidently by the inductor while the inductors have less influence on the SECE. The reason is that the ReL-SECEI and the S-SSHI operate the inversion voltage with the LC resonant loop, an inductor with a low-quality factor will decrease the inversion factor and reduce the output power. In addition, the duration time of the LC resonant loop in the ReL-SECEI and the S-SSHI is longer than that in the SECE, which increases the energy loss on the inductor. Since no inductor is used in the SEH circuit, it makes no difference to the SEH circuit.

The SECE has the best load adaptability, however, the peak output power is lower than the S-SSHI and the ReL-SECEI. This is that the S-SSHI and ReL-SECEI increase the working voltage of the PZT through the inversion voltage so that the peak output power improves. Since the S-SSHI achieves the inversion voltage through the LC resonant loop with the PZT, the output capacitor and the inductor, it has the worst load adaptability. The output power of the S-SSHI performs the best when the output voltage $V_{dc} < 3$ V while the output power of the ReL-SECEI performs the best when the output voltage $V_{dc} > 3$ V. The maximum output power of the proposed ReL-SECEI can reach 4.2 times that of the SEH circuit with the 4.7 mH inductor.

When the inductor is replaced, the output power curve of the S-SSHI is severely affected while the optimal output voltage of the S-SSHI remains unchanged. The research of Wang et al. [22] also illustrates this characteristic. The output power curve and the optimal output voltage of the proposed ReL-SECEI are both affected when the inductor is replaced. These characteristics are consistent with the description of (18) and (19). No matter, which inductor is used, the peak output power is the highest among the tested circuits. This is that a portion of electric charges generated by the PZT is inverted to improve the working voltage and the peak output power is increased. In addition, the diode rectifier bridges in the other circuits increase the energy loss, which not only decreases the conversion efficiency but also reduces the inversion factor.

In real-world scenarios, external excitation frequencies and amplitudes often vary, causing fluctuations in the output of the PZT. Since there are more nonsinusoidal vibrations in the real environment, the intermittent vibration is carried out to test the performance of the proposed ReL-SECEI, S-SSHI, and SECE circuit. Fig. 11(b) shows the open circuit voltage of the PZT under the intermittent vibration. It can be seen that the open-circuit voltage of the PZT varies from 5.6 V to 2.4 V due to the intermittent vibration. Fig. 13(a) shows the output power versus different V_{dc} under the nonsinusoidal vibration. As can be seen from the figure, the peak output power of the proposed ReL-SECEI is higher than that of S-SSHI and SECE due to

TABLE III
PERFORMANCE COMPARISON

Publication	TPEL2015 [41]	JSSC2018 [42]	JSSC2020 [43]	TCAS2018 [26]	TPEL2021 [12]	TPEL2022 [17]	This work
Process	Discrete	0.18 μ mBCD	0.18 μ mHV	0.18 μ mCMOS	Discrete	Discrete	Discrete
PZT	V22B	PPA1001	PPA1021	YiBoP8-1	PPA1014	N/A	PPA2011
C_p	18 nF	100 nF	28.42 nF	220 nF	41 nF	170 nF	190 nF
Technique	P-SSHI	Double Pile-Up Resonance	SSHC	SECE	S-SSHI	P-SSHI	ReL-SECEI
Inductor	940 μ H	680 μ H	N/A	1 mH	2.3 mH	1.56 mH	4.7 mH
Self-powered	NO	NO	NO	YES	YES	YES	YES
Boost to SEH(max)	5.8 \times	14.52 \times	9.3 \times	3.56 \times	3.7 \times	3.22 \times	4.2\times
V_{oc}	2.4–3.28 V	3–4 V	1.4 V	1.5–5 V	6 V	3.9–5.8 V	2–6 V
Frequency	225 Hz	140 Hz	200 Hz	42 Hz	19 Hz	77.5 Hz	19 Hz

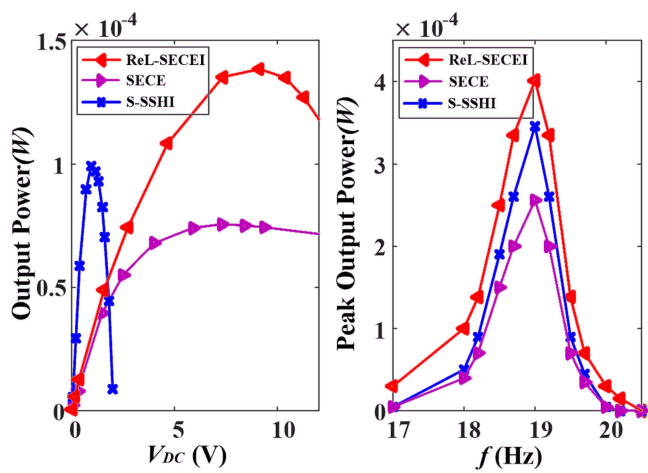


Fig. 13. (a) Measured output power versus V_{dc} under intermittent vibration. (b) Measured peak output power with different excitation frequencies f under sinusoidal vibrations.

the rectifier-less design. Especially when the input voltages are low, the energy caused by the rectifier will increase if a rectifier exists. As depicted in Fig. 13(b), the peak output power exhibits variations with changing excitation frequencies. When the PZT works near its resonant frequency, the open-circuit voltage of the PZT reaches its maximum value. Notably, the resonant frequency of the PZT is 19 Hz and the peak output power of the ReL-SECEI, S-SSHI, and SECE reaches 402μ W, 346μ W, and 256μ W, respectively. Although the peak output power curves of the ReL-SECEI, S-SSHI, and SECE are similar in terms of trend and shape, the peak output power of the ReL-SECEI are higher than those of S-SSHI and SECE. Furthermore, when the excitation frequencies deviate from 19 Hz and the output of the PZT drops, the ReL-SECEI has better adaptability. The reason is that it removes the diode bridge and has a lower energy harvesting startup voltage.

Table III provides a performance comparison with the state-of-the-art interface circuits for PE energy harvesters. The circuits proposed in [41], [26], [12], and [17] are based on three typical topologies, including SECE, S-SSHI, and P-SSHI. Except for the circuit in [41], the other circuits in [26], [12], and [17] are self-powered solutions. The circuit proposed in [42] uses the double pile-up resonance to enhance the energy harvesting

efficiency while [43] can achieve the energy harvesting without an inductor.

The circuits in [26] use the extra envelope detection modules to reduce the phase lag. The extra modules occupy a portion of energy loss and limit the energy harvesting efficiency. The circuit in [12] replaces the diode bridge with four passive switches. Eight transistors and two detecting capacitors are required to achieve the ac–dc conversion. Since the LC resonant loop in [12] has more extra energy-consuming components than in the proposed circuit, the energy loss increases. Due to the rectifier-less and simplified designs, the energy harvesting output power of the proposed circuit is higher than that of the circuits in [26], [12], and [17]. In addition, although the circuits in [41] and [42] have high energy harvesting ability, the external power supply is required to power the complicated control circuit. This means that the control circuit still consumes energy even without vibration. The circuit in [43] achieves efficient energy harvesting without an inductor. It can be fully integrated and the volume of the circuit reduces. Precharged energy is required to achieve self-starting. Hence, the inefficient passive circuit in the self-starting process affects the overall performance of the circuit.

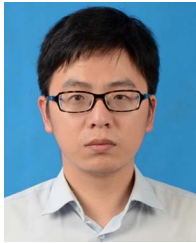
V. CONCLUSION

In this article, a ReL-SECEI interface circuit without a rectifier bridge is proposed. The ReL-SECEI divides the energy harvesting operation into two parts, charges inversion, and charges extraction, to achieve efficient energy harvesting. The inversion voltage of the ReL-SECEI circuit is significantly related to the output voltage so that the harvested power is load-dependent and the peak output power is obtained with the optimum load, which reaches 4.2 times that of the SEH circuit. In addition, the ReL-SECEI has good adaptability when the PZT outputs low voltages due to the rectifier-less designs.

REFERENCES

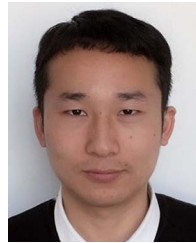
- [1] T. Ruan, Z. J. Chew, and M. Zhu, "Energy-aware approaches for energy harvesting powered wireless sensor nodes," *IEEE Sensors J.*, vol. 17, no. 7, pp. 2165–2173, Apr. 2017.
- [2] J. Sankman and D. Ma, "A 12- μ W to 1.1-mW AIM piezoelectric energy harvester for time-varying vibrations with 450-nA IQ," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 632–643, Feb. 2015.

- [3] X. D. Do, S. K. Han, and S. G. Lee, "Optimization of piezoelectric energy harvesting systems by using a MPPT method," in *Proc. IEEE 5th Int. Conf. Commun. Electron.*, 2014, pp. 309–312.
- [4] L. Y. Zhu, R. W. Chen, and X. J. Liu, "Theoretical analyses of the electronic breaker switching method for nonlinear energy harvesting interfaces," *J. Intell. Mater. Syst. Structures*, vol. 23, no. 4, pp. 441–451, Mar. 2012.
- [5] H. Liu, J. Zhong, C. Lee, S. W. Lee, and L. Lin, "A comprehensive review on piezoelectric energy harvesting technology: Materials, mechanisms, and applications," *Appl. Phys. Rev.*, vol. 5, no. 4, 2018, Art. no. 041306.
- [6] J. Liang and W.-H. Liao, "Energy flow in piezoelectric energy harvesting systems," *Smart Mater. Structures*, vol. 20, no. 1, 2010, Art. no. 015005.
- [7] G. A. Rincón-Mora and S. Yang, "Tiny piezoelectric harvesters: Principles, constraints, and power conversion," *IEEE Trans. Circuits Syst. I-Reg. Papers*, vol. 63, no. 5, pp. 639–649, May 2016.
- [8] D. Guyomar, A. Badel, E. Lefeuvre, and C. Richard, "Toward energy harvesting using active materials and conversion improvement by nonlinear processing," *IEEE Trans. Ultrasonics, Ferroelect. Freq. Control*, vol. 52, no. 4, pp. 584–595, Apr. 2005.
- [9] E. Lefeuvre, A. Badel, C. Richard, L. Petit, and D. Guyomar, "A comparison between several vibration-powered piezoelectric generators for standalone systems," *Sensors Actuators A, Phys.*, vol. 126, no. 2, pp. 405–416, 2006.
- [10] L. Zhu and R. Chen, "A new synchronized switching harvesting scheme employing current doubler rectifier," *Sensors Actuators A, Phys.*, vol. 174, pp. 107–114, 2012.
- [11] L. Garbuio, M. Lallart, D. Guyomar, C. Richard, and D. Audigier, "Mechanical energy harvester with ultralow threshold rectification based on SSHI nonlinear technique," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1048–1056, Apr. 2009.
- [12] Z. Chen, J. He, J. Liu, and Y. Xiong, "Switching delay in self-powered nonlinear piezoelectric vibration energy harvesting circuit: Mechanism, effects and solution," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2427–2440, Mar. 2019.
- [13] M. Lallart, L. Garbuio, L. Petit, C. Richard, and D. Guyomar, "Double synchronized switch harvesting (DSSH): A new energy harvesting scheme for efficient energy extraction," *IEEE Trans. Ultrasonics, Ferroelect. Freq. Control*, vol. 55, no. 10, pp. 2119–2130, Oct. 2008.
- [14] H. Shen, J. Qiu, H. Ji, K. Zhu, and M. Balsi, "Enhanced synchronized switch harvesting: A new energy harvesting scheme for efficient energy extraction," *Smart Mater. Structures*, vol. 19, no. 11, 2010, Art. no. 115017.
- [15] Z. Chen, Y. Xia, G. Shi, X. Wang, H. Xia, and Y. Ye, "Self-powered multi-input serial SSHI interface circuit with arbitrary phase difference for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9183–9192, Aug. 2021.
- [16] Z. Long, P. Li, X. Wang, B. Wang, H. S.-H. Chung, and Z. Yang, "A self-powered P-SSHI array interface for piezoelectric energy harvesters with arbitrary phase difference," *IEEE Trans. Ind. Electron.*, vol. 69, no. 9, pp. 9155–9164, Sep. 2022.
- [17] H. Xia et al., "Self-powered dual-inductor MI-PSSHI-VDR interface circuit for multi-PZTs energy harvesting," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3753–3762, Apr. 2022.
- [18] Z. Chen, M. K. Law, P. I. Mak, X. Zeng, and R. P. Martins, "Piezoelectric energy-harvesting interface using split-phase flipping-capacitor rectifier with capacitor reuse for input power adaptation," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2106–2117, Aug. 2020.
- [19] X. Yue and S. Du, "Performance optimization of SSHC rectifiers for piezoelectric energy harvesting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 4, pp. 1560–1564, Apr. 2023.
- [20] X. Yue and S. Du, "A synchronized switch harvesting rectifier with reusable storage capacitors for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2597–2606, Sep. 2023.
- [21] S. Fang et al., "An efficient piezoelectric energy harvesting circuit with Series-SSHI rectifier and FNOV-MPPT control technique," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 7146–7155, Aug. 2021.
- [22] X. Wang et al., "A novel MPPT technique based on the envelope extraction implemented With passive components for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12685–12693, Nov. 2021.
- [23] X. Yue, S. Javvaji, Z. Tang, K. A. A. Makinwa, and S. Du, "30.3 a bias-flip rectifier with a duty-cycle-based MPPT algorithm for piezoelectric energy harvesting with 98% peak MPPT efficiency and 738% energy-extraction enhancement," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2023, pp. 442–444.
- [24] E. Lefeuvre, A. Badel, C. Richard, and D. Guyomar, "Piezoelectric energy harvesting device optimization by synchronous electric charge extraction," *J. Intell. Mater. Syst. Structures*, vol. 16, no. 10, pp. 865–876, Oct. 2005.
- [25] Y. P. Wu, A. Badel, F. Formosa, W. Q. Liu, and A. Agbossou, "Self-powered optimized synchronous electric charge extraction circuit for piezoelectric energy harvesting," *J. Intell. Mater. Syst. Structures*, vol. 25, pp. 2165–2176, Nov. 2014.
- [26] G. Shi, Y. Xia, X. Wang, L. Qian, Y. Ye, and Q. Li, "An efficient self-powered piezoelectric energy harvesting CMOS interface circuit based on synchronous charge extraction technique," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 65, no. 2, pp. 804–817, Feb. 2018.
- [27] M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A nanopower synchronous charge extractor IC for low-voltage piezoelectric energy harvesting with residual charge inversion," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1263–1274, Feb. 2016.
- [28] K. Cheng, H. Chen, M. Lallart, and W. Wu, "A 0.25 μm HV-CMOS synchronous inversion and charge extraction (SICE) interface circuit for piezoelectric energy harvesting," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2018, pp. 1–4.
- [29] A. Romani, M. Filippi, and M. Tartagni, "Micropower Design of a Fully Autonomous Energy Harvesting Circuit for Arrays of Piezoelectric Transducers," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 729–739, Feb. 2014.
- [30] M. Dini, A. Romani, M. Filippi, V. Bottarel, G. Ricotti, and M. Tartagni, "A nanocurrent power management IC for multiple heterogeneous energy harvesting sources," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5665–5680, Oct. 2015.
- [31] X. Wang et al., "Multi-input SECE based on buck structure for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3638–3642, Apr. 2021.
- [32] L. Costanzo and M. Vitelli, "Maximum power transfer in electromagnetic vibration energy harvesters driven by non-sinusoidal vibrations," in *Proc. Int. Conf. Clean Elect. Power*, 2019, pp. 235–241.
- [33] L. Costanzo, A. Lo Schiavo, and M. Vitelli, "Power extracted from piezoelectric harvesters driven by non-sinusoidal vibrations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 3, pp. 1291–1303, Mar. 2019.
- [34] L. Costanzo, A. Lo Schiavo, and M. Vitelli, "A self-supplied power optimizer for piezoelectric energy harvesters operating under non-sinusoidal vibrations," *Energies*, vol. 16, no. 11, May 2023, Art. no. 4368.
- [35] E. M. Dalin and S. M. R. Hasan, "A low phase-lag self-powered SECE interface circuit for pressure-type piezoelectric energy-harvesting Compatible With COTS Pressure Sensors," *IEEE Trans. Very Large Scale Integration Syst.*, vol. 31, no. 10, pp. 1634–1638, Oct. 2023.
- [36] Y. Cai and Y. Manoli, "A piezoelectric energy-harvesting interface circuit with fully autonomous conjugate impedance matching, 156% extended bandwidth, and 0.38 μW power consumption," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2018, pp. 148–150, 2018.
- [37] S. Du, Y. Jia, C. Do, and A. A. Seshia, "An efficient SSHI interface with increased input range for piezoelectric energy harvesting under variable conditions," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2729–2742, Nov. 2016.
- [38] A. Shareef, L. Wang, Y. G., and N. Srikanth, "A rectifier-less AC–DC interface circuit for ambient energy harvesting from low-voltage piezoelectric transducer array," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1446–1456, Feb. 2019.
- [39] G. Shi, Y. Xia, Y. Ye, L. Qian, and Q. Li, "An efficient self-powered synchronous electric charge extraction interface circuit for piezoelectric energy harvesting systems," *J. Intell. Mater. Syst. Structures*, vol. 27, pp. 2160–2178, Jan. 2016.
- [40] H. Xia et al., "A self-powered S-SSHI and SECE hybrid rectifier for PE energy harvesters: Analysis and experiment," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1680–1692, Feb. 2021.
- [41] S. Lu and F. Boussaid, "A highly efficient P-SSHI rectifier for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5364–5369, Oct. 2015.
- [42] K. S. Yoon, S. W. Hong, and G. H. Cho, "Double pile-up resonance energy harvesting circuit for piezoelectric and thermoelectric materials," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1049–1060, Apr. 2018.
- [43] Z. Chen, M. K. Law, P. I. Mak, X. Zeng, and R. P. Martins, "Piezoelectric energy-harvesting interface using split-phase flipping-capacitor rectifier with capacitor reuse for input power adaptation," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2106–2117, Aug. 2020.



Zhidong Chen received the B.E. degree in electronic and information engineering and the M.S. degree in electronic circuit and system from Hangzhou Dianzi University, Zhejiang, China, in 2011 and 2014, respectively, and the Ph.D. degree in micro-nano information system from Ningbo University, Ningbo, China, in 2022.

He is currently a Lecturer with Zhejiang Wanli University, Ningbo, China. His research interests include energy harvesting systems, sensors, and measuring technology.



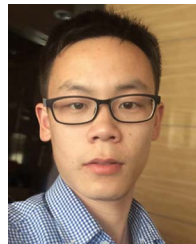
Xiudeng Wang received the B.E. degree in communication engineering, the M.E. degree in electronic circuits and systems, and the Ph.D. degree in electronic science and technology from Ningbo University, Ningbo, China, in 2016, 2019, and 2023, respectively.

Since 2023, he has been an Associate Professor with the Key Laboratory of Analog Integrated Circuits and Systems (Ministry of Education), School of Microelectronics, Hangzhou Institute of Technology, Xidian University, Xi'an, China. His current research interests include energy harvesting technologies, sensor and measurement technologies, power management, and energy-efficient integrated circuits.



Yinshui Xia received the B.S. degree in physics and the M.S. degree in electronic engineering from Hangzhou University, Zhejiang, China, in 1984 and 1991, respectively, and the Ph.D. degree in electronic engineering from Edinburgh Napier University, Edinburgh, U.K., in 2003.

He was a Visiting Scholar with King's College London in 1999 and then with Edinburgh Napier University as a Research Assistant and Research Fellow from 2000 to 2005. He is currently a Professor with the Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo, China. His research interests include low-power digital circuit design, logic synthesis and optimization, system on chip design, and energy harvesting systems.



Huakang Xia received the B.E. degree in aircraft design and engineering and the Ph.D. degree in instrument science and technology from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2012 and 2017, respectively.

He is currently a Lecturer with Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo, China. His current research interests include energy harvesting system, ultralow power circuit design, as well as embedded system.



Ge Shi received the B.E. degree in electrical engineering and automation and the M.S. degree in detection technology and automation from China Jiliang University, Zhejiang, China, in 2004 and 2010, respectively, and the Ph.D. degree in micro-nano information system from Ningbo University, Ningbo, China, in 2018.

He is a senior experimentalist with China Jiliang University, Hangzhou, China. His research interests include energy harvesting systems, sensors and measuring technology, ultralow power ICs design, as well as embedded system.



Yidie Ye (Member, IEEE) received the B.E. degree in electronic engineering and the Ph.D. degree in circuits and systems from Zhejiang University, Hangzhou, China, in 2007 and 2012, respectively.

She is currently an Assistant Professor with the Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo, China. Her current research interests include low-power circuit design and optimization.