A Bandwidth-Boosted Hybrid LDO With Spike-To-Time Converter for Near-Threshold Regulation

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***Abstract*—A fully integrated output-capacitorless hybrid low-dropout regulator (HLDO) with enhanced transient response and tight regulation, able to operate at ultralow supply, is proposed in this article. The proposed HLDO contains a dual-control-loop structure to separate the proportional and derivative controls. A spike-to-time converter is used in the derivative control loop to convert the output transient spikes into digital signals and then activates the digital control loop to adjust the output current rapidly to speed up the recovery of output. In the proportional control loop, an analog controller based on the ring-amplifier structure with the proposed compensation scheme utilizes a hybrid algorithm to achieve a rippleless output. The proposed HLDO is fabricated in a 65-nm CMOS process with a regular threshold voltage of about 0.45 V. The chip area is 0.0302 mm^2. The total on-chip capacitance is 4.4 pF. The minimum supply voltage is as low as 0.5 V with a minimum dropout voltage of 20 mV. At 1-V supply, the measured undershoot at the output is 142 mV and its settling time is 17 ns when the output current increases from 100 μA to 300 mA in 5 ns. The figure-of-merit is 2.05 fs.**

***Index Terms*—Low-dropout (LDO) regulator, near-threshold regulation, power-management-integrated circuits, ring amplifier, transient response.**

I. Introduction

THE emerging sensor applications for Internet-of-things motivate the development of the advanced power-management techniques to minimize the tradeoffs between power consumption and signal processing performance [1], [2], [3]. It is especially essential for portable electronic devices to extend the lifetime of battery [4]. Low-dropout (LDO) regulator, as a fundamental member in power-management-integrated circuits, is required to operate in a wide supply range. Conventional analog LDO (ALDO) is still the mainstream regulator used in many current commercial electronic devices due to its excellent power-supply rejection and low quiescent current (I_Q). As shown in Fig. 1(a), an ALDO consists of an error amplifier (EA), feedback resistors (R_1 and R_2), a power pMOSFET, and an output capacitor (C_O). When the supply voltage (V_{DD}) is very low, a large dropout voltage ($V_{\rm DO}$) is needed for a sufficiently high loop gain to retain both the high regulation accuracy and output-current capacity [5]. Moreover, the design of the EA at ultralow V_{DD} is critical and difficult as the voltage headroom is insufficient for proper operation.

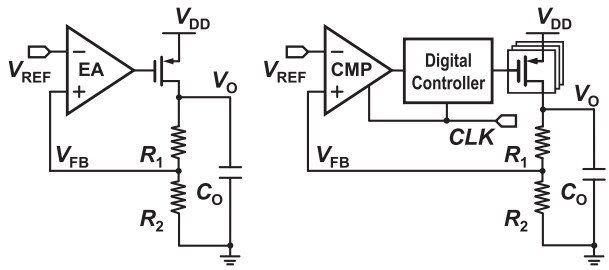

Fig. 1. Classical structures of (a) ALDO and (b) DLDO.

Digital LDO (DLDO) was developed to overcome the aforementioned low-supply problem of ALDO. The classical topology is shown in Fig. 1(b). A fast digital comparator is used to compare the feedback voltage ($V_{\rm FB}$) with the reference voltage ($V_{\rm REF}$). There are various algorithms used in the digital controller in the state-of-the-art designs, such as the successive approximation recursive binary search algorithm [6] and analog-proportional digital-integral multiloop control [7]. However, an extra clock signal, which consumes more power, is needed for both the comparator and digital controller. A high clock rate, which substantially increases I_Q, is required for the reduction of the output's voltage spikes and recovery time. To enhance the response speed and avoid the latency between a sudden load-change event and the clock edge, some techniques, such as the dual-coarse-fine loop architecture [8], [9], event-driven and self-triggering control [10], [11], and adaptive clocking [12], were proposed. Digital-like LDO based on inverters was proposed in [13] to achieve a fast transient response. Switching LDO [14] was proposed to obtain high accuracy and carry large load current (I_O). Nevertheless, the intrinsic quantization error of the analog-to-digital converter and the resultant

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large output ripples are still the key problems of these reported LDO designs. For the output-rippleless solution, inverter-based ALDO [15], ALDO with voltage-to-time conversion [16], ring-amplifier-based ALDO [17], and analog-assisted DLDO [18] were proposed. The unity-gain bandwidth (UGB) of the design in [15] is too small, and thus, the design is unable to handle a fast I_O change. The transient response of the design in [16] degrades significantly at low supply due to the insufficient voltage headroom. A clock signal is still necessary to control the switches inside the ring amplifier in [17] and the shift registers in [18], and a large C_O is extremely important and needed for maintaining the closed-loop stability and enhancing the transient performance.

Digitally assisted (DA) ALDO [19] and hybrid LDO (HLDO) [20], [21] were developed to combine the advantages of the ALDO and DLDO into a single design. The HLDOs in [19] and [20] are simply a parallel connection of an ALDO and DLDO. The digitally controlled power pMOSFET array is fully turned ON or OFF to increase the output-current capacity. The event-driven technique is used to temporarily turn OFF the digital controller such that the dynamic loss due to the fast-switching clock can be reduced substantially, and the regulation is then handed over to the ALDO in the steady state to achieve output-rippleless regulation. Nevertheless, the comparators in the HLDOs in [19] and [20] introduce extra signal delays to cause unsatisfactory transient response for the fast-changing load circuits. The HLDO in [21] takes the gate voltage (V_{GA}) of the "analog" power pMOSFET as an input of the digital controller. When V_{GA} exceeds the range defined by $V_{\rm HIGH}$ and $V_{\rm LOW}$, the digital controller turns ON or OFF the digital power pMOSFET array accordingly to adjust the required amount of current provided by the ALDO. Hence, the operation of the ALDO is always within the high-gain region. To enhance the transient response, a circuit block for droop-edge injection is added. However, similar to the designs in [19] and [20], folded-cascode amplifiers are used to reduce the stacked transistors, but they fail to function properly at a low V_{DD} (e.g., below 0.6 V). Moreover, the circuit performance is highly related to the boundaries of V_{GA} (i.e., $V_{\rm HIGH}$ and $V_{\rm LOW}$), which are suspected to be very sensitive to the process, voltage, and temperature (PVT) variations. The application of this HLDO is, therefore, highly restricted as additional tuning circuits to provide the corresponding voltage levels of $V_{\rm HIGH}$ and $V_{\rm LOW}$ at different V_{DD} are needed.

In this article, a fully integrated output-capacitorless (OCL) HLDO is proposed to solve the aforementioned problems. A spike-to-time converter (STC) is developed to achieve fast transient performance even under an ultralow supply of 0.5 V. A clock-free ring-amplifier-based structure of the EA is used, and thus, the proposed HLDO provides voltage regulation independent of the PVT variations. Moreover, a voltage-to-time converter (VTC) is proposed to convert analog signals into digital signals to adaptively adjust the required voltage threshold for triggering the operation of the DLDO part under different V_{DD}.

The rest of this article is organized as follows. Section II describes the proposed HLDO architecture and its circuit implementation. Section III presents the measurement results. Finally, Section IV concludes this article.

II. Proposed HLDO With STC

A. Overview of Working Principle of the Proposed LDO

The proposed HLDO was designed and fabricated using a 65-nm CMOS process, and the threshold voltages ($V_{\rm TH}$) of the regular and low-$V_{\rm TH}$ MOSFETs are around 0.45 V and 0.25 V, respectively. The overall structure, as shown in Fig. 2, is formed by the proposed STC, an analog controller to control V_{GA} of the "analog" power pMOSFET (M_{PA}) with aspect size ratio of 2.5×(W/L), and a digital controller to turn ON or OFF a "digital" power transistor array composed of 30 parallel-connected pMOSFETs (M_{PD}) with a unit size of (W/L). As shown in the top-right corner of Fig. 2, an ALDO has high regulation accuracy due to the high dc loop gain, but its loop bandwidth is seriously limited by its analog structure and utilized frequency compensation scheme. Thus, the introduction of a digital loop to the ALDO to form an HLDO provides the possibility of the improvement of the loop bandwidth since a comparator-based circuit, in general, is fast. To further extend the loop bandwidth of the HLDO, in this article, the proposed STC, which is a differentiator-based circuit and the core circuit of the derivative control loop, is added and used to achieve the transient-response enhancement. When I_O has rapid changes and the HLDO cannot respond immediately to provide the exact amount of current to the load, charging/discharging mechanisms of C_O happen to cause an overshoot or undershoot (or a voltage spike) at the HLDO output. The proposed STC is able to detect the rapidly changing voltage spikes better than the EA and comparator, and it immediately informs the digital controller to turn ON or OFF more transistors in the M_{PD} array subsequently. To ensure stability, the output of the STC (i.e., $V_{\rm STCH}$ and $V_{\rm STCL}$) is not considered by the digital controller when certain conditions are satisfied (more details will be explained in Section II-E). After that, the analog controller, which forms the proportional control loop, is dominant to regulate the output voltage (V_O). When the difference between $V_{\rm FB}$ and $V_{\rm REF}$ is large, the comparator is dominant to control the digital controller to control the M_{PD} array. After the regulation by the previous two regulation mechanisms, $|V_{\rm FB} - V_{\rm REF}|$ becomes very small to be detectable by the comparator, and then the EA takes over the regulation. The combination of the EA and M_{PA} is simply a typical ALDO, and thus, the steady-state V_O is rippleless and has high regulation accuracy. V_{GA} is evaluated by the analog controller, and thus, when V_{GA} is too low, which means that the current provided by M_{PA} is close to its upper limit, the digital controller will turn ON one more transistor in the M_{PD} array to supply more current to the load and then the current from M_{PA} can be reduced to make V_{GA} increase. Similarly, when V_{GA} is too high and close to V_{DD}, which means that the current provided by M_{PA} is too small, the digital controller will then turn OFF one transistor in the M_{PD} array to reduce the current to the load. Then, the current from M_{PA} is required to increase, and this is done by a smaller V_{GA}. Finally, V_{GA} will settle to a suitable value in the steady state.

For the circuit implementation and the operation details of each block used in the proposed HLDO, they will be covered in the following sections.

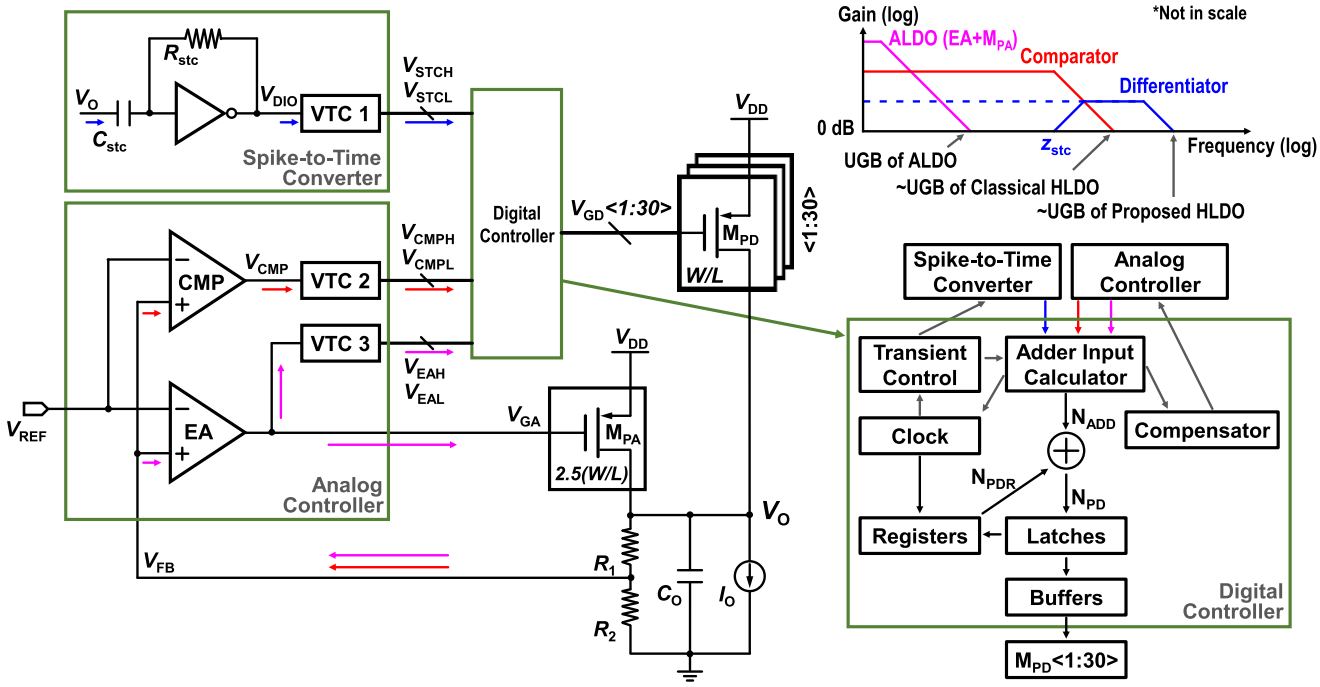


Fig. 2. Overall structure of the proposed HLDO (left) and concept of loop-bandwidth extension of the proposed HLDO (top right).

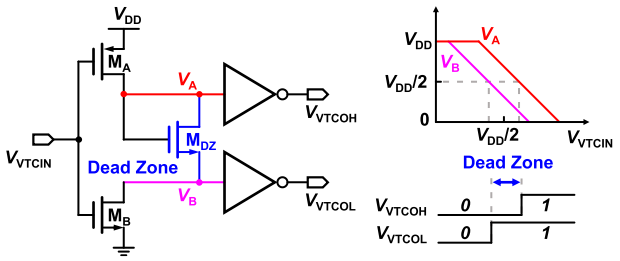


Fig. 3. Schematics of VTC and relationships among V_A, V_B, V_{VTCOH}, V_{VTCOL}, and V_{VTCIN}.

B. Voltage-to-Time Converter

The proposed VTC is used to convert the analog comparison results into digital signals. As shown in Fig. 3, M_A and M_B are used as the input stage, while M_{DZ} is added to create a dead-zone region. V_A and V_B vary with the input of VTC (i.e., V_{VTCIN}), and $|V_A - V_B|$ is roughly a constant value, which is normally close to and larger than the threshold voltage of M_{DZ}. When V_{VTCIN} is within the dead-zone region, $V_B < V_{DD}/2$ and $V_A > V_{DD}/2$. Hence, V_{VTCOH} and V_{VTCOL} are driven by the inverters and become LOW and HIGH, respectively. When V_{VTCIN} is higher than the dead-zone region, V_{VTCOH} flips its value and becomes HIGH. Similarly, when V_{VTCIN} is lower than the dead-zone region, V_{VTCOL} becomes LOW. As a result, the input range of V_{VTCIN} is separated into three regions automatically. Then, V_{VTCOH} and V_{VTCOL} indicate the exact region in which V_{VTCIN} is currently located. To adjust the range of the dead-zone region, the size of M_{DZ} is carefully selected, and the PVT simulations of the whole HLDO have proven that the VTC functions properly within the operation ranges of PVT.

C. Analog Controller

The analog controller, as shown in Fig. 2, is mainly constructed by ring-amplifier-based circuits, including an EA and a comparator. The output of the comparator (V_{CMP}) is directly used to reflect the comparison result of V_{FB} and V_{REF}. V_{CMP} is also connected to a VTC to generate V_{CMPH} and V_{CMPL}, which indicate whether V_{FB} is within a small range of around V_{REF} or not. Similarly, V_{GA} is connected to another VTC to generate V_{EAH} and V_{EAL}, which indicate the voltage level of V_{GA}. The digital signals are then utilized by the digital controller to decide the number of turned-ON transistors in the M_{PD} array.

The EA and M_{PA} are the main components of the proposed ALDO, which is working continuously and independently in the proposed HLDO circuit. The structure of the proposed ALDO is illustrated in Fig. 4. The EA is constructed by the amplification part to compare V_{FB} with V_{REF} and the compensation part to ensure stability. The amplification part consists of a common-mode feedback (CMFB) circuit and a ring amplifier. The first stage of the ring amplifier is formed by M_{01}–M_{08}, and the second one is formed by M_{09}–M_{12}. M_{PA} functions as the third stage. Similar to the proposed VTC, M_{05}–M_{08} are utilized to create a dead-zone region, where the ring amplifier will lock in when it is settling, and thus, the stability is improved. Compared with the resistors in the classical ring-amplifier designs, the usage of MOSFETs enjoys the advantage of its insensitivity to the PVT variations [22]. Both pMOSFETs and nMOSFETs are used to reduce the effects of varying threshold voltage at different corners. By adjusting the sizes of these dead-zone MOSFETs, tradeoffs among gain, UGB, and stability are minimized. Low-threshold devices are employed for M_1–M_{12} to extend the voltage headroom and obtain a larger loop gain at the ultralow V_{DD}. The CMFB circuit

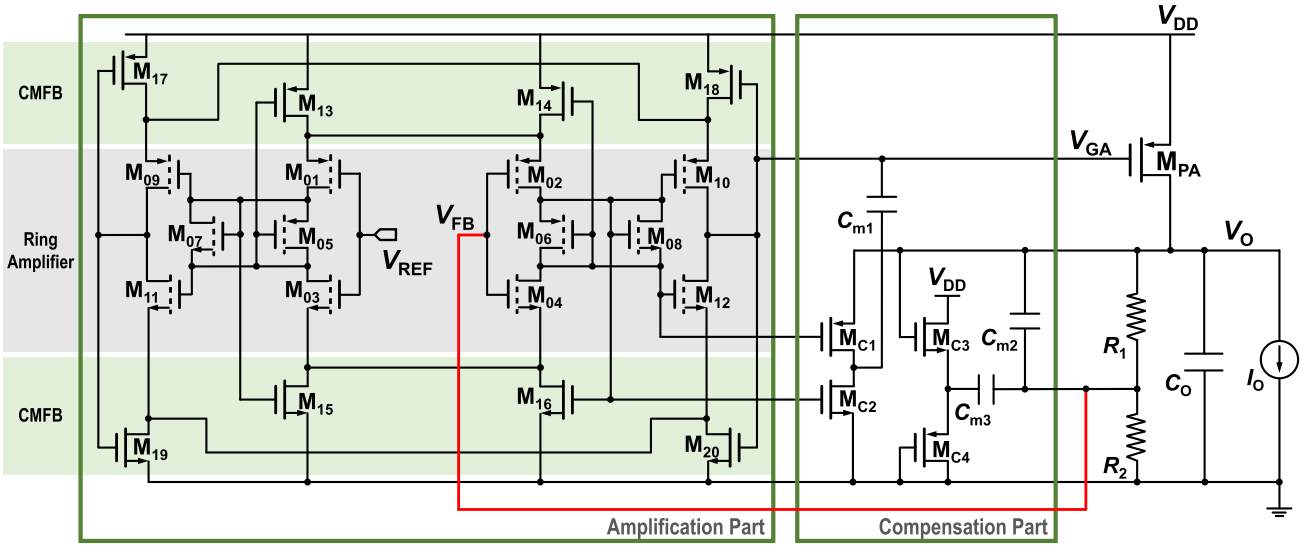


Fig. 4. Schematics of the proposed ALDO.

includes two pairs of MOSFETs (i.e., the top and bottom parts in the amplification part), which detect the differential output of the first and second stage of the ring amplifier and then coarsely set the common-mode range [23]. Moreover, due to the small sizes of M_{13}–M_{20}, the current flow in the amplification part is limited, and thus, a lower I_Q design is achieved. Due to the OCL structure of the proposed ALDO, the pole at V_O moves to a high frequency. Therefore, the poles generated at the nodes at $V_{\rm FB}$, V_{GA}, and V_O are all located at high frequencies, resulting in severe stability problems. To solve these problems, in this design, both the pole–zero cancelation and Miller compensation are adopted.

To analyze the loop-gain transfer function of the proposed ALDO, the corresponding small-signal model is illustrated in Fig. 5. G_{m1}, G_{m2}, G_{mp}, R_{O1}, R_{O2}, R_O, C_{O1}, C_{O2}, and C_O are the transconductance, equivalent output resistance, and lumped output capacitance of the three stages of ring amplifier and C_{i1} is the input capacitance of the first amplification stage, for simplification, assuming that the pMOSFETs used in the ring amplifier have the same small-signal parameters [i.e., transconductance (g_m) and output resistance (r_o)] as the nMOSFETs. M_{C1} and M_{C2} and a compensation capacitor of C_{m1} form a feedforward path from the output of the first stage to the node at V_{GA}, and a feedback path from the node at V_O to V_{GA}. The transconductances of these two paths are $-G_{m3}$ and $G_{m3}/2$, respectively, assuming that M_{C1} and M_{C2} have the same g_m. The output resistance and capacitance are R_{O3} and C_{O3}. C_{m2} with R_1 and R_2 are used to create a high-pass network [24]. C_{m3} provides another fast path from the node at V_O to $V_{\rm FB}$. The transconductance and output resistance of the common-drain amplifier formed by M_{C3} and M_{C4} are G_{m4} and R_{O4}, respectively, with $R_{O4} \approx 1/G_{m4}$. To obtain the transfer function of the proposed ALDO, several assumptions are made as follows.

1) To simplify the analysis, the small-signal model is divided into two parts by V_O. Hence, $C_{m2} << C_O$ is required.

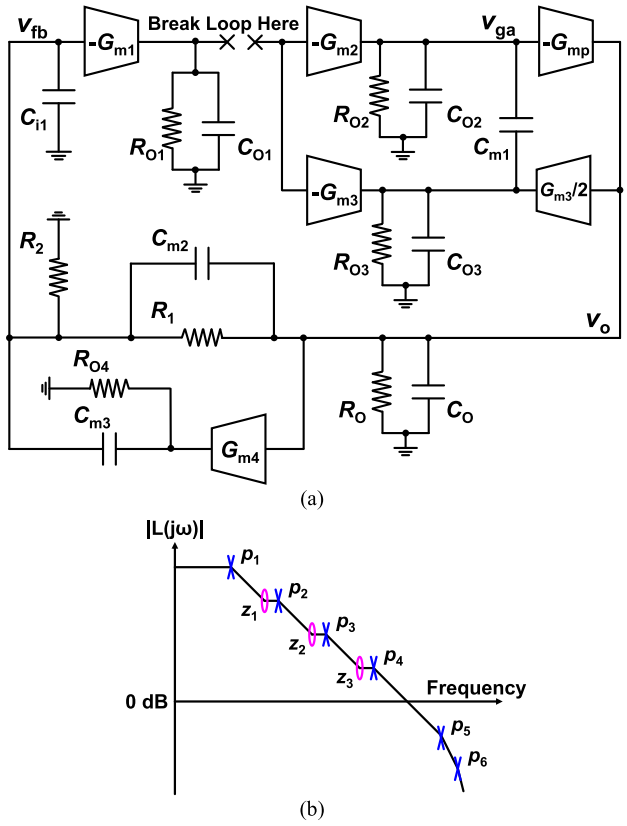


Fig. 5. (a) Small-signal model and (b) bode plot of the proposed ALDO.

2) $C_{O3} << C_{m1}$ so that C_{O3} is ignored in the analysis.
3) C_{m3} is small (<30 fF) and, hence, no complex pole is generated.
4) $C_{m2} << C_O$; $C_{i1} << C_{m2}$, $C_{i1} << C_{m3}$; $R_{O4} << R_1$; and $R_{O4} << R_2$.

The evaluation result shows that the ALDO is a system with six poles and three zeros, given as follows:

$$T(s) = -A_{\mathrm{DC}} \frac{\left(1-\frac{s}{z_1}\right)\left(1-\frac{s}{z_2}\right)\left(1-\frac{s}{z_3}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)\left(1-\frac{s}{p_3}\right)\left(1-\frac{s}{p_4}\right)\left(1-\frac{s}{p_5}\right)\left(1-\frac{s}{p_6}\right)} \quad (1)$$

where the dc gain is defined by the amplification part and the feedback resistors given by

$$A_{\mathrm{DC}} = -G_{m1}G_{m2}G_{mp}R_{o1}R_{o2}R_o\left(\frac{R_2}{R_1+R_2}\right). \quad (2)$$

Due to the Miller effect, the original dominant pole (p_1) located at the node at V_{GA} is moved to a lower frequency, while the second pole (p_2) at the node of V_O is moved to a higher frequency. The equations of p_1 and p_2 are given as follows:

$$p_1 = -\frac{1}{\left(C_{m1}+C_{o2}+\frac{1}{2}C_{m1}G_{m3}G_{mp}R_{o3}R_o\right)R_{o2}} \quad (3)$$

$$p_2 = -\frac{\left(C_{m1}+C_{o2}+\frac{1}{2}C_{m1}G_{m3}G_{mp}R_{o3}R_o\right)}{\left(C_oC_{o2}\right)R_o}. \quad (4)$$

There are another four parasitic poles, and they are as follows:

$$p_3 = -\frac{1}{\left(C_{m2}+C_{m3}\right)\left(R_1//R_2\right)} \quad (5)$$

$$p_4 = -\frac{C_{m2}+C_{m3}}{C_{m2}C_{m3}R_{o4}} \quad (6)$$

$$p_5 = -\frac{1}{C_{o1}R_{o1}} \quad (7)$$

$$p_6 = -\frac{1}{C_{m1}R_{o3}} \quad (8)$$

where p_5 and p_6 are the high-frequency poles as R_{O3} and C_{O1} are small. The feedforward path of C_{m1} generates a left-half-plane (LHP) zero of

$$z_1 = -\frac{1}{C_{m1}R_{o3}\left(1+\frac{G_{m3}}{G_{m2}}\right)}. \quad (9)$$

Since $G_{mp}R_OG_{m2}R_{O2} >> 1$, z_1 locates at a frequency higher than p_1. Even though C_{m1} is desired to be small to avoid the generation of complex poles and to move p_6 to a high frequency, a relatively larger C_{m1} is also needed to separate p_1 and p_2. As a result, $C_{m1} = 27$ fF is chosen. In this case, z_1 is close to p_2 to cancel each other.

The introduction of C_{m2} and the signal path containing C_{m2} altogether generate another two LHP zeros as follows:

$$z_2 = -\frac{1}{\left(C_{m2}+C_{m3}G_{m4}R_{o4}\right)R_1} \quad (10)$$

$$z_3 = -\frac{\left(C_{m2}+C_{m3}G_{m4}R_{o4}\right)}{C_{m2}C_{m3}R_{o4}}. \quad (11)$$

Since R_1 and R_2 are in the same order of magnitude, and $R_{O4} \approx 1/G_{m4}$, z_2 is close to p_3. Similarly, z_3 is close to p_4. Because of the Miller effect and the pole–zero cancelation technique, the whole system can be viewed as a system with one dominant pole of p_1 and two parasitic poles of p_5 and p_6, which are located at high frequencies. Fig. 5(b) shows the bode plot of the ALDO. The theoretical phase margin of the proposed ALDO is approximately 90°. Postlayout simulations at different PVT corners are conducted. As shown in Fig. 6(a), the proposed ALDO has a minimum phase margin above 40°. In most cases, the phase margin is larger than 60°. The UGB of the ALDO, as illustrated in Fig. 6(b), which achieves as high as a hundred of MHz at $V_{DD} = 1$ V, implies that the ALDO is able to respond fast to a small change of I_O. Moreover, according to the simulation results and to be further proven by experimental results, the proposed ALDO structure designed in the 65-nm CMOS process, as shown in Fig. 4, can operate at as low as 0.5 V.

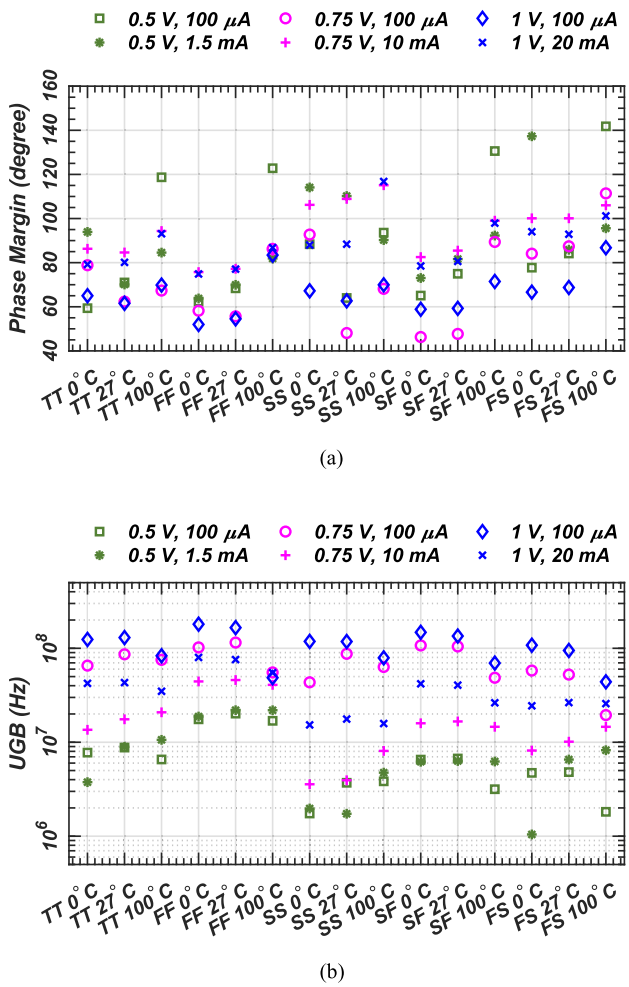
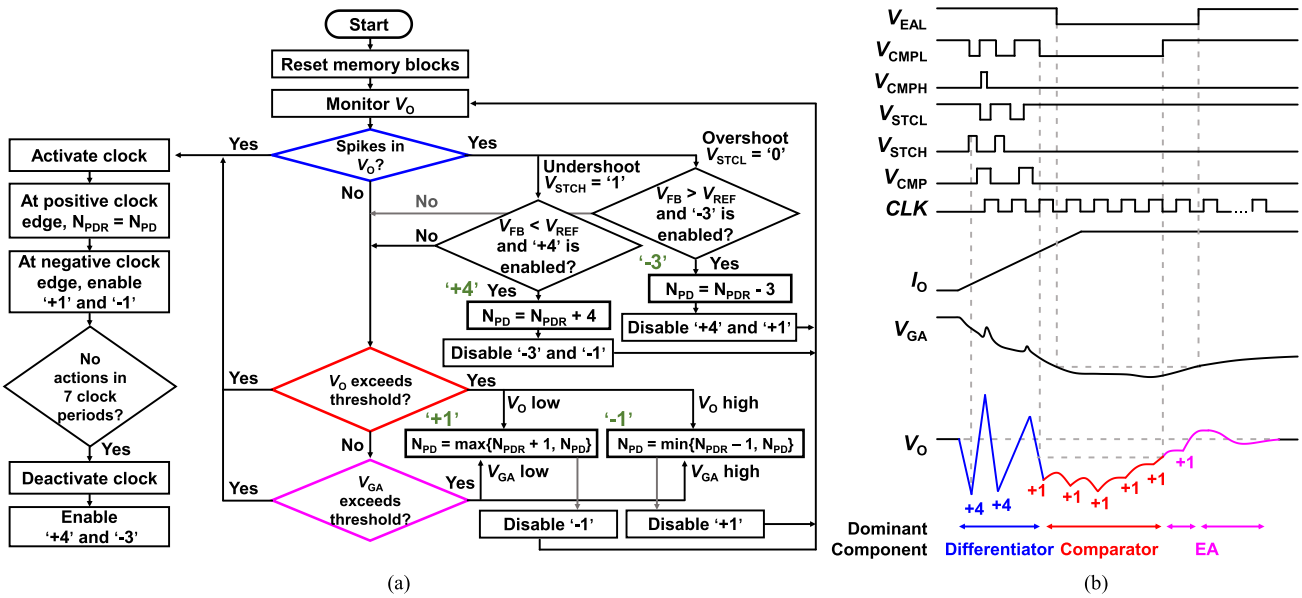


Fig. 6. Simulated (a) phase margins and (b) UGBs of the proposed ALDO at different PVT corners: Typical–Typical (TT), Fast–Fast (FF), Slow–Slow (SS), Slow–Fast (SF), and Fast–Slow (FS) for nMOSFET and pMOSFET.

To enable the operation of the proposed HLDO at V_{DD} close to 0.5 V, the comparator in the analog controller, having a similar structure to the second stage of the EA, consists of a CMFB circuit with only one pair of MOSFETs and two inverters as the amplification stage, of which the inputs are V_{FB} and V_{REF}.



(a) (b)

Fig. 7. (a) Flowchart of algorithm used in the proposed HLDO. (b) Transient response of the HLDO.

D. Digital Controller

As demonstrated at the bottom-right corner of Fig. 2, the digital controller is constructed by an adder, an adder input calculator, an event-driven clock, a transient control circuit, a compensator, latches, registers, and buffers. The adder input calculator takes the signal inputs from the STC and analog controller, and it outputs a value of N_{ADD}. N_{ADD} refers to the number of transistors in the M_{PD} array that should be turned ON in the current clock period, and it is negative when there are transistors in the M_{PD} array that need to be turned OFF. The registers are to store the total number of turned-ON transistors in the M_{PD} array (N_{PDR}) in the previous clock edge. The adder sums N_{PDR} with N_{ADD} and then outputs the final number of turned-ON transistors in the M_{PD} array (N_{PD}) to subsequently set/reset the latches, which directly control the M_{PD} array through buffers.

Fig. 7(a) shows the flowchart of the algorithm used in the digital controller. An external reset signal is applied to reset the registers at the initial stage and N_{PDR} is reset when the reset signal arrives. A clock signal is generated by an embedded clock, which is activated by the STC and analog controller and deactivated when there is no action taken by the digital controller in seven clock periods. The embedded clock is a ring-oscillator-based clock with a maximum frequency of 0.9 GHz. At the positive clock edge, N_{PDR} is updated to the value of N_{PD}. There are four actions that are conducted by the digital controller, which are "+4," "−3," "+1," and "−1," respectively. The plus and minus signs represent turning ON and OFF transistors in the M_{PD} array, respectively. The subsequent number is the number of transistors in the M_{PD} array involved in these actions (i.e., ΔN_{PD}).

When there is a voltage spike, the STC distinguishes the steep slope of V_O and triggers two signals, V_{STCH} and V_{STCL}. If V_{STCH} is HIGH, it means that V_O is decreasing rapidly. Then, V_{CMP} is checked. When $V_{\mathrm{FB}} > V_{\mathrm{REF}}$, the HLDO is undergoing regulation and no action is taken. When $V_{\mathrm{FB}} < V_{\mathrm{REF}}$, it indicates that there is an abrupt increase of I_O to cause V_O to drop instantaneously. Therefore, the action "+4" is applied and four transistors in the M_{PD} array are turned ON immediately. To prevent conflict, the "−3" action is disabled, until the clock is deactivated again. A similar situation happens when V_{STCL} is LOW (i.e., V_O is increasing speedily).

If the HLDO has already been regulated by the STC, but there is still a great difference between V_O and the desired output value, the analog controller informs the digital controller by V_{CMPH} and V_{CMPL}. Simultaneously, when V_{GA} is close to V_{DD} or the ground, V_{EAH} and V_{EAL} will deliver this information to the digital controller. In both cases, one more transistor in the M_{PD} array is turned ON/OFF. It is noted that, within one clock period, if a "+" action is employed, the "−" action will be disabled until the next clock period arrives, and vice-versa.

To enable a stable performance, two extra signals, *RVG* and *ENB*, are generated by a transient control circuit, which is not shown in the flowchart. *RVG* is normally HIGH and becomes LOW in two cases: there are (a) more than 15 clock periods, or (b) more than 7 clock periods before another output spike is detected by the STC. If *RVG* is LOW, the change of V_{STCH} and V_{STCL} is not counted by the digital controller. After V_{STCH} and V_{STCL} return to their normal values, which are defined by VTC with operations stated in Fig. 3, *RVG* starts to recover to HIGH by a small charging current. *ENB* is normally HIGH and becomes LOW when V_{CMP} changes its direction during the time when *RVG* is LOW. If *ENB* is LOW, V_{CMPH} and V_{CMPL} are not considered by the digital controller. *ENB* becomes HIGH, when *RVG* recovers to HIGH.

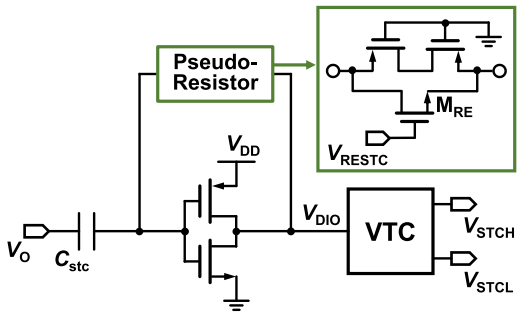


Fig. 8. Schematics of the proposed STC.

A compensator is added to reduce the sudden current gain caused by a "+" and "−" action. When there is a "+" action and $V_{\rm FB} > V_{\rm REF}$, a small pMOSFET connects V_{GA} to V_{DD} to increase the discharging time of V_{GA} and, thus, reduce the instant current gain of the "+" action. Similarly, a small nMOSFET is used to discharge V_{GA} when a "−" action arrives and $V_{\rm FB} < V_{\rm REF}$.

The transient response of the proposed HLDO with a sudden increase of I_O is illustrated in Fig. 7(b). The STC detects a voltage spike induced by the load-current change, and the digital controller applies the action of "+4" immediately. With certain delay, the clock is activated and $N_{\rm PDR}$ is updated. At this moment, N_{PD} maintains its value stored in the latches, and no action is conducted until another undershoot happens and $V_{\rm STCH}$ goes to HIGH again. During this process, the compensator charges V_{GA} when $V_{\rm FB} > V_{\rm REF}$. After two clock periods, the slope of V_O is too small to be distinguished by the STC. Since $V_{\rm FB} < V_{\rm REF}$ and $|V_{\rm FB} - V_{\rm REF}|$ is large, $V_{\rm CMPL}$ is LOW to conduct the action of "+1" and then returns to HIGH after another five clock periods. The regulation process continues, as $V_{\rm EAL}$ is still LOW due to the voltage level of V_{GA} and, thus, another "+1" action is employed. After that, V_O is finally regulated by the ALDO. According to the aforementioned process, the ratio of I_O provided by M_{PA} and the M_{PD} array is automatically decided.

E. Spike-to-Time Converter

The schematic of the STC, as illustrated in Fig. 8, includes a VTC and a differentiator with input capacitance ($C_{\rm stc}$) of 65 fF. The differentiator is sensitive to voltage spikes and enhances the transient performance to a great extent, while the VTC ignores small spikes to avoid over-regulation. Back-to-back pseudoresistors with an equivalent resistance of $R_{\rm stc}$, which are constructed by two low-$V_{\rm TH}$ pMOSFETs, are used as the feedback resistor of the differentiator. The zero ($z_{\rm stc}$), as shown in Fig. 2, can be adjusted by $C_{\rm stc}$ and $R_{\rm stc}$, and it is desired to be lower than the bandwidth of the EA and the comparator. Thus, the transient response of the HLDO covers a continuous frequency range. In slow corners, $R_{\rm stc}$ increases and moves $z_{\rm stc}$ to a low frequency. Hence, the output ripples generated due to the switching of M_{PD} are detected by the differentiator, which triggers $V_{\rm STCH}$ and $V_{\rm STCL}$. As a result, the recovery time of *RVG* is a few microseconds, and the HLDO is hard to respond to a series of load-current changes in a short time. Hence, $M_{\rm RE}$ is added to move $z_{\rm stc}$ to a higher frequency during the time when the STC is disabled by *RVG*. With the insertion of $M_{\rm RE}$, the recovery time of *RVG* is reduced to 200–400 ns in various PVT cases. The control signal $V_{\rm RESTC}$ is generated by the digital controller.

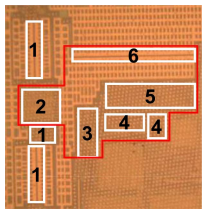
TABLE I
COMPARISONS OF SIMULATED OPEN-LOOP UGBS OF THREE REGULATION PATHS IN THE PROPOSED HLDO

Supply	0.5 V	1 V
ALDO	9 MHz	0.13 GHz
Comparator	194 MHz	5 GHz
Differentiator	504 MHz	21 GHz

Since there is no comparison of the dc voltage levels in a differentiator, a single-input single-output amplifier is qualified. Therefore, a two-transistor inverter is employed, and it occupies a small chip area. The inverter is a single-pole circuit, which means that no extra design efforts on compensation are needed. Moreover, since there are only two stacked transistors, the inverter is able to function properly even when the supply is ultralow. The simulated open-loop UGBs of the three regulation paths in the proposed HLDO are presented in Table I. The differentiator achieves an open-loop UGB of 21 GHz at 1-V supply and 504 MHz at 0.5-V supply, respectively. The UGB is 2.6–4.2 times when compared with the comparator and is 56–162 times when compared with the ALDO. Although this comparison does not include the delays of the digital controller and the buffers for the comparator and differentiator paths, it is still valid to prove the loop-bandwidth enhancement by the STC (i.e., the differentiator path) since the delays of the digital circuits and buffers are small in the used 65-nm CMOS technology. Thus, the transient speed of the HLDO is enhanced significantly by the proposed STC.

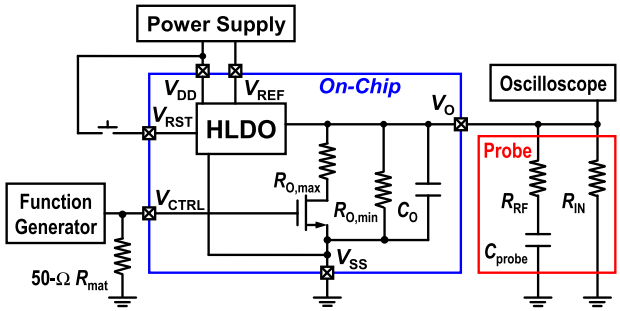
III. MEASUREMENT RESULTS

As mentioned before, the proposed HLDO was fabricated in a 65-nm CMOS process. The previously presented overall structure of the proposed HLDO (in Fig. 2), STC (in Fig. 8), VTC (in Fig. 3), ALDO (in Fig. 4), voltage comparator (explained in Section II-C), and digital part is all able to operate at a supply as low as 0.5 V, which is slightly above the regular $V_{\rm TH}$ of ∼0.45 V. The chip microphotograph of the proposed HLDO is shown in Fig. 9(a). The LDO occupies a total area of 0.0302 mm^2, with an active area of 0.0185 mm^2, including an on-chip output capacitor of 4.1 pF. The total capacitance of the LDO is 4.4 pF. The measurement setup is demonstrated in Fig. 9(b). An on-chip loading transistor is embedded in series with a 1-Ω loading resistor (i.e., $R_{O,\rm max}$). An external signal ($V_{\rm CTRL}$), which is provided by a function generator, controls the ON-resistance of the loading transistor to control the overall load resistance. The edge time of I_O is adjusted by changing the edge time of $V_{\rm CTRL}$. A 9-kΩ output resistor (i.e., $R_{O,\rm min}$) is embedded in parallel with



Load Circuits			
Proposed HLDO	1	Loading Resistors and MOSFETs	0.0035 mm²
	2	C_o	0.0024 mm²
	3	Analog Circuits	0.0015 mm²
	4	Digital Circuits	0.0042 mm²
	5	Registers and Buffers	0.0066 mm²
	6	Power MOSFETs	0.0038 mm²
		Total Area	0.0302 mm²

(a)



(b)

Fig. 9. (a) Chip microphotograph. (b) Setup for transient-response measurement of the proposed HLDO.

the loading MOSFET to define the minimum load. To reduce the reflection effect and get a clean pulse signal for $V_{\rm CTRL}$, a 50-Ω resistor (i.e., $R_{\rm mat}$) is connected between $V_{\rm CTRL}$ and the ground. The capacitance (i.e., $C_{\rm probe}$) and the resistance (i.e., $R_{\rm RF}$ and $R_{\rm IN}$) of the probe used in the measurement are 0.8 pF, 80 Ω, and 1 MΩ, respectively.

Fig. 10 illustrates the measured load transient waveforms to sudden load-change events. For the case that $V_{DD} = 1$ V, and V_O is regulated at 0.9 V, when I_O changes between 100 μA and 300 mA within an edge time ($t_{\rm edge}$) of 5 ns, the maximum undershoot and overshoot are 142 mV and 186 mV, respectively, and the corresponding recovery times are 17 ns and 44 ns, respectively. Due to the parasitic inductance of the bond wires connecting the chip between the power supply and the HLDOs input, the overshoot exceeds V_{DD} slightly during the 5-ns rising and falling of the I_O-step. When the edge time of the I_O-step increases to 20 ns, the effects of the bond-wire inductance are mild. The undershoot and overshoot are reduced to 65 mV and 91 mV, respectively, and the corresponding recovery times are ∼48 ns. Moreover, the proposed HLDO is experimentally proven to function properly at $V_{DD} = 0.5$ V. At $V_{DD} = 0.5$ V and $V_O \approx 0.45$ V with I_O-step between 50 μA and 30 mA within 20 ns, the corresponding undershoot and overshoot are 246 mV and 64 mV, respectively. It is noted that the maximum I_O of the HLDO is 300 mA when $V_{DD} = 1$ V and $V_{\rm DO}$ is 100 mV. It becomes 30 mA when $V_{DD} = 0.5$ V and $V_{\rm DO} = 50$ mV. This situation is normal since a smaller V_{SG} and V_{SD} of the power pMOSFET for the analog and digital part result in a small I_{SD}. In the zoom-in views of V_O for the cases of $V_{DD} = 1$ V and 0.5 V (on the left of Fig. 10), they prove the proposed regulation mechanism, as presented in Section II. The proposed STC activates to undergo the "+4" operation such that more transistors in the M_{PD} array are turned ON to supply more I_O to reduce the drop of V_O. Then, both the comparator and EA in the analog controller dominate the regulation to carry out the "+1" action and the adjustment of V_{GA}. Finally, the ALDO composed of the EA and M_{PA} performs the rippleless regulation. Fig. 11 demonstrates the load transient response when I_O changes within the full load-current range. The proposed HLDO is able to respond to $t_{\rm edge}$ of 3 ns even though the supply is close to the threshold voltage (i.e., $V_{DD} = 0.5$ V).

Fig. 12 shows the measured load transient responses with the minimum achievable $V_{\rm DO}$ (i.e., $V_{\rm DO(min)}$) at $V_{DD} = 1$ V, as shown in Fig. 12(a), and $V_{DD} = 0.5$ V, as shown in Fig. 12(b), with $t_{\rm edge}$ of 10 ns. It is noted that, at $V_{DD} = 1$ V and $V_{\rm DO(min)} = 50$ mV, the test range of I_O is between 106 μA and 178 mA. When $V_{DD} = 0.5$ V and $V_{\rm DO(min)} = 20$ mV, the test range of I_O is between 53 μA and 14 mA.

Fig. 13 summarizes the measured load regulations at $V_{DD} =$ 0.5–1 V and $V_{\rm DO} = 50$ mV. The proposed HLDO has a minimum load regulation of 0.038 mV/mA at $V_{DD} = 0.6$ V. The measured current efficiency of the proposed HLDO is shown in Fig. 14. It shows that the proposed HLDO achieves 99.99% when $V_{DD} =$ 0.5 V and $I_O = 25$ mA.

Fig. 15 shows the measured line transient responses. When $V_O = 0.45$ V, and V_{DD} changes with a step of 50 mV in 20 ns, the spikes at V_O are within 30 mV. When $V_O = 0.9$ V, the spikes at V_O are within 10 mV. The measured power supply rejection ratio (PSRR) is −17.65 dB and −16.53 dB at 1 kHz and 1 MHz, respectively, when $V_{DD} = 1$ V and $V_O = 0.9$ V.

Table II summarizes the measured performances of the proposed HLDO and compares the proposed design with the state-of-the-art reported in the past four years. The measured I_Q of the proposed HLDO is 21.7 μA at $V_{DD} = 0.5$ V and is 316 μA at $V_{DD} = 1$ V because of the change of steady-state current of the ring amplifiers and STC. The well-accepted figure-of-merit (FoM) used in [17]

$$\text{FoM}_1 = C_{\text{total}} \cdot \left(\frac{\Delta V_O}{\Delta I_O}\right) \cdot \left(\frac{I_Q}{\Delta I_O}\right) \tag{12}$$

is adopted to compare the transient performance of the LDOs. When considering the area efficiency, another FoM in [25]

$$\text{FoM}_2 = C_{\text{total}} \cdot \left(\frac{\Delta V_O \cdot I_Q}{I_{O,\text{max}}^2}\right) \cdot \text{Area} \tag{13}$$

is applied. However, the minimum I_O in the transient, which contributes to the gain of M_{PA} and the location of the pole at V_O, should be emphasized. Moreover, since the response time of the OCL LDOs is normally smaller than $t_{\rm edge}$, the voltage spike induced by the charging and discharging mechanisms of C_O is decided by the slope of the I_O-step. Hence, $t_{\rm edge}$ becomes an essential parameter that should be involved in the FoM. With these two considerations, the FoM proposed

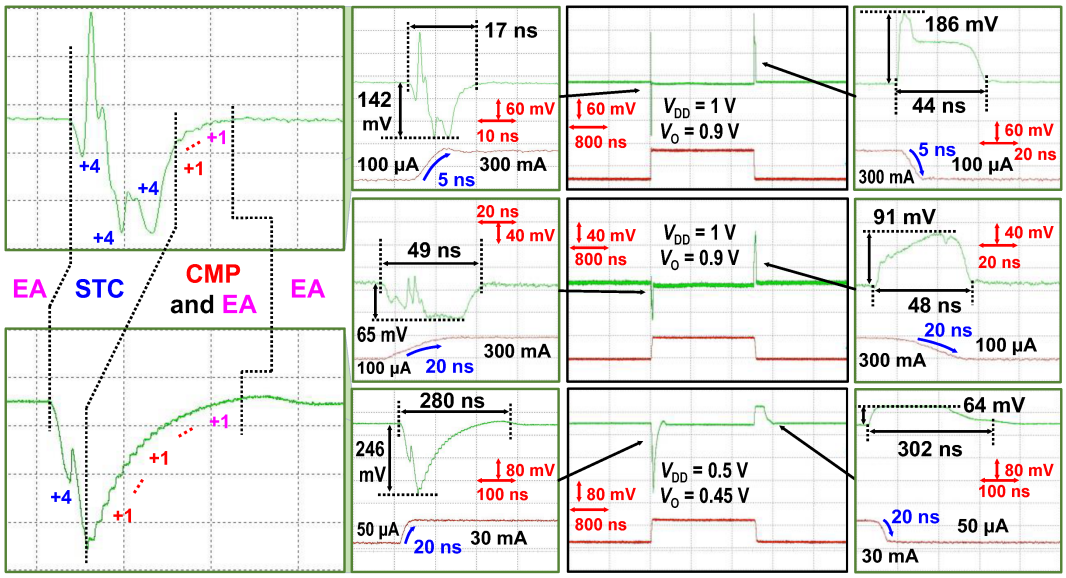


Fig. 10. Measured load transient responses at $V_{DD} = 1$ V and $V_{DD} = 0.5$ V, where I_O changes between 100 μA and 300 mA for $V_{DD} = 1$ V, as well as between 50 μA and 30 mA for $V_{DD} = 0.5$ V.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	ISSCC'20 [17]	JSSC'20 [13]	JSSC'21 [19]	JSSC'22 [14]	JSSC'22 [21]	This work
CMOS Process	40 nm	65 nm	65 nm	28 nm	65 nm	65 nm
Topology	Analog	Digital-LDO-like	DA-ALDO	Switching	Hybrid	Hybrid
External-Clock-Free	NO	NO	YES	YES*	YES	YES
Output Ripple-Less	YES	NO	YES	NO	YES	YES
Active Area [mm^2]	0.0057	0.0400	0.3600	0.0479	0.0790	0.0185
C_{Total} [pF]	90	42	250	5000	120	4.4
V_{DD} [V]	0.4–1.2	0.5–1	1.2	0.6–1	0.6–1.2	0.5–1
V_O [V]	0.2–1.18	0.45–0.95	0.6–1.15	0.5–0.9	0.55–1.18	0.45–0.95
Maximum I_O [mA]	400	105	500	1500	250	300
I_Q [µA]	4.4–1280	4.9	120	1800	15.4–152	21.7–316
Minimum V_{DO} [mV]	20	50	50	90	20	20
t_{edge} [ns]	10	10	100	10	0.5	5
Min. I_O in transient [mA]	0.21	5	50	200	24	0.1
Max. I_O in transient [mA]	1.25	105	500	1200	104	300
Voltage spike ΔV_O [mV] @(V_{DD}/V_O [V])	78 @(0.4/0.35)	88 @(0.6/0.5)	55 @(1.2/N.A.)	70 @(1/0.75)	76 @(1.2/1.18)	142 @(1/0.9)
Settling Time [ns]	500	103	220	N.A.	56	17
FoM$_1$ [fs]	28558	1.81	8.15	630	216.60**	2.05
FoM$_2$ [fs·mm^2/A]	112.68	0.07	2.38	20.96	10.13	0.04
FoM$_3$ [mV]	321.60	88.09	1225	282.52	22.94	1.97

Remarks: * A 500-MHz triangle wave is needed.
** Use the maximum I_Q for calculation.

in [26]

$$\text{FoM}_3 = K \cdot \frac{\Delta V_O \cdot (I_Q + I_{O,\min})}{\Delta I_O} \tag{14}$$

is also used for comparison in this article, where K is the edge-time ratio defined by

$$K = \frac{t_{\text{edge}} \text{ of the compared work}}{\text{The smallest } t_{\text{edge}} \text{ in the comparison table}}. \tag{15}$$

A small value of all three FoMs in (12)–(14) implies a better performance of LDO. Compared with other designs in Table II, the proposed HLDO achieves nearly the smallest values for all three FoMs, which means that it has a faster transient response against a large I_O range and high area efficiency. The design in [13] has a slightly better FoM$_1$ than the proposed HLDO, but it requires a large minimum I_O to obtain good transient

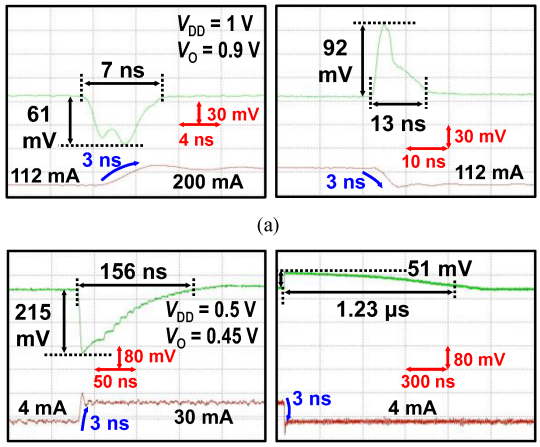


Fig. 11. Measured load transient responses at (a) $V_{DD} = 1$ V and (b) $V_{DD} = 0.5$ V, when I_O is changing within the full load-current range.

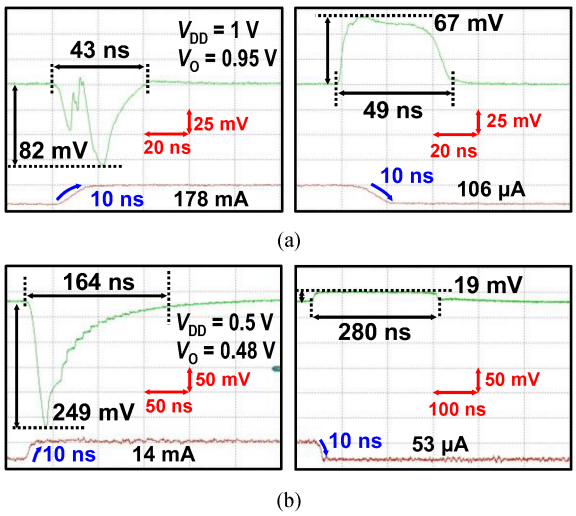


Fig. 12. Measured load transient response with minimum V_{DO} at (a) $V_{DD} = 1$ V and (b) $V_{DD} = 0.5$ V.

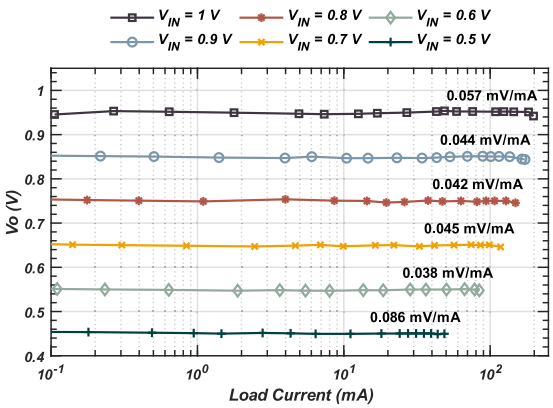


Fig. 13. Measured load regulations at $V_{DD} = 0.5$–1 V with $V_{DO} = 50$ mV.

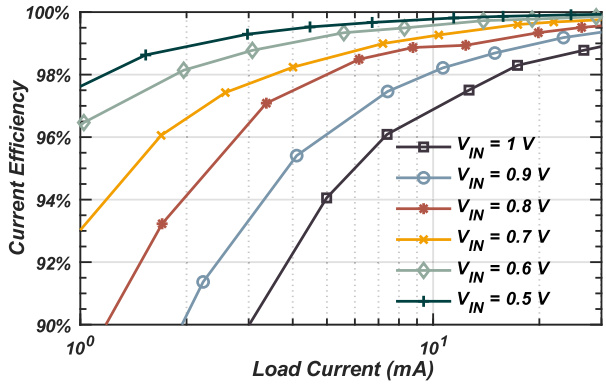


Fig. 14. Measured current efficiency of the proposed HLDO at $V_{DD} = 0.5$–1 V with $V_{DO} = 50$ mV.

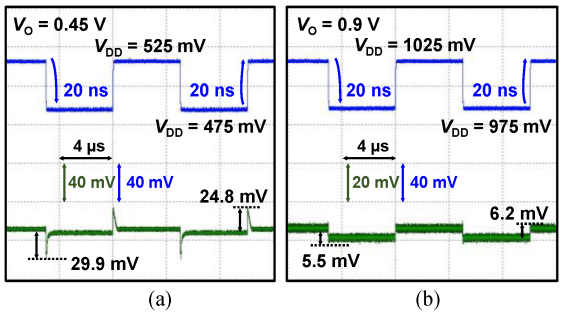


Fig. 15. Measured line transient responses when V_O is set to be (a) 0.45 V and (b) 0.9 V.

performance and, thus, its FoM_3 is much poorer than the proposed HLDO. In addition, the proposed HLDO benefits from a clock-free and rippleless regulation.

IV. Conclusion

A fully integrated OCL HLDO has been reported in this article. The proposed structure with a dual-loop control has been presented, and the circuit implementation of the proposed structure has also been explained in detail. The contributions to the design of HLDO are as follows:

1) loop-bandwidth enhancement by the proposed STC and control algorithm;
2) maintaining voltage regulation even when the supply is close to the threshold voltage of the technology by the modified structures of ring-amplified-based EA and comparator, STC, VTC, and digital circuits;
3) more robustness to the PVT variations due to the proposed VTC structure;
4) rippleless output.

Appendix

The purpose of the Appendix is to provide the simulated transient responses of the proposed HLDO at different PVT

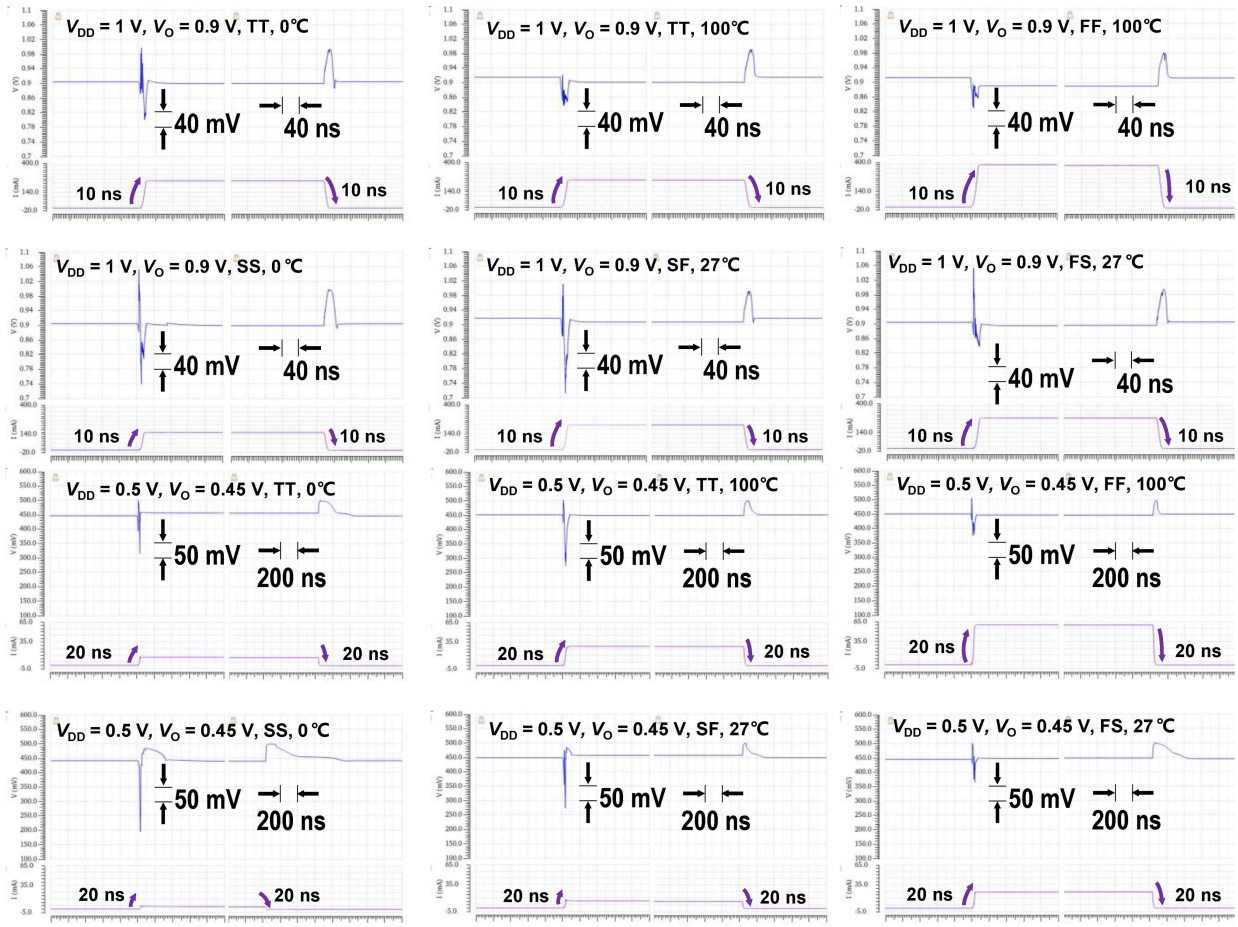


Fig. 16. Simulated transient responses of the proposed HLDO at different PVT corners.

corners. As shown in Fig. 16, the edge time is 10 ns when V_{DD} = 1 V and 20 ns when V_{DD} = 0.5 V. At V_{DD} = 1 V, V_{CTRL} changes between 0 and 600 mV. At V_{DD} = 0.5 V, V_{CTRL} changes between 0 and 300 mV. The size of the I_O-step varies due to the varying ON-resistance of the loading transistor at different PVT corners.

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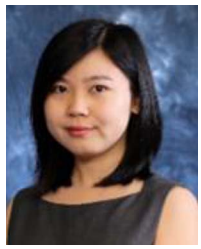

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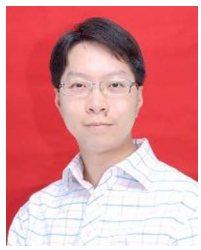

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