Letters

A 3-D Integrated Power Module of GaN HEMTs Based on Silver Sintering Processes

Zezheng Dong, Haidong Yan, Yinxiang Fan, Xinke Wu, *Senior Member, IEEE*, and Junming Zhang, *Senior Member, IEEE*

***Abstract*—A 3-D integrated packaging method is proposed in this letter. Redistributed layers (RDLs) are realized by integrating flexible printed circuit boards (PCBs) onto gallium nitride (GaN) high-electron-mobility transistor (HEMT) dies to enlarge the electrode area and the clearance between them. GaN HEMTs with RDLs are sandwiched between a multilayer PCB and an active metal brazing (AMB) board. Additionally, components like decoupling capacitors, gate driver, digital isolator, and isolated power supply are integrated into this package. Silver sintering processes are employed to maintain consistent processing temperature for multiple interconnections, addressing reliability concerns associated with conventional multi-temperature gradient soldering methods. Furthermore, sintered silver significantly improves both electrical and thermal performances. Power and thermal managements are decoupled by using a PCB and an AMB substrate, resulting in low parasitic inductances, minimal thermal resistance, and electric field shielding. The experiment-measured power loop inductance is as low as 0.54 nH, and the simulated thermal resistance from GaN die to AMB board bottom is only 0.05 °C/W. A detailed description of manufacturing processes, thermal performance test, and dynamic switching performance with circuit-level simulated verification is provided in this letter.**

***Index Terms*—Gallium nitride (GaN), integrated power module (IPM), low parasitic inductance, low thermal resistance, packaging, redistributed layer (RDL), silver sintering.**

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I. Introduction

In RECENT years, gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have firmly established themselves in numerous commercial applications, with consumer power supplies like fast chargers leading the way. According to a report by Yole, the power GaN device market is predicted to be worth $2 billion by 2028, expecting two more growth drivers, automotive and datacom applications [1]. As the market continues to expand, GaN applications will span a wide range of power levels, from several tens of watts to several tens of kilowatts. In high-power applications, it becomes crucial to give special consideration to both parasitic inductance and thermal performance [2].

Various packaging methods from chip-level to module-level for GaN HEMTs have been explored [3]. Among these techniques, the printed circuit board (PCB) embedded package can achieve an extremely low power loop inductance, as low as 0.305 nH [4]. However, thermal conductivity of the dielectric layers in the PCB is poor and the manufacturing steps are too complex and challenging. In [5] and [6], hybrid packages combining conventional direct bonded copper (DBC) or insulated metal substrate (IMS) with a PCB are introduced for repackaging discrete GaN HEMTs. The magnetic flux cancellation effect of the multilayer PCB and high thermal conductivity of DBC (or IMS) are utilized to realize both low parasitic power loop inductance and low thermal resistance. This results in power loop inductance of 2.65 nH and junction-to-heatsink thermal resistance of 2.1 °C/W [5]. The adoption of prepackaged devices leads to an increase in packaging cost and introduces additional thermal resistance. To further enhance the thermal performance, a double-sided cooling (DSC) method is proposed in [7], involving sandwiching GaN HEMT dies between two direct plated copper (DPC) substrates. On top side of the dies, the two copper layers of DPC substrates are connected by vias, forming a small power loop. The power loop inductance and junction-to-case thermal resistance R_{jc} are reduced to 0.94 nH and 0.31 °C/W, respectively. However, as a lateral device, all electrodes of GaN HEMT are distributed on the top side with limited area for thermal dissipation. Besides, extra insulation and thermal interface material (TIM) with low

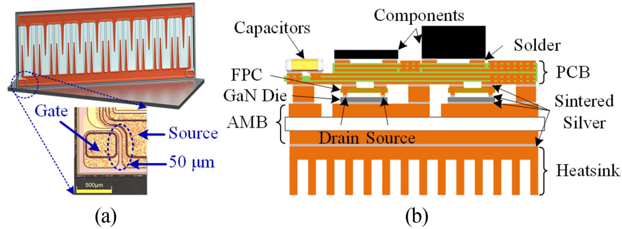

Fig. 1. (a) Clearance between electrodes on GaN HEMTs. (b) Cross-sectional structure of the proposed GaN integrated power module.

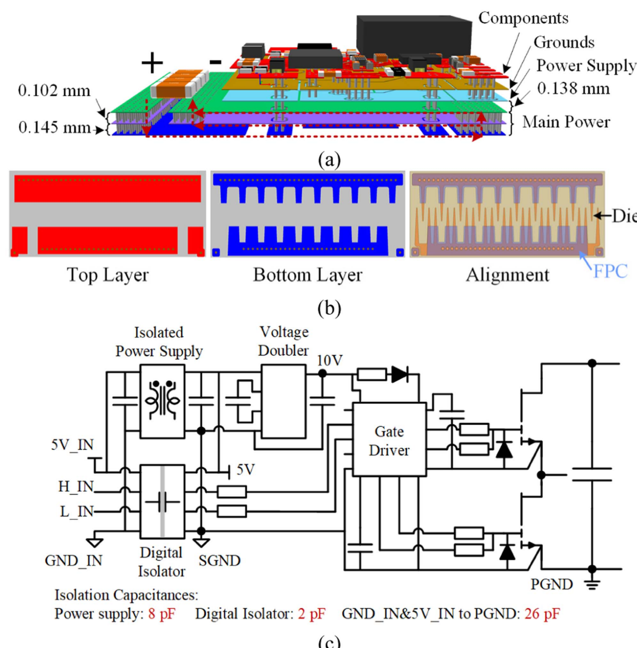

Fig. 2. PCB, FPC, and schematic of GaN IPM. (a) Magnified view of different PCB layers. (b) Layout of FPC and alignment with GaN die. (c) Simplified schematic of GaN IPM.

thermal conductivity are required for the final heatsink assembly. These factors collectively limit the thermal improvement achievable through double-sided cooling. Additionally, the clearance between electrodes is tiny, as shown in Fig. 1(a), with only 50 μm between the gate and source. So, solder overflow during the reflow process may happen, reducing creepage distance or even causing short-circuit issues.

Both the hybrid package and DSC package require multi-temperature gradient soldering processes, necessitating careful selection of solder with different melting point temperatures [8]. Nevertheless, Pb-free high-Sn-content solder alloys have exhibited problems related to void formation, while low melting temperature solders containing bismuth (Bi) have the potential segregation and cracking issues [9]. Recognizing the outstanding attributes of silver sintering technology, which include high thermal conductivity and reliability, it has been successfully applied in automotive silicon carbide (SiC) power modules and offers a promising packaging solution for GaN HEMTs [10], [11].

The primary contribution of this letter lies in the concept of a compact 3-D packaging method of GaN integrated power module (IPM) based on silver sintering technology, characterized by its remarkably small size, low power loop parasitic inductance, and thermal resistance. The key features can be summarized as follows:

1) redistributed layers (RDLs) implemented through flexible printed circuit (FPC) boards, enlarging the electrodes areas and clearance between them;
2) sintering technology at the same processing temperature, enhancing both electrical and thermal performance;
3) low power loop inductance of 0.54 nH and junction-to-case thermal resistance of 0.05 °C/W;
4) remarkably compact dimension (28 mm × 16 mm × 5 mm) with integrated decoupling capacitors, gate driver, digital isolator, and isolated power supply;
5) incorporation of electrical shielding for mitigating interference at input signal pins.

II. Structure and Manufacture of 3-D GaN IPM

A. *Structure and Schematic of the Proposed 3-D GaN IPM*

The proposed packaging structure is illustrated in Fig. 1(b). FPC boards are employed as RDLs of the GaN dies' top electrodes. This helps fix the alignment and short-circuit issues by enlarging original small areas of electrodes and narrow clearance between them. Subsequently, two GaN HEMT dies with RDLs are sandwiched between a multilayer PCB and an active metal brazing (AMB) substrate, forming a half-bridge topology. The multilayer PCB also accommodates other components in the IPM, including decoupling capacitors, gate driver, auxiliary power supply, etc. Furthermore, to enhance thermal performance of the proposed module, an integrated heatsink can also be included.

In Fig. 1(b), five interconnections are required in vertical direction, namely components-to-PCB, PCB-to-FPC, FPC-to-GaN, GaN-to-AMB, and AMB-to-heatsink. Conventional packaging methods would necessitate the use of multi-temperature gradient soldering processes with different melting point solders, leading to either too high or too low reflow temperature. None of those is expected due to reliability problems related to warpage and low connecting strength. Thanks to the emerging silver sintering technology, which is based on atomic diffusion and particles consolidation, all interconnections can be completed in the same temperature (260 °C) in different sintering and reflow processes. Furthermore, other advantages, such as elimination of solder overflow concern, ultra-thin thickness ($\leq$20 μm), high thermal conductivity, and robust shear strength all contribute to reducing thermal resistance and enhancing overall reliability.

A six-layers PCB with a thickness of 1 mm is employed to create small power loop and gate driving loops, effectively minimizing the parasitic inductances. Fig. 2(a) illustrates the layer structures of the PCB. The bottom three layers are dedicated for main power loop, shown as the red dash lines. The commutation

TABLE I
COMPONENTS IN THE PROPOSED GAN IPM

Components	Part No.	Parameters
GaN die	GS-065-150-1-D2	12.65 mm×5.6 mm
Gate driver	NCP51820	QFN15 (4 mm×4 mm)
Isolated Power Supply	B0505MT-1WR4	DFN (7 mm×9 mm×3 mm)
Voltage doubler	MAX1683	SOT-23-5 (2.9 mm ×2.8 mm)
Digital isolator	NSi8120D0	DFN8 (3 mm ×2 mm)
Decoupling capacitors	C3225C0G2J822J 125AA	630V/8.2 nF × 4
FPC	Two layers, 2 OZ	12.65 mm ×5.6 mm ×0.165 mm
PCB	Six layers, 2 OZ	28 mm ×16 mm ×1 mm , Cavity
AMB	Cu/AlN/Cu	28 mm ×16 mm ×0.58 mm

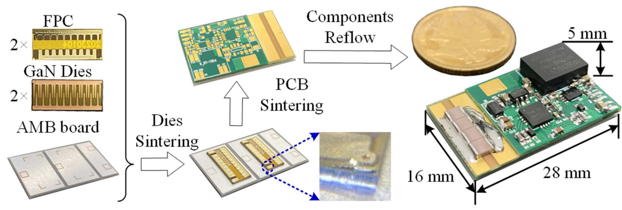

Fig. 3. Illustration of the manufacturing processes of GaN IPM.

current during switching transitions starts from positive terminal and passes through vias and GaN dies on the bottom layer, and then, returns through vias and the other two layers to the negative terminal. Thicknesses of dielectric between adjacent layers are only 0.102 or 0.145 mm, as annotated in Fig. 2(a), enhancing transient magnetic flux cancellation. So, an ultra-low power loop inductance can be achieved. As shown in Fig. 1(b), cavity technology is implemented in this PCB to shorten vias for decoupling capacitors. One benefit of the cavity technology adopted here is that power loop inductance and resistance can be reduced slightly due to short vias. Another benefit is that this technology eliminates the blind vias from top layer to the fifth layer. So, additional lamination and hole-drilling processes are saved, and the cost of the PCB is also reduced. The bottom layer facilitates connections to the dies and other two layers serve as return paths for power ground. Top three layers are designated for components, signal grounds, and power supplies, respectively. Power supply planes, along with their corresponding ground planes, function as busbar structures, significantly enhancing voltage stability. Additionally, ground planes beneath components also act as shielding layers, effectively mitigating interference coupled by parasitic capacitances from power stage [12].

Layouts of the two-layer FPC and its alignment with the GaN die are illustrated in Fig. 2(b). The thicknesses of the copper layers and dielectric layer (polyimide, PI) are 2 OZ and 25 μm, respectively. The hole size of vias is 0.15 mm. The FPC boards are intentionally designed to be the same size as the GaN dies to ensure easy alignment.

All pads of the PCB and FPC are gold-plated to achieve a higher strength after fabrication.

A simplified schematic is shown in Fig. 2(c) and key components are listed in Table I. A half-bridge non-isolated gate driver NCP51820 with dedicated voltage regulators and split outputs is adopted, requiring only a single power supply. The isolated power supply B0505MT-1W4 is employed to provide 5 V for the secondary side of a two-channel digital isolator, as well as a voltage doubler to generate a 10 V for NCP51820. The overall schematic demands only one 5-V power supply and two channel PWM signals for operation. The selected components are intentionally small in size to achieve a compact prototype. Isolation capacitances of the power supply and digital isolator are only 8 and 2 pF, respectively, also listed in Fig. 2(c). As shown in Fig. 2(a), dielectric thickness between input power planes (GND_IN&5V_IN) and main power planes (PGND) is only 0.138 mm, which introduces total 26-pF parasitic capacitance in this design, as listed in Fig. 2(c). Further reduction of this parasitic capacitance can be realized by increasing dielectric thickness and smaller layout area of input power plane. Both gate driver and digital isolator claim to provide stable dv/dt operation rated up to 200 V/ns. All the isolation capacitance in this design is very small, and it is suitable for fast switching of GaN HEMTs.

B. Manufacturing Processes

Detailed manufacturing processes are illustrated in Fig. 3.

1) Dies and FPC Boards Sintering Process: First, the GaN HEMT dies and FPC boards are positioned on the AMB substrate carefully and sintered together at the same time. The AMB substrate is silver-plated and prior to sintering, locations of the dies are accurately marked using laser. The sintering process condition is set as 260 °C under 15 MPa for 5 min. The type of silver paste adopted is ASP338-28F1510 from Heraeus. After sintered, the silver layers form solid connections and will never melting (melting point of silver: 961 °C) in following fabrication processes. The magnified view of gate point shows successful interconnections of FPC-to-GaN and GaN-to-AMB.

2) PCB Sintering Process: Then, the multilayer PCB with cavity for decoupling capacitors is sintered to the top of FPC boards. This sintering process is also conduct at 260 °C and under 15 MPa for 5 min.

3) Components Reflow Process: Finally, components including decoupling capacitors, gate driver, isolated power supply, and digital isolator are soldered onto the top of the PCB by reflow process. The reflow temperature is also set at 260 °C with SAC305.

The compact size of the final half-bridge GaN IPM shown in Fig. 3 is only 28 mm × 16 mm × 5 mm. The height is mainly limited by the isolated power supply. The manufacturing procedure takes two sintering processes and one reflow process, all at the same processing temperature to easy warpage issue and enhance the overall reliability. Shear tests are done to check the strength of different interconnections between coppers. Test results show sintered silver layer is as high as 112.8 MPa, more than double of the solder layer after reflow process (46.3 MPa). The strength of the sintered silver layer on a silver- or gold-plated surface could reach more than 130 MPa under the proposed sintering conditions. It should be pointed out that in this preliminary stage, the heatsink is not directly integrated, as careful design of the heatsink needs to be done to further decrease junction-to-ambient thermal resistance, which will be explained

in the thermal simulation part. For future heatsink integration, an additional sintering process will be added at the beginning or merged with the dies sintering process.

III. Parasitic Extraction and Thermal Evaluation

A. Parasitic Extraction

As shown in Fig. 2(a), the arrangement of power loop leads to a significant reduction in parasitic inductances due to the increasing cancellation of the magnetic flux. So, an ultralow power loop inductance of 0.52 nH at 100 MHz is achieved, which is simulated in ANSYS Q3D. Similarly, the gate loop inductances are minimized to be around 3–4 nH in this design. Kelvin connection of the driving source and power source is realized through vias in the PCB. The two sources are connected at a single point on the bottom layer of the PCB.

In Fig. 1(b), the top side of the AMB board at left GaN die's position is connected to the middle point of the half-bridge, which introduces about 32-pF parasitic capacitance between the middle point and heatsink in this design. This parasitic capacitance will introduce electromagnetic interference (EMI) noise when the heatsink is grounded. To optimize the EMI noise, the middle point copper area of the AMB can shrink half for just placing GaN die and post. Ceramic thickness can also increase to reduce the parasitic capacitance but should be balanced with thermal performance. After all, EMI problem is a big issue for the proposed packaging method and there are lots of interesting things to explore, and it will be researched in the future work.

B. Thermal Test and Simulations

A simple liquid cooling heatsink with pin-fins is designed and assembled with three GaN IPMs to construct a three-phase inverter, as illustrated in Fig. 4(a).

A liquid-cooling system is built up to evaluate the thermal performance of the proposed packaging method. As shown in Fig. 4(b), only a GaN die and an AMB board are sintered to the heatsink. As shown in the zoomed-in picture, connections of GaN die are realized by bonding wires, and a constant current is supplied from source to drain of the device. Gate and source are shorted to get a higher conducting voltage, so a high power can be generated with a low applied current. Liquid flow rate is kept constant at 0.5 liter per minute (LPM), and the applied power is monitored by a power analyzer PA333H. The thermal test is kept running for about 30 min, which is enough to reach the steady state, and then, the water temperature is monitored by a thermocouple and device temperature is capture by an infrared camera (FOTRIC 348). The monitored voltage is 3.04 V and current is 18.314 A, so the total power applied is 55.7 W. Water temperature is steady at 27.8 °C. Fig. 4(c) shows the captured thermal image of the module at steady state.

The whole module is imported into ANSYS Icepak with the same power 55.7 W, liquid temperature 27.8 °C, and flow rate 0.5 LPM applied. Other thermal parameters are listed in Table II. The simulated temperature distribution is shown in Fig. 4(d). The highest temperatures of the experiment and simulation are

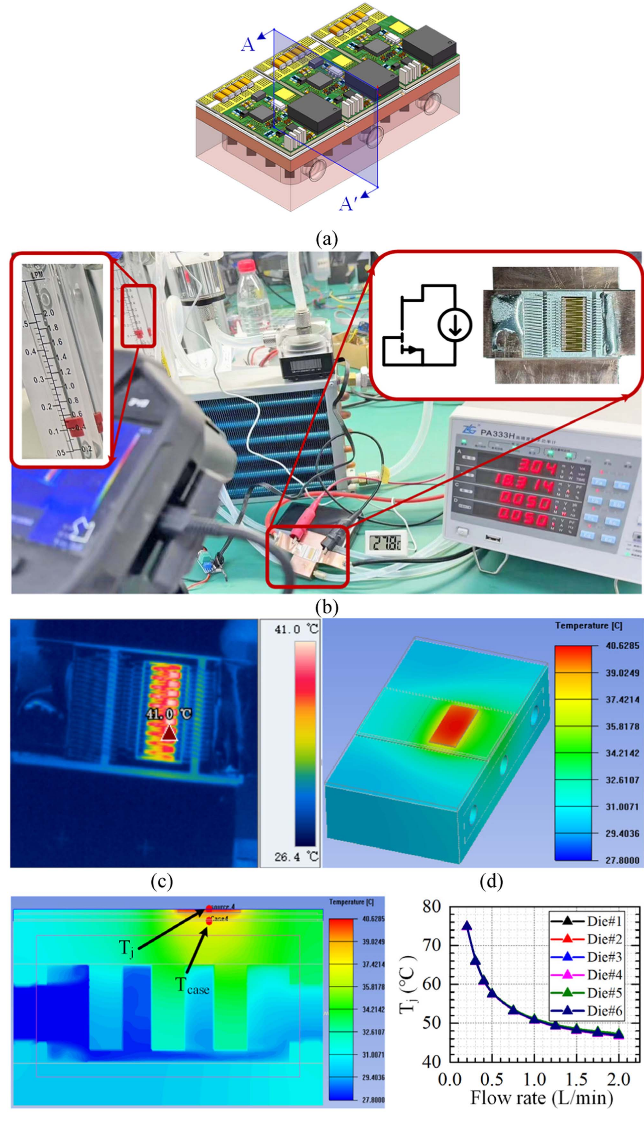

Fig. 4. Thermal test and simulation of GaN IPM at 27.8 °C ambient. (a) GaN IPM inverter assembly with heatsink. (b) Thermal experiment setup. (c) Captured thermal image at steady state. (d) Simulated thermal distribution. (e) Thermal distribution at A–A′ section. (f) T_j versus different flow rate.

TABLE II
Thermal Simulation Parameters

Layers	Thickness (mm)	K ($W\cdot m^{-1}\cdot K^{-1}$)
GaN Die	0.25	180
Silver_Die	0.02	200
AMB(Cu/AlN/Cu)	0.1/0.38/0.1	388/180/388
Silver_AMB	0.02	200
Heatsink (Base)	3	388
Heatsink (Pinfin)	6 (2×2 mm^2)	388

41.0 °C and 40.6 °C, and the calculated junction-to-ambient thermal resistance R_{ja} are 0.236 °C/W and 0.229 °C/W, respectively, showing high consistence. Cross-sectional thermal distribution of A–A′ is depicted in Fig. 4(e). The center point temperature of the die's top side T_j and corresponding temperature directly beneath the die on the bottom copper layer of the AMB board T_{case} are monitored. Temperature difference ΔT between T_j and T_{case}

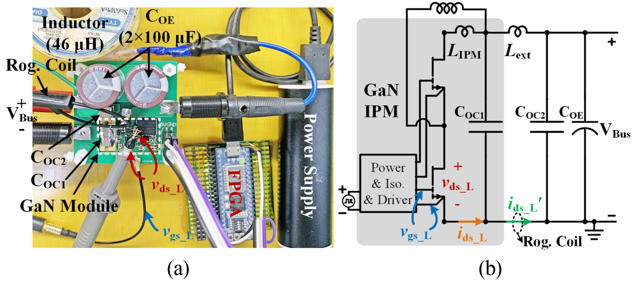

Fig. 5. DPT. (a) Setup. (b) Equivalent circuit.

is only 2.8 °C, so the calculated R_{jc} is 0.05 °C/W, far less than conventional discrete package. As thermal resistance is related to die size, the specific thermal resistance ($R_{jc}\times$Area) is derived to be 3.54 °C/W·mm^2 (die size in this letter is 12.65 mm × 5.6 mm). While the value in [7] can be calculated as 3.97 °C/W·mm^2 (R_{jc} = 0.31 °C/W, die size equals 5.87 mm × 2.18 mm). So, although single-sided cooling is adopted in this letter, R_{jc} is better than that of the double-sided cooling design.

Then, each die in this three-phase converter is applied with 55.7-W power loss, and the liquid temperature is set as 27.8 °C. Fig. 4(f) shows junction temperature versus different liquid flow rate. Due to the excellent thermal performance, T_j of the six dies are almost the same to each other. Compared to Fig. 4(d), T_j rises to 57.5 °C at 0.5 LPM due to more power needs to be dissipated. When liquid flow rate rises, T_j decrease dramatically and gradually become stable. So, the heatsink design needs more improvement to further explore high power potential of GaN power devices.

IV. Double Pulse Tests (DPTs) and Analysis

Fig. 5(a) shows the DPT setup for GaN IPM. A motherboard consisting of two electrolytic capacitors (2 × 100 μF, C_{OE}), four multilayer ceramic capacitors (MLCCs, 4 × 440 nF at 400 V C_{OC2}), and power sockets are assembled on a heatsink. The manufactured GaN IPM with four MLCCs (4 × 8.2 nF at 400 V, C_{OC1}) integrated is also attached to the heatsink at the cutout of the motherboard. Bus voltage terminals of GaN IPM are connected to the motherboard by two wires.

An optical isolated probe OIP500B and a passive high-voltage probe RP1300H are employed to capture gate-to-source voltage v_{gs_L} and drain-to-source voltage v_{ds_L} of the low-side switch, respectively. Equivalent circuit is illustrated in Fig. 5(b). The device current i_{ds_L} is hard to measure for such a compact module with decoupling capacitors integrated. So, the current i_{ds_L}' between the GaN IPM and the motherboard is monitored by an ultra-mini Rogowski coil surrounding the negative V_{Bus} wire.

A 5-V power supply and an FPGA board are used to control the module. Gate resistances of turn-ON and OFF are 4.7 and 1 Ω, respectively. Switching waveforms at 400 V/70 A are presented in Fig. 6. The complete DPT waveforms, as captured from the oscilloscope MSO8064, are displayed in Fig. 6(a), while zoomed-in switching transitions are shown in Fig. 6(b).

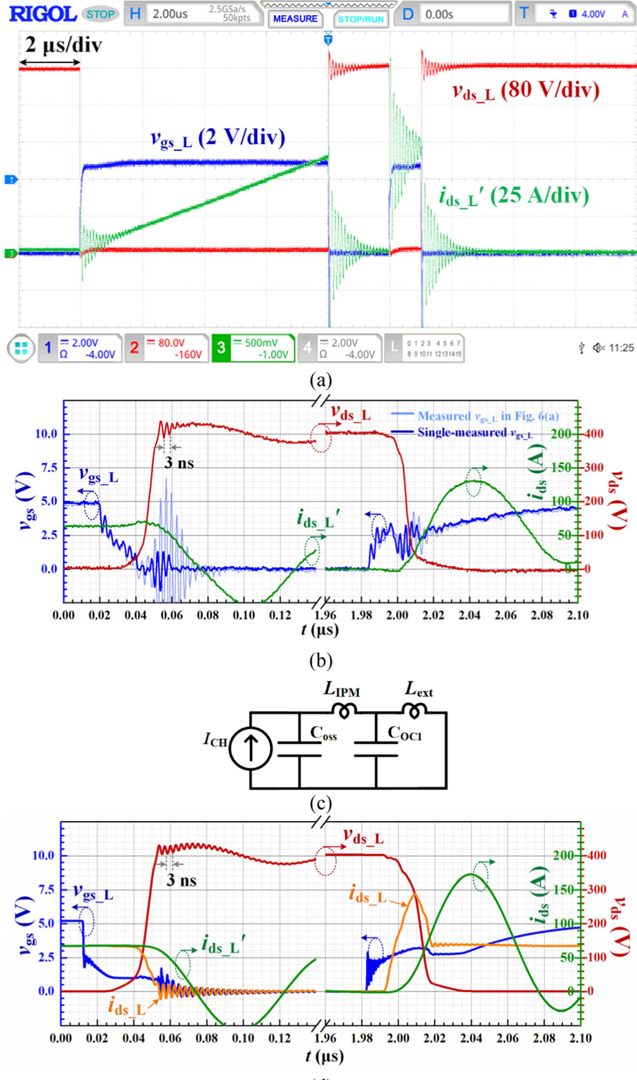

Fig. 6. Waveforms of DPT at 400 V/70 A (R_{g_on} = 4.7 Ω, R_{g_off} = 1 Ω). (a) Full waveforms. (b) Zoomed-in turn-ON and turn-OFF waveforms. (c) Small-signal model of switching ringings. (d) Simulated switching waveforms in LTspice.

Light-blue line shows severe ringing of v_{gs_L} during turn-OFF transition, but no false turn ON is found on v_{ds_L} when the ringing surpasses threshold voltage. So, it is believed that the ringing measured by v_{gs_L} probe may be interfered by the dv/dt coupled through high-voltage probe. DPT is repeated to capture only v_{gs_L} with the same probe and oscilloscope. The waveform of single-measured v_{gs_L} is shown as the dark-blue line in Fig. 6(b). Without the interference from the high-voltage probe, the turn-OFF ringing is much less and more accurate. Even when 0 V is applied at gate during OFF-state, there is no false turn-ON issue at a rapid 50 V/ns v_{ds_L} slew rate. This result confirms the effectiveness of the shielding design in the PCB structure.

Two oscillation frequencies of v_{ds_L} after turn-OFF are observed. This can be explained by the small-signal model during turn-OFF transition [13], as shown in Fig. 6(c). The network is a two-order system, and when excitation from change of channel

current I_{CH} comes, ringing with two resonate frequencies occurs. The high-frequency ringing period is around 3 ns, caused by the resonance between GaN die's output capacitance C_{oss} (423 pF at 400 V) and power loop inductance L_{IPM} in the GaN IPM. So, the calculated L_{IPM} is about 0.54 nH, which is very close to the simulated value of 0.52 nH. The low-frequency ringing period is around 100 ns, caused by the resonance between on-board decoupling capacitance C_{OC1} and the external loop inductance L_{ext}. This inductance is mainly induced by the connecting wires between the GaN IPM and the motherboard, calculated to be around 7.7 nH.

Furthermore, matrices of the distributed RLGC parameters simulated in Q3D and spice model offered by device manufacturer are imported into LTspice for circuit simulation. The simulated switching waveforms in Fig. 6(d) show high consistence with experiment waveforms. Device current $i_{\mathrm{ds_}L}$ in Fig. 6(d) also shows the same high-frequency ringing as $v_{\mathrm{ds_}L}$ and $i_{\mathrm{ds_}L}'$ shows the same low-frequency ringing as $v_{\mathrm{ds_}L}$. So, analysis based on the small-signal model is verified.

V. Conclusion

In this letter, a 3-D packaging method of GaN HEMT IPM based on silver sintering processes is proposed. A multi-layer PCB is adopted to achieve low parasitic inductances design and an AMB substrate is used to enhance the thermal performance. Additionally, the PCB can accommodate electric field shielding for control signals and integration of other components. So, a compact module (28 mm $\times$ 16 mm $\times$ 5 mm) is manufactured with both signal and power supply isolation. Furthermore, silver sintering processes are employed to improve electrical, thermal performances, and increase overall reliability. Manufacturing processes, simulations, and DPT are illustrated in detail. The experiment-measured power loop inductance of the proposed GaN IPM is as low as 0.54 nH and the simulated R_{jc} is only 0.05 °C/W. Both thermal and circuit simulations coincide with experiment results very well, verifying the excellent properties of the proposed GaN IPM. Switching waveforms show fast switching transitions without false behaviors even when the OFF-state gate voltage is 0 V.

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