Transient Analysis and Overcurrent Limited Strategy for Supply Restoration-Oriented Hybrid Soft Open Point

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***Abstract*—The hybrid soft open point (HSOP), formed by the parallel combination of the normally open point (NOP) and the soft open point (SOP), combines the advantages of flexibility and high cost-efficiency. At the power outage moment, the seamless switching process of HSOP contains a co-operation state with NOP and SOP parallel working together. This state involves current transitions between NOP and SOP, which may cause overcurrent and trigger the protection shutdown. To address this issue, a wide-band mathematical model is established to analyze and evaluate the transiting current, including high-frequency transiting current caused by the phase difference of pulsewidth modulation, and low-frequency overcurrent caused by a grid voltage step change. Based on the analysis, a high-frequency overcurrent limitation strategy is introduced, relying on the synchronization modulation strategy, and a low-frequency overcurrent limitation strategy is proposed, based on virtual impedance. The effectiveness of the proposed strategy is validated by operating the whole switching process with the simulation and a downscaled experimental platform. According to the experimental results, the SOP can support the load voltage within 20 ms after the power outage. Moreover, the high-frequency currents can be suppressed to around 10% compared to extreme cases, and the low-frequency overcurrent can be completely inhibited.**

***Index Terms*—Hybrid soft open point (HSOP), mode switching, overcurrent limited strategy, power outage, resilient distribution networks, transient analysis.**

I. Introduction

THE resilient distribution networks have attracted significant attention since their self-healing ability can guarantee power supply as much as possible under grid faults [1]. After a power outage caused by a grid fault happens in the resilient distribution system, distributed generations (DG) and restoration devices are utilized to realize the structural reconfiguration of networks and power supply restoration [2], [3], [4]. Hence, the restoration device plays an important role in enhancing system resilience.

The restoration device that connects multiple networks is typically the remote-controlled switch or the manual switch, designed to close only in the event of a grid fault [1]. Therefore, they are also referred to as the normally open point (NOP). With the advancement of power electronic technology, the soft open point (SOP) with enhanced functionalities receives significant attention and is anticipated to replace the NOP. Among the various SOP structures, the back-to-back (B2B) type and the unified power flow controller (UPFC) are the two main configurations. However, the former is more suitable to construct a resilient distribution system despite the low cost of UPFC [5].

Compared to the NOP, the SOP usually operates in the grid-following mode during normal conditions and automatically switches to the grid-forming mode to support load voltage during power grid outages [6], [7]. A mode switching control strategy of the SOP has been proposed to realize the seamless switching transitions in [8]. In addition to supply restoration, the SOP can interconnect asynchronous systems and achieve various control objectives with rapid response, such as balancing feeders' load [9], coordinating renewable energy resources [10], and addressing power quality issues [11]. The ability of flexible interconnection is the core reason that make the SOP more anticipated than the NOP. However, the capacity required for normal operating conditions is significantly lower than that needed for the supply restoration [12]. Furthermore, the power density and loss issues are major drawbacks of power electronic devices [13], [14]. Utilizing the SOP for supply restoration requires designing power electronics devices with large capacity and volume, leading to decreased cost-efficiency. On the contrary, mechanical switches offer the advantages of lower losses and smaller sizes, making the NOP more widely adopted in engineering applications despite its single-function design. For this reason, combining the merits of NOP and SOP to design the hybrid soft open point (HSOP) holds meaningful potential.

Parallel connection of the SOP and the NOP, with the SOP operating under normal conditions and the NOP restoring load under a power outage, leads to a typical structure of the HSOP. In [12] and [15], the system restoration algorithm of the HSOP is proposed; however, detailed control strategies at the device

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level have been overlooked. In [16], the control strategy of the HSOP is proposed to realize the island mode and grid-connected mode of the microgrid. However, grid fault conditions are not taken into the consideration. In [17], a complete mode switching process is provided, including the fault ride through stage and the supply restoration. The control strategy of the HSOP under grid faults have been proposed in [18] with the objects of minimizing the voltage fluctuation when the fault occurs and limiting the current of the interconnection switch when the fault is eliminated. Nevertheless, the supply restoration process involves the current transitions between the NOP and the SOP, which may lead to overcurrent and cause damage to power-semiconductors. In [19], the equivalent circuit of the transient structure of the HSOP is built to calculate the overcurrent, and the overcurrent limited strategy is introduced, but only the low-frequency overcurrent is considered, and the voltage sags caused by output power saturation have been overlooked. The actual situation of insufficient SOP capacity is critical for the analysis of HSOP's switching process, and the corresponding high-frequency and low-frequency overcurrent are still the unresolved issues. Accordingly, this article aims to provide a comprehensive analysis of the HSOP during a power outage, especially addressing the capacity of SOP relative to the power of the load and the wideband transient overcurrent caused generated by the switching process.

The high-frequency overcurrent can be mitigated through modified modulation strategies or the use of hardware solutions. As mentioned in [19], the HSOP is regarded as the parallel connected converters under the short-circuit state of the switching process. In [20], a novel modulation strategy based on the space vector pulsewidth modulation (SVPWM) is introduced to restrain the zero-sequence circulating current (ZSCC). Additionally, a novel carrier-based pulsewidth modulation is proposed to achieve effects similar to the SVPWM and limit the ZSCC with the autonomous synchronization of the carrier phase [21], [22]. The implementation of these methods needs more complex calculations. A modified *LCL*-filter is analyzed in [23], [24], and [25], and ZSCC can be suppressed by the modified the connection of *LCL* filter, which is easily achievable. However, these strategies only focus on the ZSCC, which is insufficient for the high-frequency current suppression. Fourier Series is employed in this article to describe the transient high-frequency component that is hardly influenced by control systems, and the synchronization modulation strategy is proposed to suppress the high-frequency output current, encompassing but not limited to ZSCC.

In another respect, research on low-frequency overcurrent suppression predominantly centers around the current limiting strategy. The objectives of the current limitation for grid-following converters include two aspects. The first one is to avoid the output overcurrent by constraining the current reference. The second one is to prevent other abnormal phenomena, including suppressing the output power fluctuation [26], supporting the bus voltage [27], and limiting the negative- and zero- sequence fault current [28]. The virtual impedance can be employed as part of the current limiting strategy for grid-forming converters. In [29], the virtual synchronous machine and the virtual impedance are combined to suppress the overcurrent. In contrast, the virtual impedance is added to the control system only under the grid fault in [30] and [31]. Moreover, when the virtual impedance's voltage is added to the modulation waveform, it can enhance the response speed of the virtual impedance component [31]. The design process of the virtual impedance is also critical, with stability and response speed as key objectives [32], [33]. Combining the current limiting strategy for both grid-following and grid-forming converters, a control strategy for more effectively completing the switching process of the HSOP is proposed in this rticle. In addition, the proposed method's effect is evaluated in both the time domain and frequency domain [34].

Compared to these previous research works, the synchronization modulation strategy and the control strategy based on the virtual impedance are proposed to ensure the smooth operation of the HSOP's switching process. The rest of the article is organized as follows.

1) In Section II, a detailed description of the HSOP switching process is provided, emphasizing its capability to achieve seamless mode switching during a power outage. The corresponding mathematical model of the system in the co-operation state is built, enabling the theoretical calculation of the output current.
2) In Section III, the high-frequency transient component is calculated. Through the analysis, the optimal modulation strategy is identified to mitigate the risk of the high-frequency overcurrent and prevent potential damages during the switching process.
3) In Section IV, the design process of the proposed control strategy incorporating virtual impedance is elaborated. By meticulously designing the parameters, the HSOP can rapidly support the load voltage during a power outage and prevent low-frequency overcurrent during the seamless switching process.
4) In Sections V and VI, the simulation and the experiment of the proposed switching process are presented. Finally, Section VII concludes this article.

II. Switch Process and Mathematical Model

As illustrated in Fig. 1, the hybrid soft open point is comprised of an interconnection switch and a B2B-type SOP. The B2B-type SOP consists of two voltage source converters (VSC), the topology of which is usually the modular multilevel converter, the cascaded H-bridge converter, the multilevel converter, and so on [35], [36]. In this article, a three-level neutral clamped converter (NPC) is used as a case study for analysis. Under the normal operating conditions, VSC1 is controlled to stabilize the voltage of the dc bus and VSC2 is controlled to output fundamental-frequency and harmonic current according to the given commands. Thus, the current loop of each VSC is important, and the proportional-resonant (PR) controller is adopted. The detailed information about the current loop has been omitted, as it has been applied widely and is well-known.

The interconnection switch is a mechanical device used to divert high-power load during the supply restoration. The capacity of the SOP is much smaller than the total power of

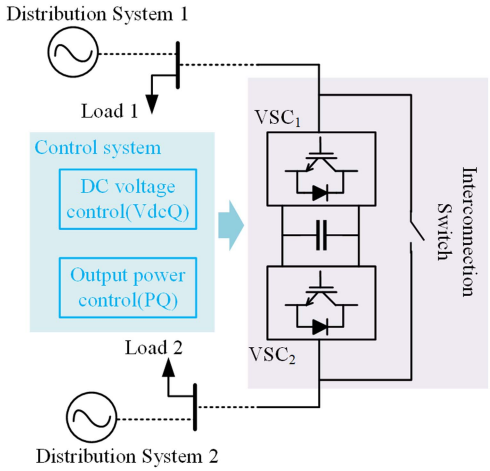


Fig. 1. Typical structure of HSOP.

substation outage load since the SOP is only used to regulate the power flow and mitigate harmonic and unbalanced current in normal operating conditions. Consequently, the switching process signifies the HSOP transitioning from the SOP working mode to the interconnection switch working mode.

A. Mode Switching Process Under Power Outage

The switching process of HSOP occurs only if the primary power supply of one side is cut off. The entire process is illustrated in Fig. 2. The diagram of the load voltage and output current of the VSC at the fault side is also depicted.

In normal operating conditions, the SOP regulates the power flow between feeders, as shown in Fig. 2(a). After the grid fault happens, as illustrated in Fig. 2(b), the load voltage decreases, and the fault ride through strategies can be immediately applied to the grid-connected converter [26]. The relay protections will open the circuit breakers near the fault by detecting the features of grid fault [37], [38], [39]. Primary power may be cut off as soon as relay protections actuate, resulting in some loads losing the power supply. The control system of the SOP will turn into grid-forming mode to support the load voltage and send the close command to the interconnection switch, as depicted in Fig. 2(c). The SOP needs to support load voltage alone because the close action of the interconnection switches typically takes tens of milliseconds [40]. As shown in Fig. 2(d), at the moment the interconnection switch closes, the SOP and the interconnection switch work together, defined as the co-operation state for convenience. After that, the SOP shuts down.

As presented in the above description, the stage (d) of Fig. 2 will introduce a transient short-circuit loop into the device. Therefore, it is critical to analyze the principles of voltage and current during this transient state.

B. Output Current Model Under Transient State

During the co-operation state, the converters of the SOP share the same dc bus and ac bus, adopting a structure similar to paralleled interleaved converters. Each half-bridge can be equivalent to a controlled voltage source, with the negative electrode being the neutral point of the dc bus [20]. With the same equivalent method in [19], the output current can be expressed as follows:

$$i_{xk} = \frac{Z_2/2}{Z_1\left(Z_{\text{eq}}+Z_2\right)}\frac{V_{\text{dc}}}{2}\left(S_{xk}-S_{x,(3-k)}\right) + \frac{1}{2\left(Z_{\text{eq}}+Z_2\right)}\left(\frac{V_{\text{dc}}}{2}S_{xk}-u_{gx}+u_{NN'}\right) \quad (1)$$

Where x means the phase x (x = A, B, C); k means the number of B2B converters ($k = 1$ or 2); Z_1 represents the filter impedance of converters and Z_2 represents the line impedance of the power system; Z_{eq} represents the equivalent impedance of each converter's filter and is equal to $Z_1/2$; u_{gx} is the grid voltage and $u_{NN'}$ is the common mode voltage (CMV) of HSOP; S_x represents the switching function; and V_{dc} is the rated value of dc voltage.

By applying the switching function, (1) always holds, regardless of whether it is the high-frequency or low-frequency current under the co-operation state.

III. Modulation Strategy

The high-frequency current resulting from the co-operation state is primarily influenced by the modulation strategy, switching frequency, and filter impedance. The detailed analysis of the high-frequency current will be conducted in this section based on (1), an aspect that has been minimally explored in this scenario.

A. Calculation of Output High-Frequency Current

The high-frequency components generated by the semiconductors are associated with the modulation strategy [41]. This article uses the phase-disposition pulsewidth modulation (PD-PWM) as the case study, since PD-PWM is a prevalent scheme in the practical engineering [42].

The output phase voltage of NPC using PD-PWM can be expressed in a Fourier series to reveal the amplitude and phase of each frequency, as written in the following [42]:

$$\begin{aligned} S_k = {} & A_k\cos\left(\omega_0 t+\theta_{0k}\right) \\ & + \sum_{m=1}^{+\infty} B_{m-k}\cos\left[\left(2m-1\right)\left(\omega_c t+\theta_{ck}\right)\right] \\ & + \sum_{m=1}^{+\infty}\sum_{n=-\infty}^{+\infty} C_{mn-k}\cos\left[2m\left(\omega_c t+\theta_c\right)\right. \\ & \left. + \left(2n+1\right)\left(\omega_0 t+\theta_0\right)\right] \\ & + \sum_{m=1}^{+\infty}\sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} D_{mn-k}\cos\left[\left(2m-1\right)\left(\omega_c t+\theta_c\right)\right. \\ & \left. + 2n\left(\omega_0 t+\theta_0\right)\right] \end{aligned} \quad (2)$$

where ω_0 and θ_{0k} are the frequency and the phase of the modulation wave; and ω_c and θ_{ck} are the frequency and the phase of the carrier wave.

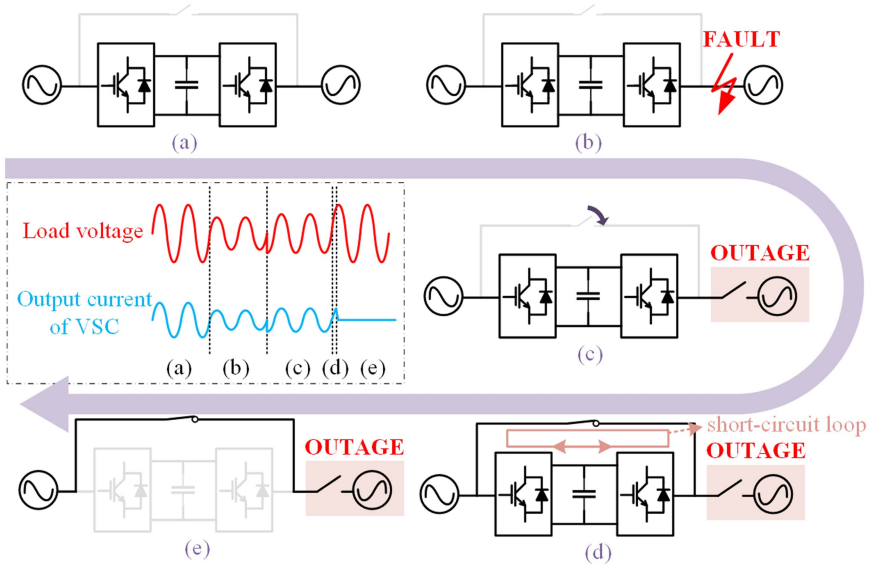


Fig. 2. Entire process under power outage. (a) Normal operating condition. (b) Fault ride through. (c) B2B-type SOP restores load. (d) Co-operation state. (e) NOP restores load.

The detailed expressions of A_k, $B_{m\text{-}k}$, $C_{mn\text{-}k}$, and $D_{mn\text{-}k}$ are written in the following:

$$\begin{cases} A_k = M_k \\ B_{m-k} = \frac{8}{\pi^2}\frac{1}{2m-1}\sum\limits_{d=1}^{+\infty}\frac{J_{2d-1}[(2m-1)\pi M_k]}{2d-1} \\ C_{mn-k} = \frac{1}{m\pi}J_{2n+1}\left(2m\pi M_k\right)\cos n\pi \\ D_{mn-k} = \frac{8}{\pi^2}\sum\limits_{d=1}^{+\infty}\frac{J_{2k-1}[(2m-1)\pi M_k](2k-1)\cos n\pi}{(2k-1+2n)(2k-1-2n)(2m-1)} \end{cases} \tag{3}$$

where M_k is the modulation ratio of VSC_k and J means the Bessel function.

According to the definition of parallel converters' CMV, its expression can be derived from the output phase voltage of converters, which means that

$$u_{NN'} = -\frac{\mathrm{V_{dc}}}{2}\sum_{x}^{\mathrm{A,B,C}}\sum_{k=1}^{2}S_{xk}. \tag{4}$$

The high-frequency current can be obtained by substituting (2)–(4) into (1). From the mathematical formula, the high-frequency output current under the co-operation state can be influenced by the phase difference between two VSCs' carrier wave, filter impedance, and line impedance. It is apparent that the output high-frequency current decreases with increasing the switching frequency and the filter inductance. Nevertheless, the switching frequency and the inductance are constrained by factors such as practical device limitations, engineering application costs, etc. In engineering applications, the HSOP is often designed with modularity in mind, where each converter of one port is produced individually. Consequently, the converters within the entire equipment may not share the same microprocessor, potentially leading to common phase differences among the converters' carriers.

TABLE I
SYSTEM PARAMETERS OF CALCULATION EXAMPLES

Item	Value
Grid line-voltage	380 V
Fundamental frequency	50 Hz
Line impedance	(0.1+j0.1) Ω
VSC-side filter inductance	1.2 mH
Capacitor of *LCL* filter	20 μF
Grid-side filter inductance	45 μH
Switching frequency	5 kHz
Modulation ratio	0.89

B. Phase Difference of Carrier Waves

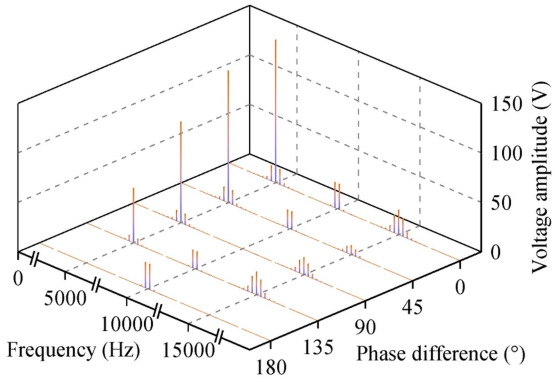
Based on the system parameters listed in Table I, the influence of the phase difference is discussed here.

According to (1), there are three components influencing the output current: the CMV, the difference between the two converters' phase voltage (DPV), and the output phase voltage (OPV). Since only the CMV and the DPV vary with the phase difference, and the spectra of these two components are depicted in Fig. 3.

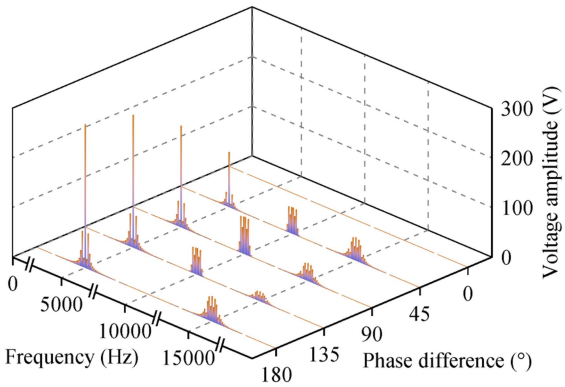
As shown in Fig. 3, the changing principles of CMV and DPV are completely different. The following will focus on the switching frequency component, as it dominates the entire high-frequency spectrum.

The switching frequency components of CMV, DPV, and OPV are expressed in the following equations:

$$u_{\mathrm{CMV}} = \frac{2V_{\mathrm{dc}}}{\pi^2}\bar{J}_1\sqrt{2\left[1+\cos\left(\theta_{c1}-\theta_{c2}\right)\right]} \times \cos\left(\omega_c t + \frac{\theta_{c1}+\theta_{c2}}{2}+\pi\right) \tag{5}$$



(a)



(b)

Fig. 3. Amplitude of CMV and DPV with different carrier wave angle difference. (a) Spectrum of CMV. (b) Spectrum of DPV.

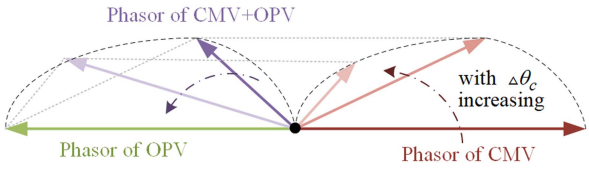


Fig. 4. Phasor diagram of CMV and OPV with different angle difference.

$$u_{\mathrm{DPV}} = \frac{8V_{\mathrm{dc}}}{\pi^2}\bar{J}_1 \sin\left(\frac{\theta_{c1}-\theta_{c2}}{2}\right)\cos\left(\omega_c t + \frac{\theta_{c1}+3\theta_{c2}}{4} + \frac{\pi}{2}\right) \tag{6}$$

$$u_{\mathrm{OPV}} = \frac{4V_{\mathrm{dc}}}{\pi^2}\bar{J}_1 \cos\left(\omega_c t + \theta_{ck}\right) \tag{7}$$

where $\bar{J}_1 = \sum_{d=1}^{+\infty} \frac{J_{2d-1}(\pi M)}{2d-1}$.

With the phase difference between two carrier waves increasing from 0 to π, CMV decreases, but the phase between CMV and OPV decreases as well. The phasor diagram is drawn in Fig. 4. This phenomenon indicates that the sum of CMV and OPV increases although CMV is smaller. Consequently, it is meaningless to only consider the variation of CMV unless taking into account the sum of CMV and OPV. Fig. 5 gives spectrum of the sum of CMV and OPV with the carrier phase difference changing. Combining the results of Figs. 3 and 5, increasing the angle difference will increase both DPV and CMV+OPV, which exhibits a monotonic characteristic. As a result, it is preferable to have carrier phase synchronization and a phase difference of 0 when PD-PWM is applied to the paralleled interleaved NPCs.

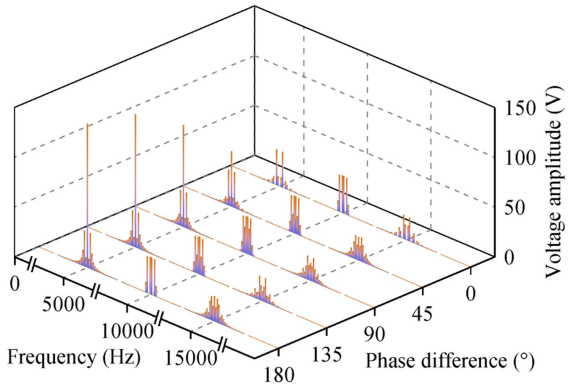


Fig. 5. Amplitude of CMV+OPV with different angle difference.

C. High-Frequency Current Comparison

The above analysis of the high-frequency current determines the optimal phase difference causing minimum high-frequency overcurrent with the existing switching frequency and filter inductance. Hence, the high-frequency current under normal operating conditions (single grid-connected converter) and that under co-operation state (equivalent to the paralleled converters) should be compared to decide whether the high-overcurrent will occur under the switching process of HSOP.

As mentioned before, DPV and CMV+OPV are the two main factors contributing to high-frequency currents under the co-operation state. The most extreme scenario of these two factors will be calculated respectively, and the combination of these two components can describe the maximum current of each frequency. To express frequency more intuitively, the frequency of $m \cdot \omega_c + n \cdot \omega_0$ is represented as (m, n).

First, CMV+OPV of the co-operation state is calculated. Based on the definition of CMV, $u_{NN'}$ is nonzero only when $m \geq 1$ and $n = 0, 3, 6, 9$, etc. The mathematical expression is shown in (8). The frequency making CMV nonzero is defined as *zero-sequence frequency*, since the output phase voltages at these frequencies are identical for all three phases

$$u_{NN'-mn} = \begin{cases} -\frac{u_{x1-mn}+u_{x2-mn}}{2}, & m \geq 1, n = 0, 3, 6, 9 \ldots\ldots \\ 0, & \text{others} \end{cases} \tag{8}$$

where the variable with subscript m and n means the component of frequency (m, n).

Consequently, the sum of CMV and OPV can be written as follows:

$$u_{x1-mn} + u_{NN'-mn} = \begin{cases} \frac{u_{x1-mn}-u_{x2-mn}}{2}, & m \geq 1, n = 0, 3, 6, 9 \ldots\ldots \\ u_{x1-mn}, & \text{others} \end{cases}. \tag{9}$$

TABLE II
HIGH-FREQUENCY VOLTAGE OF TRANSIENT STATE

Frequency	CMV+OPV	DPV
n=0	$\frac{u_{x1-mn}-u_{x2-mn}}{2}$	0
n=3,6,9…	$\frac{u_{x1-mn}-u_{x2-mn}}{2}$	$u_{x1-mn}-u_{x2-mn}$
others	0	$u_{x1-mn}-u_{x2-mn}$

TABLE III
HIGH-FREQUENCY VOLTAGE OF NORMAL OPERATING CONDITION

Frequency	CMV+OPV	DPV
n=0	0	0
n=3,6,9…	0	0
others	u_{x-mn}	0

Second, DPV of the co-operation state is calculated. Unlike CMV, DPV is the difference between the output phase voltages of two converters. The expression of it can be u_{x1}–u_{x2} of all frequencies. Therefore, the high-frequency voltage expressions of the co-operation state are listed as in Table II.

On the other hand, the output current of the grid-connected converter is calculated in the following:

$$i_x = \frac{1}{Z_1+Z_2}\left(\frac{V_{\rm dc}}{2}S_x - u_{gx} + u_{NN'}\right). \tag{10}$$

Only the sum of CMV and OPV needs to be taken into account when considering a single grid-connected converter. According to the analysis of paralleled interleaved converters, the zero-sequence frequency component of CMV is opposite to that of OPV, and CMV is equal to 0 at other frequencies. Thus, the expression of CMV+OPV is written as follows:

$$u_{x1-mn}+u_{NN'-mn} = \begin{cases} 0, & m\geq 1, n=0,3,6,9\ldots \\ u_{x1-mn}, & \text{others} \end{cases}. \tag{11}$$

Above all, the high-frequency voltage expressions of normal operating conditions are listed in Table III.

Substitute the high-frequency voltage expressions in Tables II and III into (1) and (10), and the output current of all high frequency can be obtained. The expressions of output current under the co-operation state and the normal operating condition are written in the following:

$$i_1 = \begin{cases} \frac{1}{4(Z_{eq}+Z_2)}(u_{x1}-u_{x2}) & n=0 \\ \left(\frac{1}{4(Z_{eq}+Z_2)}+\frac{Z_2/2}{Z_1(Z_{eq}+Z_2)}\right)(u_{x1}-u_{x2}) & n=3,6,9\ldots \\ \frac{Z_2/2}{Z_1(Z_{eq}+Z_2)}(u_{x1}-u_{x2}) & \text{others} \end{cases} \tag{12}$$

$$i_2 = \begin{cases} 0 & n=0 \\ 0 & n=3,6,9\ldots \\ \frac{1}{Z_1+Z_2}u_x & \text{others}. \end{cases} \tag{13}$$

According to (2), (12), and (13), the phases of two converters' modulation wave influence the high-frequency current. Under the switching process, the modulation wave, as the output of the control system, may have fluctuating parameters. Therefore, it is necessary to calculate the most extreme condition. In (2), the high-frequency output voltage of each phase can be simplified as follows:

$$\begin{cases} u_{x1} = \sum_{m=1}^{+\infty}\sum_{n=-N}^{+N} F_{1mn}\cos\left[(m\omega_c+n\omega_0)t+m\theta_c+n\theta_1\right] \\ u_{x2} = \sum_{m=1}^{+\infty}\sum_{n=-N}^{+N} F_{2mn}\cos\left[(m\omega_c+n\omega_0)t+m\theta_c+n\theta_2\right]. \end{cases} \tag{14}$$

The maximum amplitude of DPV with nonzero n can be derived from (14), the expression of which is (15). The condition for taking "=" in (15) is $n\theta_1+n\theta_2=\pi$, and it is apparent that DPV of each frequency cannot get its maximum value meanwhile

$$u_{x1-mn}-u_{x2-mn} \leq F_{1mn}+F_{2mn}. \tag{15}$$

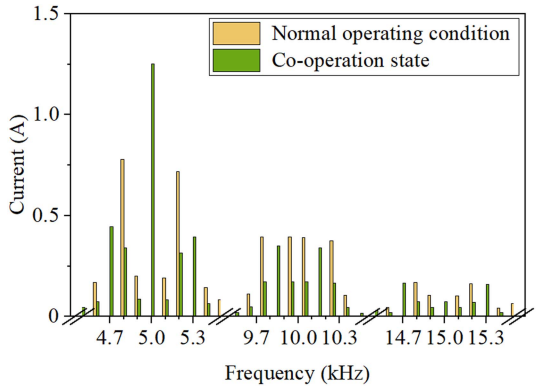


Fig. 6. High-frequency current comparison between normal operating condition and transient state.

Fig. 6 illustrates the high-frequency current of the normal operating condition and the co-operation state. The latter represents the maximum values of each frequency, although they cannot exist at the same time. There is about 65% increase in the maximum amplitude of high-frequency current from Fig. 6. According to the general grid codes, the high-frequency current under the normal operating condition has already been sufficiently suppressed, so a 65% increase is not enough to cause damage to the equipment. Consequently, the device can tolerate the high-frequency current by synchronizing the carrier phase difference to zero.

D. Robustness of the Synchronization Modulation Strategy

The operation of the proposed synchronization modulation strategy is to keep the phase difference at zero, and the current or the voltage does not need to be measured to fed back to the control system. Therefore, the sampling disturbance cannot influence the suppression of the high-frequency overcurrent. Additionally, the phase difference is synchronized at regular intervals to ensure the consistency of the time bases between different microprocessors. Although there may be a slight difference between the time bases of different microprocessors, it

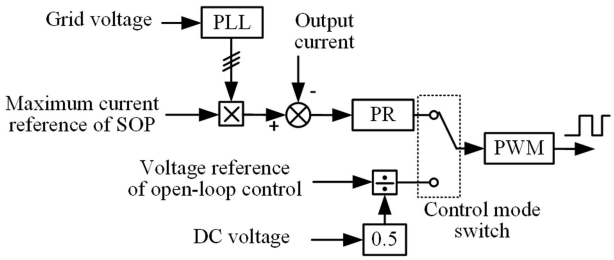


Fig. 7. Control block diagram of B2B-type SOP during switching process.

is negligible. Even if the synchronizing signal is disturbed, and the phase synchronization cannot be realized for a few switching cycles, the phase difference of the carriers will not become very large. For the switching process, the duration time of a few switching cycles is transitory.

In conclusion, the robustness of the synchronization modulation strategy is acceptable.

IV. Control Strategy

There are several intermediate states during the switching process, and the voltage and current will change with the control mode switching. The main stages and corresponding requirements for HSOP are as follows.

1) The SOP restores the outage load, as shown in Fig. 2(c): During this stage, the SOP initially outputs its maximum current at first, as it needs to quickly support the load voltage. However, the mismatch between SOP's capacity and load may cause voltage sags during this stage.
2) The co-operation state, as shown in Fig. 2(d): The close action of the interconnection switch connects the normal grid to the fault side, the voltage of which is supported by SOP before that. The output voltage of SOP must track the grid voltage to avoid the overcurrent.

A. B2B-Type SOP Restores Load

The control mode switching process is proposed, and the block diagram of the fault-side VSC is drawn in Fig. 7, where the converter is still controlled as a current source to output its maximum current. In the majority of cases, the power of the outage load is larger than the capacity of the SOP. Consequently, it is appropriate for SOP to be controlled as a current source to output its maximum current, and the load voltage will be below the rated value. Nevertheless, the load voltage will exceed the rated value when the outage load power is smaller than the capacity of the SOP. In such a situation, the SOP should restrict its output voltage. To achieve rapid voltage support in this stage, the open-loop control is applied instead of the voltage control loop, which has a slow response speed.

The flowchart of this control system is depicted in Fig. 8, and the control mode switching criterion is whether the output voltage crosses the threshold. If not, the outage load's power is larger than the capacity of SOP, and it keeps outputting maximum current. On the contrary, the open-loop control is applied.

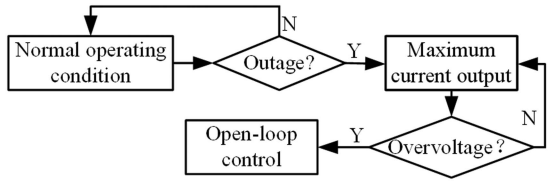


Fig. 8. Flowchart of B2B-type SOP diverting outage load.

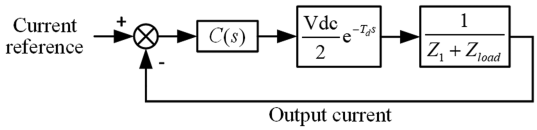


Fig. 9. System block diagram when B2B-type SOP restores load.

Under the current control, the system's model is drawn in Fig. 9, and the PR controller is chosen to realize the precise control effects. Besides the precise aims of the control system, the bandwidth is critical as well in this scenario. The expression of the loop gain can be easily obtained from Fig. 9. Based on the bode plot of the loop gain, the increasing proportional coefficient can improve the bandwidth but decreases the stability margin. In contrast, increasing the resonant coefficient would not decrease the stability margin but still improve the response speed. As a result, increasing the resonant coefficient after the power outage is detected can guarantee a better voltage supporting ability. Eventually, the resonant coefficient under this state is set as 2.5.

B. Co-Operation State

Due to the time delay caused by the detecting threshold setting, sampling, digital control, and the switching action of semiconductors, the SOP cannot exit the operation immediately at the moment of the switch closure. The voltage difference between the two ends of the interconnection switch will lead to the low-frequency overcurrent.

The evolution of the average model of (1), where the switching actions are neglected, is given by (16). The approximate reason in (16) is based on the similarity between the converter output voltage of the normal side and the grid voltage

$$\begin{aligned} i_{xk} &= \frac{Z_2/2}{Z_1\left(Z_{\text{eq}}+Z_2\right)}\left(u_{xk}-u_{x,(3-k)}\right) \\ &\quad + \frac{1}{2\left(Z_{\text{eq}}+Z_2\right)}\left(u_{xk}-u_{gx}\right) \\ &\approx \left[\frac{Z_2/2}{Z_1\left(Z_{\text{eq}}+Z_2\right)}+\frac{1}{2\left(Z_{\text{eq}}+Z_2\right)}\right]\left(u_{xk}-u_{gx}\right) \end{aligned} \tag{16}$$

where u_{xk} is the average value of the VSC_k.

When the power of the outage load is smaller than the capacity of the SOP, it is controlled by the open-loop. Based on (16), the voltage reference of the open-loop control in Fig. 7 uses the grid voltage of the normal operating side to restrain the overcurrent.

When the power of the outage load is larger than the capacity of the SOP, the approximated system block diagram is drawn

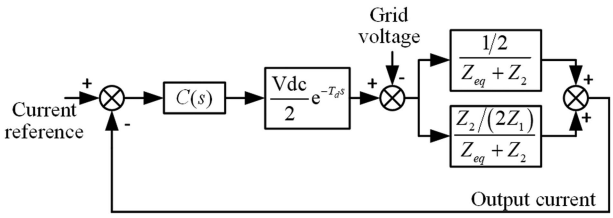


Fig. 10. System block diagram when SOP and NOP work together.

in Fig. 10. The grid voltage, e_g, in Fig. 10 is the step sinusoidal signal, with the time-domain and frequency-domain expressions written in the following equations:

$$e_g(t) = E_g \cos(\omega_o t + \theta_g)\,\varepsilon(t) \tag{17}$$

$$E(s) = \frac{E_g e^{j\theta_g}}{s - j\omega_0} \tag{18}$$

where E_g is the amplitude of the grid voltage, and θ_g is the phase of the grid voltage at the moment of the switch closure.

The output current caused by the step grid voltage can be derived as follows:

$$I_e(s) = \frac{E_g e^{j\theta_g}}{s - j\omega_0} \cdot H(s) \tag{19}$$

where $H(s)$ is the closed-loop transfer function of system structure, and the detailed expression can be derived from Fig. 10.

Assuming θ_g is equal to 0, the time-domain waveform of output current caused by the step grid voltage can be calculated using *Laplace inverse transform*. The results are shown in Fig. 11. K_p and K_r represent the proportional coefficient and the resonant coefficient of the PR controller, respectively, and T_d represents the time delay of the whole control system.

According to the theoretical computation results, increasing the resonant coefficient can only improve the decay rate of the overcurrent but has an insignificant effect on the overcurrent's amplitude. Instead, increasing the proportional coefficient can reduce the amplitude of the overcurrent. The reason is that increasing the resonant coefficient has no effect on increasing the bandwidth of the system, in contrast to increasing the proportional coefficient. However, increasing the proportional coefficient brings about the stability issues. The effect of decreasing digital control delay on overcurrent is negligible. Consequently, the overcurrent cannot be suppressed by optimizing the values of the control parameters in the conventional current control.

Based on the virtual impedance, an overcurrent limited strategy is proposed in this article, the control block diagram of which is depicted in Fig. 12(a). The voltage of filter inductance is calculated by the sampled output current and is added to the modulation wave directly after normalization. K_{ff} is the virtual impedance coefficient. The virtual impedance used in this proposed strategy can be regarded as the modification of the feedback coefficient, and the equivalent block diagram is shown in Fig. 12(b). The modified feedback coefficient can be expressed as follows:

$$F(s) = K_{ff}\frac{2L_1}{C(s)\,\mathrm{V_{dc}}}s + 1 \tag{20}$$

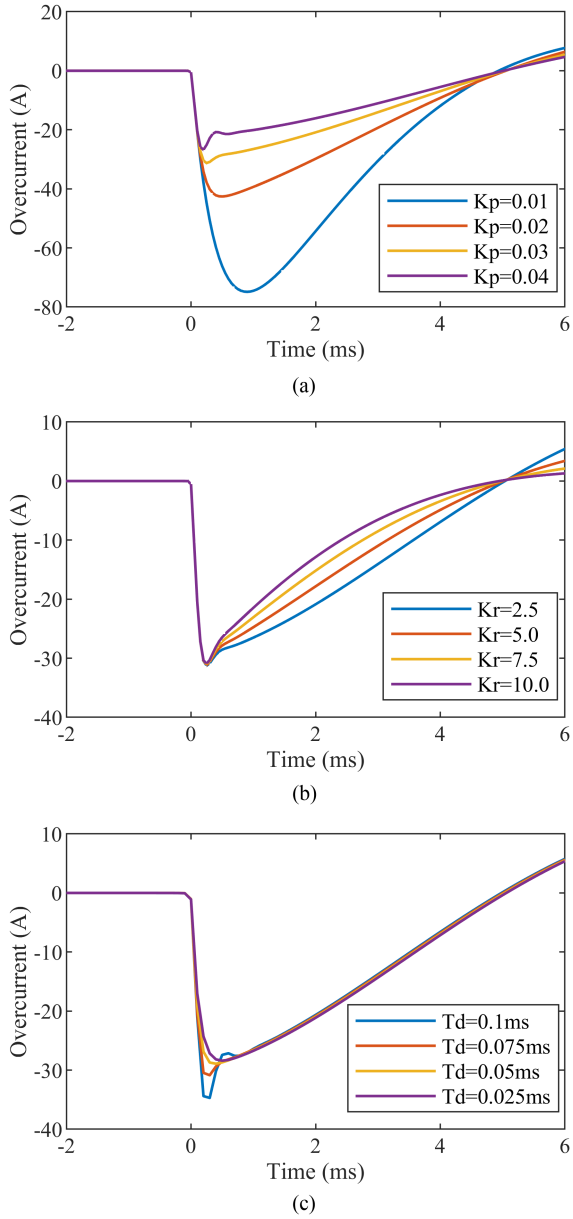


Fig. 11. Time-domain waveform of output current caused by grid voltage under different conditions. (a) Different proportional coefficient ($K_r = 2.5$, $T_d = 0.05$ ms). (b) Different resonant coefficient ($K_p = 0.03$, $T_d = 0.05$ ms). (c) Different delay time ($K_p = 0.01$, $K_r = 2.5$).

where $C(s)$ is the transfer function of the PR controller, L is the filter inductance derived from (16), and $F(s)$ is the modified feedback coefficient.

The bode plot of the modified feedback transfer function is illustrated in Fig. 13, showing significant increases in gain in the high-frequency band. The modified feedback coefficient presents a characteristic of the phase compensation. After adding virtual impedance to the control system, the loop gain of the system can be expressed as follows:

$$T(s) = C(s) \cdot \frac{\mathrm{V_{dc}}}{2} e^{-T_d s} \cdot F(s) \cdot \frac{1}{Z} \tag{21}$$

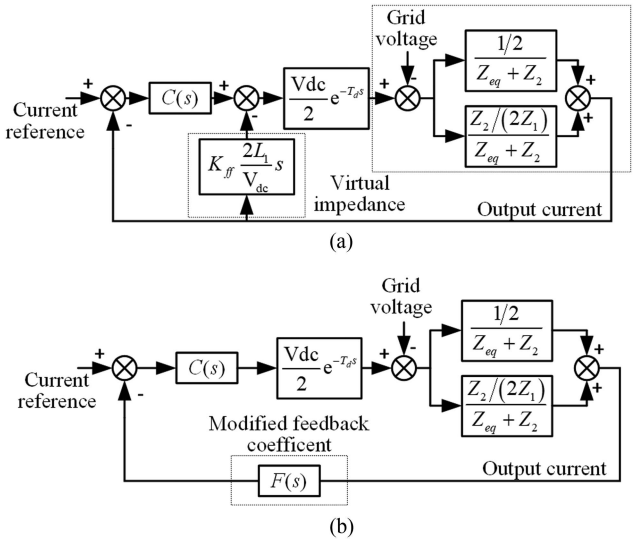


Fig. 12. Control block diagram of overcurrent limited strategy. (a) System block diagram with virtual impedance. (b) Equivalent block diagram.

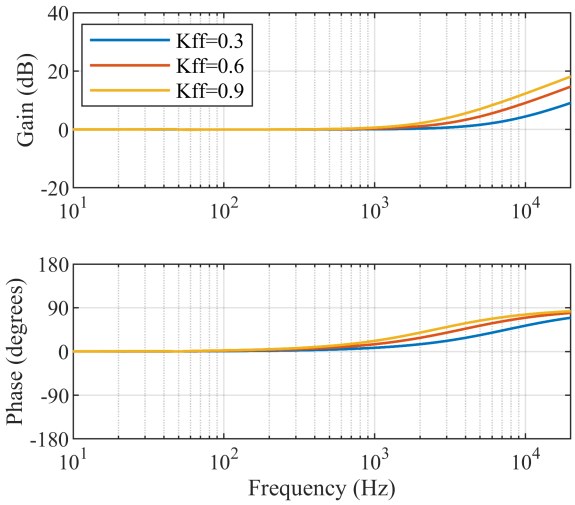


Fig. 13. Bode plot of modified feedback transfer function.

where T_d is the delay time of digital controller, Z is the equivalent impedance between the VSC and the grid, and $T(s)$ represents the loop gain.

The order of the numerator and the denominator is equal, resulting in the loop gain approaching a constant value rather than negative infinity. The limit value is calculated by the following:

$$\lim_{s\to\infty} |T(s)| = K_{ff}. \tag{22}$$

Consequently, the impedance coefficient K_{ff} must be smaller than 1; otherwise, the system is unstable.

To illustrate the effect of the proposed method, three sets of parameters are selected, as listed in Table IV. First, compare the group A and the group B, and the function of the virtual impedance can be demonstrated.

Fig. 14 presents the bode plot of the loop gain with these parameters. According to this figure, the influence of the virtual

TABLE IV
COMPARISON OF CONTROL PARAMETERS

Group number	K_p	K_{ff}
A	0.01	0
B	0.01	0.8
C	0.03	0.3

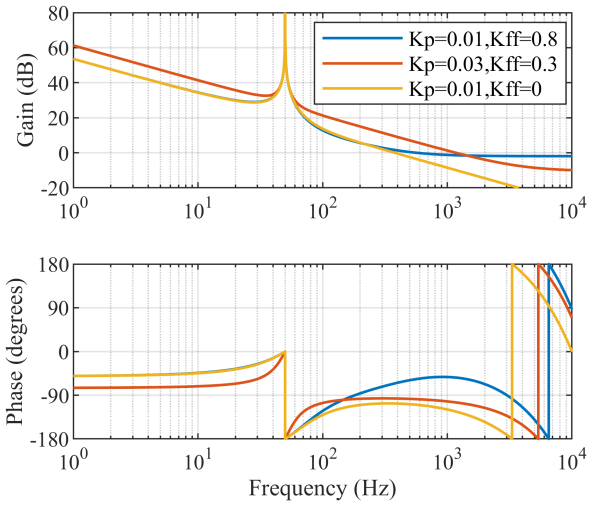


Fig. 14. Bode plots of loop gain with different control coefficients.

impedance coefficient on the bandwidth is inconspicuous compared to increasing the proportional coefficient. Meanwhile, the gain margin is decreased, which lets the loss outweigh the gain. For better stability, the value of K_{ff} is recommended to be less than 0.5 to achieve a gain margin of around 6 dB. In addition, due to the phase compensation of the virtual impedance, the proportional coefficient has more zoom to be increased without causing stability problems. Therefore, it is helpful for both stability and response speed to choose a smaller impedance coefficient and increase the proportional coefficient, which is reflected by the group C. After applying the values of the group C, the bandwidth of the loop gain increases significantly without the stability issues.

Laplace Transform is typically used to analyze transient signals, and the frequency-spectrum of the output current caused by the step grid voltage input is depicted in Fig. 15. Adding the virtual impedance can slightly reduce the components of the high-frequency band, while increasing the proportional coefficient at the same time can reduce the components except for the fundamental component. The numerical computation results of the time-domain output current are shown in Fig. 16. Because of the fewer high-frequency components after adding the virtual impedance, the overcurrent has a slower rising speed compared to that without the virtual impedance. The overcurrent suppression effect of adding the virtual impedance and increasing the proportional coefficient simultaneously is much better than in the original condition.

In conclusion, based on the results of Figs. 14 and 16, the effect of the virtual impedance can be summarized in two aspects.

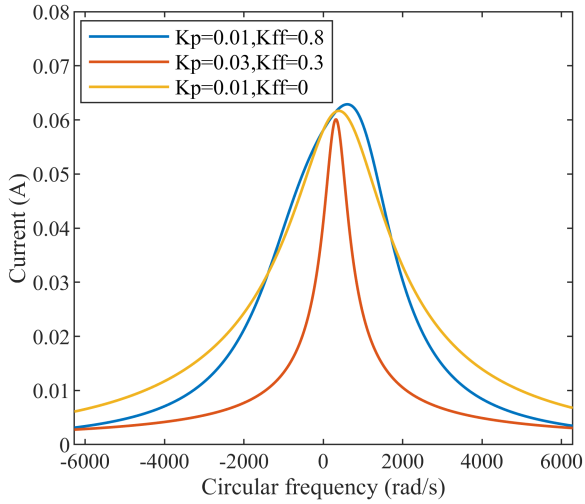


Fig. 15. Spectrum of output current caused by step gird voltage input (Damping coefficient = 10).

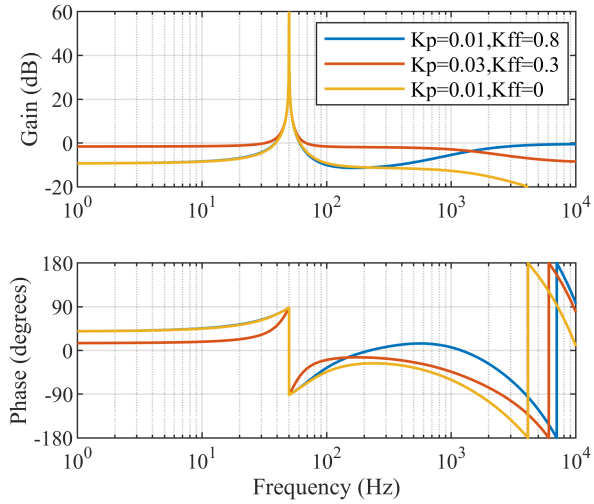


Fig. 17. Bode plot of loop gain when B2B-type SOP restores load (with virtual impedance).

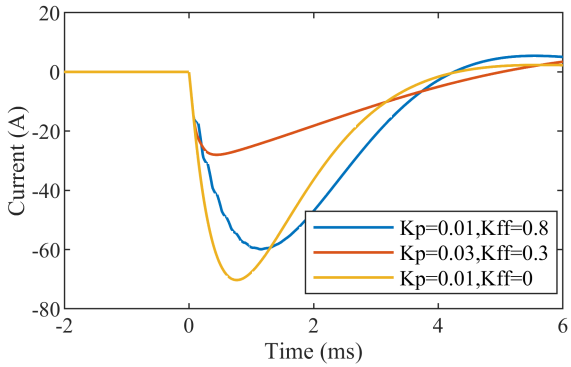


Fig. 16. Numerical computation results of time-domain output current.

1) Compensate for the phase margin, enabling a larger proportional coefficient.
2) Reduce the rate of overcurrent generation.

Building upon the aforementioned capability of the virtual impedance, the proposed method effectively suppresses overcurrent at the instant of the interconnection switch closure.

Commencing from the instant the SOP initiates the restoration of the outage load, the virtual impedance ought to be incorporated into the control system. Fig. 17 illustrates the bode plot of the control system with the virtual impedance when SOP restores the load, indicating that the addition of the virtual impedance solely influences the high-frequency range. Thus, the value of the resonant coefficient can adopt the prior design in Section IV-A.

C. Robustness of the Control Strategy and Analysis of the Bouncing Behavior of the Mechanical Switch

Compared to the original control system, the proposed control strategy only requires one additional multiplication and two additions, without increasing the complexity of the control system. This is beneficial for the robustness.

In addition, the bouncing behavior of the mechanical switch is the most significant disturbance during the switching process, as it essentially involves repetitive switching between the ON and OFF states. Each time the switch closes, the proposed control system can respond to the step grid voltage, which is the primary focus of this article. Therefore, the bouncing behavior does not pose a threat of equipment damage. In conclusion, the proposed current limited strategy demonstrates acceptable robustness.

V. Simulation Verification

The focus of this article is on the overcurrent and the overvoltage during the switching process of HSOP. Consequently, the criteria for assessing the effectiveness of the proposed method are whether the overcurrent and the overvoltage will cause damage to the equipment. The effect of the proposed method will be demonstrated by comparing the amplitude of the current and the voltage with that of normal operating conditions or conditions without the proposed method.

In this section, the simulation model of HSOP, based on Table I, is set up in PLECS. The semiconductors (IGBT and diode) used in the simulation model are based on the ideal model. The high-frequency current spectrum is analyzed during the switching process, and the proposed current limited strategy is verified.

A. Analysis on High-Frequency Current of Switching Process

As indicated by (15), the phases of converters' modulation waves are typically unequal. However, a larger fundamental frequency overcurrent occurs when there is a phase difference in the modulation waves. To emphasize the high-frequency current rather than the fundamental frequency overcurrent, the modulation waves of two converters have been set to be the same, with the difference lying in the carrier wave.

In Fig. 18, the amplitude of the current at different frequencies is illustrated with varying carrier wave phase differences through

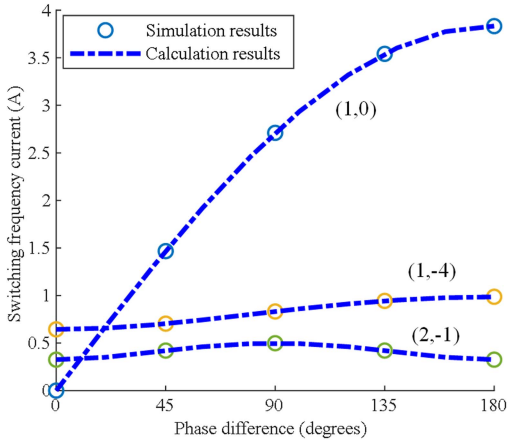


Fig. 18. Amplitude of switching frequency current in steady state.

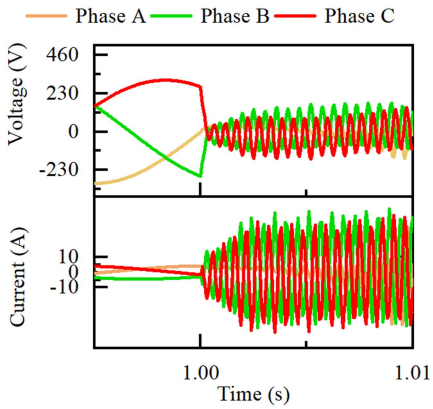


Fig. 19. Instable waveform when the SOP starts to restores the outage load ($K_p = 0.03$, $K_r = 0.25$).

both the simulation and the theoretical calculation. It is evident that the mathematical model of current is accurate.

B. Control Strategy of B2B-Type SOP Restoring Load

Under this stage, the instability will be caused if the proportional coefficient is excessively large, as shown in Fig. 19. As depicted in Fig. 20, the overvoltage will manifest if the SOP outputs its maximum current despite the light load. Moreover, the overmodulation is generated when the output voltage of the SOP is too high, leading to the harmonics caused by the overmodulation. Fig. 21 gives the transient waveforms of the voltage and the current when the outage occurs. The maximum output current of the SOP is set as 10 A (the maximum capacity of the SOP is around 5 kW). In Fig. 21(a), where the power of the outage load surpasses the capacity, the SOP keeps outputting its maximum current, and the load voltage is lower than the rated value. In Fig. 21(b) and (c), when the load voltage reaches the threshold value, the system transitions into open-loop control since the outage load is less than the capacity.

LCL filter may be applied to some converters at its ac port to eliminate the high-frequency ripple preferably. In such scenarios, the resonance point of the *LCL* filter can induce oscillations

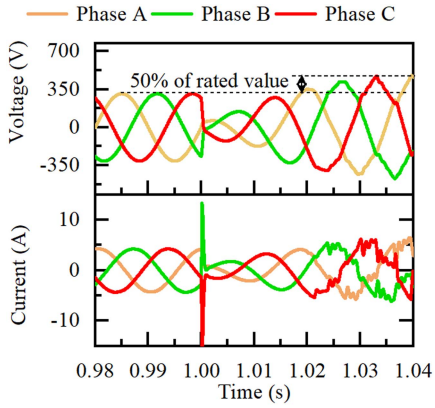


Fig. 20. Overvoltage caused by the light load without the proposed switching control strategy (the power of the outage load is 3.6 kW).

when the control system transition to the open-loop control, as illustrated in Fig. 22. The oscillation frequency, approximately 1 kHz in simulation, is determined by the system impedance when the SOP restores the outage load. The system impedance can be expressed as (23) and the absolute value based on simulation parameters is depicted in Fig. 23

$$Z_{\text{system}} = j\omega L_c + \frac{Z_{\text{load}}\left(j\omega L_g - j/\omega C_f\right)}{Z_{\text{load}} + j\omega L_g - j/\omega C_f} \tag{23}$$

where L_c and L_g are the filter inductance of the converter side and the gird side, respectively, C_f is the capacitance of the *LCL* filter, and Z_{load} is the impedance of the outage load.

According to Fig. 23, the impedance reaches its minimum value at 1 kHz, which corresponds to the oscillation frequency in Fig. 22. Several studies have explored the addition of damping to the *LCL* filter using active or passive methods [43], [44]. Implementing these methods can effectively address the oscillation issue shown in Fig. 22.

C. Overcurrent Limited Strategy When Interconnection Closes

Fig. 24 depicts the current and voltage waveforms when the interconnection switch closes under the light load conditions. Since the open-loop voltage reference is selected as the grid voltage of the normal operating side, there is minimal current insurge.

Fig. 25 illustrates the overcurrent resulting from the closure of the interconnection switch under overload conditions with different control parameters. The simulation results show that widening the bandwidth of the current control loop contributes to the suppression of overcurrent. Without the virtual impedance, the simulated overcurrent exceeds 40 A. Instead, the addition of the virtual impedance control has a marginal inhibitory effect on overcurrent, for offering a slight improvement in bandwidth. However, with the proper impedance coefficient and increased proportional coefficient, the overcurrent can be completely suppressed. The simulation results are in agreement with the previous theoretical analysis.

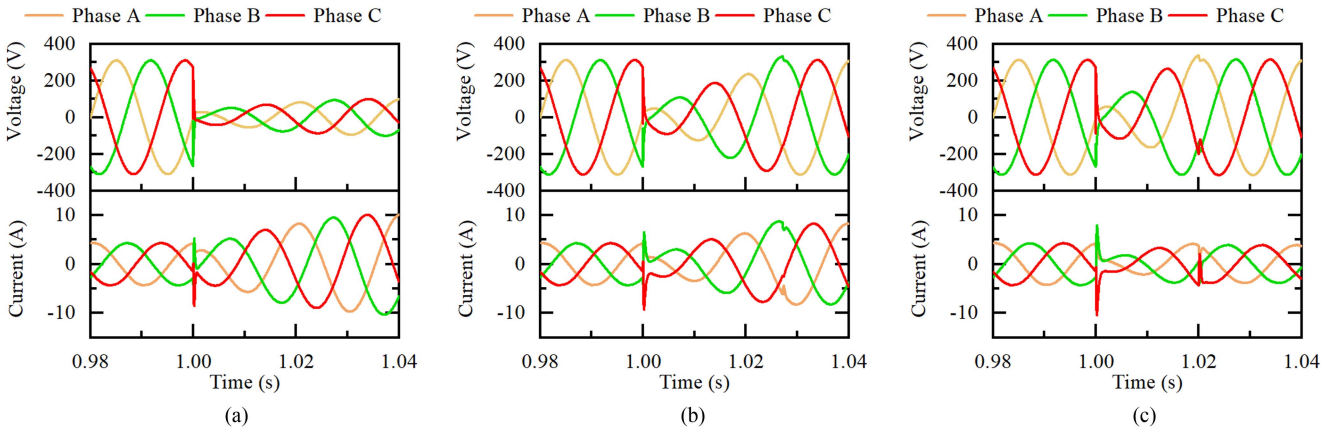


Fig. 21. Transient waveforms when SOP restores the outage load. (a) Outage power is 15 kW. (b) Outage power is 3.6 kW. (c) Outage power is 1.5 kW.

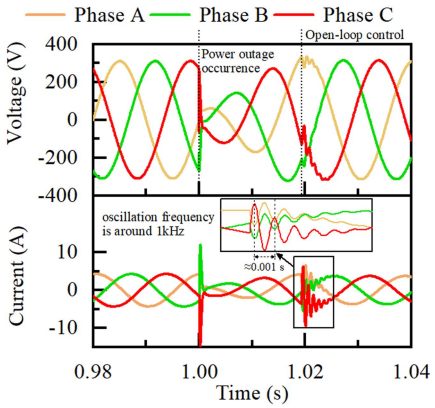


Fig. 22. Transient waveforms when SOP restores the outage load (with *LCL* filter and light load).

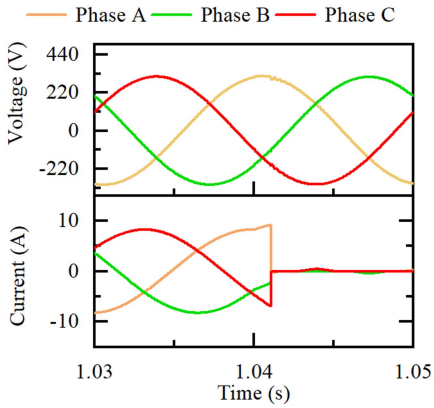


Fig. 24. Transient waveforms when the interconnection switch closes (light load).

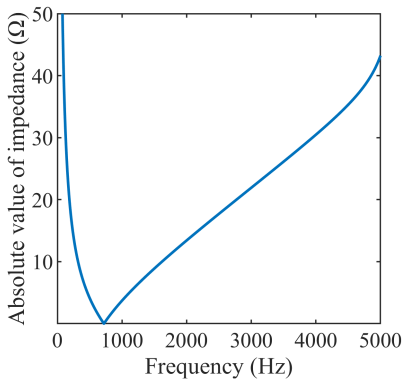


Fig. 23. Absolute value of System equivalent impedance when SOP restores the outage load.

TABLE V
PARAMETERS OF EXPERIMENT PLATFORM

Item	Value
Grid line-voltage	110 V
DC voltage	200 V
Filter inductance	1.2 mH
Load power	900 W
Maximum current set for SOP	3.5 A
Fundamental frequency	50 Hz
Switching frequency	5 kHz

VI. EXPERIMENTAL RESULTS

A downscaled experimental platform of HSOP is depicted in Fig. 26. The reverse parallel thyristors are used to emulate the interconnection switch for their precisely controlled conduction time. The controller adopts TMS320F28377D from Texas Instruments, and the grid simulator adopts IT7909 from Itech Electronic. The hardware of the B2B-type SOP, along with the control blocks and sensing terminals, is designed by the research group. Other parameters of the experimental platform are listen in Table V. Given that this article focuses on the transient analysis of HSOP, the overvoltage and overcurrent may appear during the experimental process. To safeguard the experimental platform, the voltage and current values are deliberately selected to be lower than those in the simulation.

The experimental results will be described and analyzed in the sequence of the entire switching process under heavy load or light load conditions.

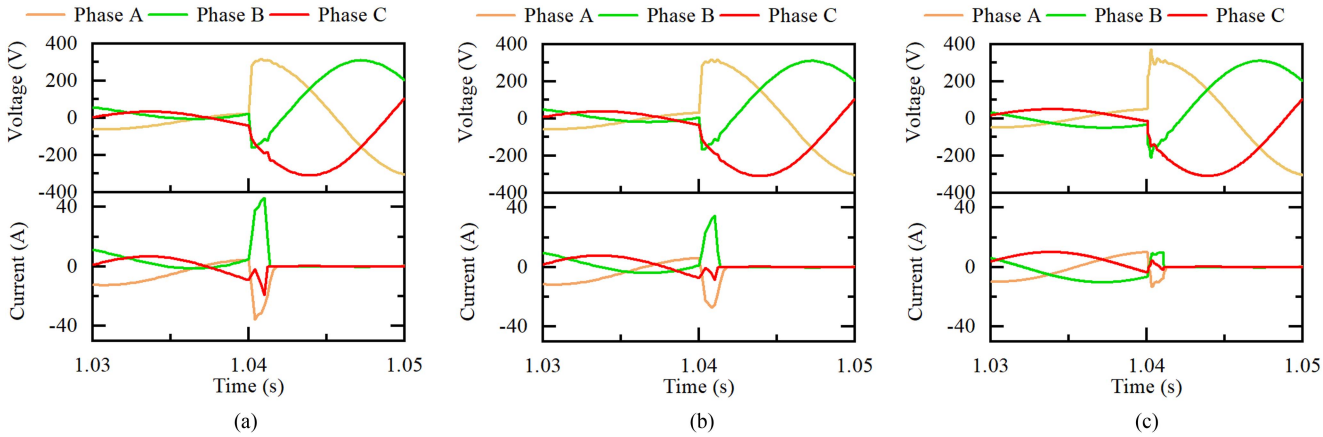


Fig. 25. Transient waveforms when the interconnection switch closes (overload). (a) $K_p = 0.01$, $K_{ff} = 0$. (b) $K_p = 0.01$, $K_{ff} = 0.8$. (c) $K_p = 0.03$, $K_{ff} = 0.3$.

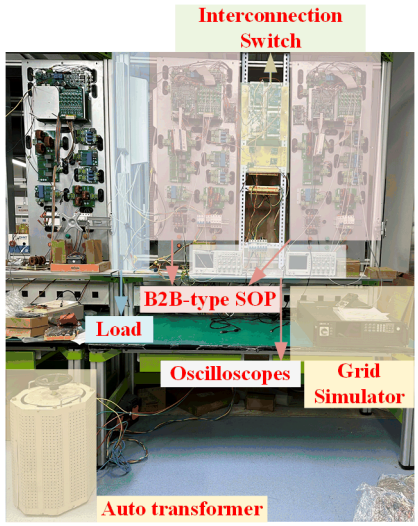


Fig. 26. Experimental platform of HSOP.

A. Stage 1 of Heavy Load: Supply Restoration by SOP

As analyzed before, the resonance coefficient is critical for the response speed, while the proportional coefficient is the key to maintaining stability during this stage. Fig. 27 shows the period from the power outage to the load restoration with the SOP, excluding the process of the interconnection switch closing, which will be presented in the following part. Fig. 27(a) and (b) demonstrate that an improper resonance coefficient impedes the system from achieving a sufficiently rapid response speed, and a large proportional coefficient can increase the bandwidth but lose the stability. Fig. 27(c) indicates a responsive and stable system with appropriately tuned parameters.

B. Stage 2 of Heavy Load: Co-Operation State

In this stage, the closure of the interconnection switch causes an abrupt change in the grid voltage of the outage side converter. Fig. 28 represents the waveforms of the voltage and current during the co-operation state with different control structures

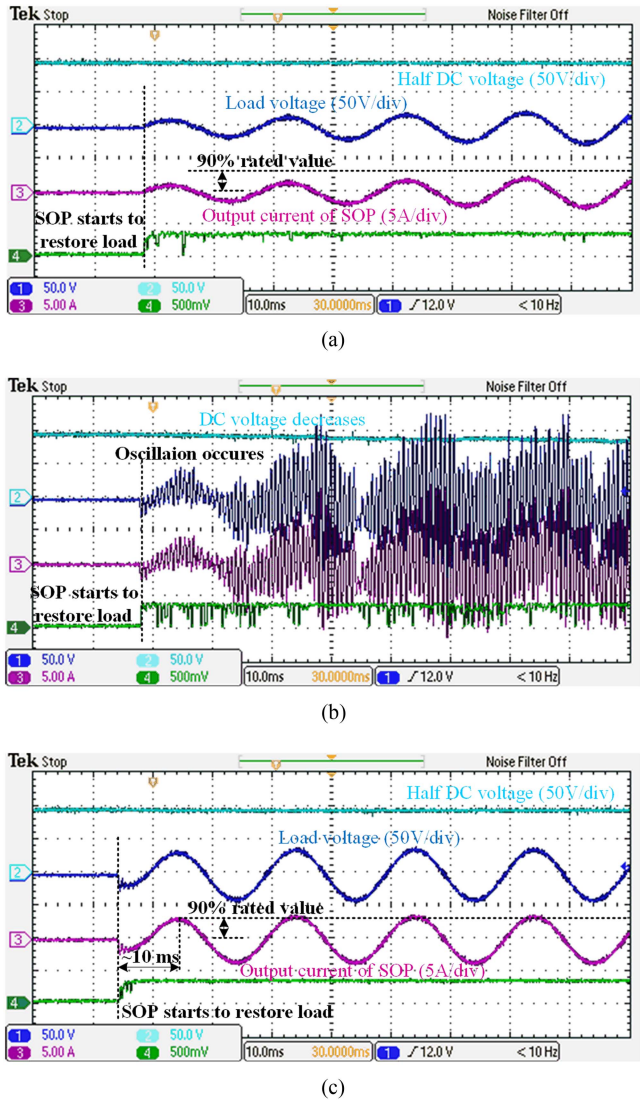


Fig. 27. Transient experiment waveforms when SOP restores load. (a) Resonant coefficient is too small ($K_p = 0.06$, $K_r = 0.3$). (b) Proportional coefficient is too large ($K_p = 0.18$, $K_r = 1.75$). (c) Resonant coefficient and proportional coefficient are suitable ($K_p = 0.06$, $K_r = 1.75$).

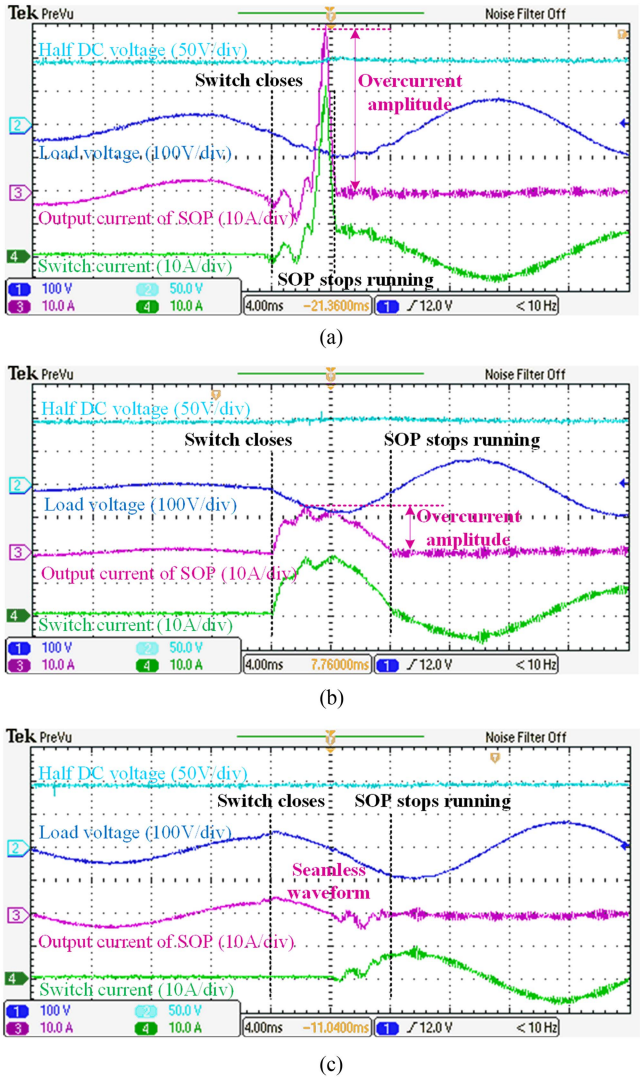


Fig. 28. Transient experiment waveforms when the interconnection switch closes. (a) Without virtual impedance ($K_p = 0.06, K_{ff} = 0$). (b) Large impedance coefficient but small proportional coefficient ($K_p = 0.06, K_{ff} = 0.8$). (c) Suitable impedance coefficient and increased proportional coefficient ($K_p = 0.18, K_{ff} = 0.3$).

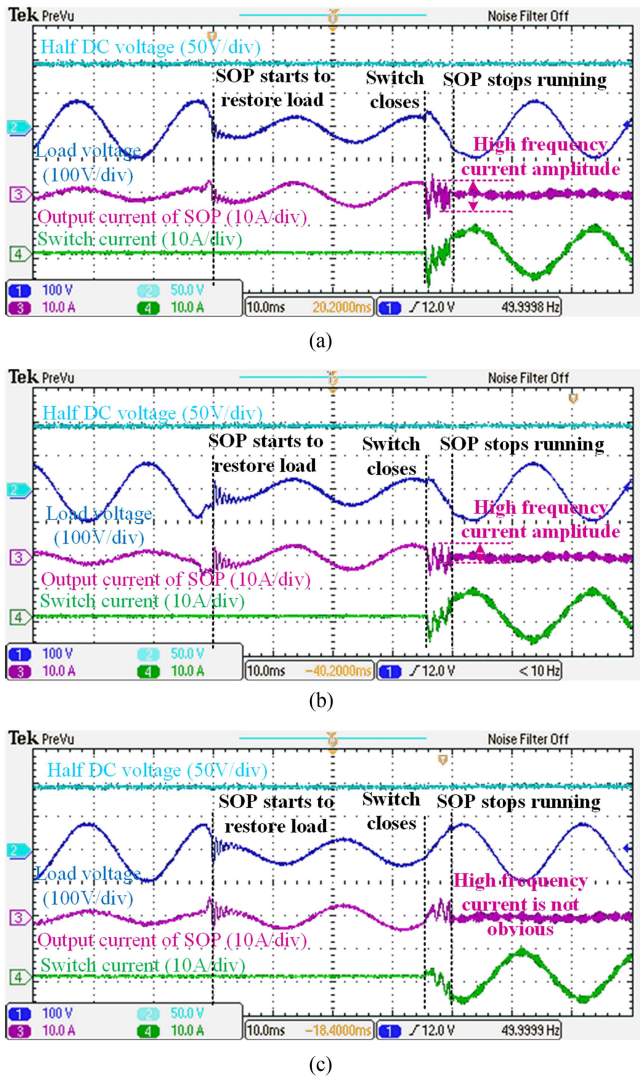


Fig. 29. Experiment waveforms of the entire switching process with different angle difference. (a) Angle difference is 180°. (b) Angle difference is 90°. (c) Angle difference is 0°.

or parameters. Utilizing the original control strategy without the virtual impedance, the experimental result is as Fig. 28(a), where the overcurrent of nearly 40 A appears, significantly exceeding the maximum current set of the SOP. By incorporating the virtual impedance, the overcurrent can be reduced to 10 A, as depicted in Fig. 28(b). In Fig. 28(c), increasing the proportional coefficient simultaneously with the virtual impedance eliminates the overcurrent.

C. Stage 3 of Heavy Load: High-Frequency Current Observation at the Moment When Interconnection Switch Closes

When PD-PWM is applied to the SOP, the phase difference between two VSCs' carrier waves becomes a key factor influencing the high-frequency overcurrent. Fig. 29 illustrates the entire switching process, encompassing the occurrence of the power outage, supply restoration with the SOP, and the closure of the interconnection switch. According to the experimental waveforms in Fig. 29, the amplitude of the high-frequency current reaches the worst situation when the phase difference is 180°, with the peak-to-peak value of the high-frequency current reaching nearly 8 A. In contrast, the high-frequency current is insignificant after achieving carrier phase synchronization at 0°.

D. Light Load Conditions

Under light load conditions, the control strategy of HSOP switches to the open-loop control. Fig. 30 shows the entire switching process when the maximum current set of the SOP is changed to 10 A. Following a power outage, the HSOP outputs its maximum current, and open-loop control is applied within 2 ms.

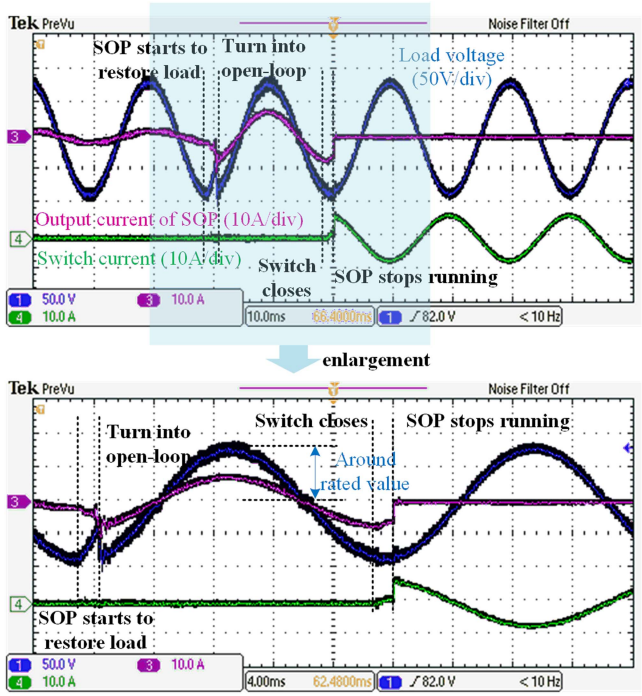


Fig. 30. Experiment waveforms of the entire switching process under light load.

VII. Conclusion

The seamless switching process of an HSOP under the power outage is comprehensively analyzed in this article. For the fast supply restoration, a co-operation state is introduced during the switching process, which contains a short-circuit loop between the parallel-operating SOP and NOP. Hence, with a focus on the co-operation state of HSOP, the main contributions of this article are summarized as follows.

1) By keeping the phase difference at zero when PD-PWM is applied, the maximum amplitude of the high-frequency transiting current can be suppressed to a comparable level to that of normal switching ripple.
2) In the event of a power outage with the light load, a transiting current limiting strategy involving the open-loop control and an increased resonance coefficient is introduced, which can quickly restore the nominal power supply within 20 ms.
3) For the power outage with the heavy load, the transiting overcurrent is mainly caused by the grid voltage step, and a transiting current limiting strategy based on the proper virtual impedance is proposed.

By interconnecting the distribution networks through HSOP, the flexibility can be significantly enhanced. This article provides a detailed analysis of HSOP from the equipment perspective. Future research works will delve into the system level, exploring collaborative coordination between HSOP, DG, and protective devices, which enhance the application of HSOP in distribution systems.

References

[1] Y. Bian, C. Chen, Y. Huang, Z. Bie, and J. P. S. Catalão, "Service restoration for resilient distribution systems coordinated with damage assessment," *IEEE Trans. Power Syst.*, vol. 37, no. 5, pp. 3792–3804, Sep. 2022, doi: 10.1109/TPWRS.2021.3137257.

[2] X. Sun, J. Chen, H. Zhao, W. Zhang, and Y. Zhang, "Sequential disaster recovery strategy for resilient distribution network based on cyber–physical collaborative optimization," *IEEE Trans. Smart Grid*, vol. 14, no. 2, pp. 1173–1187, Mar. 2023, doi: 10.1109/TSG.2022.3198696.

[3] H. Zhang, C. Chen, S. Lei, and Z. Bie, "Resilient distribution system restoration with communication recovery by drone small cells," *IEEE Trans. Smart Grid*, vol. 14, no. 2, pp. 1325–1328, Mar. 2023, doi: 10.1109/TSG.2022.3210771.

[4] Y. Du, H. Tu, X. Lu, J. Wang, and S. Lukic, "Black-start and service restoration in resilient distribution systems with dynamic microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 4, pp. 3975–3986, Aug. 2022, doi: 10.1109/JESTPE.2021.3071765.

[5] X. Jiang, Y. Zhou, W. Ming, P. Yang, and J. Wu, "An overview of soft open points in electricity distribution networks," *IEEE Trans. Smart Grid*, vol. 13, no. 3, pp. 1899–1910, May 2022, doi: 10.1109/TSG.2022.3148599.

[6] P. Li, J. Ji, H. Ji, G. Song, C. Wang, and J. Wu, "Self-healing oriented supply restoration method based on the coordination of multiple SOPs in active distribution networks," *Energy*, vol. 195, Mar. 2020, Art. no. 116968.

[7] H. Ji, C. Wang, P. Li, G. Song, and J. Wu, "SOP-based islanding partition method of active distribution networks considering the characteristics of DG, energy storage system and load," *Energy*, vol. 155, pp. 312–325, Jul. 2018.

[8] Z. Ma, J. Chen, Z. Fang, Y. Hao, and G. Yang, "A seamless transfer control strategy of SNOP for the critical load safety under network faults," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf.*, 2020, pp. 2347–2351, doi: 10.1109/IPEMC-ECCEAsia48364.2020.9367728.

[9] C. Wang, J. Sun, M. Huang, X. Zha, and W. Hu, "Two-stage optimization for active distribution systems based on operating ranges of soft open points and energy storage system," *J. Modern Power Syst. Clean Energy*, vol. 11, no. 1, pp. 66–79, Jan. 2023, doi: 10.35833/MPCE.2022.000303.

[10] T. Heggarty, J.-Y. Bourmaud, R. Girard, and G. Kariniotakis, "Multitemporal assessment of power system flexibility requirement," *Appl. Energy*, vol. 238, pp. 1327–1336, 2019.

[11] R. You and X. Lu, "Voltage unbalance compensation in distribution feeders using soft open points," *J. Modern Power Syst. Clean Energy*, vol. 10, no. 4, pp. 1000–1008, Jul. 2022, doi: 10.35833/MPCE.2021.000565.

[12] M. Deakin et al., "Hybrid open points: An efficient tool for increasing network capacity in distribution systems," *IEEE Trans. Power Del.*, vol. 37, no. 2, pp. 1340–1343, Apr. 2022, doi: 10.1109/TPWRD.2021.3136772.

[13] W. Cao, J. Wu, and N. Jenkins, "Feeder load balancing in MV distribution networks using soft normally-open points," in *Proc. IEEE PES Innov. Smart Grid Technol.*, 2014, pp. 1–6, doi: 10.1109/ISGTEurope.2014.7028874.

[14] Y. Li, X. Pei, Z. Chen, M. Yang, Z. Lyu, and C. Wang, "The steady-state and fault ride-through control strategies of soft normally open point in distribution network," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 1146–1150, doi: 10.1109/ECCE.2018.8557615.

[15] X. Ge, M. Shi, C. Zhang, W. Gao, and F. Zhang, "A low-cost hybrid back-to-back soft open point," in *Proc. IEEE 1st China Int. Youth Conf. Elect. Eng.*, 2020, pp. 1–6, doi: 10.1109/CIYCEE49808.2020.9332640.

[16] R. An, J. Liu, Z. Liu, and Z. Song, "Flexible transfer converters enabling autonomous control and power dispatch of microgrids," *IEEE Trans. Power Electron.*, vol. 37, no. 11, pp. 13767–13781, Nov. 2022, doi: 10.1109/TPEL.2022.3180562.

[17] Y. Li et al., "Research on interconnection structure and control technology of flexible distribution network based on soft open point in parallel with interconnection switch," *Proc. CSEE*, vol. 42, no. 13, pp. 4749–4760, Jul. 2022, doi: 10.13334/j.0258-8013.pcsee.210479.

[18] T. Xu, X. Ge, J. Dou, M. Shi, C. Zhang, and H. Miao, "Technology of hybrid back-to-back soft open point," *Elect. Power Eng. Technol.*, vol. 40, no. 4, pp. 130–135, Jul. 2021, doi: 10.12158/j.2096-3203.2021.04.018.

[19] Z. Lai, X. Zhang, H. Yi, K. Fu, F. Zhuo, and K. Zhao, "Transient analysis on transfer process of hybrid soft open point under power grid outage," in *Proc. IEEE Int. Power Electron. Application Conf. Expo.*, 2022, pp. 355–360, doi: 10.1109/PEAC56338.2022.9959556.

[20] H. Xu, L. Xu, C. Li, K. Wang, Z. Zheng, and Y. Li, "Improved interleaved discontinuous PWM for zero-sequence circulating current reduction in three-phase paralleled converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 8676–8686, Sep. 2021, doi: 10.1109/TIE.2020.3016273.

[21] W. Jiang, W. Ma, J. Wang, W. Wang, X. Zhang, and L. Wang, "Suppression of zero sequence circulating current for parallel three-phase grid-connected converters using hybrid modulation strategy," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3017–3026, Apr. 2018, doi: 10.1109/TIE.2017.2750625.

[22] J. Wang, F. Hu, W. Jiang, W. Wang, and Y. Gao, "Investigation of zero sequence circulating current suppression for parallel three-phase grid-connected converters without communication," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 7620–7629, Oct. 2018, doi: 10.1109/TIE.2018.2798613.

[23] X. Li, X. Xing, C. Qin, C. Zhang, and G. Zhang, "Design and control method to suppress resonance circulating current for parallel three-level rectifiers with modified LCL filter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 7012–7023, Aug. 2021, doi: 10.1109/TIE.2020.3007081.

[24] C. Zhang, X. Li, X. Xing, B. Zhang, R. Zhang, and B. Duan, "Modeling and mitigation of resonance current for modified LCL-type parallel inverters with inverter-side current control," *IEEE Trans. Ind. Informat.*, vol. 18, no. 2, pp. 932–942, Feb. 2022, doi: 10.1109/TII.2021.3076090.

[25] R. Zhang, C. Zhang, X. Xing, Z. Chen, and X. Liu, "Modeling and control method to suppress common-mode resonance circulating current for high-power parallel three-level inverters system with improved LCL filter," *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2484–2496, Mar. 2023, doi: 10.1109/TIE.2022.3169845.

[26] J. Jia, G. Yang, and A. H. Nielsen, "A review on grid-connected converter control for short-circuit power provision under grid unbalanced faults," *IEEE Trans. Power Del.*, vol. 33, no. 2, pp. 649–661, Apr. 2018, doi: 10.1109/TPWRD.2017.2682164.

[27] M. Garnica, L. G. de Vicuña, J. Miret, M. Castilla, and R. Guzmán, "Optimal voltage-support control for distributed generation inverters in RL grid-faulty networks," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8405–8415, Oct. 2020, doi: 10.1109/TIE.2019.2949544.

[28] Y. Li, X. Pei, M. Yang, X. Lin, and Z. Li, "An advanced fault control of transformerless modular multilevel converters in AC/DC hybrid distribution networks under the single-phase grounding fault," *IEEE Trans. Power Del.*, vol. 36, no. 2, pp. 932–942, Apr. 2021, doi: 10.1109/TPWRD.2020.2997797.

[29] C. Glöckler, D. Duckwitz, and F. Welck, "Virtual synchronous machine control with virtual resistor for enhanced short circuit capability," in *Proc. IEEE PES Innov. Smart Grid Technol. Conf. Europe*, 2017, pp. 1–6, doi: 10.1109/ISGTEurope.2017.8260278.

[30] X. Lu, J. Wang, J. M. Guerrero, and D. Zhao, "Virtual-impedance-based fault current limiters for inverter dominated AC microgrids," *IEEE Trans. Smart Grid*, vol. 9, no. 3, pp. 1599–1612, May 2018, doi: 10.1109/TSG.2016.2594811.

[31] T. Liu, X. Wang, F. Liu, K. Xin, and Y. Liu, "A current limiting method for single-loop voltage-magnitude controlled grid-forming converters during symmetrical faults," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 4751–4763, Apr. 2022, doi: 10.1109/TPEL.2021.3122744.

[32] T. Qoria, H. Wu, X. Wang, and I. Colak, "Variable virtual impedance-based overcurrent protection for grid-forming inverters: Small-signal, large-signal analysis and improvement," *IEEE Trans. Smart Grid*, vol. 14, no. 5, pp. 3324–3336, Sep. 2023, doi: 10.1109/TSG.2022.3232987.

[33] Y. Wang, Y. Kuang, and Q. Xu, "A current-limiting scheme for voltage-controlled inverter using instantaneous current to generate virtual impedance," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 13, no. 2, pp. 524–535, Jun. 2023, doi: 10.1109/JETCAS.2023.3248964.

[34] J. A. Martinez-Velasco, "Introduction to electromagnetic transient analysis of power systems," in *Transient Anal. of Power Syst.: Solution Techn., Tools and Appl.*. Hoboken, NJ, USA: Wiley-IEEE Press, 2015, pp. 1–8, doi: 10.1002/9781118694190.ch1.

[35] S. Ouyang, J. Liu, Y. Yang, X. Chen, S. Song, and H. Wu, "DC voltage control strategy of three-terminal medium-voltage power electronic transformer-based soft normally open points," *IEEE Trans. Ind. Electron.*, vol. 67, no. 5, pp. 3684–3695, May 2020, doi: 10.1109/TIE.2019.2922915.

[36] D. Ma, W. Chen, L. Shu, X. Qu, and K. Hou, "A MMC-based multiport power electronic transformer with shared medium-frequency transformer," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 2, pp. 727–731, Feb. 2021, doi: 10.1109/TCSII.2020.3012293.

[37] D. P. Mishra, S. R. Samantaray, and G. Joos, "A combined wavelet and data-mining based intelligent protection scheme for microgrid," *IEEE Trans. Smart Grid*, vol. 7, no. 5, pp. 2295–2304, Sep. 2016, doi: 10.1109/TSG.2015.2487501.

[38] S. F. Zarei, H. Mokhtari, and F. Blaabjerg, "Fault detection and protection strategy for islanded inverter-based microgrids," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 472–484, Feb. 2021, doi: 10.1109/JESTPE.2019.2962245.

[39] T. E. Sati, M. A. Azzouz, and M. Shaaban, "Optimal protection coordination of islanded microgrids utilizing an adaptive virtual impedance fault current limiter," *IEEE Trans. Ind. Appl.*, vol. 59, no. 3, pp. 2866–2876, May/Jun. 2023, doi: 10.1109/TIA.2023.3244176.

[40] J. M. Bloemink and T. C. Green, "Benefits of distribution-level power electronics for supporting distributed generation growth," *IEEE Trans. Power Del.*, vol. 28, no. 2, pp. 911–919, Apr. 2013, doi: 10.1109/TPWRD.2012.2232313.

[41] Z. Quan and Y. W. Li, "Phase-disposition PWM based 2DoF-interleaving scheme for minimizing high frequency ZSCC in modular parallel three-level converters," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10590–10599, Nov. 2019, doi: 10.1109/TPEL.2019.2900019.

[42] D. Grahame Holmes and T. A. Lipo, "Carrier based PWM of multilevel inverters," in *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken, NJ, USA: Wiley-IEEE Press, 2003, pp. 453–530, doi: 10.1109/9780470546284.ch11.

[43] E. Rodriguez-Diaz, F. D. Freijedo, J. C. Vasquez, and J. M. Guerrero, "Analysis and comparison of notch filter and capacitor voltage feedforward active damping techniques for LCL grid-connected converters," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3958–3972, Apr. 2019, doi: 10.1109/TPEL.2018.2856634.

[44] L. Yang, J. Yang, M. Gao, A. Watson, and P. Wheeler, "Current control of LCL-type shunt APFs: Damping characteristics, stability analysis, and robust design against grid impedance variation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 5026–5042, Aug. 2021, doi: 10.1109/JESTPE.2020.3017551.

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