Reduction Method of Circulating Current in Parallel Three-Level Inverters Using Modified Discontinuous Pulse-Width Modulation Based on Interleaving Scheme

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***Abstract*—This article presents a reduction method of circulating current in parallel three-level inverters using modified discontinuous pulse-width modulation (DPWM) based on an interleaving scheme. The harmonics and current ripple are the same as that of a single inverter with the same current capacity as the parallel system with DPWM. An interleaved DPWM improves the output current quality. However, a circulating current is generated by the asynchronous phase carriers. The circulating current limits the power rating. To alleviate these problems, the proposed method reduces the high-frequency circulating current with switching frequency by 79% even at a high modulation index. The switching sequence and high-frequency circulating current are analyzed to prove the performance of the proposed method. The effectiveness and reliability of the proposed reduction method are compared to the conventional SVM. The validity of the proposed method is verified through simulations and experimental results.**

***Index Terms*—Circulating current, discontinuous pulse-width modulation (DPWM), interleaving scheme, parallel-three-level inverter.**

I. Introduction

THREE-PHASE voltage source inverters have been used in various applications such as renewable energy generation systems, motor drives, and distributed generation systems. The two-level inverters are generally used in power conversion systems. A large filter is inevitable to satisfy the IEEE-519 standard in grid-tied systems [1]. To mitigate this disadvantage, a three-level NPC inverter has been widely used in high-power industrial applications [2]. The output currents of inverters have components of fundamental frequency in an ideal. However, the output currents of inverters in general contain harmonics that deteriorate the performance of the systems. It is inevitable to reduce the distortion of harmonic components by designing a filter. The inductance filter of power conversion systems has been applied generally to reduce these harmonics satisfying the IEEE-519 standard [3].

Parallel-connected inverters are the alternative topologies to achieve a higher power rating than the single three-level inverter. The flexibility of voltage capability in parallel-connected inverters can improve the efficiency of systems over a wide range of application conditions [4], [5], [6]. However, parallel inverters have problems with increasing output current ripples and the losses of switches. A discontinuous pulse-width modulation (DPWM) based on an interleaving scheme has been proposed to reduce the output current ripple because of overlapping in the current ripple of each inverter and switching losses [7], [8]. The DPWM has a higher capability of diminishing the stress on power semiconductors and minimizing power loss. Moreover, the DPWM is advantageous because it improves system efficiency. The power loss of conventional DPWM is reduced by 33% [9]. However, the difference in the carrier phase of the interleaving scheme generates a circulating current [10], [11].

The circulating current has disadvantages in power conversion systems, such as increased power loss and decreased system efficiency. The unexpected circulating current causes the saturation of filter inductance. In addition, the harmonic components of circulating current increase the thermal stress of dc-link capacitors and power semiconductors and cause the limitation of the power rating [12]. The circulating current can be classified into low- and high-frequency components, which should be treated differently. The imperfect symmetry of each inverter causes a low-frequency circulating current. In contrast, the carrier difference between each inverter can result in asynchronous switching sequences generating high-frequency circulating current [13].

Reduction methods for low-frequency circulating current have been studied based on minimizing differences in zero-sequence voltages between parallel inverters. An injection method was proposed in [14] to eliminate the circulating current by compensating the reference voltage with the optimized zero sequence voltage. In addition, an improved SVM based on adjusting the switching sequence was proposed in [15],

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[16], and [17] for reducing the circulating current and common mode voltage. Various conventional reduction methods for high-frequency circulating current have been studied using hardware to suppress circulating current [18], [19]. The current path of the circulating current is eliminated by adding isolated transformers to the ac sides of the parallel inverter [18]. Another conventional reduction method adding high-impedance inductors and modified filters to restrain the circulating current is studied in [19]. However, the power density of the system is decreased by this hardware.

Recently, control methods based on modulation have attempted to reduce the circulating current without additional volume [20], [21], [22], [23], [24], [25]. The reduction methods based on carrier synchronization are the representative methods for high-frequency circulating current. The carrier period of the slave module is adjustable, and the carrier period of the master module is constant. Therefore, the carriers of modules are resynchronized quickly avoiding the completely reversed carriers [21]. However, these control methods do not apply to inverters using interleaved PWM for reducing output current ripple [22]. The high-frequency circulating current caused by the interleaved PWM cannot be suppressed through the PWM sequence synchronization between inverters [23]. Therefore, various research on reduction methods based on the interleaving scheme has been studied in [24] and [25]. In [24], the proposed modulation method suppresses zero-sequence circulating current caused by the interleaved PWM. However, it has an adverse effect that significantly increases the output current's total harmonic distortion (THD). An interleaved DPWM, a recently proposed modulation method, achieves both the circulating current suppression and the output current quality improvement in the interleaved PWM [25]. However, the interleaved DPWM has been analyzed only in parallel two-level inverters without considering redundant voltage vectors.

This article proposed the reduction method of high-frequency circulating current in parallel three-level inverters using modified interleaved DPWM. The modified interleaved DPWM was analyzed for its complex switching sequence in the parallel three-level inverter. In addition, this study proved that the proposed modulation method has better efficiency at a high modulation index (MI) through a five-level space vector diagram analysis and the complex calculation of the dwell time. The high-frequency circulating current was discussed by comparing the conventional interleaved DPWM to prove the effectiveness of the proposed method. Finally, the proposed modulation method's performance was verified in the simulation and experimental results.

II. Circulating Current With Switching Sequence

A. Analysis of Circulating Current

The circuit configuration of a two-parallel-connected three-level NPC inverter is shown in Fig. 1. The circulating current of the parallel inverter is generated when the modular inverter has a common load and connection to the DC source. The output currents of each phase in each inverter $i_{\text{out},x1}$ and $i_{\text{out},x2}$ ($x = a, b, c$) are defined as follows:

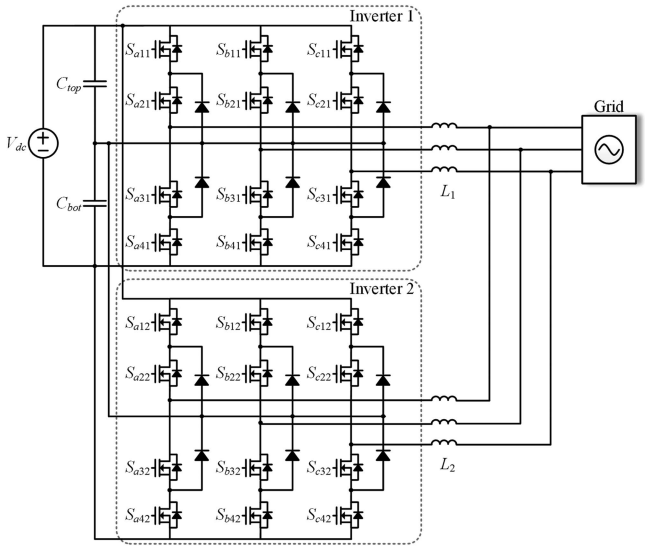

Fig. 1. Configuration of a two-parallel three-level NPC inverter.

$$\begin{aligned} i_{\text{out},x1} &= i_{x1} - i_{\text{cir},x} \\ i_{\text{out},x2} &= i_{x2} + i_{\text{cir},x} \end{aligned} \tag{1}$$

where i_{x1} and i_{x2} represent the phase x current of inverters 1 and 2, and $i_{\text{cir},x}$ is the circulating current of interphase. The circulating current flowing between interphase $i_{\text{cir},x}$ can be defined as follows

$$i_{\text{cir},x} = \frac{i_{x1} - i_{x2}}{2}. \tag{2}$$

The voltages of each phase V_{x1} and V_{x2} are determined by the switching states S_{x1} and S_{x2}, shown as.

$$V_{x1} = \frac{V_{\text{dc}}\,(S_{x1}-1)}{2}, \quad V_{x2} = \frac{V_{\text{dc}}\,(S_{x2}-1)}{2}, \quad S_{x1,2} = 0, 1, 2 \tag{3}$$

where V_{dc} is the dc-link voltage of the modular inverter. The voltage equation of the two-parallel inverter can be expressed by the currents and inductance of each phase, shown as

$$V_{x1} - V_{x2} = (L_1 + L_2)\,\frac{di_{\text{cir},x}}{dt} \tag{4}$$

where L_1 and L_2 are the inductance of each inverter.

The common mode voltage of each inverter is the voltage variation between the neutral point of dc-link and load ground as shown in Fig. 1. The common mode voltage $V_{\text{cm},k}$ is defined as the sum of three-phase voltage as follows

$$V_{\text{cm},k} = -\frac{V_{a,k} + V_{b,k} + V_{c,k}}{3}, \ (k = 1, 2)\,. \tag{5}$$

In addition, the difference in common mode voltage $V_{\text{cm,diff}}$ can be expressed using the switching states shown as

$$V_{\text{cm,diff}} = V_{\text{cm},1} - V_{\text{cm},2} = \frac{V_{\text{dc}}}{6} \sum_{x=a,b,c} (S_{x2} - S_{x1}). \tag{6}$$

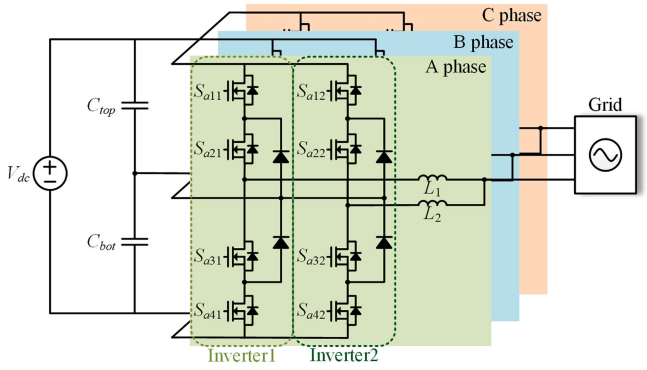

Fig. 2. Equivalent circuit of the two parallel inverters.

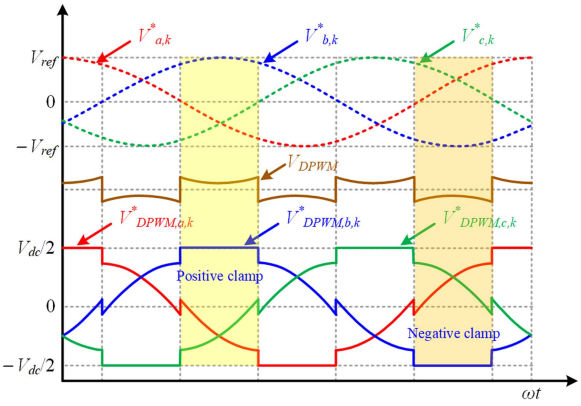

Fig. 3. Reference voltages and offset voltage with 60° DPWM.

TABLE I
SWITCHING STATES AND POLE VOLTAGES

Inverter1		Inverter2		Output	
Switching	Voltage	Switching	Voltage	Switching	Voltage
N	$-V_{dc}/2$	N	$-V_{dc}/2$	0	$-V_{dc}/2$
N	$-V_{dc}/2$	O	0 V	1	$-V_{dc}/4$
O	0 V	N	$-V_{dc}/2$		
N	$-V_{dc}/2$	P	$+V_{dc}/2$		
O	0 V	O	0 V	2	0 V
P	$+V_{dc}/2$	N	$-V_{dc}/2$		
O	0 V	P	$+V_{dc}/2$	3	$+V_{dc}/4$
P	$+V_{dc}/2$	O	0 V		
P	$+V_{dc}/2$	P	$+V_{dc}/2$	4	$+V_{dc}/2$

The circulating current i_{cir} of the parallel inverter is defined as the sum of the three-phase switching differences between inverters or the difference in common mode voltage as follows

$$\frac{di_{\text{cir}}}{dt} = \frac{V_{\text{dc}}}{2\left(L_1+L_2\right)} \sum_{x=a,b,c} \left(S_{x1}-S_{x2}\right) = \frac{3}{\left(L_1+L_2\right)} V_{\text{cm,diff}}. \tag{7}$$

The parallel-connected three-level inverters can be equivalent to a five-level inverter, as shown in Fig. 2. There are five switching states and output pole voltages, as presented in Table I according to the combination of each inverter's switching states. When the even switching states 0, 2, and 4 are only selected, the circulating current is not generated because the switching states of each inverter are the same. However, the switching states 0, 1, 2, 3, and 4 are all used to ensure the output current quality. Each inverter's switching state differs when the output stage's switching state is 1 or 3. In order not to generate circulating current while using switching states 1 and 3, the two phases must have opposite polarities. However, when switching states 1 and 3 generate only in one phase, circulating current generates inevitably. Therefore, the opposite polarity must be used in the next switching half cycle to make the average circulating current of the one switching cycle zero.

B. Conventional Discontinuous PWM

The DPWM method has advantages such as minimization of power loss and reducing stress on power semiconductors. Each phase of the inverter is clamped to the $-V_{\text{dc}}/2$ or $+V_{\text{dc}}/2$ for an amount of time, as shown in Fig. 3. If a large offset voltage is injected, the resultant DPWM signal waveforms can be overlapped with each other, causing distortions in the phase current. Although there are several different DPWM methods, the conventional 60° DPWM is the most generally used for systems with the unity power factor.

The three-phase reference voltages are expressed as

$$\begin{aligned} V^*_{a,k} &= V_{\text{ref}} \cos\left(\omega t\right), \\ V^*_{b,k} &= V_{\text{ref}} \cos\left(\omega t - 2\pi/3\right) \\ V^*_{c,k} &= V_{\text{ref}} \cos\left(\omega t + 2\pi/3\right) \end{aligned} \tag{8}$$

where V_{ref} is the magnitude of the reference voltage. When the conventional 60° DPWM is applied, the reference voltage with offset is calculated by adding a modified zero-sequence offset

$$\begin{aligned} V^*_{\text{DPWM},a,k} &= V^*_{a,k} + V_{z,\text{DPWM},k} \\ V^*_{\text{DPWM},b,k} &= V^*_{b,k} + V_{z,\text{DPWM},k} \\ V^*_{\text{DPWM},c,k} &= V^*_{c,k} + V_{z,\text{DPWM},k}. \end{aligned} \tag{9}$$

$V_{z,\text{DPWM},k}$ can be defined using the maximum and minimum values of the phase voltage references as

$$V_{z,\text{DPWM},k} = \begin{cases} \frac{V_{\text{dc}}}{2} - V_{\max,k}, & \left(V_{\max} + V_{\min} \geq 0\right) \\ -\frac{V_{\text{dc}}}{2} - V_{\min,k}, & \left(V_{\max} + V_{\min} < 0\right) \end{cases} \tag{10}$$

where $V_{\max,k}$ and $V_{\min,k}$ are defined as follows:

$$\begin{aligned} V_{\max,k} &= \max\left(V^*_{a,k}, V^*_{b,k}, V^*_{c,k}\right) \\ V_{\min,k} &= \min\left(V^*_{a,k}, V^*_{b,k}, V^*_{c,k}\right). \end{aligned} \tag{11}$$

The voltage vector is divided into 12 sectors according to the reference voltages. The reference voltage of a-phase is clamped to the $+V_{\text{dc}}/2$ in sector 1 and sector 2. In addition, it is sector 1 when the reference voltage of c-phase is larger than the reference voltage of b-phase. In contrast, it is sector 2 when the reference voltage of b-phase is larger than the reference voltage of c-phase.

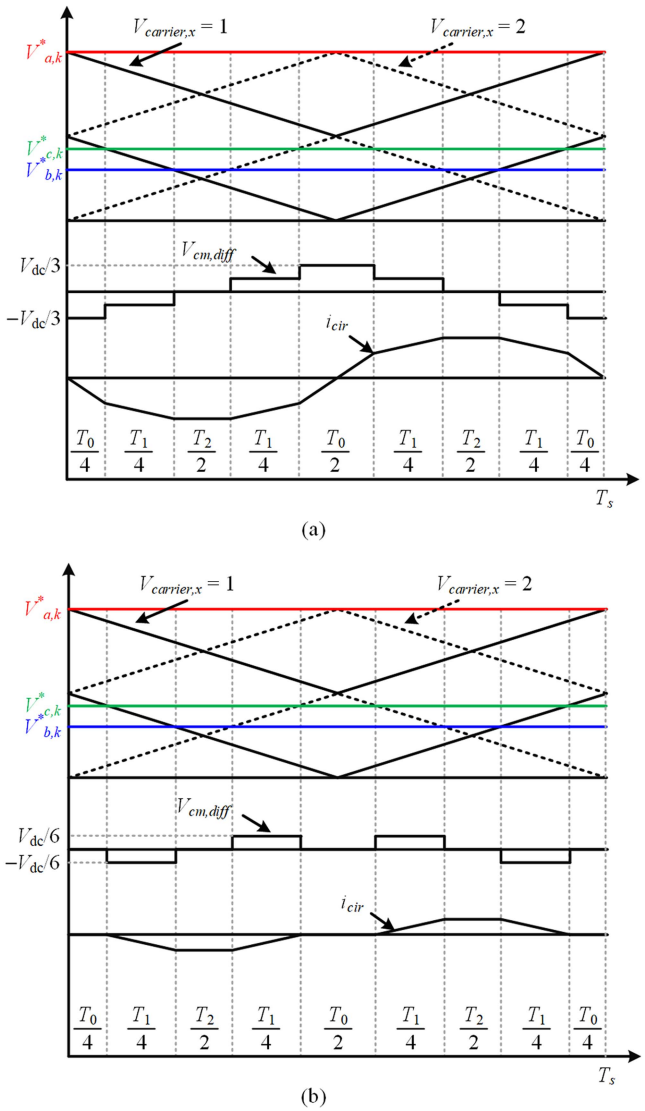

Fig. 4. Reduction of difference of common mode voltage and circulating current with carrier phase shift algorithm. (a) Conventional interleaved DPWM. (b) Proposed modulation.

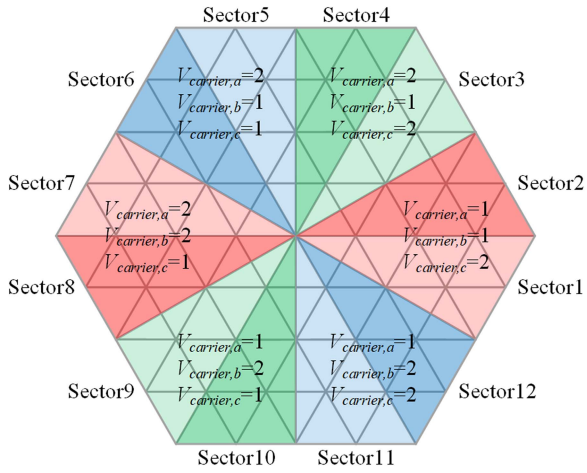

Fig. 5. Space vector diagram for two-parallel three-level inverters and carrier selection method of one inverter.

III. Modified Interleaving DPWM Method

A. Carrier Phase Shift Algorithm

The conventional interleaved PWM generates high-frequency circulating current by the difference in carriers due to the difference in common mode voltage. Fig. 4(a) represents the difference in common mode voltage and circulating current at conventional interleaved DPWM. Inverter 1 uses carrier 1, and inverter 2 uses carrier 2. When the magnitude of difference in common mode voltage is the largest, the circulating current is increased rapidly. When the output switching state is 411, the circulating current is the largest by the voltage redundant vectors PNN and POO of each inverter at sector 2. Each voltage vector is selected alternatively to ensure the zero-average difference in common mode voltage and circulating current. The voltage vector PNN is selected in the first-half switching period, and the voltage vector POO is selected in the second-half switching period of inverter 1. In inverter 1, the voltage vector POO is selected in the first-half switching period, and the voltage vector PNN is selected in the second-half switching period. The principle of high-frequency circulating current suppression is to reduce the peak value of the difference in common mode voltage or to reduce the dwell time of the switching sequence generating the difference in common mode voltage. The modified interleaved DPWM applies the carrier phase shift algorithm for reducing the high-frequency circulating current.

The 60° DPWM method is applied to reduce switching loss at peaks of phase current. The reference voltage of a-phase is clamped to the top and bottom in sectors 1, 2, 7, and 8, as shown in the red region of Fig. 5. When the sector is 1 or 2, the reference voltage of a-phase is clamped to the $+V_{\rm dc}/2$. When the sector is 7 or 8, the reference voltage of a-phase is clamped to the $-V_{\rm dc}/2$. Similarly, the reference voltage of b-phase and c-phase are clamped in blue and green regions, respectively. The carrier waves $V_{{\rm carrier},x}$ have two types: one sinusoidal carrier wave ($V_{{\rm carrier},x}=1$) and 180° phase shifted carrier wave ($V_{{\rm carrier},x}=2$). The reference voltage of inverter 1 is compared with carrier wave 1, and the reference voltage of inverter 2 is compared with the phase-shifted carrier wave 2 in all sectors at conventional interleaved DPWM. In the proposed method, the reference voltage of b-phase is compared with carrier wave 1, and the reference voltage of c-phase is compared with the phase-shifted carrier wave 2 in sector 2 of inverter 1. In contrast, the reference voltage of b- and c-phase of inverter 2 are compared with interleaved carriers selected at inverter 1 to reduce the circulating current by modifying the switching sequence.

The voltage vectors of each inverter are replaced by the shifted carrier waves when the switching states generate the largest difference in common mode voltage. Table II represents the switching states and difference in common mode voltage at sector 1 and sector 2 clamping a-phase. The difference in common mode voltage is $\pm V_{\rm dc}/3$ when the switching states of conventional interleaved DPWM are 411, 413, 431, and 433.

TABLE II
DIFFERENCE IN COMMON MODE VOLTAGE ACCORDING TO THE SELECTED VECTORS AT SECTOR2

Switching state	Selected vectors	$V_{cm,diff}$
411	POO, PNN → PON, PNO	±Vdc/3 → 0 V
413	POP, PNO → PNP, POO	
431	PPO, PON → PPN, POO	
433	PPP, POO → PPO, POP	
410	PON, PNN	±Vdc/6
413	PPN, PON	
421	POO, PON	
423	POP, POO	
430	PPN, PON	
432	PPO, POO	
441	PPO, PPN	
443	PPP, PPO	

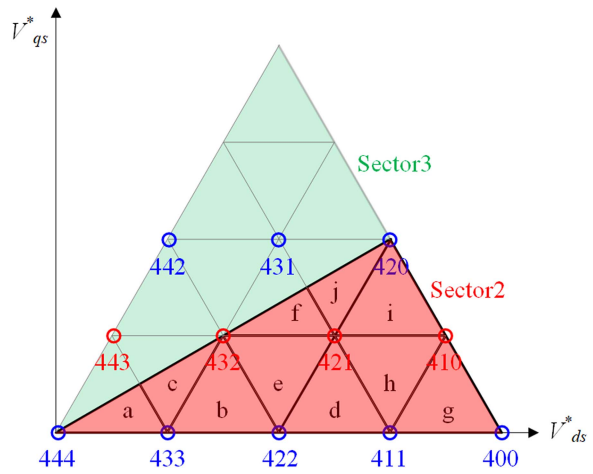

Fig. 6. Switching vectors of sector 2 in a parallel three-level inverter.

To eliminate the difference in common mode voltage, the voltage vectors of each inverter are replaced by PON and PNO when the switching state is 411. Each redundant voltage vector is selected alternatively every half-switching period. The circulating current is reduced by replacing the voltage vectors when the switching states are 411, 413, 431, and 433 by applying the proposed method. The circulating current is only generated in other switching states 410, 413, 421, 423, 430, 432, 441, and 443. The difference in common mode voltage of these switching states is $\pm V_{\rm dc}/6$ by the different switching vectors in only one phase. Fig. 4(b) represents the reduced difference in common mode voltage and circulating current at the proposed method.

B. Analysis of Circulating Current

Fig. 6 represents the subsector with switching states generating circulating current marked in red points of sector 2. The switching states marked in red generate circulating current, and the switching states marked in blue do not generate circulating current. Table III represents the switching sequences of each subsector. The modified interleaved DPWM makes the average circulating current of the switching half cycle zero by 180° carrier phase shift of the specific phase. Therefore, the overlap of common mode voltage is prevented and the peak value of difference in common mode voltage becomes small. The peak value of circulating current $i_{\rm cc,peak}$ after applying the proposed modified interleaved DPWM can be calculated by the dwell time of the switching sequence as follows:

TABLE III
SWITCHING SEQUENCE ACCORDING TO THE SUBSECTOR OF SECTOR2

Subsector	Switching sequence
a	444 – 443 – 433 – 443 – 444 – 443 – 433 – 443 – 444
b	433 – 432 – 422 – 432 – 433 – 432 – 422 – 432 – 433
c	433 – 432 – 442 – 432 – 433 – 432 – 442 – 432 – 433
d	422 – 421 – 411 – 421 – 422 – 421 – 411 – 421 – 422
e	422 – 421 – 431 – 421 – 422 – 421 – 431 – 421 – 422
f	422 – 432 – 431 – 432 – 422 – 432 – 431 – 432 – 422
g	411 – 410 – 400 – 410 – 411 – 410 – 400 – 410 – 411
h	411 – 410 – 420 – 410 – 411 – 410 – 420 – 410 – 411
i	411 – 421 – 420 – 421 – 411 – 421 – 420 – 421 – 411
j	431 – 421 – 420 – 421 – 431 – 421 – 420 – 421 – 431

$$i_{\rm cc,peak} = \frac{3T_{\rm cc}}{L_1 + L_2} \cdot V_{\rm cm,diff} \tag{12}$$

where $T_{\rm cc}$ is the dwell time of the switching sequence generating circulating current.

The dwell time of the switching sequence generating circulating current in each subsector is calculated as follows:

$$\begin{aligned}
&\text{(a)}\ T_{\rm cc} = 2\sqrt{3}\cdot \text{MI}\cdot\sin\theta\cdot T_s,\\
&\text{(b)}\ T_{\rm cc} = 2\sqrt{3}\cdot \text{MI}\cdot\sin\theta\cdot T_s,\\
&\text{(c)}\ T_{\rm cc} = (6\cdot \text{MI}\cdot\cos\theta - 2)\cdot T_s,\\
&\text{(d)}\ T_{\rm cc} = 2\sqrt{3}\cdot \text{MI}\cdot\sin\theta\cdot T_s,\\
&\text{(e)}\ T_{\rm cc} = (6\cdot \text{MI}\cdot\cos\theta - 4)\cdot T_s,\\
&\text{(f)}\ T_{\rm cc} = (4 - 6\cdot \text{MI}\cdot\cos\theta)\cdot T_s,\\
&\text{(g)}\ T_{\rm cc} = 2\sqrt{3}\cdot \text{MI}\cdot\sin\theta\cdot T_s,\\
&\text{(h)}\ T_{\rm cc} = (6\cdot \text{MI}\cdot\cos\theta - 6)\cdot T_s,\\
&\text{(i)}\ T_{\rm cc} = (6 - 6\cdot \text{MI}\cdot\cos\theta)\cdot T_s,\\
&\text{(j)}\ T_{\rm cc} = \left(2 - 2\sqrt{3}\cdot \text{MI}\cdot\sin\theta\right)\cdot T_s
\end{aligned} \tag{13}$$

where MI is defined as follows:

$$\text{MI} = \frac{2V_{\rm ref}}{V_{\rm dc}} \tag{14}$$

where $V_{\rm ref}$ is the reference voltage.

C. Balancing of Neutral Point Voltage

The parallel-connected three-level inverter has two series-connected dc-link capacitors C_{top} and C_{bot} as shown in Fig. 1. The voltage of two series-connected capacitors should be kept equal to ensure the performance of the parallel-connected inverter. The neutral-point voltage ΔV_{np} can be expressed as the difference between the voltages of dc-link capacitors V_{top} and V_{bot}.

$$\Delta V_{\text{np}} = V_{\text{top}} - V_{\text{bot}}. \tag{15}$$

The neutral-point voltage ΔV_{np} is determined by the average of neutral-point current I_{np} during a control period T_s. The neutral-point voltage ΔV_{np} and current I_{np} are expressed by the switching vectors as follows:

$$\Delta V_{\text{np}} = \int_{T_s} I_{\text{np}} dt. \tag{16}$$

$$I_{\text{np}} = \begin{cases} I_a & (\text{OPN, ONP, OPP, and ONN}), \\ I_b + I_c = -I_a & (\text{POO and NOO}), \\ I_b & (\text{PON, NOP, POP, and NON}), \\ I_a + I_c = -I_b & (\text{OPO and ONO}), \\ I_c & (\text{NPO, PNO, PPO, and NNO}), \\ I_a + I_b = -I_c & (\text{OOP and OON}). \end{cases} \tag{17}$$

The voltages of dc-link capacitors are balanced in the conventional SVM with an interleaving scheme. The integrated charge by neutral-point current during a control period T_s is expressed as follows:

$$\begin{aligned} \Delta V_{\text{np}} = & \int_0^{T_0/2} (I_a)\, dt + \int_0^{T_0/2} (I_b + I_c)\, dt \\ & + \int_0^{T_1/2} (0)\, dt + \int_0^{T_1/2} (I_c)\, dt + \int_0^{T_2} (I_c)\, dt \\ = & \int_0^{(T_1/2+T_2)} (I_c)\, dt. \end{aligned} \tag{18}$$

When the conventional interleaved DPWM is applied, the switching sequences are modified according to the reference voltage clamped phase. The highest current flows at the neutral point in each sector when the interleaved DPWM is applied. In sector 1, the voltage vectors POO and PNN are used in switching state 411. The magnitude of neutral-point current in voltage vector POO is a-phase current. The a-phase current is the highest current compared to the other phase currents in sector 1. The integrated charge by neutral-point current during T_s of the conventional interleaved DPWM is derived as

$$\begin{aligned} \Delta V_{\text{np}} = & \int_0^{T_0/2} (0)\, dt + \int_0^{T_0/2} (I_b + I_c)\, dt \\ & + \int_0^{T_1/2} (I_c)\, dt + \int_0^{T_1/2} (I_b + I_c)\, dt + \int_0^{T_2} (I_c)\, dt \\ = & \int_0^{(T_0/2+T_1/2)} (-I_a)\, dt + \int_0^{(T_1/2+T_2)} (I_c)\, dt. \end{aligned} \tag{19}$$

The voltage ripple of capacitors increases when the interleaved DPWM is applied. In contrast, the switching loss of power semiconductors is reduced by clamping the voltage vectors in interleaved DPWM to improve output current quality.

TABLE IV
NEUTRAL-POINT CURRENT AND VOLTAGE ACCORDING TO SECTOR

Sector	Integrated charge of neutral-point current	Neutral-point voltage
1	$\int_0^{(T_0/2+T_1/2)}(I_b+I_c)dt + \int_0^{(T_1/2+T_2)}(I_c)dt$	Decrease
2	$\int_0^{(T_0/2+T_1/2)}(I_b+I_c)dt + \int_0^{(T_1/2+T_2)}(I_b)dt$	Decrease
3	$\int_0^{(T_0/2+T_1/2)}(I_a+I_b)dt + \int_0^{(T_1/2+T_2)}(I_b)dt$	Increase
4	$\int_0^{(T_0/2+T_1/2)}(I_a+I_b)dt + \int_0^{(T_1/2+T_2)}(I_a)dt$	Increase
5	$\int_0^{(T_0/2+T_1/2)}(I_a+I_c)dt + \int_0^{(T_1/2+T_2)}(I_a)dt$	Decrease
6	$\int_0^{(T_0/2+T_1/2)}(I_a+I_c)dt + \int_0^{(T_1/2+T_2)}(I_c)dt$	Decrease
7	$\int_0^{(T_0/2+T_1/2)}(I_b+I_c)dt + \int_0^{(T_1/2+T_2)}(I_c)dt$	Increase
8	$\int_0^{(T_0/2+T_1/2)}(I_b+I_c)dt + \int_0^{(T_1/2+T_2)}(I_b)dt$	Increase
9	$\int_0^{(T_0/2+T_1/2)}(I_a+I_b)dt + \int_0^{(T_1/2+T_2)}(I_b)dt$	Decrease
10	$\int_0^{(T_0/2+T_1/2)}(I_a+I_b)dt + \int_0^{(T_1/2+T_2)}(I_a)dt$	Decrease
11	$\int_0^{(T_0/2+T_1/2)}(I_a+I_c)dt + \int_0^{(T_1/2+T_2)}(I_a)dt$	Increase
12	$\int_0^{(T_0/2+T_1/2)}(I_a+I_c)dt + \int_0^{(T_1/2+T_2)}(I_c)dt$	Increase

Likewise, the integrated charge by neutral-point current during a sampling period of the proposed method is shown in Table IV. The neutral-point voltage is 0 V within one period of output current by compensating the difference in voltage generated in each sector to maintain balance. In sector 1 or sector 7, the integrated charge by the neutral-point current is given as

$$\begin{aligned} \Delta V_{\text{np}} = & \int_0^{T_0/2} (I_c)\, dt + \int_0^{T_0/2} (I_b)\, dt \\ & + \int_0^{T_1/2} (I_c)\, dt + \int_0^{T_1/2} (I_b + I_c)\, dt + \int_0^{T_2} (I_c)\, dt \\ = & \int_0^{(T_0/2+T_1/2)} (-I_a)\, dt + \int_0^{(T_1/2+T_2)} (I_c)\, dt. \end{aligned} \tag{20}$$

The magnitudes of neutral-point current in sector 1 and sector 7 are the same; however, the direction is opposite.

The neutral-point voltage and current are related to the reliability of dc-link capacitors. The lifetime estimation process to predict the wear-out failure is studied in [26]. First, the hot-spot temperature of the capacitor caused by the RMS value of ripple current and ESR is as follows:

$$T_{\text{hot-spot}} = T_{\text{ambient}} + R_{ha} \times \sum_{i=1}^{n} \left[I_{\text{rms}}^2 (f_i) \times \text{ESR}(f_i) \right] \tag{21}$$

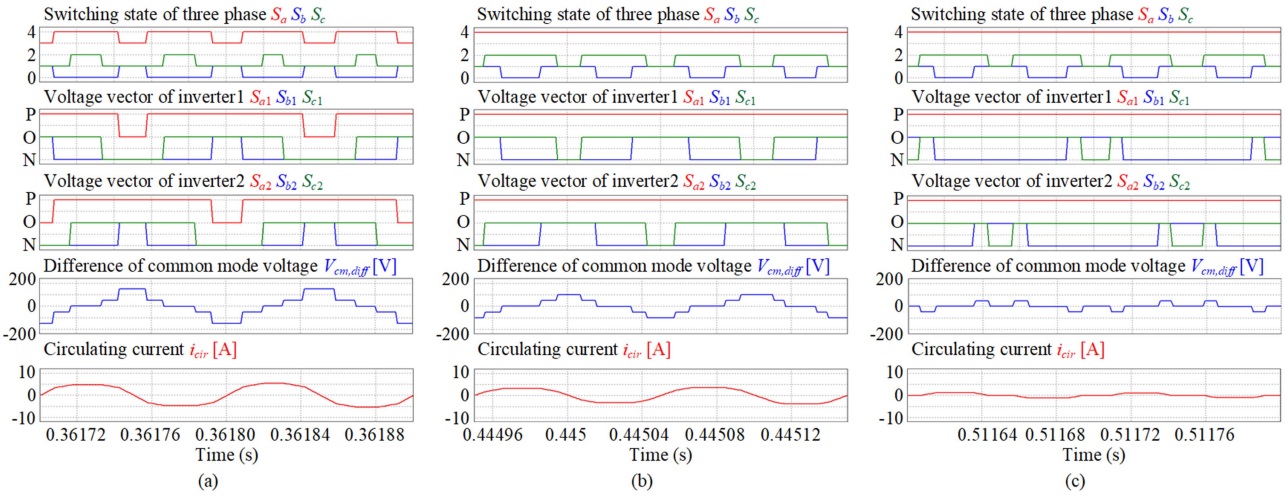

Fig. 7. Switching sequence, difference of common mode voltage, and circulating current. (a) Conventional interleaved SVM. (b) Conventional interleaved DPWM. (c) Proposed modulation.

TABLE V
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Value
DC-link voltage, V_{dc}	300 V
DC-link capacitor, C_{top}, C_{bot}	1000 μF
Grid frequency, f_{grid}	60 Hz
Filter inductor, L_1, L_2	2 mH
Switching frequency, f_{sw}	10 kHz
Modulation index, MI	0.5, 1.0

where $I_{\rm rms}(f_i)$ and ESR(f_i) are the RMS value of the ripple current and the ESR at frequency f_i, respectively. $T_{\rm ambient}$ is the ambient temperature, and R_{ha} is the equivalent thermal resistance for the variation in temperature from ambient to hot-spot temperature. The lifetime of the capacitor is finally calculated using the hot-spot temperature as follows:

$$L = L_0 \times \left(\frac{V_0}{V}\right)^{k_0} \times 2^{\frac{T_0 - T_{\rm hot-spot}}{k_1}} \tag{22}$$

where L_0, V_0, T_0, and V are the rated lifetime, rated voltage, maximum allowable hot-spot temperature, and actual voltage, respectively. k_0 and k_1 are coefficients provided by the manufacturer.

IV. SIMULATIONS

Simulations of the parallel inverter were conducted using PSIM software to demonstrate the validity of the proposed reduction method. The circuit of the two-parallel three-level NPC inverter used for the simulations is shown in Fig. 1, and the simulation parameters are listed in Table V. The grid of fundamental frequency is connected to the parallel inverter. Each inverter is controlled using the angle with the 60 Hz by line-to-line voltages of the grid. The simulation is implemented by changing the grid voltage to verify the characteristics according to the MI. The grid voltage is decreased in the MI 0.5, and the reference current is set to 7.5 A. In contrast, the grid voltage is increased to verify the proposed method in MI 1.0, and the reference current is set to 15 A. The filter inductor is used to reduce the harmonics. The inductances are set to 2 mH to satisfy the IEEE-519 standard 5% limit applying the proposed method. In addition, the simulation results are compared with the conventional SVM with the interleaving scheme and interleaved DPWM method to demonstrate the performance of the proposed method.

Fig. 7 shows the difference in common mode voltage and circulating current waveforms according to the modulation methods. When the conventional SVM is applied, the difference in common mode voltage fluctuates from $-V_{\rm dc}/2$ to $+V_{\rm dc}/2$, as shown in Fig. 7(b). The voltage vectors ONN and POO are selected when the switching state is 311 with the largest difference in common mode voltage. The waveform of the difference in common mode voltage and circulating current of conventional interleaved DPWM is shown in Fig. 7(b). The circulating current is increased rapidly when the difference in common mode voltage is $\pm V_{\rm dc}/3$. The switching state of a-phase is always 4 in sector 2 because of the positive clamped voltage. When the switching state is 411, the voltage vectors PNN and POO are selected. These vectors generate $\pm V_{\rm dc}/3$ of difference in common mode voltage. To reduce the difference in common mode voltage and circulating current, the modified interleaved DPWM method is applied in Fig. 7(c). In sector 2, the a-phase is positively clamped. The b-phase of inverter 1 and c-phase of inverter 2 use conventional carrier wave $V_{\rm carrier1}$. In contrast, the c-phase of inverter 1 and b-phase of inverter 2 use the 180° shifted carrier wave $V_{\rm carrier2}$. Consequently, the difference in common mode voltage is zero when the switching state 411 is selected. The fluctuations of circulating current in these regions are eliminated.

Figs. 8 and 9 represent the output currents and high-frequency circulating current according to the modulation methods and

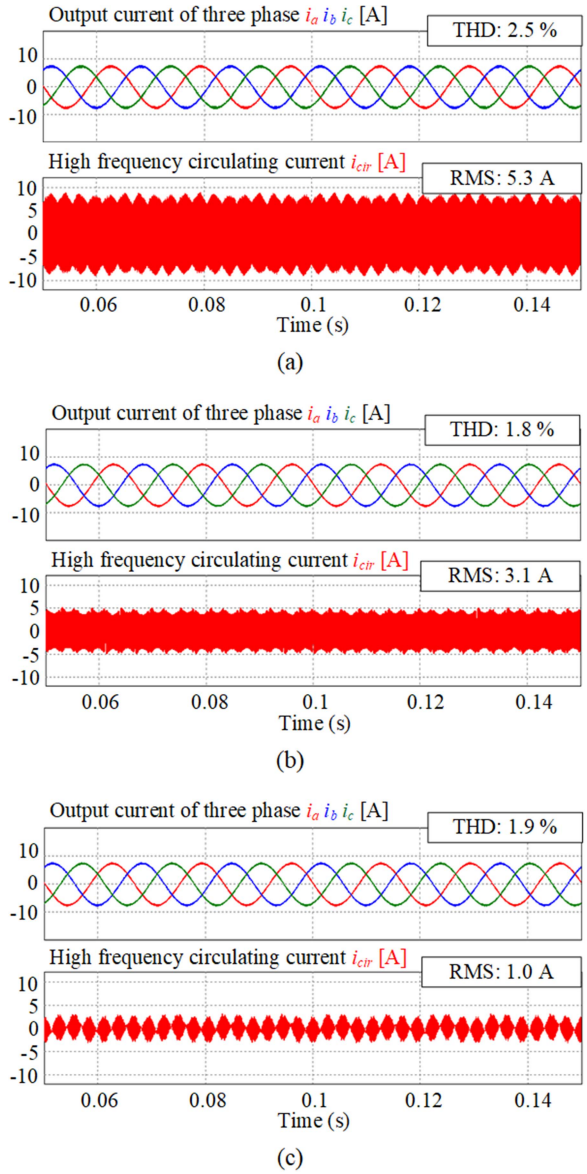

Fig. 8. Output current and high-frequency circulating current at MI 0.5. (a) Conventional interleaved SVM. (b) Conventional interleaved DPWM. (c) Proposed modulation.

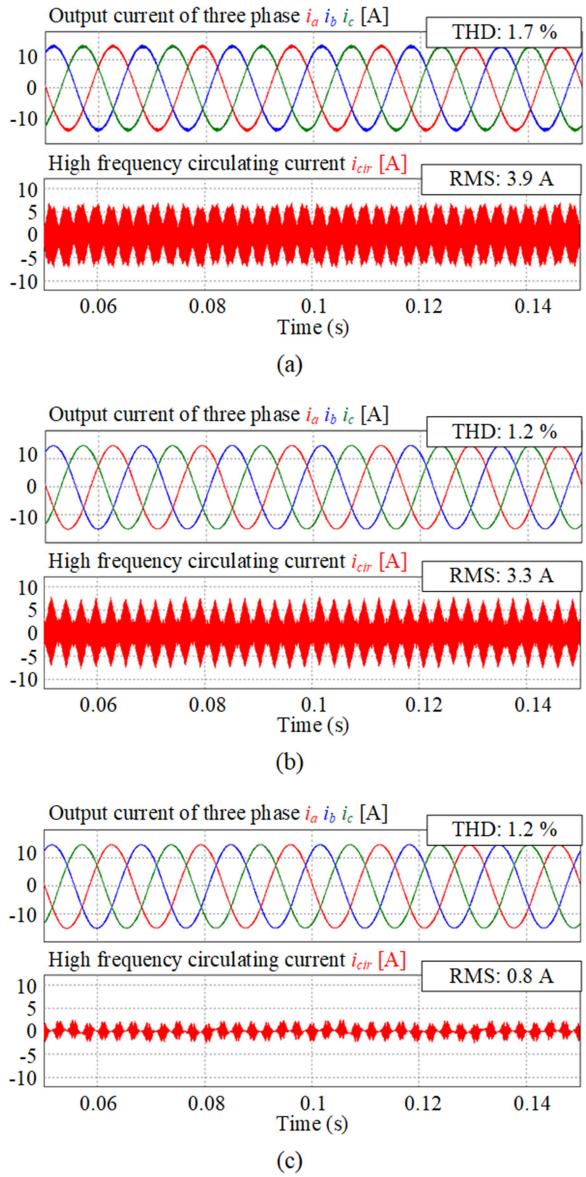

Fig. 9. Output current and high-frequency circulating current at MI 1.0. (a) Conventional interleaved SVM. (b) Conventional interleaved DPWM. (c) Proposed modulation.

MI. The MIs set 0.5 and 1.0 to verify the applicability of the proposed reduction method. When the conventional SVM with the interleaving scheme as shown in Figs. 8(a) and 9(a) are applied to improve the output quality, the high-frequency circulating currents are 5.3 and 3.9 A, and the THDs of output current are 2.5% and 1.7%, respectively. To reduce the switching loss and high-frequency circulating current, the DPWM is added to the conventional SVM with the interleaving scheme, as shown in Figs. 8(b) and 9(b). The THD of output current is reduced compared with the conventional SVM; however, the high-frequency circulating current is increased by the MI. Hence, the reduction rate decreased from 41.5% to 20.5%, according to the increment of MI. The proposed reduction method, as shown in Figs. 8(c) and 9(c), is applied to reduce high-frequency circulating current with decreased difference in common mode voltage. The THDs of output current are 1.9% and 1.2%, respectively. In addition, the high-frequency circulating currents of the proposed method are 1.0 and 0.8 A, respectively. The reduction rates compared to the conventional interleaved DPWM are 67.7% and 75.8%, according to MI. Therefore, the proposed modulation method reduced the high-frequency circulating current, ensuring the performance in full MI.

Fig. 10 represents the dc-link voltages and neutral-point currents in each reduction method. The ripple of dc-link voltages is 1.6 V in the conventional interleaving scheme as shown in Fig. 10(a). In contrast, the ripples of dc-link voltages are

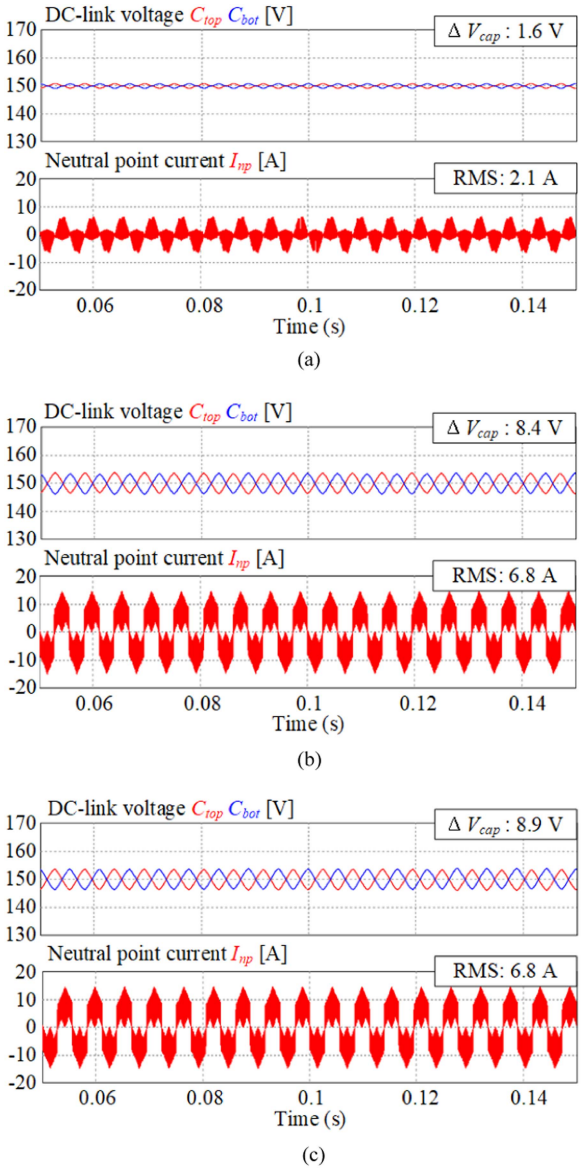

Fig. 10. DC-link voltages and neutral point current at MI 1.0. (a) Conventional interleaved SVM. (b) Conventional interleaved DPWM. (c) Proposed modulation.

8.4 and 8.9 V when the conventional interleaved DPWM and proposed reduction method are applied. As mentioned earlier, each reduction method ensures the balancing of neutral-point voltage. However, the neutral-point current is increased by the proposed method.

V. Experimental Results

Fig. 11 represents the experimental setup of the two parallel three-level NPC inverters to verify the proposed modulation method. The parameters used in the experiments are the same as the simulation parameters listed in Table IV. The proposed modulation was programmed on a TMS320R28377S digital signal processor from Texas Instruments. Each EPWM signal is generated by a shadow mode to coincide with the phase of carriers. The NPC cascade SiC MOSFET modules are applied in

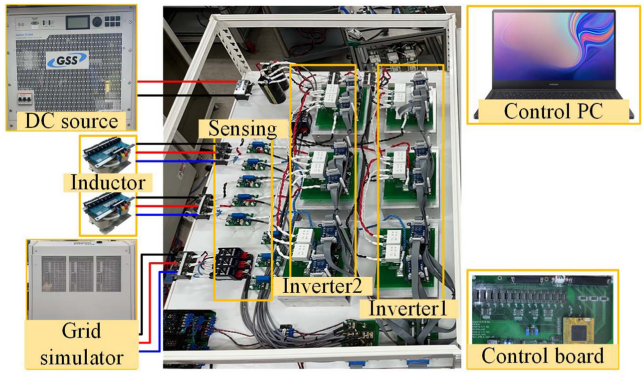

Fig. 11. Experimental setup.

the experimental setup from Semi Powerex, and the gate driver (CGD12HBMP) made by CREE is used. ALC70 1000 μF/250 V capacitors from KEMET are used as the dc-link capacitor to estimate the improvement in the capacitor lifetime. Specifically, the power analyzer WT3000 from Yokogawa is used to compare the efficiency of methods.

Figs. 12 and 13 show the experimental waveforms of the output currents and the high-frequency circulating current. The MI of each method sets 0.5 and 1.0 to compare the performance of modulation methods similar to simulation. The conventional SVM with the interleaving scheme at MI 0.5 is shown in Fig. 12(a). The THD of the output current is 2.5%; however, the largest value of high-frequency circulating current is generated compared to other modulation methods because of the interleaving scheme. Fig. 12(b) represents the experimental result when the conventional interleaved DPWM is applied. The THD of the output current is 2.3%, and the RMS value of the high-frequency circulating current is 5.1 A. The reduction rate of high-frequency circulating current compared with the conventional SVM is 32%. Fig. 12(c) represents the experimental result of the proposed modulation. The THD of output current is decreased to 2.3%, and the high-frequency circulating current is reduced to 1.7 A. The reduction rate of high-frequency circulating current compared with the conventional interleaved DPWM is 66.7%. The THDs of output current are improved when the conventional interleaved DPWM and proposed reduction methods are applied because of the decreased difference in common mode voltage. The magnitude and fluctuation of difference in common mode voltage generate a leakage current affecting the output current quality.

The waveform of conventional interleaved SVM at MI 1.0 is shown in Fig. 13(a). The THD of the output current is 2.4%, and the RMS value of high-frequency circulating current is 5.6 A. Fig. 13(b) shows the experimental waveform applied to the conventional interleaved DPWM modulation. The THD of the output current is 2.3%, and the RMS value of high-frequency circulating current is 5.2 A. The high-frequency circulating current is increased by increasing MI when the conventional interleaved DPWM is applied, unlike the SVM. The experimental result of the proposed modulation is shown in Fig. 13(c). The THD of output current is improved compared to conventional SVM and interleaved DPWM. The RMS value of high-frequency

TABLE VI
COMPARISON OF HIGH-FREQUENCY CIRCULATING CURRENT REDUCTION METHODS

Methods	High-frequency circulating current	Difference in common mode voltage	Complexity	THD of output current	Lifetime of capacitor	Efficiency
Conventional interleaved SVM	5.6 A	$\pm V_{dc}/2$	Simple	2.4%	28.5years	91.6%
Conventional interleaved DPWM	5.2 A	$\pm V_{dc}/3$	Simple	2.3%	26.5yesrs	91.9%
Proposed modulation	1.2 A	$\pm V_{dc}/6$	Moderate	1.7%	26.5years	93.5%

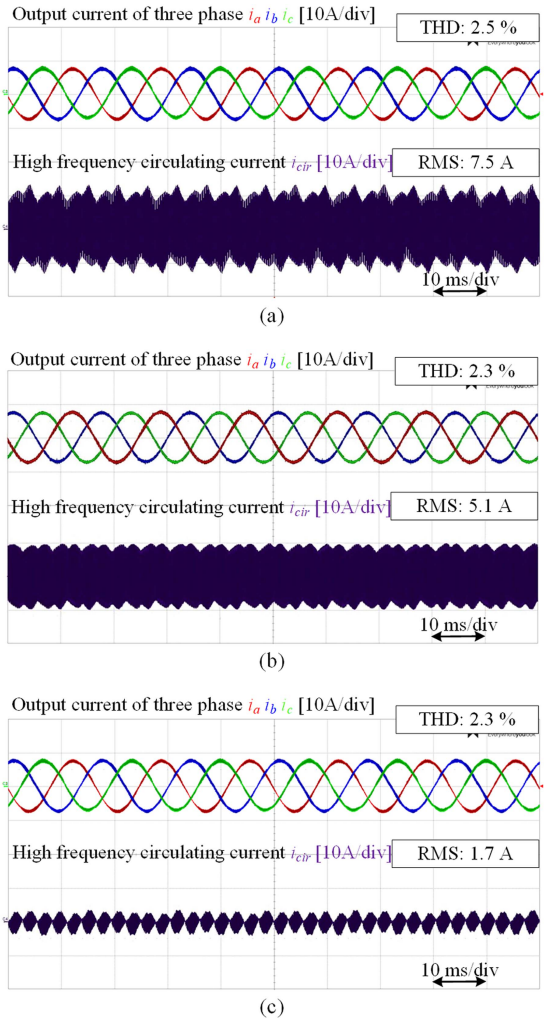

Fig. 12. Experimental results of output current and high-frequency circulating current at MI 0.5. (a) conventional interleaved SVM. (b) Conventional interleaved DPWM. (c) Proposed modulation.

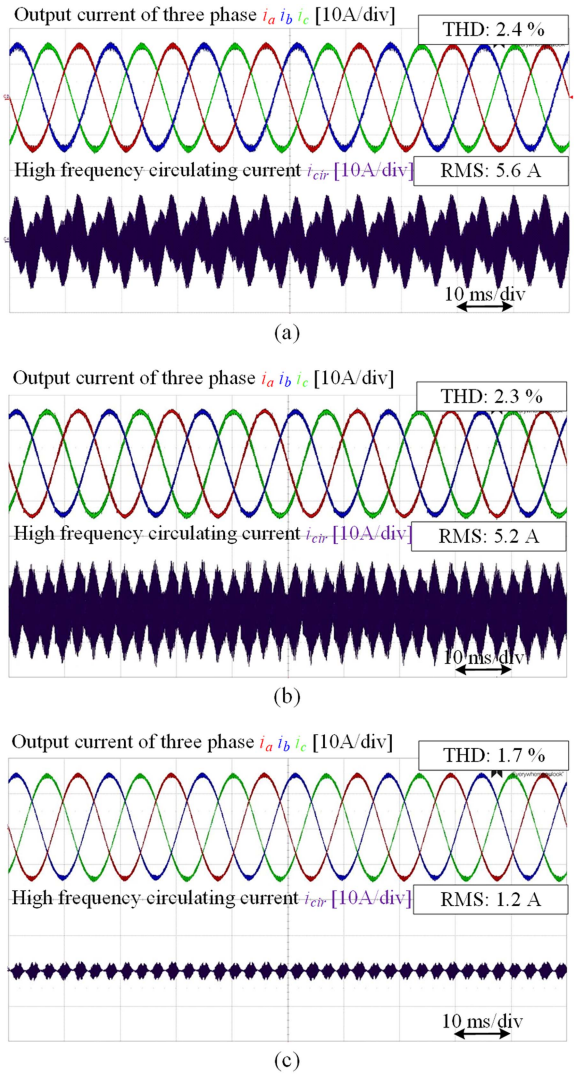

Fig. 13. Experimental results of output current and high-frequency circulating current at MI 1.0. (a) Conventional interleaved SVM. (b) Conventional interleaved DPWM. (c) Proposed modulation.

circulating current is reduced to 1.2 A. The reduction rates of high-frequency circulating current compared with other methods are 78.6% and 76.9%, respectively. Hence, the proposed reduction method verified the performance in full MI.

Fig. 14 represents the experimental waveforms of dc-link voltages and neutral-point currents. The ripple of dc-link voltage is increased by 7.9 V in the conventional interleaved DPWM with reduced switching loss of power semiconductors. The proposed method suppresses the high-frequency circulating current based on DPWM to reduce the switching loss by balancing neutral-point voltage 8.1 V. The neutral-point voltage and current are increased in the proposed method compared to the conventional method. The lifetime of capacitors in each method is estimated

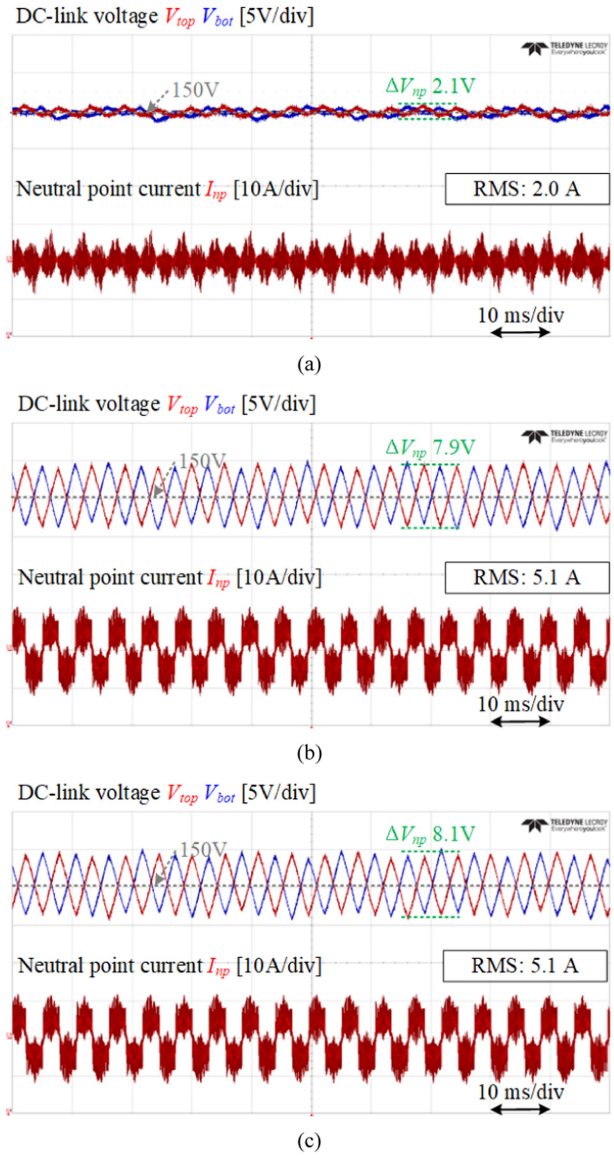

Fig. 14. Experimental results of dc-link voltages and neutral-point current at MI 1.0. (a) Conventional interleaved SVM. (b) Conventional interleaved DPWM. (c) Proposed modulation.

based on ALC70/KEMET. The lifetime of the proposed method is decreased by 7.0% compared to the conventional SVM according to the lifetime estimation process.

The characteristics of each method are analyzed in Table VI. The difference in common mode voltage inducing the circulating current is $V_{\rm dc}/2$, and the high-frequency circulating current is generated by 5.6 A in conventional SVM. However, the circulating current has been reduced to 1.2 A according to the proposed modulation that decreases the difference in common mode voltage to $V_{\rm dc}/6$. The THD average of output currents in the proposed modulation is improved from 2.4% to 1.7%. In addition, the efficiencies of each method are analyzed using the power analyzer, and the efficiency of the proposed reduction modulation is improved from 91.6% to 93.5%. The proposed method can operate more efficiently despite the lower lifetime of the capacitor.

VI. Conclusion

This article proposed the reduction method of circulating current in parallel three-level inverters using modified interleaved DPWM. Parallel inverters have been widely applied in requiring high power and efficiency due to their adjustable power rating. However, the high-frequency circulating current is generated when the inverter operates asynchronously to increase the output quality. The high-frequency circulating current in parallel inverter causes deterioration of reliability by increasing output current ripples and the losses of switches. Various reduction methods for high-frequency circulating current using additional hardware have been proposed in previous studies. These methods have disadvantages such as increment of volume and cost in parallel inverters. To alleviate these problems, the modified interleaved DPWM modulation method was proposed to reduce the high-frequency circulating current. The modified interleaved DPWM modulation method used the carrier phase shift algorithm to suppress high-frequency circulating current caused by the carrier phase difference in the interleaving scheme. The switching sequences of each modulation method were analyzed to reduce the difference in common mode voltage causing the fluctuation of high-frequency circulating current. The proposed method effectively reduced the high-frequency circulating current without the MI limit. The THD of the output current and the efficiency of inverter are improved by applying the proposed modulation. The proposed method's effectiveness in various conditions was verified by the simulation and experimental results.

References

[1] X. Xing, C. Zhang, A. Chen, H. Geng, and C. Qin, "Deadbeat control strategy for circulating current suppression in multiparalleled three-level inverters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6239–6249, Aug. 2018.

[2] C. Zhang, X. Li, X. Xing, B. Zhang, R. Zhang, and B. Duan, "Modeling and mitigation of resonance current for modified LCL-type parallel inverters with inverter-side current control," *IEEE Trans. Ind. Inform.*, vol. 18, no. 2, pp. 932–942, Feb. 2022.

[3] M. Takongmo, C. Zhang, and J. Salmon, "Coupled inductors for high-frequency drives with parallel-connected inverter lags," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 7055–7066, Jun. 2022.

[4] K.-B. Lee and J.-S. Lee, *Reliability Improvement Technology for Power Converters*. Berlin, Germany: Springer-Verlag, 2017.

[5] J. Liu, X. Sun, B. Ren, and Q. Zhang, "Dynamic circulating current suppression method for multiple hybrid power parallel grid-connected inverters with model reference adaptive system," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4364–6375, May 2022.

[6] Y.-J. Kim, S.-M. Kim, and K.-B. Lee, "Improving DC-link capacitor lifetime for three-level photovoltaic hybrid active NPC inverters in full modulation index range," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5250–5261, May 2021.

[7] I. M. Alsofyani and K.-B. Lee, "Simple capacitor voltage balancing for three-level NPC inverter using discontinuous PWM method with hysteresis neutral-point error band," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12490–12503, Nov. 2021.

[8] J.-S. Lee, R. Kwak, and K.-B. Lee, "Novel discontinuous PWM method for a single-phase three-level neutral point clamped inverter with efficiency improvement and harmonic reduction," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9253–9266, Nov. 2018.

[9] H.-W. Lee, S.-J. Jang, and K.-B. Lee, "Advanced DPWM method for switching loss reduction in isolated DC type dual inverter with open-end winding IPMSM," *IEEE Access*, vol. 11, pp. 2700–2710, 2023.

[10] Z. Zeng, Z. Li, and S. M. Goetz, "Optimal discontinuous space vector PWM for zero-sequence-circulating current reduction in two paralleled three-phase two-level converter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1252–1262, Feb. 2021.
[11] J. Wang, F. Hu, W. Jiang, W. Wang, and Y. Gao, "Investigation of zero sequence circulating current suppression for parallel three-phase grid-connected converters without communication," *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 7620–7629, Oct. 2018.
[12] S.-W. An, S.-M. Kim, and K.-B. Lee, "Capacitor lifetime extension in a hybrid active neutral-point-clamped inverter with reduction of DC-link ripple current and common-mode voltage," *IEEE Access*, vol. 9, pp. 40336–40348, 2021.
[13] Q. Zhang, X. Xing, and K. Sun, "Space vector modulation method for simultaneous common mode voltage and circulating current reduction in parallel three-level inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3053–3066, Apr. 2019.
[14] J. S. S. Prasad, R. Ghosh, and G. Narayanan, "Common-mode injection PWM for parallel converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 789–794, Feb. 2015.
[15] X. Xing, X. Li, C. Qin, J. Chen, and C. Zhang, "An optimized zero-sequence voltage injection method for eliminating circulating current and reducing common mode voltage of parallel-connected three-level converters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6583–6596, Aug. 2020.
[16] H.-W. Choi and K.-B. Lee, "Circulating current reduction for parallel-connected modular inverters based on suppression of common-mode voltage," *IEEE Trans. Power Electron.*, vol. 38, no. 9. pp. 11091–11101, Sep. 2023.
[17] S. He, Y. Wang, and B. Liu, "A modified DPWM method with minimal line current ripple and zero-sequence circulating current for two parallel interleaved 2L-VSIs," *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 11879–11889, Dec. 2022.
[18] A. Laka, J. A. Barrena, J. C. Zabalza, M. A. R. Vidal, and G. Calvo, "Novel zero-sequence blocking transformer (ZSBT) using three single-phase transformers," *IEEE Trans. Energy Convers.*, vol. 28, no. 1, pp. 234–242, Mar. 2013.
[19] X. Li, X. Xing, C. Qin, C. Zhang, and G. Zhang, "Design and control method to suppress resonances circulating current for parallel three-level rectifiers with modified LCL filter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 7012–7023, Aug. 2021.
[20] H.-W. Choi and K.-B. Lee, "Review of methods for reducing circulating currents in parallel connected modular inverters," *J. Elect. Eng. Technol.*, vol. 18, no. 2, pp. 1227–1242, Mar. 2023.
[21] W. Jiang, Y. Gao, B. Xiao, J. Wang, X. Ding, and L. Wang, "Suppression of high-frequency circulating current caused by asynchronous carriers for parallel three-phase grid-connected converters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1031–1040, Feb. 2018.
[22] Z. Xueguang, W. Li, Y. Xiao, G. Wang, and D. Xu, "Analysis and suppression of circulating current caused by carrier phase difference in parallel voltage source inverters with SVPWM," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 11007–11020, Dec. 2018.
[23] Z. Zeng, Z. Li, and S. M. Geotz, "A high performance interleaved discontinuous PWM strategy for two paralleled three-phase inverter," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13042–13052, Dec. 2020.
[24] A. Tcai, Y. Kwon, S. Pugliese, and M. Liserre, "Reduction of the circulating current among parallel NPC inverters," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12504–12514, Nov. 2021.
[25] H. Xu, L. Xu, C. Li, K. Wang, Z. Zheng, and Y. Li, "Improved interleaved discontinuous PWM for zero-sequence circulating current reduction in three-phase paralleled converters," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 8676–8686, Sep. 2021.
[26] H. Wang, P. Davari, H. Wang, D. Kumar, F. Zare, and F. Blaabjerg, "Lifetime estimation of DC-link capacitors in adjustable speed drives under grid voltage unbalances," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4064–4078, May 2019.

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