Novel Bidirectional High-Frequency Isolated Direct AC/AC Converter With Unipolar Phase-Shifted Modulation Strategy

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***Abstract*—This article introduces a novel bidirectional high-frequency isolated direct ac/ac converter with unipolar phase-shifted modulation strategy based on double dc modulation indexes. The main idea of topological construction is that the non-isolated two-level nondifferential bipolar direct ac/ac converter is combined to the bidirectional phase-shifted full-bridge converter, which inherits the advantages of no commutation problem, zero voltage switching, simple control, bipolar output voltage gains, et al. The operating principles of this converter and the design considerations for the key parameters are given in detail. Moreover, the application in voltage sag/swell compensation is simply analyzed. Thanks to the high-frequency isolation capability, it satisfies needs of distribution networks in terms of sensitive loads protection, voltage resilience control without applying the bulky line frequency transformers. Finally, the feasibility of this proposed topology is verified by the various experimental results of the prototype.**

***Index Terms*—Commutation problem, direct ac/ac converter, high-frequency isolated, unipolar phase-shifted modulation strategy.**

I. Introduction

With the continuous implementation and promotion of the national strategy of carbon peaking and carbon neutralization, the proportion of renewable energy represented by wind power and photovoltaic will be higher and higher in energy consumption and utilization in the future. As one of the key equipment of renewable energy generation and utilization, the development and research of power electronic converter plays an indispensable role in the utilization of renewable energy. Besides with the increasing demand of loads for high-quality power supply, highly reliable electricity supply has become an important issue [1]. As the ac/ac conversion among the four power conversion technologies of power electronics, it is broadly used in a wide range of industrial applications in distributed energy systems, dynamic voltage regulation, variable-speed electric drive systems, wind power generation systems and so on [2], [3]. For ac/ac power conversions in industry, the traditional way is to use ac thyristor power converters, which can produce the desired output voltage by implementing the phase angle or integral cycle control on input ac voltage [4]. However, this type of ac converter has some significant drawbacks such as harmonic performance, low power factor and efficiency, and slow dynamic response [5], [6]. To overcome the above weakness of ac thyristor power converters, a variety of ac/ac converters using pulsewidth modulation (PWM) modulation are proposed. Thanks to the high working frequency of the converter (the carrier frequency of the converter is much greater than the line frequency of the input ac source), it will not produce low-order harmonics and the dynamic response is fast. These numerous topologies of PWM ac/ac converters can be broadly divided into: the indirect ac/ac converters with dc-links [7], [8], [9], [10], and the direct ac/ac converters [11], [12], [13], [14], [15], [16]. Although the indirect ac/ac converters can realize the conversion of ac voltage amplitude and frequency at the same time, this advantage is not obvious in applications where only the voltage amplitude needs to be adjusted. Moreover, the indirect ac/ac converters require dc energy storage elements in the form of electrolytic capacitors, which are the prominent factor effecting reliability of the power converters in addition to slowing response speed of the systems [17]. The direct ac/ac converters have no dc-link, single power processing stage, smaller size, and low cost [18], [19], which makes it more attractive for this kind of applications where only need to maintain the voltage amplitude without changing phase-shift and frequency at the same time. Dynamic voltage restores dynamic voltage restore (DVR) based on ac/ac converters, as shown in Fig. 1, are commonly used FACTS facilities that stabilized the load voltage during grid voltage disruptions.

The common direct ac/ac converters include buck [13], [15], boost [20], buck-boost [12], Z-source [21], [22], [23], matrix

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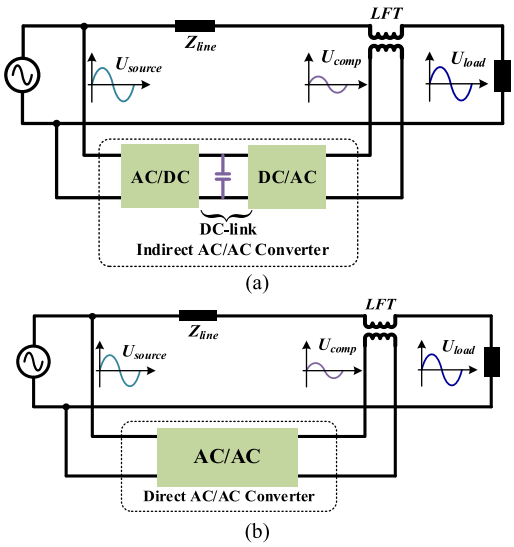

Fig. 1. Equivalent circuit of a DVR supplied through the ac line. (a) DVR based on indirect AC/AC converter. (b) DVR based on direct AC/AC converter.

converters [24], [25], [26], and so on. Matrix direct ac/ac converters are also capable of providing simultaneous alternating voltage amplitude and frequency control, but they have only achieved low market penetration owing to suffering from the limited voltage transfer ration and commutation issues [27], [28], [29]. Most of Z-source converters need soft commutation strategy or lossy resistor-capacitor snubber circuits [30], but the two methods have some limitations such as output voltage waveforms are distorted and soft commutation strategy does not have the ability of reliable commutation when the input/output voltage or current is highly distorted [31], [32], [33]. To achieve reliable commutation, many topologies have been proposed in recent studies. A novel single-phase direct ac/ac converter adopting switching cell structure without commutation problems is proposed in the literature [34]. Based on this infrastructure, many extended direct ac/ac converter topologies have been proposed by relevant scholars [35], [36]. Moreover, a bipolar direct ac/ac converter was proposed in [13] and [15], which solves the commutation problem and realizes bipolar output voltage gain. However, these topologies are nonisolated, therefore they need external bulky line-frequency transformers (LFTs) when they are used in occasions requiring electrical isolation. The LFTs have drawbacks such as large size, high cost, saturation, and high inrush current [37]. In addition, the impedance of LFT results in voltage drops and increases load harmonics, which become more severe for nonlinear loads.

In order to overcome the above weakness of nonisolated direct ac/ac converter in application, some scholars have proposed a variety of high frequency isolated direct ac/ac converter topologies. Compared with LFT, high-frequency isolation transformer has obvious advantages, such as high-power density and small volume. Therefore, many scholars have conducted research on the topology of high-frequency isolated direct ac/ac converters. A direct ac/ac dual-active-bridge converter was proposed for solid-state transformer by the scholars in [38] and [39], this converter allows bidirectional power flow and can regulate output voltage when input voltage changes. However, it needs to adopt a soft commutation strategy to ensure safe and reliable commutation owing to the use of bidirectional switches (each switch is composed of two fully controlled devices in reverse series). A single-phase buck matrix converter with high-frequency transformer (HFT) isolation was also presented in [40]. Although the topology does not use bidirectional switches, it still needs a special soft commutation strategy to achieve safe commutation. A high-frequency isolated converter without soft commutation strategy was proposed in [41], but essentially, it still has dc-link and the conversion process is complex. Research works in [42] and [43] presented high-frequency isolated direct ac/ac converter, but the converter in [42] can mitigate voltage sags with maximum depths of only 25% of line voltage and the converter in [43] cannot compensate voltage sags with depths of less than 50%. Scholar proposes a high-frequency isolated multilevel cascaded-type bipolar direct ac/ac converter in [44], its biggest superiority is that it can provide higher output voltages with standard low-voltage rated devices. However, there may also be commutation issues owing to the use of back-to-back switches in the converter.

In addition, high-frequency isolated direct ac/ac converter with folding and unfolding bridges were proposed in [45], [46], and [47]. These topologies have the ability of high-frequency isolation and can achieve ZVS, but they essentially contain dc-links.

This article proposes a novel bidirectional high-frequency isolated direct ac/ac converter topology by combing the nonisolated two-level nondifferential bipolar direct ac/ac converter with the bidirectional phase-shifted full-bridge converter (PSHB). The converter proposed has no commutation problem and does not use back-to-back switches, and it can achieve bipolar gain of output voltage with high frequency isolation and can achieve ZVS thanks to the proposed modulation strategy and its topology.

The rest of this article is organized as follows. In Section II, the topology of the proposed converter is presented, and its modulation strategy is analyzed in detail. In Section III, the converter steady operations are discussed. Then, the analysis and design key component of the proposed converter are carried out in Section IV. The feasibility of the proposed converter in grid voltage regulation is analyzed theoretically in Section V. In Section VI, the experimental results verify the correctness of the theoretical analysis. Finally, Section VII concludes this article.

II. Proposed Novel Bidirectional HFT-Isolated Direct AC/AC Converter and Modulation Strategy

A. Topology of the Proposed Converter

A non-isolated novel H-bridge direct ac/ac converter was first proposed in [13], which it effectively overcomes the commutation problems due to the use of two-level nondifferential ac chopper legs. On this basis, we integrate it with PSHB and propose a novel bidirectional high-frequency isolated direct ac/ac converter as shown in Fig. 2. The proposed converter

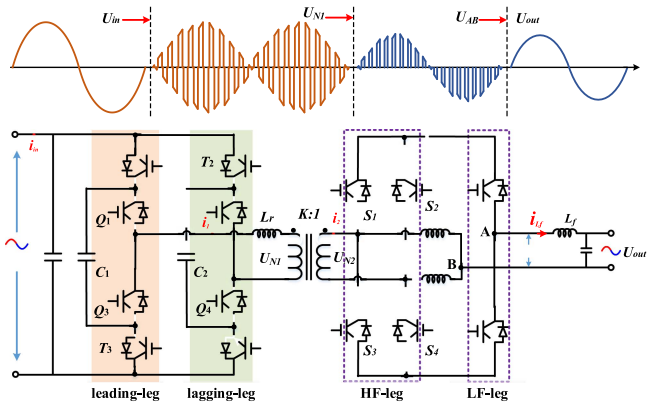

Fig. 2. Topology of high-frequency isolated direct AC/AC converter.

commendably retains the benefits of the non-isolated novel H-bridge direct ac/ac converter and PSHB, such as no commutation problem, ZVS, simple control, bipolar output voltage gains.

The proposed converter consists of an input direct ac/ac converter, a HFT, an output hybrid converter, and output filter as seen in Fig. 2. The input converter is comprised of one input capacitor (C_{in}), leading-leg and lagging-leg. Each leg contains four switches ($T_1 \sim T_4$ or $Q_1 \sim Q_4$), and one capacitor (C_1 or C_2). The capacitor (C_1 or C_2) is used to absorb stray energy in the line. Due to the inability to provide completely safe and reliable commutation adopting RC snubber circuits or special commutation strategies, the proposed converter does not require these two commutation methods, thus improving the reliability of the converter to a certain extent.

The output hybrid converter is composed of three half bridge legs and two separated inductors. The two legs composed of switches $S_1 \sim S_4$ are defined as high-frequency bridge leg, which work in high-frequency mode, and the bridge leg composed of switches $S_{B1} \sim S_{B2}$ are defined as line-frequency bridge legs, which work in line frequency mode. The high-frequency bridge legs are connected with two separated inductors L_1 and L_2. The use of separated inductors can make the output hybrid converter effectively avoid the shoot-through when switches $S_1 \sim S_4$ are turned ON, simultaneously.

HFT realizes the function of electrical isolation instead of traditional LFT, and its transformation ration is $k = N_1{:}N_2$. The primary side of the HFT is connected to the input converter, and the secondary side is connected to the output converter as shown in Fig. 2.

In order to better understand the topology proposed and have an objective comparison, this article is compared with the existing HFT-isolated direct ac/ac converters in Table I.

TABLE I
COMPARISON BETWEEN THE PROPOSED CONVERTER AND PREVIOUSLY PUBLISHED CONVERTERS

	This article	Qin and Kimball [38]	Nasir et al. [39]	Kang et al. [41]	Filho et al. [48]	Ahmed et al. [49]
Adopt bidirectional switches	No	Yes	Yes	No	No	Yes
Commutation solutions	No	Commutation strategy	Commutation strategy	No	No	Commutation strategy
Number of switches	14	16	16	16	8,12, 16	6
Number of passive components	6	3	1	2	11, 11, 15	8
Output voltage gain	Bipolar	Unipolar	Bipolar	Bipolar	Unipolar	Bipolar
Bidirectional power flow	Yes	Yes	Yes	Yes	Yes	Yes

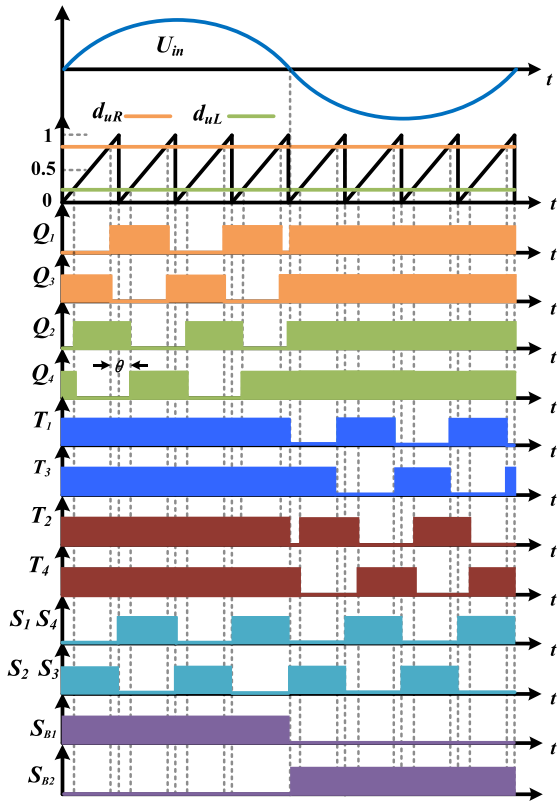

Fig. 3. Modulation principle for the proposed converter.

B. Unipolar Phase-Shifted Modulation Strategy

Based on the PSHB modulation strategy, a unipolar phase-shifted modulation strategy based on double dc modulation wave is proposed in this article, as shown in Fig. 3. In Fig. 3, d_{uR} and d_{uL} are dc modulated wave signals of leading-leg and lagging-leg respectively, whiles u_C represents sawtooth carrier signal, and there is a phase difference θ between the leading-leg and lagging-leg of the input converter. The high-frequency leg in the output converter adopts high-frequency square wave modulation with fixed frequency, and the line frequency leg uses line frequency modulation with frequency of 50 Hz. By giving different driving signals to line frequency bridge leg switches S_{B1} and S_{B2}, the converter can work both noninverting and inverting operations.

As can be seen from Figs. 2 and 3, the input 50 Hz sinusoidal ac voltage is modulated into bipolar three state $(+1, 0, -1)$ high frequency pulse ac voltage (U_{N1}, U_{N2}) by the input converter, meanwhile the output hybrid converter can demodulate bipolar three state high frequency pulse ac voltage into unipolar three state high frequency pulse ac voltage (U_{AB}). The unipolar three state high frequency pulse ac voltage (U_{AB}) ripple is smaller, which is conducive to obtaining a stable and high-quality 50 Hz sinusoidal ac voltage through output filtering. This modulation strategy not only enables the converter to realize ZVS, but also effectively reduces output filter volume. In addition, it should be noted that the dead time of the input converter has been analyzed in detail in [23], and the application of the separated inductor effectively solves the bridge arm shoot-through problem of the output converter, so the dead time is not shown in Fig. 3.

III. Circuit Steady Operation

Combined with the topology of the converter shown in Fig. 2 and the modulation strategy shown in Fig. 3, the working modes of the converter can be divided into four types according to the input voltage U_{in} and the direction of current i_{Lf}. Regardless of whether the output voltage is in phase or out of phase with the input voltage, the converter has the following four operating processes within an ac voltage cycle: type I ($U_{\text{in}} > 0$, $i_{Lf} > 0$); type II ($U_{\text{in}} < 0$, $i_{Lf} < 0$); type III ($U_{\text{in}} < 0$, $i_{Lf} > 0$); and type IV ($U_{\text{in}} > 0$, $i_{Lf} < 0$). Because there are similarities in the working process of the converter in these four working modes, in order to avoid repeated description, this article only takes type I and type II when the output voltage is in phase with the input voltage as examples for detailed analysis. In the steady-state theoretical analysis, it is assumed that the switches, capacitors, and inductors in the converter are ideal components, and the wingding ratio of HFT is $k = N_1/N_2$. Moreover, the following analysis considers dead time of the converter.

A. Type I Working Mode ($U_{in} > 0$, $i_{Lf} > 0$)

In this working mode of the converter, the switches $T_1 \sim T_4$ and S_{B1} are always turned ON, the switch S_{B2} is always turned OFF, and the switches $Q_1 \sim Q_4$ and $S_1 \sim S_4$ are all subject to high frequency modulation. As shown in Fig. 4, ten operation stages exist within a high frequency switching period under steady-state operation.

1) *Stage 1 [$t_1 \sim t_{11}$]:* Before time t_1, the switch Q_1 is ON, and the current i_1 flows through the sources, the body diode of T_1, Q_1, Q_4, the body diode of T_4; At the same time, the switches S_1 and S_4 are ON, and the current i_2 flows through the body diode of S_1, S_{B1}, and L_2, the working process can be described in Fig. 5(h).

At moment t_1, the switch Q_1 is turned OFF at full voltage, and the converter is in passive mode. The time period [$t_1 \sim t_{11}$] is a dead time of the converter when the switch Q_3 has not yet been turned ON, and the body diode of the switch Q_3 is forward biased conduction during this time interval. So, the primary side current i_1 forms a closed loop through the body diodes of the Q_3 and T_4, the switches T_3 and Q_4; the current i_{Lf} flows through S_1 body diode, S_{B1}, and the separated inductors L_2 to form a circulation loop during this time interval. The working process of the converter is shown in Fig. 5(a). Since the body diode of switch S_3 is still in the reverse bias state, there is no circulating current between the two separated inductors in this stage.

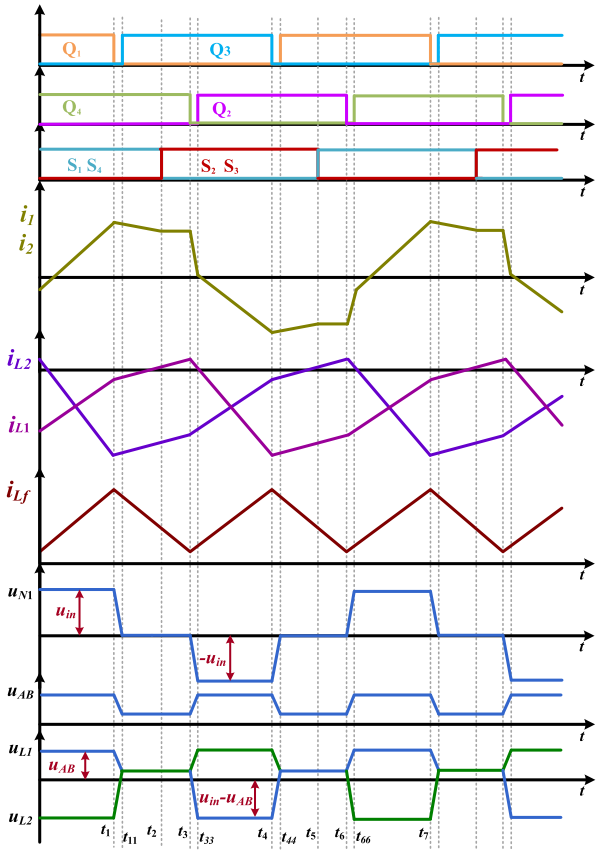

Fig. 4. Steady schematic waveforms of proposed converter in type I working mode.

At this stage, the energy on the power side cannot be transferred to the load side, and the converter begins to enter freewheeling mode (passive mode). Meanwhile, the primary side current i_1 and output filter inductor current i_{Lf} decrease linearly, as shown in Fig. 4. The setting of the dead time is discussed in detail in the Section IV.

2) *Stage 2 [$t_{11} \sim t_2$]:* At this stage, the converter is still *n* freewheeling mode, and the relationship between voltage and current is the same as at *stage 1*. At time t_{11}, the switch Q_3 is turned ON. Since the body diode of the switch Q_3 has been turned ON at *stage 1*, the switch Q_3 is turned ON with zero voltage switching (ZVS) at t_{11}. The working process of the converter at this stage can still be described in Fig. 5(a). During this process, the current flow direction of the separated inductor L_1 changes. The voltage and current relationship as follows:

$$\begin{cases} u_{N1} = u_{N2} = 0 \\ u_{L1} = u_{L2} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} \\ u_{L1} = u_{L2} = u_{AB} = u_{\text{out}} - L_f \frac{di_{Lf}}{dt} \\ i_2 = i_{L2} = i_{L1} + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} \end{cases}. \tag{1}$$

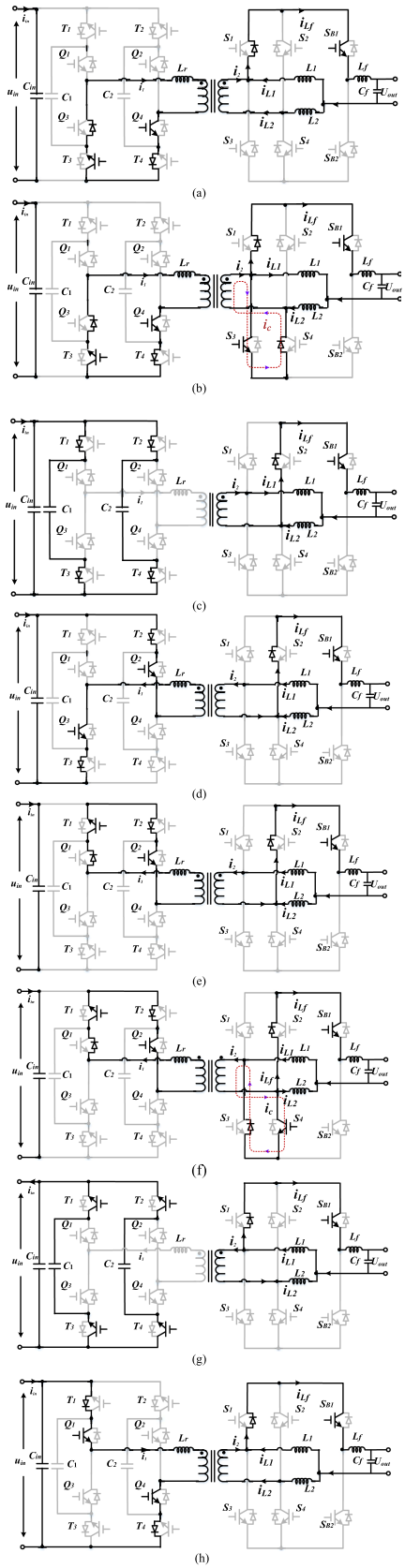

Fig. 5. Operation stages of the proposed converter in one switching cycle. (a) *Stages* 1 and 2. (b) S*tage* 3. (c) S*tage* 4. (d) *Stage* 5. (e) *Stages* 6 and 7. (f) *Stage* 8. (g) *Stage* 9. (h) *Stage* 10.

3) *Stage 3 [t_2∼t_3]:* The switches Q_3 and Q_4 are in the ON state, and the switches Q_1 and Q_2 are in the OFF state during this time interval. At time t_2, the switches S_1 and S_4 are turned OFF with ZVS, and the switches S_2 and S_3 are turned ON with ZVS. The primary side current i_1 still flows through Q_4, the body diode of T_4, T_3, and the body diode of Q_3; the current i_{Lf} also flows through S_1 body diode, S_{B1}, and the separated inductor L_2 during this time interval. Compared to *stage 2*, the branch current i_c will be generated at this stage due to the forward bias of the switch S_4 body diode and the switch S_3 is turned ON, as indicated by the red dotted line in Fig. 5(b). It should be pointed out that the current flow direction of the separated inductor L_1 has changed during this stage. The working process of the converter is shown in Fig. 5(b), the voltage and current relationship as follows:

$$\begin{cases} u_{N1} = u_{N2} = 0 \\ u_{L1} = u_{L2} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} \\ u_{L1} = u_{L2} = u_{AB} = u_{\text{out}} - L_f \frac{di_{Lf}}{dt} \\ i_2 = i_{L1} + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} + i_c \\ i_{L2} = i_{L1} + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} \end{cases}. \tag{2}$$

The converter is still in freewheeling mode (passive mode) during this time interval.

4) *Stage 4 [t_3∼t_{33}]:* This period is the dead time of the input side converter, the input ac power supply charges the input capacitors C_{in}, the capacitor C_1, and the capacitor C_2. Additionally, the switch S_4 body diode reverse bias during this time interval, so the branch current i_c disappears. The current i_2 realizes safe commutation when the secondary side voltage $u_{N2} = 0$. The specific working process of the converter can be referred to Fig. 5(c).

5) *Stage 5 [t_{33}∼t_4]:* From *stage 4*, it can be seen that the switch Q_2 body diode has turned ON with a forward bias during the dead time. Therefore, the switch Q_2 is turned ON with ZVS at t_{33}.

The primary side current i_1 flows through the body diode of T_2, Q_2, Q_3, and the body diode of T_3; the current i_{Lf} flows through S_2 body diode, S_{B1}, and the separated inductor L_2 during this time interval. The working process of the converter is shown in Fig. 5(d). The voltage and current relationship as follows:

$$\begin{cases} u_{N1} = -u_{\text{in}}, u_{N2} = \frac{1}{k} u_{N2} \\ u_{AB} = u_{\text{out}} + L_f \frac{di_{Lf}}{dt} = u_{L2} = L_2 \frac{di_{L2}}{dt} \\ u_{L1} = L_1 \frac{di_{L1}}{dt} = u_{N2} + u_{L2} \\ i_2 = k \cdot i_1 = i_{L1} \\ i_{L2} = -i_2 + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} \end{cases}. \tag{3}$$

During this period, the converter reenters the active mode and establishes a negative level ($U_{N1} = -U_{\text{in}}$, $U_{N2} = \frac{1}{k} U_{N1}$) for the primary and secondary sides of the HFT. At this stage, since the body diode of switch S_1 is reverse biased and the body diode of switch S_2 is forward biased, output filter inductor current i_{Lf} can realize safe commutation.

6) *Stage 6 [t_4∼t_{44}]:* This period is also the dead time of the input side converter. At time t_4, the switch Q_3 is turned

OFF with full voltage, and the switch Q_1 body diode is forwarded bias conduction. The working process can be described in Fig. 5(e).

7) *Stage 7 [t_{44}~t_5]:* During this stage, the switches Q_2, S_2 and S_3 are in the ON state, the switches Q_4, S_1, and S_4 are in the OFF state. At time t_{44}, the switch Q_1 is turned ON with ZVS. The primary side current i_1 flows through the body diode of Q_1, T_1, the body diode of T_2, Q_2; the current i_{Lf} flow circuit is the same as that in stage 5. The working process of the converter is can also be described in Fig. 5(e), the voltage and current relationship as follows:

$$\begin{cases} u_{N1} = u_{N2} = 0 \\ u_{AB} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} \\ u_{AB} = u_{\text{out}} - L_f \frac{di_{Lf}}{dt} \\ i_2 = k \cdot i_1 = i_{L1} \\ i_{L2} = -i_2 + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} \end{cases}. \tag{4}$$

At this stage, the converter is also in freewheeling mode (passive mode), and the primary side current i_1 successfully achieves commutation. Moreover, since the body diode of the switch S_4 has no forward conduction bias, there is no branch current in this process.

8) *Stage 8 [t_5~t_6]:* The switches Q_1 and Q_2 are in the ON state, and the switches Q_3 and Q_4 are in the OFF state during this time interval. At time t_5, the switches S_1 and S_4 are turned ON with ZVS, and the switches S_2 and S_3 are turned OFF with ZVS. Due to the S_4 is turned ON and the body diode of S_3 is forwarded bias conduction, this process also produces a branch current i_c, as shown in the red dotted line marked part of Fig. 5(f). The working process of the converter is shown in Fig. 5(f), the voltage and current relationship as follows:

$$\begin{cases} u_{N1} = u_{N2} = 0 \\ u_{AB} = L_1 \frac{di_{L1}}{dt} = L_2 \frac{di_{L2}}{dt} \\ u_{AB} = u_{\text{out}} - L_f \frac{di_{Lf}}{dt} \\ i_2 = C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} + i_{L2} + i_c \\ i_{L1} = i_{L2} + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} \end{cases}. \tag{5}$$

At this stage, the converter is also in freewheeling mode (passive mode).

9) *Stage 9 [t_6~t_{66}]:* This period is also the dead time of the input side converter. At time t_6, the switch Q_2 is turned OFF with full voltage. The capacitors C_1 and are C_2 is discharged, and the switch Q_4 body diode is turned ON with a forward bias. The working process of the converter can be described in Fig. 5(g).

10) *Stage 10 [t_{66}~t_7]:* In this stage, the switches Q_1, S_1 and S_4 are in the ON state, and the switches Q_2, S_2 and S_3 are in the OFF state. Due to the Q_4 body diode is turned ON with a forward bias in *stage 9*, the Q_4 is turned ON with ZVS at time t_{66}. The primary side current i_1 forms a closed loop through the body diodes of the T_1 and T_4, the switches Q_1 and Q_4; the current i_{Lf} flows through S_1 body diode, S_{B1}, and L_1 to form a circulation loop during this time interval. The working process of the converter is shown in Fig. 5(h). Because the leakage inductance is very small, the voltage drop of the leakage inductors is ignored in the analysis. The voltage and current relationship as follows:

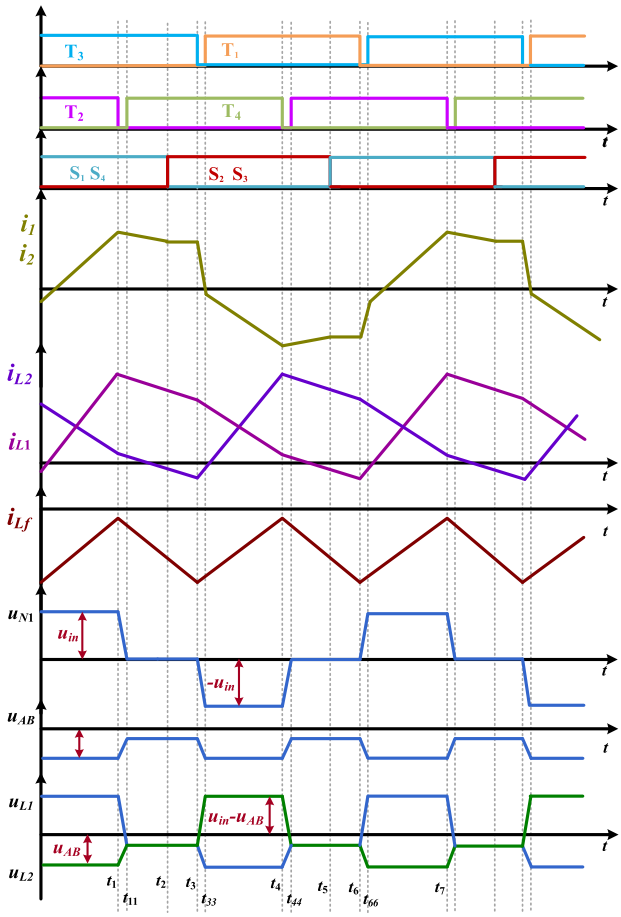

Fig. 6. Steady schematic waveforms of proposed converter in type II working mode.

$$\begin{cases} u_{N1} = u_{\text{in}} = k \cdot u_{N2} \\ u_{L1} = L_1 \frac{di_{L1}}{dt} = u_{AB} \\ u_{AB} = u_{\text{out}} + L_f \frac{di_{Lf}}{dt} \\ u_{L2} = u_{N2} - u_{AB} \\ i_{L1} = i_{L2} + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}}, i_{L2} = i_2 \end{cases}. \tag{6}$$

During this period, the converter is in the active mode, and the energy on the power side is transferred to the load side through the HFT. At the same time, the primary side current i_1 and output filter inductor current i_{Lf} increase linearly. In addition, since the body diode reverse bias of the switch S_3 cannot be turned ON, there is no circulating current between the two separated inductors of the converter in this process. It can be seen from Fig. 5(h) that when $i_{Lf} < 0$, the converter can also provide a current flow loop. After time t_7, the converter enters the next switching cycle.

B. Type II Working Mode ($U_{in} < 0$, $i_{Lf} < 0$)

As can be seen from Fig. 6, when the input ac voltage is negative half wave and the dead time of the converter is considered, the converter also has ten operating stages. In this working mode,

the switches $Q_1 \sim Q_4$ are always in the on state, and the switches $T_1 \sim T_4$ operate in a high-frequency modulation.

1) *Stage 1 [$t_1 \sim t_{11}$]:* This period is the dead time of the input side converter. Before time t_1, the switch T_2 is ON, and the current i_1 flows through the sources, the switch T_3, the body diode of Q_3, the body diode of Q_2, and the switch T_2; At the same time, the switches S_1 and S_4 are ON, and the current i_2 flows through the L_1, the switch S_{B2}, the body diode of S_4, the working process can be described in Fig. 7(h).

At time t_1, the switch T_2 is turned OFF with full voltage and the switch T_4 is not conductive. The working process can be described in Fig. 7(a). Additionally, the body diode of the switch T_4 forward bias conduction.

2) *Stage 2 [$t_{11} \sim t_2$]:* The switch T_4 is turned ON with ZVS at time t_{11} owing to the body diode of the switch T_4 forward bias conduction before time t_{11}. The primary side current i_1 passes through the primary side winding, the switch Q_4, the body diode of the switch T_4, the switch T_3, and the body diode of the switch Q_3 to form a flow circuit. The flow path of the secondary side current i_2 is a circuit composed of a separated inductor L_1, a filter inductor L_f, a switch S_{B2}, and the switch S_4 body diode. The working process also can be described in Fig. 7(a). The mathematical relationship between converter voltage and current is as follows:

$$\begin{cases} u_{N1} = k \cdot u_{N2} = 0 \\ u_{L1} = L_1 \frac{di_{L1}}{dt} = u_{L2} = L_2 \frac{di_{L2}}{dt} \\ u_{AB} = u_{\text{out}} + L_f \frac{di_{Lf}}{dt} = u_{L1} \\ i_2 = i_{L1} = k \cdot i_1 \\ i_{L1} = -i_{L2} + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} \end{cases} . \tag{7}$$

3) *Stage 3 [$t_2 \sim t_3$]:* The output side converter realizes commutation when the voltage is 0. Therefore, at time t_2, the switches S_1 and S_2 are turned ON with ZVS, and the switches S_3 and S_4 are turned OFF with ZVS. Due to the conduction of the switch S_1 body diode and the switch S_2, there is a branch current i_m during this time interval. The voltage and current relationship as follows:

$$\begin{cases} u_{N1} = k \cdot u_{N2} = 0 \\ u_{L1} = L_1 \frac{di_{L1}}{dt} = u_{L2} = L_2 \frac{di_{L2}}{dt} \\ u_{AB} = u_{\text{out}} + L_f \frac{di_{Lf}}{dt} = u_{L1} \\ i_2 = i_{L1} = k \cdot i_1 \\ i_{L1} = i_{L2} + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} + i_m \end{cases} . \tag{8}$$

At *this* stage, the converter remains in passive mode and the working process can be described in Fig. 7(b).

4) *Stage 4 [$t_3 \sim t_{33}$]:* The switches $T_1 \sim T_2$ and the switches S_1, S_4 are OFF state in this stage, and the switches T_4, S_2, S_3 are ON state simultaneously. Additionally, the switch T_3 is turned OFF with full voltage at time t_3. This stage is also a dead time of the input converter. The energy on the primary side is charged to the input capacitor C_{in} through the switch Q_4, the body diodes of the switch T_4 and T_1, the switch Q_1. The secondary side current achieves safe commutation, while the branch current i_m disappears.

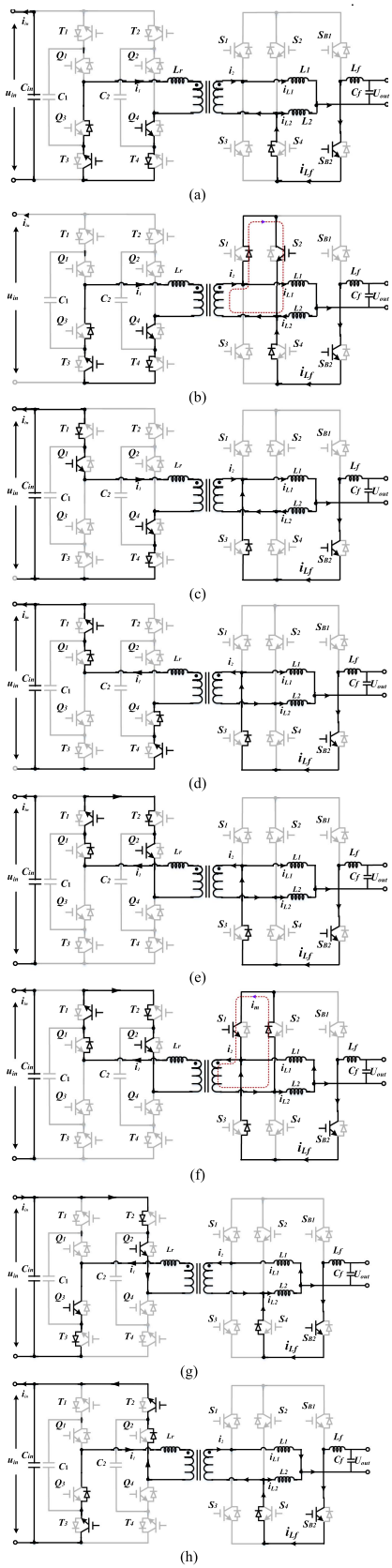

Fig. 7. Operation stages of the proposed converter in one switching cycle. (a) *Stages* 1 and 2. (b) *Stage* 3. (c) *Stage* 4. (d) *Stage* 5. (e) *Stages* 6 and 7. (f) *Stage* 8. (g) *Stage* 9. (h) *Stage* 10.

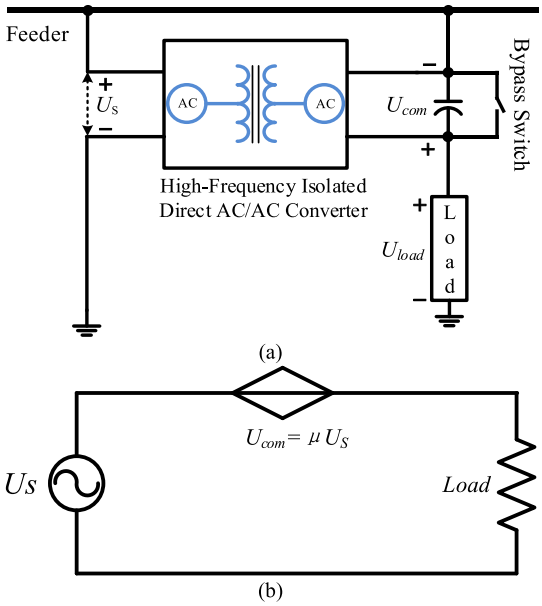

Fig. 8. Schematic diagram of the proposed converter for voltage regulation. (a) System wiring diagram. (b) Equivalent circuit diagram.

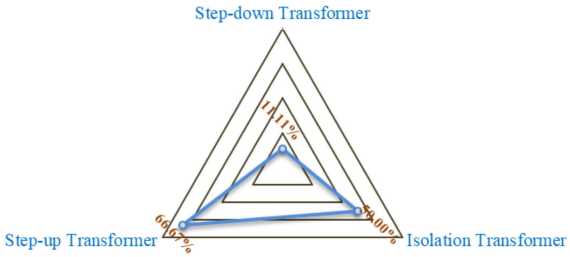

Fig. 9. Theoretical compensation degree of grid voltage under different types of high frequency isolation transformers.

The working process of the converter can be displayed in Fig. 7(c).

5) *Stage 5 [t_{33}~t_4]:* During this time interval, the switches T_2~T_3, S_1, S_4 are OFF state and the switches T_4, S_2, S_3 are ON state. The switch T_1 are turned ON with ZVS at time t_{33} owing to the body diode of the switch T_1 has been conducting before t_{33} moment. The primary side current i_1 flows through the switch T_4, the body diode of the switches Q_4 and Q_1, and the switch T_1 to form a flow circuit. The secondary side current i_2 flows through the filter inductor L_f, the switch S_{B2}, the body diode of the switch S_3, and the separated inductor L_2. The currents i_1 and i_2 are reversed during this stage, and the working process of the converter can be described in Fig. 7(d). The relationship between voltage and current is as follows:

$$\begin{cases} u_{N1} = -k \cdot u_{N2} = -u_{\text{in}} \\ u_{L2} = L_2 \frac{di_{L2}}{dt} = u_{N2} + u_{AB} \\ u_{AB} = u_{\text{out}} + L_f \frac{di_{Lf}}{dt} = u_{L1} \\ i_2 = -i_{L2} = k \cdot i_1 \\ i_{Lf} = i_{L1} + i_2 = C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} \end{cases} . \tag{9}$$

During this process, the converter is in active mode, and energy is transferred to the load side through a HFT.

6) *Stage 6 [t_4~t_{44}]:* The switch T_4 is turned OFF with full voltage and the body diode of the switch T_2 forward bias conduction at time t_4. The flow direction of the secondary side current does not change. The working process of the converter can be described in Fig. 7(e).

7) *Stage 7 [t_{44}~t_5]:* The switch T_2 is turned ON with ZVS at time t_{44} owing to its body diode forward bias conduction at time t_4. The working process of the converter can also be described in Fig. 7(e). The relationship between voltage and current is as follows.

$$\begin{cases} u_{N1} = k \cdot u_{N2} = 0 \\ u_{L2} = L_2 \frac{di_{L2}}{dt} = L_1 \frac{di_{L1}}{dt} \\ u_{AB} = u_{\text{out}} + L_f \frac{di_{Lf}}{dt} = u_{L1} \\ i_2 = k \cdot i_1 = i_{L2} \\ i_{L1} = i_2 + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} \end{cases} . \tag{10}$$

The converter is in passive mode during this stage.

8) *Stage 8 [t_5~t_6]:* During this stage, the switches S_2, S_3 are turned ON with ZVS and the switches S_1, S_4 are turned OFF with ZVS because of the secondary side voltage u_{N2} is 0. In this process, the primary side current i_1 flow circuit of the converter is the same as in *stage 7*. The body diode of switch S_2 conducts forward bias, and branch current i_m is generated during this process. The working process of the converter can be described in Fig. 7(f). The converter is still in freewheeling mode during this time interval. The relationship between voltage and current is as follows:

$$\begin{cases} u_{N1} = k \cdot u_{N2} = 0 \\ u_{L2} = L_2 \frac{di_{L2}}{dt} = L_1 \frac{di_{L1}}{dt} \\ u_{AB} = u_{\text{out}} + L_f \frac{di_{Lf}}{dt} = u_{L1} \\ i_2 = k \cdot i_1 = i_{L2} + i_m \\ i_{L2} = i_{L1} + C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} \end{cases} . \tag{11}$$

9) *Stage 9 [t_6~t_{66}]:* The switch T_1 is turned OFF with full voltage at time t_6, and the body diode of the switch T_3 forward bias conduction. The converter begins to establish a forward level ($+u_{\text{in}}$) and enters active mode in this stage. The working process shown in Fig. 7(g).

10) *Stage 10 [t_{66}~t_7]:* The switch T_3 is turned ON with ZVS at time t_{66} owing to its body diode has been turned ON at time t_6. During this time interval, the converter is in active mode, and the primary side current i_1 flows through the switch T_3, the body diodes of the switches Q_3 and Q_2, and the switch T_2. The secondary side current i_2 flows through the separated inductor L_1, the filter inductor L_f, the switch S_{B2}, the body diode of the switch S_4. The working process shown in Fig. 7(h), and the relationship between voltage and current is as follows:

$$\begin{cases} u_{N1} = k \cdot u_{N2} = u_{\text{in}} \\ u_{L1} = u_{N2} - u_{L2} = L_1 \frac{di_{L1}}{dt} \\ u_{AB} = u_{\text{out}} + L_f \frac{di_{Lf}}{dt} = u_{L2} \\ i_2 = k \cdot i_1 = i_{L1} \\ i_{L1} + i_{L2} = C_f \frac{du_{\text{out}}}{dt} + i_{\text{out}} \end{cases} . \tag{12}$$

After time t_7, the converter will work in the next cycle.

Based on the above analysis and the volt-second balance principle, the expression of the output voltage gain of the converter can be derived as follows:

$$\begin{cases} u_{\text{out}} = \frac{D}{2} u_{N2} = \frac{D}{2} \cdot \frac{1}{k} u_{\text{in}} \\ \theta = D \cdot 180^\circ, D \in [-1, 1] \end{cases} \tag{13}$$

where D represents the duty cycle of the converter, and k represents the transformation ration of the HFT, and the phase shift angle θ. Additionally, the all switches of the input side converter can only achieve ZVS when there is a dead time on the input side, but the output side converter can achieve ZVS within the full input voltage range.

IV. Design Considerations for Key Components of the Proposed Converter

A. Design of High Frequency Transformer

As we all know, when the primary side current i_1 of HFT changes the flow direction, the current value will decrease. Therefore, the secondary side of HFT is easy to lose the voltage square wave, resulting in the reduction of secondary side voltage. In order to solve this trouble, it is necessary to pay attention to the loss of duty cycle at the secondary side in the design of HFT. Assume that the maximum duty cycle of the secondary side of HFT in the converter is 0.95, i.e., $D_{\text{sec(max)}} = 0.95$. According to (27) in [31], the minimum value of secondary side voltage of HFT can be calculated as follows:

$$u_{\text{sec(min)}} \geq \frac{u_{\text{out(max)}} + 2u_D}{D_{\text{sec(max)}}/2}. \tag{14}$$

In the above formula (14), $u_{\text{sec(min)}}$ represents the minimum voltage at the secondary side, $u_{\text{out(max)}}$ represents the maximum output voltage, which is set as 80 V, and u_D is the on state voltage drop, which is 0.7 V. Therefore, the minimum voltage at the secondary side can be calculated as 171.37 V through formula (14). The transformation ratio of HFT is calculated by formula (15), which is 1.28

$$k = \frac{u_{\text{in}}}{u_{N2(\text{min})}}. \tag{15}$$

The calculation formula for the number of turns of primary winding of high frequency transformer is as follows:

$$N_1 = \frac{u_{\text{in}}}{K_f f_S B_W A_e}. \tag{16}$$

In (16), K_f is the waveform scale coefficient $K_f = 4.0$, f_S is the working frequency of HFT $f_S = 10$ kHz, B_W is the magnetic flux density $B_W = 0.37$ T, and the value of effective cross-sectional area A_e is 3 cm^2. Therefore, the primary winding of HFT is calculated as $N_1 = 49.55$ turns by (16), and the secondary winding N_2 of HFT is 38.71. Finally, the turns of the primary and secondary windings of the HFT are 50 turns.

B. Design of Absorption Capacitors

In order to absorb the energy stored by the stray inductors in the line, the two absorption capacitors (C_1, C_2) at the input converter side are designed as follows:

$$\begin{cases} C_1 \geq \frac{i_{S.0}^2 L_1^2}{u_{S.\max}^2 (L_X + L_{C1})} \\ C_2 \geq \frac{i_{S.0}^2 L_1^2}{u_{S.\max}^2 (L_X + L_{C2})} \end{cases}. \tag{17}$$

In the above formula, $U_{S.\max}$ is the maximum voltage stress borne by the switches, L_X is the equivalent inductance of stray inductors, L_{C1} and L_{C2} are the parasitic inductance of absorption capacitors C_1 and C_2 respectively, and $i_{S.0}$ is the initial current value when the switch is turned OFF. Since the parasitic inductance of the capacitor is much smaller than the stray inductors, because of ignoring the parasitic inductance of the capacitor, the corresponding value is brought in, and the calculated capacitance value is 19.26 uF. Finally, the capacitance of the two absorption capacitors (C_1, C_2) is determined to be $C_1 = C_2 = 20\mu$F. In addition, in order to increase the stability of the voltage at the input side of the converter, an input capacitor C_{in} is added, and its capacitance value is also taken as $C_{\text{in}} = 20\mu$F.

C. Design of Separated Inductors

The application of two separate inductors effectively solves the shoot-through problem of output converter, so the output converter does not need to consider the dead time. No matter what operating mode the converter is in, we all want the inductive current on the converter to be in continuous mode. According to the input and output voltage values, the maximum and minimum equivalent duty cycle of the converter can be calculated by the following formula:

$$D_{\max} = \frac{u_{\text{out.max}}}{u_{\text{in.min}}}, \quad D_{\min} = \frac{u_{\text{out.min}}}{u_{\text{in.max}}}. \tag{18}$$

The parameter design of the separated inductor is discussed below. The following relationship exists in a switching cycle T_s:

$$L_{\text{eq}} \frac{\Delta i_L}{(1 - d_{uR}) T_s} = u_{\text{out}} \tag{19}$$

$$u_{\text{in}} i_{\text{in}} \eta = u_{\text{out}} i_{\text{out}}, \ \eta i_{Lf} = i_{\text{out}} \tag{20}$$

$$i_{\text{in}} = (d_{uR} - d_{uL}) i_{Lf} \tag{21}$$

$$L = \frac{u_{\text{out.max}} (1 - d_{uR.\max}) \eta_{\min}}{2 \times k_i \times T_c \times i_{\text{out.min}}}. \tag{22}$$

In the above formula (22), k_i is the maximum ripple coefficient of current, and the value is 20%, T_c is the carrier frequency, and the value is 10 kHz. η is the efficiency of the converter, we choose the lowest estimated efficiency value as 80% based on the actual engineering situation. Take the value into (22) and calculate the separated inductor as $L_1 = L_2 = L/2 = 0.182$ mH.

D. Design of Output Filter Inductors and Capacitors

Without considering the component loss, the converter follows the law of conservation of energy in each working cycle. Using the law of conservation of energy, the maximum current of the filter inductor can be calculated

$$I_{Lf.\min} = d_{uR} u_{\text{in}} \left[\frac{1}{Z} - \frac{(1 - d_{uR})}{2L_f} T_s \right] \tag{23}$$

$$I_{Lf.\max} = d_{uR}u_{\text{in}}\left[\frac{1}{Z} + \frac{(1-d_{uR})}{2L_f}T_s\right]. \tag{24}$$

In order to ensure that the current of the converter can maintain continuity under all operating modes, it is necessary to ensure that the current of the filter inductor remains in the freewheeling state when the output current $i_{\text{out.min}}$ is minimum. The calculation formula of the filter inductor is shown in the following formula:

$$L_f = \frac{u_{\text{out.max}}\left[1-(d_{uR}-d_{uL})\right]\eta_{\min}}{2\times k_i \times T_c \times i_{\text{out.min}}}. \tag{25}$$

Based on the requirements of engineering specifications, the maximum voltage ripple value is selected as 10%, so the output filter capacitor can be designed according to

$$C_f = \frac{i_{\text{out.max}}\left(\frac{d_{uR}-d_{uL}}{2}\right)_{\min}}{k_v \times u_{\text{out.min}} \times T_c}. \tag{26}$$

According to simultaneous (22)–(26), the output filter inductor and output filter capacitor can be calculated as: $L_f = 731.43\ \mu$H and $C_f = 19.88\ \mu$F, respectively.

E. Design of the Dead Time for the Converter

According to the analysis of the working process of the converter, it can also be known that when the dead time of the converter is greater than the charging and discharging time of the junction capacitor in the switches, the switches can realize ZVS turn-ON. Based on this principle and the operation of the proposed converter, we can obtain the following formula:

$$\begin{cases} \Delta i_{CQ1} = C_{Q1}\frac{du_{CQ1}}{dt} = C_{Q1}\frac{\Delta u_{CQ1}}{\Delta t_1} \\ \Delta i_{Lf} = \frac{u_{Lf}\cdot\Delta t_1}{k\cdot L_f} = \frac{u_{\text{in}}\left(1-D/2\right)\cdot\Delta t_1}{k\cdot L_f} \\ 2C_{CQ1}\cdot\frac{\Delta u_{CQ1}}{\Delta t_1} = \frac{u_{\text{in}}\left(1-D/2\right)\cdot\Delta t_1}{k\cdot L_f} \end{cases}. \tag{27}$$

According to formula (27), the charging time of the junction capacitor can be expressed as formula

$$\Delta t_1 = \sqrt{\frac{2kC_{Q1}L_f\cdot\Delta u_{CQ1}}{u_{\text{in}}\left(1-D_{\max}/2\right)}}. \tag{28}$$

In (28), k represents the turn ratio of the HFT, C_{Q1} represents the junction capacitance of the switches, L_f represents the output filtering inductor, Δu_{CQ1} represents the junction capacitor voltage, u_{in} is input ac voltage, and $D_{\max}$ is the maximum duty cycle of the converter.

The switches model number we used is IKW75N60T, and by consulting its datasheet, we can know that the capacitance value of the junction capacitor is 150 nF. By incorporating the relevant parameters into (4), it is calculated that the time for the junction capacitor to complete charging and discharging is 1.653 ms. In addition, considering the influence of stray parameters in the line, to ensure that the input side converter can achieve ZVS, the dead time is set to be greater than 2 ms.

V. Application of the Proposed Converter in Voltage Regulation

Compared with other types of converters, PWM direct ac/ac converter has great advantages in applications where only the voltage amplitude needs to be adjusted. Because the direct ac/ac converter only performs amplitude chopping control on the input ac voltage, the phase of its output voltage always follows the phase of the source side voltage. Therefore, it is unnecessary to use phase locked loop when direct ac/ac converter is applied to power grid voltage regulation. Moreover, with the development of advanced semiconductor devices, it is possible to apply PWM direct ac/ac converter to the power grid voltage regulation of higher voltage level (distribution network voltage level). As shown in Fig. 8(a) and (b), the system wiring diagram and equivalent circuit diagram (taking 0.4 kV low-voltage single-phase system as an example) when the converter proposed in this article is applied to grid voltage regulation are shown respectively.

The high-frequency isolated direct ac/ac converter proposed in this article only controls the amplitude of the input voltage, its output voltage can always maintain the same phase or 180° phase difference with the source voltage. Therefore, it can be equivalent to a controllable ac voltage source connected in series with the source side, so as to realize the dynamic control of the load side voltage. It can be seen from Fig. 8 that when the converter proposed in this article is used for voltage regulation, the connection mode of front parallel and rear series is adopted, and its principle can be shown in Fig. 8(b). According to Fig. 8, the relationship among the grid voltage u_S, the load side voltage u_{load} and the controllable voltage u_{com} generated by the converter can be listed as follows:

$$u_{\text{load}} = u_S + u_{\text{com}}. \tag{29}$$

Since the phase of the output voltage of the converter and the grid voltage are either in the same phase or 180° different from each other, the relationship between the three can be expressed as (29). In combination with (13), (29) can be expressed as follows:

$$u_{\text{load}} = u_S + \frac{D}{2}\cdot\frac{N_2}{N_1}\cdot u_S. \tag{30}$$

It can be seen from (30) that the load side voltage u_{load} can be controlled by changing the duty cycle D and the transformation ratio k of the HFT. Fig. 6 shows the radar diagram of theoretical compensation degree for load side voltage under three different types of high frequency isolation transformers. This article is only a theoretical exposition and explanation when analyzing the theoretical compensation degree, and the transformation ratio k of the three types of transformers is set without considering the specific actual working conditions. In Fig. 9 , the transformation ratios of step-down high-frequency isolation transformer, step-up high-frequency isolation transformer and isolation transformer are $k = 0.25$, $k = 4$, and $k = 1$, respectively. The corresponding maximum theoretical compensation degrees of the three types of HFTs are 11.11%, 66.67%, and 50%, respectively. Therefore, on the basis of fully considering the actual working conditions, system capacity and voltage compensation range of the transformer, the HFT can be optimized to achieve the purpose of optimal cost and voltage regulation. However, this article only

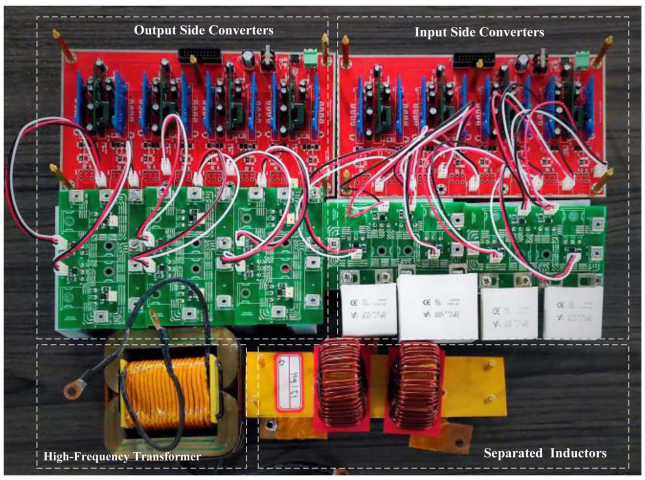

Fig. 10. Photograph of the prototype.

TABLE II
EXPERIMENTAL PARAMETERS

Number	Parameter category	Parameter value
1	Input voltage (u_{in})	180–220 Vrms/50 Hz
2	Duty cycle range	(0,1)
3	Input capacitor (C_{in})	20 μF
4	Absorption capacitor (C_1 , C_2)	20 μF
5	Leakage inductance of HFT	3 μH
6	Excitation inductance of HFT	2 mH
7	Separated inductor (L_1 , L_2)	200 μH
8	Output filter inductor (L_f)	800 μH
9	Output filter capacitor (C_f)	20 μF
10	Loads	R_{load} = 10 Ω/ Z_{load} = 6+j9.58 Ω
11	Winding turns of HFT	N_1 = 50, N_2 = 50
12	Rated power and working voltage	1.5 kW 220 Vrms
13	Power density	4.079 W/cm^3
14	Switching frequency	10 kHz

analyzes the feasibility of applying the frequency isolated direct ac/ac converter to voltage regulation.

VI. ANALYSIS OF EXPERIMENTAL RESULTS

A. Experimental Results of the Proposed Converter

An experimental prototype (as shown in Fig. 10) of the proposed HFT-isolated direct ac/ac converter is built to sufficiently demonstrate previous analysis. The parameters of experimental prototype shall be taken according to the above design, and relevant parameters are given in Table II. In addition, an field programmable gate array is applied to generate the gating signals show in Fig. 3.

Fig. 11 shows the gate signal waveforms of some key switches of the converter proposed in this article. It can be seen from Fig. 11(a) that there is a phase shifted angle of θ between the leading-leg arm and the lagging-leg of the input side converter.

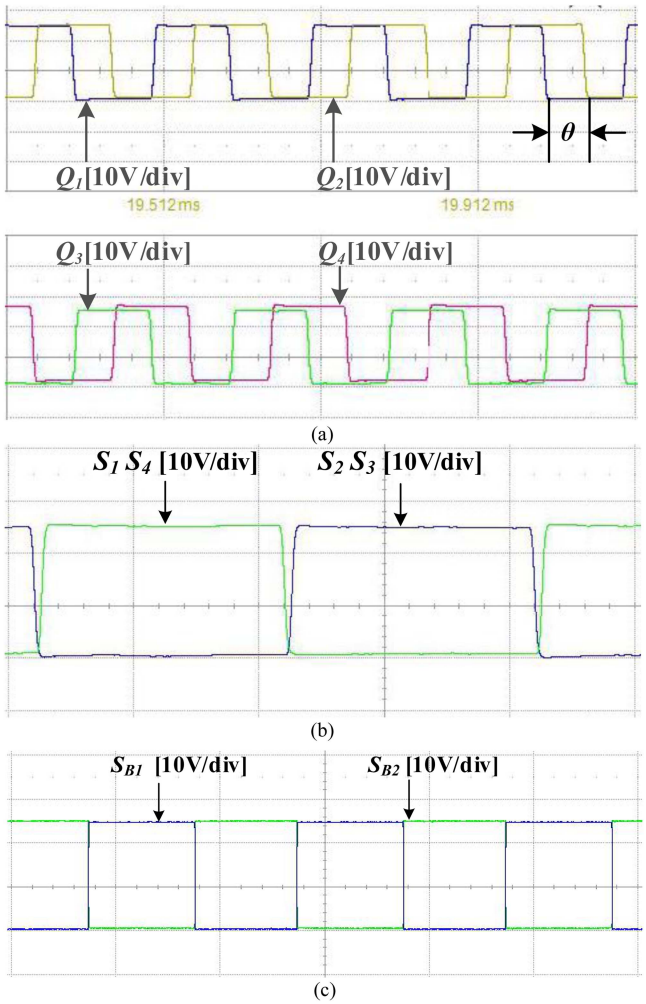

Fig. 11. Experimental gate signals waveforms of key switches. (a) Gate signals of switches Q_1~Q_4. (b) Gate signals of switches S_1~S_4. (c) Gate signals of switches S_{B1}~S_{B2}.

Therefore, the phase-shifted modulation strategy is adopted in this article. Fig. 11(b) and (c) show the gate signal waveforms of the output side converter, which are consistent with the principle shown in Fig. 3. It should be noted that when the opposite signals are given to the switches S_{B1} and S_{B2}, the converter proposed in this article will produce the output voltage U_{out} with a phase difference of 180° from the input voltage. Therefore, the proposed converter has the ability of output voltage bipolar gain.

Fig. 12 shows the experimental results under the working conditions of converter duty cycle of $D = 0.75$, input voltage of $U_{\text{in}} = 212$ Vrms, resistive load $Z = 13.11\ \Omega$ (where $R = 10\ \Omega$, $X_L = 7.85\ \Omega$). Fig. 12 shows the waveforms of the primary and secondary side voltage (u_{N1} and u_{N2}), primary side current i_1 and output voltage u_{out} of the HFT of the converter under the above working conditions. It can be seen from the partially amplified waveforms in Fig. 12 that the primary and secondary side voltage of the HFT are a bipolar three state high frequency voltage ($+U_{\text{in}}$, 0, $-U_{\text{in}}$), and the secondary side current i_1 waveform is consistent with the theoretical analysis waveform shown in Fig. 4, and the output voltage u_{out} is a 50 Hz sinusoidal

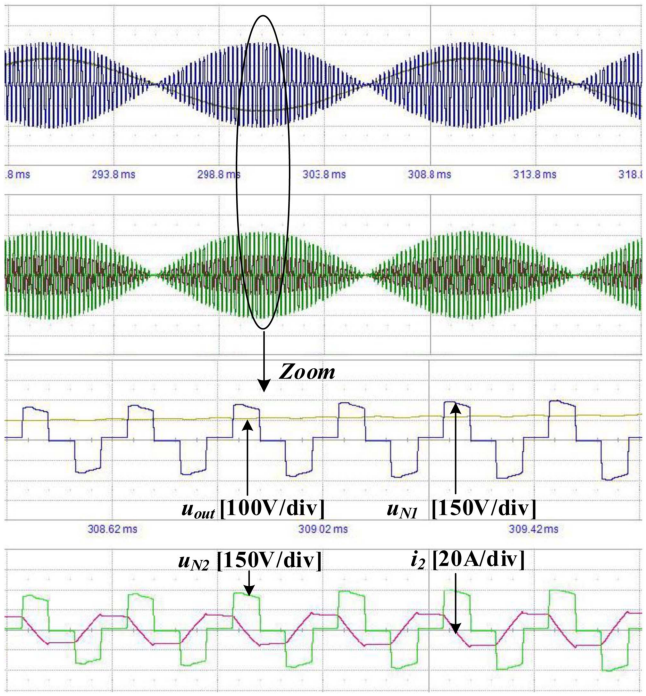

Fig. 12. Experimental waveforms of primary and secondary side voltage (u_{N1} and u_{N2}), primary side current (i_1) of HFT, and output voltage (u_{out}) of the converter.

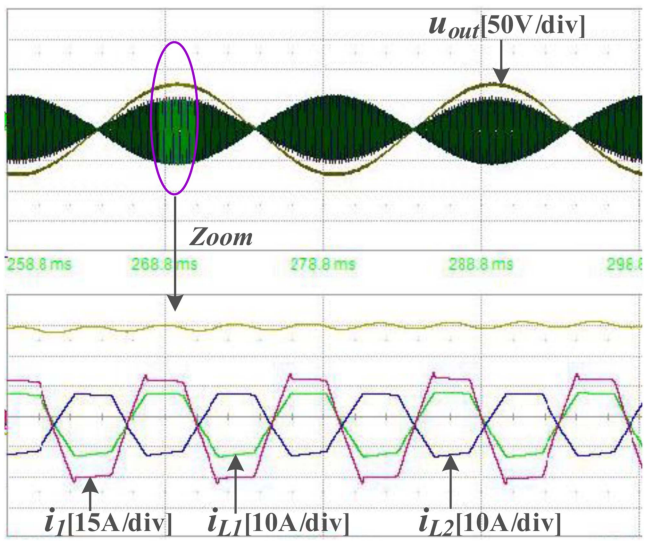

Fig. 13. Experimental waveforms for separated inductor currents (i_{L1},i_{L2}), primary side current (i_1) of HFT and output voltage (u_{out}) of the converter.

ac voltage. According to the analysis of the experimental results in Fig. 12, the experimental results are completely consistent with the above theoretical analysis.

Fig. 13 shows the experimental results of the converter under the operating conditions of input voltage $U_{\text{in}} = 200$ Vrms, the duty cycle $D = 0.6$ and pure resistive load $R = 10$. It can be seen from Fig. 13 that the current waveform of the two separated inductors is also consistent with the theoretical waveform in Fig. 3.

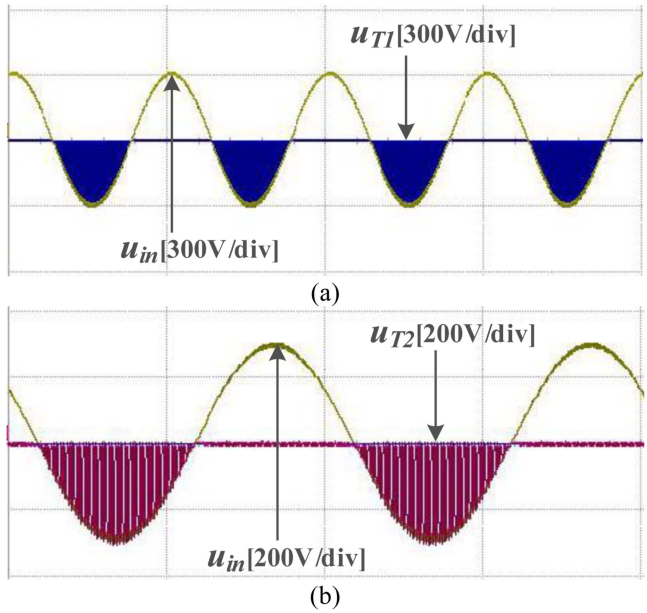

Fig. 14. Waveform diagram of voltage stress borne by switches. (a) Switch T_1 of leading-leg. (b) Switch T_2 of lagging-leg.

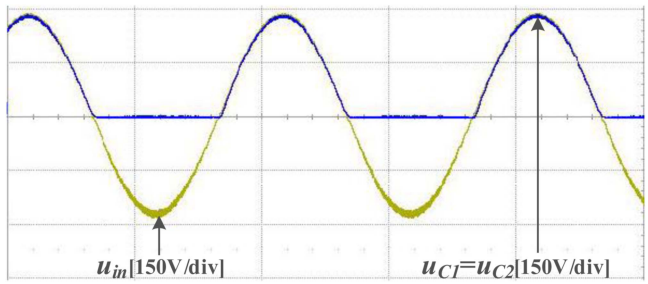

Fig. 15. Experimental waveforms of two absorption capacitors under the working condition of 300 V maximum input voltage.

Fig. 14 shows the voltage stress waveform of the switches in the converter. In order to avoid repetition, the switch T_1 of the leading-leg and the switch T_2 of the lagging-leg are only selected for display. It can be seen from the experimental results that the maximum voltage stress borne by the switch is the peak value of the input voltage, and each switch only bears the half wave voltage stress of the input voltage.

Fig. 15 shows the voltage waveform of the two absorption capacitors when the input voltage is 300 V maximum. It can be seen from the experimental results that the maximum voltage stress borne by the two absorption capacitors is the peak voltage of the input voltage and only a half wave voltage.

Fig. 16(a) and (b) shows the experimental results of the converter under different working conditions. The experimental result shown in Fig. 16(a) is obtained when the input voltage is 200 Vrms, the duty cycle is $D = 0.6$, and the pure resistive load is $R = 10\ \Omega$.

It can be seen from the experimental results that the output voltage waveform of the converter is of good quality and can operate normally under pure resistive load conditions. In addition,

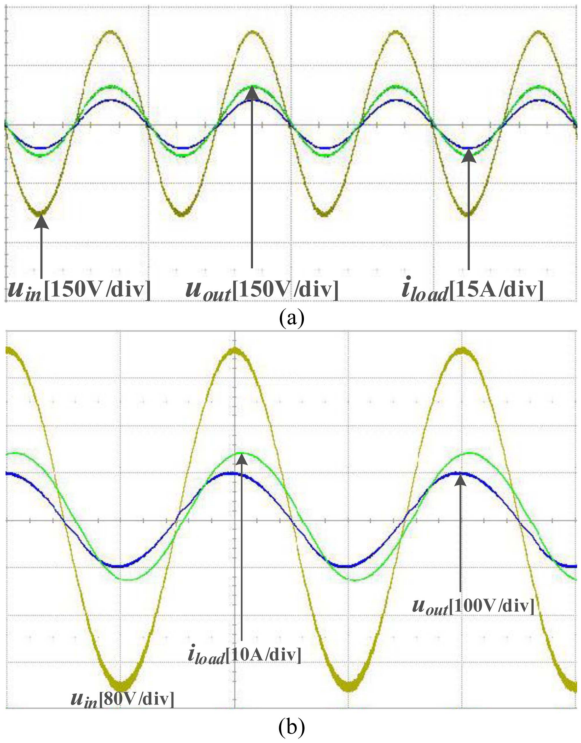

Fig. 16. Experimental results under different types of loads. (a) $R = 10\ \Omega$. (b) $R = 6\ \Omega$, $X_L = 9.58\ \Omega$.

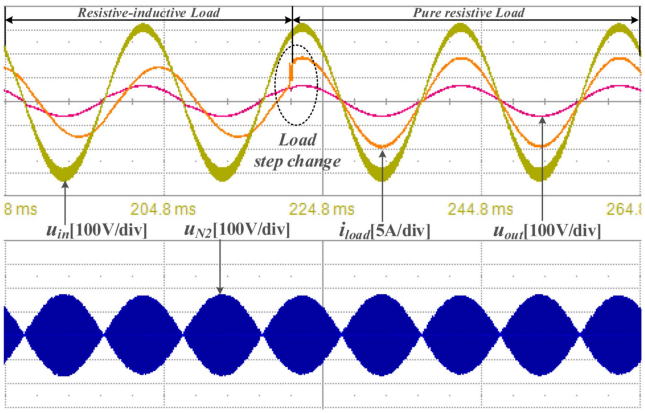

Fig. 17. Experimental results of the proposed converter under load step change conditions.

the experimental results in Fig. 16(b) show that the converter can work normally when the resistive inductive load is connected.

Fig. 17 shows that the experimental results of the proposed converter under load step change conditions. From Fig. 17, it can be seen that when the load step changes from resistive-inductive load to pure resistive load, the converter can still operate normally, and there is no overvoltage in the output voltage, input voltage, and secondary side voltage of the HFT.

Figs. 18 and 19 show the experimental results of the input side converter and output side converter achieving ZVS, respectively.

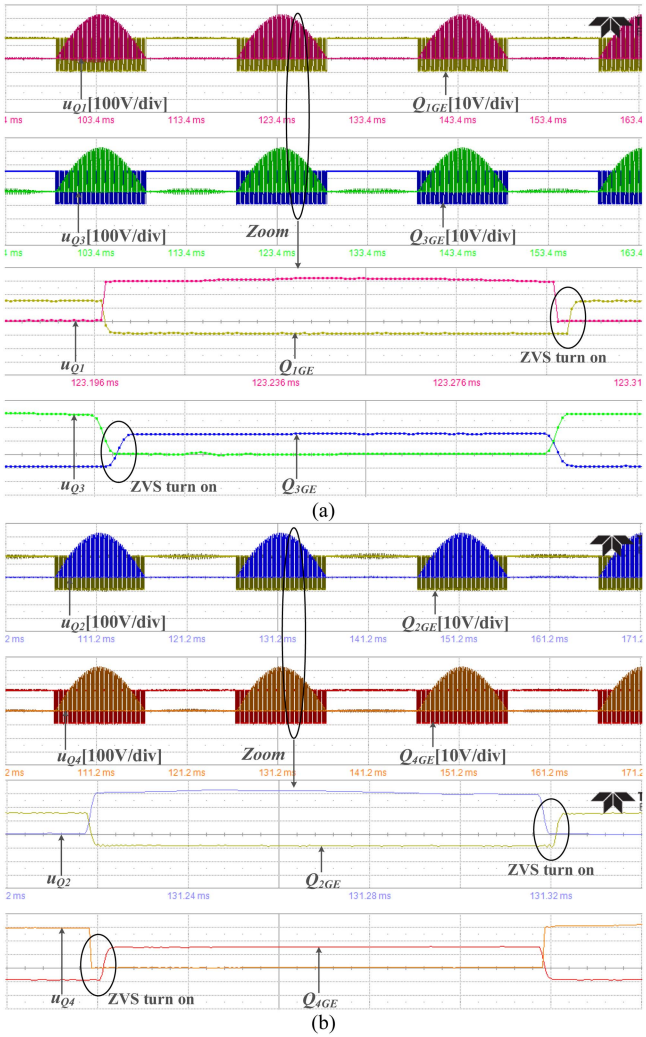

Fig. 18. ZVS experimental waveforms of the input side converter under the pure resistive load. (a) Switches Q_1, Q_3 of the left bridge. (b) Switches Q_2, Q_4 of the right bridge.

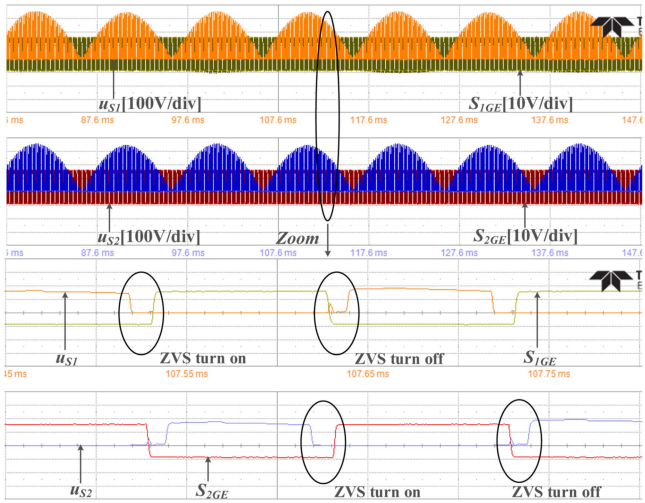

Fig. 19. ZVS experimental waveforms of the output side converter under resistive-inductive loads.

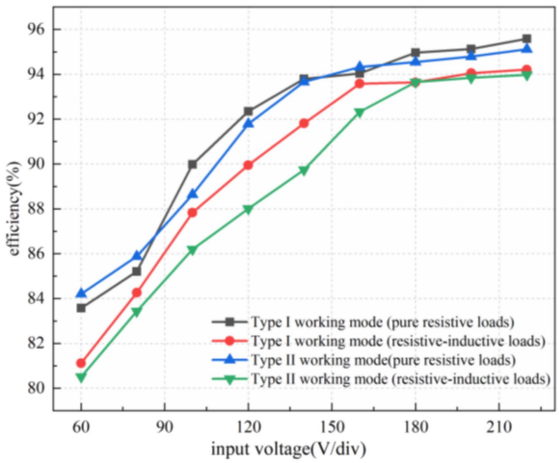

Fig. 20. Efficiency of the proposed converter under different conditions.

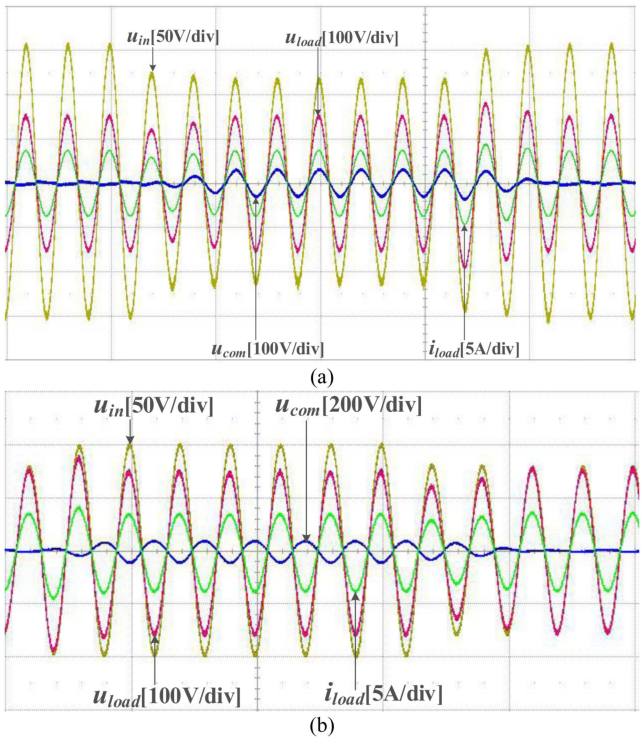

Fig. 21. Experimental waveforms of the proposed converter applied to voltage regulation. (a) Voltage sags at source side. (b) Voltage swells at source side.

It can be seen from Fig. 18 that when the input side converter has a dead time, the switches of the input side converter can achieve ZVS.

It can be seen from Fig. 19 that the output side converter switches can achieve full range ZVS. The actual measurement efficiency curve of the proposed converter under different operating conditions is shown in Fig. 20. From Fig. 20, it can be seen that regardless of whether the converter operates in type I working mode or type II working mode, the efficiency of the converter under pure resistive load conditions is higher than that under resistive-inductive load conditions.

B. Experimental Results of the Proposed Convert ER Applied to Voltage Regulation

To verify the feasibility of the proposed converter in voltage regulation, Fig. 21 shows the experimental waveform when the grid voltage sag or swell. It can be seen from Fig. 21 that when the source side voltage u_S sag or swell, the converter proposed in this article will respond in time and output the corresponding compensation voltage $u_{\rm com}$ to ensure the stability of the load side voltage $u_{\rm load}$. The relationship among voltage u_S, $u_{\rm com}$, and $u_{\rm load}$ follows (28).

VII. Conclusion

This article presented a novel bidirectional high-frequency isolated direct ac/ac converter with unipolar phase-shifted modulation strategy based on double dc modulation indexes. The main idea of topological construction is that the nonisolated two-level nondifferential bipolar direct ac/ac converter is combined to the bidirectional PSHB, which inherits the advantages of no commutation problem, ZVS, simple control, bipolar output voltage gains, etc. The proposed converter can eliminate the need of bulky LFT in the application in power grid voltage regulation thanks to it provides the electrical isolation and safety with the HFT. The circuit steady operation analysis and design considerations of the proposed converter are explained, and then, the application of the proposed converter in voltage regulation is analyzed. A laboratory prototype is also built and experimental results are given to validate its advantages.

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