New Step-Up DC/DC Converter With Ripple-Free Input Current

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***Abstract*—This article introduces a new single-switch high-voltage-gain dc/dc converter with soft-switching performance for renewable energy applications. By using an auxiliary circuit, zero input current ripple is achieved that significantly reduces the size of the input inductor compared with the conventional converter. Therefore, the inductor equivalent series resistance (ESR) will be significantly lower for improving power efficiency. In this converter, a coupled inductor (CI) along with a voltage multiplier circuit are used to achieve high voltage gains. While achieving high voltage gains, the maximum voltage stress across the single power switch is mitigated by means of a simple regenerative clamp circuit. A resonant tank that absorbs the leakage inductance of the CI is adopted to achieve soft switching and alleviate reverse-recovery issues of the converter diodes. In this article, the operating principle of the suggested topology and analysis for voltage gain, voltage stress, and efficiency have been presented. A comparison against the latest counterparts is thoroughly discussed. Finally, the theoretical analysis is validated by a 300-W (25 V/400 V) sample prototype.**

***Index Terms*—Coupled-inductor, soft-switching, step-up dc-dc converter.**

I. Introduction

In order to protect the environment, renewable energy sources (RESs), such as photovoltaic panels, fuel cells (FCs), and wind turbines, have become a proper alternative to respond to the required energy of the electrical utilities and local loads. However, the output voltage of such sources is typically low (<50 V) and it cannot be used directly [1]. Therefore, a step-up dc/dc converter with a wide voltage-gain range should be applied to increase the output voltage level. Moreover, to satisfy the optimum power transfer of RES, a continuous and ripple-free input current is required [1], [2]. In addition, high step-up dc–dc converters have various applications, such as renewable energy resources, lighting systems, energy harvesting, medical devices, uninterruptible power supply, portable devices, and data center. For low-power applications, nonisolated structures are preferred that have been widely explored in the literature [3].

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So far, many nonisolated step-up converters have been introduced to raise the low-voltage level of RES. To increase the voltage gain, some effective methods, such as switched inductors/capacitors, and voltage multipliers (VMs) are often applied. Nonetheless, such topologies suffer from large component count and hard-switching performance, which decrease their efficiency and power density [4].

In recent years, magnetically devices, including coupled inductors (CIs) or transformers, along with the typical voltage boosting methods are widely considered to improve the performance of step-up topologies [4]. In this state, the circuit voltage conversion ratio can be further increased without needing an extreme duty cycle. However, to limit the voltage stress across the power switch, active or passive regenerative clamp circuits are often used [5].

Recently, many types of modified CI-based step-up dc–dc converters with high voltage gain and low input current have been introduced in recent years. For example, a new two-winding CI-based step-up dc–dc converter is introduced in [6]. Also, in [6], [7], and [8], new high-voltage-gain dc–dc converters with low input current ripple are proposed. Using three-winding coupled, high voltage gains can be obtained in these circuits. Also, in the series connection between an inductor in series with the input dc source, continuous input current with low ripple is achieved in the mentioned topologies. However, a high input inductance is needed to suppress the input current ripple, which leads to an increase in wire consumption and ohmic losses.

To solve this problem, in some converters, cancelation of the input current ripple has been done with the help of a CI along with a capacitor at the input stage of the converter. In this method, a special relationship between the leakage and magnetizing inductances and the turns ratio of the CI should be considered, which usually leads to significant leakage of the inductor. In [9], [10], [11], and [12], several different ripple-free input structures of step-up dc–dc converters are presented. However, the voltage gain of these converters is severely limited. In [13], [14], [15], [16], [17], and [18], to achieve a higher voltage gain, an additional CI has been used in the circuit. Nevertheless, in the mentioned converters, high voltage gain was obtained with the help of several active switches and a large number of component counts. Moreover, a new zero input current step-up dc–dc converter is suggested in [14]. However, in this topology, two CIs are used to cancel the input current ripple. Also, using four active switches is another disadvantage of this topology. Moreover, a new high-voltage-gain dc–dc converter based on CI is proposed in [19]. In this topology, using a CI and

capacitor in the front stage of the circuit, high voltage gain in quadratic form is created. However, hard-switching performance for power switch and high reverse-recovery issues for diodes are considered as its disadvantages. In [20], a new ripple-canceling circuit to eliminate the pulsating input current of the conventional flyback converter is proposed. Nevertheless, low voltage gain is the main demerit of this circuit. In addition, in [21] and [22], two new types of nonisolated ripple-free input current ripple step-up dc–dc converters with soft-switching performance are presented.

Using an inductor instead of CI is another simple method to suppress the input current ripple. In [23] and [24], two new designs of boost converter are proposed, in which a new auxiliary circuit is used to achieve zero input current ripple. However, low voltage gain is a disadvantage in this circuit. Moreover, a new wide voltage-gain range dc–dc converter with zero input current ripple and low-voltage stresses is presented in [25] for fuel cell vehicles. Nevertheless, using three magnetic components along with two power switches are considered a demerit of this topology. In [26], an extendable soft-switched high step-up converter with near zero-ripple input current using a three-winding CI is suggested. In this circuit, soft-switching performance zero voltage switching (ZVS) is created using an auxiliary switch. In [27], a family of impedance source dc–dc converters with zero input current ripple is proposed. However, this topology needs three magnetic devices (two inductors and four-winding CI) to achieve high voltage gains. In addition, a new structure of zero input current ripple for high step-up nonisolated dc–dc converters is provided in [28]. Despite soft-switching performance, in this circuit, high voltage gains are achieved using a large number of passive components.

Keeping in mind the merits and demerits of the discussed high step-up converters, this article proposes a new type of zero input current ripple high-voltage-gain dc–dc converter using a CI. The novelties of the introduced topology are as follows:

1) high voltage gain;
2) low component count;
3) zero input current ripple;
4) low-voltage stress across the main power switch;
5) soft-switching performance;
6) mitigation of reverse-recovery issues for all diodes;
7) quasi-resonant performance to reduce the power loss.

The rest of this article is organized as follows. Operational principles and mathematical derivations of the proposed circuit are given in Sections II and III. In Section IV, the performance of the proposed circuit is compared with some similar counterparts. Sections V and VI provide the parameters design considerations and experimental results. Finally, Section VII concludes this article.

II. Operational Principles of the Proposed Converter

A. Topology of the Proposed Converter

The general structure of the proposed topology is shown in Fig. 1. In this circuit, one power switch (S_w), along with one two-winding CI, are used. The diode D_c with the capacitor C_c forms the passive clamp circuit, which restricts the maximum

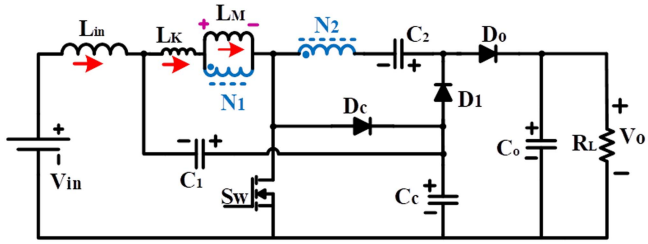


Fig. 1. Circuit configuration of the proposed converter.

voltage stress across the single power switch. Moreover, the capacitor C_2 and the secondary side of the CI (N_2) act as a VM to improve the voltage-gain ratio. Diode D_o and C_o indicate the output diode and capacitor of the circuit, respectively. In the proposed converter, an input inductor (L_{in}) and the capacitor C_1 are used to remove the ripple of the input current, which is very friendly to FC. It should be noted that the size of the input inductor (L_{in}) in the proposed topology is much smaller than the inductors required in the typical current-fed step-up dc–dc converters with low input current ripple. In addition, by designing a resonant tank among the secondary side of the CI along with the middle capacitors C_2 and C_c, the current waveforms of D_1 and S_w are changed to a sinusoidal form, which alleviates the power dissipations of these switching components. Moreover, in this suggested circuit, the reflected leakage inductance of the CI on the secondary side helps to eliminate the reverse-recovery issue for all diodes. For better performance of the resonance tank and input current ripple cancelation process, in this converter, the capacitor (C_1) is also linked to the middle capacitors of the circuit to participate in the resonance frequency adjustment process. In this case, more degrees of freedom are created to adjust the resonance frequency and input current ripple.

B. Operating Principles

To simplify the analysis of the proposed converter, the power switch and all diodes of the converter are supposed ideal. Also, the voltages across the capacitors are considered to be constant values. Moreover, the CI of the converter is considered an ideal transformer with a turns ratio $n = N_2/N_1$, along with a magnetizing (L_M) and a merged leakage (L_k) inductances on the primary side. Fig. 2 depicts the main theoretical key waveforms in five states of the proposed topology in a working cycle. The equivalent circuits of each switching mode in continuous conduction mode (CCM) are displayed in Fig. 3.

Mode-1 [t_0 - t_1]: Before $t = t_0$, the currents of the primary and secondary sides of the CI are equal; thus, the single power switch begins to conduct under zero current switching (ZCS) conditions at $t = t_0$. Regarding Fig. 3(a), the output diode D_o is also conducting, while other diodes are OFF. During this transient mode, the capacitor C_1 and the magnetic inductance of the CI (L_m) are discharging. Due to the effect of the reflected leakage inductance on the secondary side of the CI, the current of D_o reaches zero without a low reverse-recovery (LRR) problem at the end of this operating mode. Therefore, the switching noises of the output dc voltage are considerably alleviated.

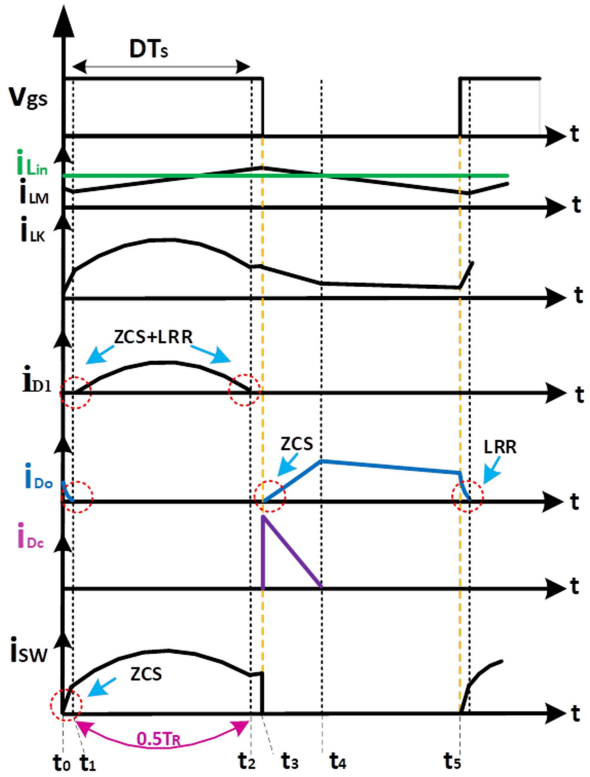


Fig. 2. Steady-state theoretical key waveforms of the proposed converter in CCM operation.

Mode-2 [t_1 - t_2]: In the second interval, the power switch (S_w) remains ON, and at $t = t_1$, the diode D_1 starts to conduct with a gentle slope. Same as Mode-1, the capacitor C_1 is charged by the input dc source. The energy stored in the clamp capacitor C_c is delivered to the middle capacitor C_2. Besides, during this operating mode, magnetizing inductance gets charged due to the positive induced voltage. During this state, to decrease the switch turn-OFF power loss, a resonant tank is considered. Regarding Fig. 3(b), the capacitors C_1, C_2, and C_c along with the CI are in resonance; thus, the waveforms of the currents i_{LK}, i_{Sw}, and i_{D1} are changed into quasi-sinusoidal form. According to the circuit configuration, the resonant frequency (f_R) of this resonant tank is obtained as follows:

$$f_R = \frac{1}{T_R} = \frac{1}{2\pi\sqrt{L_k\left(C_1 \| n^2 C_2 \| \left(\frac{n}{1+n}\right)^2 C_c\right)}}. \quad (1)$$

Regarding Fig. 4, to reduce the maximum current stress for the power switch and the diode D_1 during the resonant time, adjusting the resonant frequency at the critical mode ($T_R/2 \approx DT_S$) is recommended.

During this state, the circuit expression can be expressed as follows:

$$v_{Lin} = V_{in} + v_{C1} - v_{Cc} \quad (2)$$

$$v_{LM} = v_{Cc} - v_{C1} \quad (3)$$

$$v_{C2} = v_{Cc} + n \cdot v_{LM}. \quad (4)$$

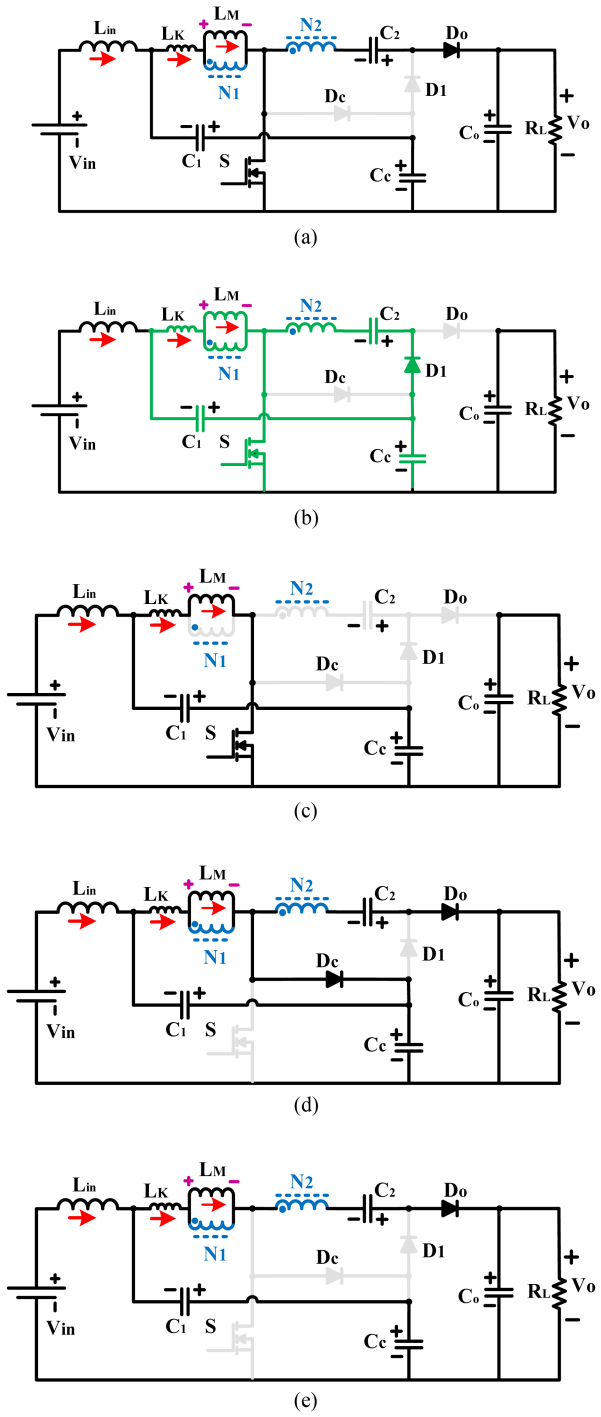


Fig. 3. Equivalent circuits of the proposed converter. (a) Mode-1. (b) Mode-2. (c) Mode-3. (d) Mode-4. (e) Mode-5.

Moreover, the current of the single power switch can be obtained as follows:

$$i_{Sw} = i_{D1} + i_{LK}. \quad (5)$$

This operating mode ends when the current i_{D1} reaches zero with a low slope without a reverse-recovery issue.

Mode-3 [t_2 - t_3]: After turning OFF D_1, the leakage current of the CI (i_{Lk}) is equal to its magnetizing inductance current

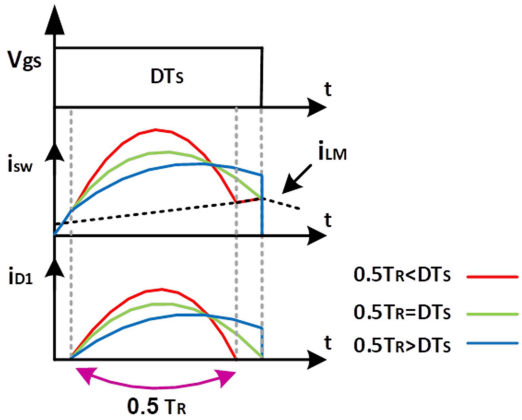


Fig. 4. Current waveforms of the switch and diode $D1$ in resonant modes.

(i_{Lm}). During this short time interval, the capacitors C_1 and C_c are charging and discharging, respectively. During this state, the current passes from the power switch, which is obtained as follows:

$$i_{\mathrm{Sw}} = i_{Lm}. \tag{6}$$

Mode-4 [t_3 - t_4]: In this case, as soon as the power switch at time $t = t_3$ is turned OFF, the diodes D_c and D_o begin to conduct. Therefore, the voltage of the single power switch is clamped [see Fig. 3(d)]. The capacitor C_c begins to get energy from the input and magnetizing inductors. Thus, i_{LM} starts to decrease linearly. During this state, the energies stored in the CI along with the capacitor C_2 are released to the output capacitor. This state ends when the clamp capacitor C_c is completely charged and the current of D_c reaches zero with an LRR problem. The following equations for the voltage are derived in this state:

$$v_{L\mathrm{in}} = V_{\mathrm{in}} + v_{C1} - v_{Cc} \tag{7}$$

$$v_{LM} = -v_{C1} \tag{8}$$

$$v_o = v_{Cc} + v_{C2} - n v_{LM}. \tag{9}$$

Mode-5 [t_4 - t_5]: In this state, the output diode D_o is still ON [see Fig. 3(e)]. Meanwhile, the leakage inductance of the CI charges the output capacitor. Besides, in this time interval, the following equation can be derived:

$$v_o = v_{Cc} + v_{C2} - v_{LM}(1+n). \tag{10}$$

III. Steady-State Analysis

A. Voltage Gain

By applying the KVL law on the magnetic components, including L_{in} and L_m, the average voltage of the capacitors C_c and C_1 can be obtained as follows:

$$V_{Cc} = \frac{V_{\mathrm{in}}}{1-D} \tag{11}$$

$$V_{C1} = \frac{D \cdot V_{\mathrm{in}}}{1-D}. \tag{12}$$

Here, D is the power switch duty cycle. According to operating mode-2 and using (3), (4), (11), and (12), the average voltage upon the capacitor C_3 is determined as follows:

$$V_{C2} = \frac{1+n(1-D)}{1-D} \cdot V_{\mathrm{in}}. \tag{13}$$

Using (8) and (9) and (11)–(13), the overall ideal voltage gain of the proposed circuit in CCM is obtained as follows:

$$M = \frac{V_o}{V_{\mathrm{in}}} = \frac{2+n}{1-D}. \tag{14}$$

Equation (14) shows that the output dc voltage of the proposed converter can be easily regulated in a wide range by setting the parameters D and n. Fig. 5 depicts the voltage gain M of the converter as a function of the duty cycle under several turns ratio of the CI *(n)*.

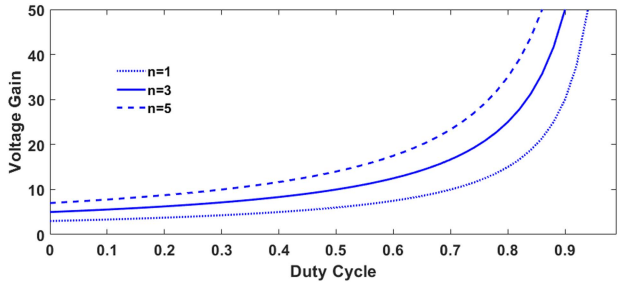


Fig. 5. Voltage gain of the presented converter versus D and n.

B. Zero Input Current Ripple

According to Fig. 3(a)–(e), the voltage upon the input inductor L_{in} is the same for all operation modes, which equals as follows:

$$v_{L\mathrm{in}} = V_{\mathrm{in}} + v_{C1} - v_{Cc}. \tag{15}$$

According to the volt-second balance law, the average voltage of the input inductor L_{in} is forced to be zero value in each switching period. Therefore, the following equation can be expressed as:

$$\int V_{L\mathrm{in}} dt = 0. \tag{16}$$

Thus, the voltage across the input inductor should be equal to zero value

$$v_{L\mathrm{in}} = L_{\mathrm{in}} \frac{di_{\mathrm{in}}}{dt} = V_{\mathrm{in}} + v_{C1} - v_{Cc} = 0. \tag{17}$$

This means the cancelation of the input current ripple. However, as mentioned, in the proposed converter, a resonant tank is considered to improve the efficiency. Thus, in practice, the voltage across the capacitors C_1 and C_c might not be purely dc. In this condition, according to Fig. 6(a), their resultant voltage ripple will be reflected across the input inductor, which introduces a small current ripple.

According to Fig. 6, the input current ripple of the proposed converter can be achieved as follows:

$$\frac{1}{4} T_s \left(\Delta V_{C1} + \Delta V_{Cc}\right) = L_{\mathrm{in}} \Delta I_{\mathrm{in}} \tag{18}$$

$$\Delta I_{\mathrm{in}} = \frac{\left(\Delta V_{C1} + \Delta V_{Cc}\right)}{4 f_s L_{\mathrm{in}}}. \tag{19}$$

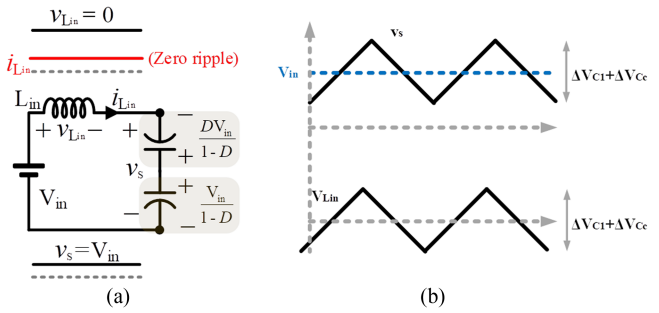


Fig. 6. (a) Equivalent circuit of the proposed converter to remove the input current ripple. (b) Voltage ripple across the input inductor.

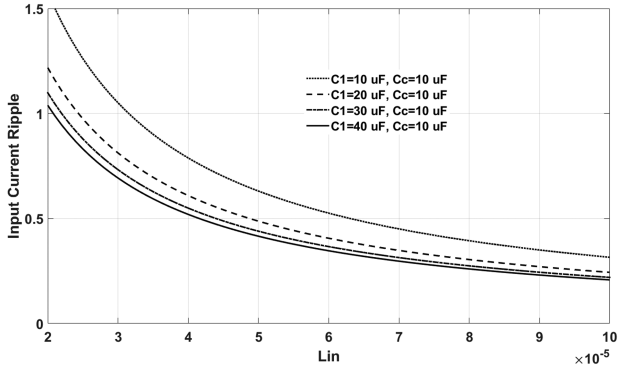


Fig. 7. Input current ripple of the proposed converter versus the input inductance value at some values of the clamp capacitor (C_c).

Regarding (19), the input current ripple is dependent on the voltage ripple of the capacitors C_1 and C_c. Based on the operating mode-2 of the converter [see Fig. 2(b)], the currents of C_c and C_1 are calculated as follows:

$$i_{C1}^{DT}(t) = n\frac{\pi I_o}{D}\sin(\omega_r t) \tag{20}$$

$$i_{Cc}^{DT}(t) = (1+n)\frac{\pi I_o}{D}\sin(\omega_r t). \tag{21}$$

By considering the critical mode operation ($0.5T_R \approx DT_S$), the averaged values of the currents passed through these capacitors are obtained as follows:

$$I_{C1}^{DT} = nI_o \tag{22}$$

$$I_{C2}^{DT} = (1+n)\,I_o. \tag{23}$$

Thus, the voltage ripple of C_1 and C_c can be estimated as follows:

$$\Delta V_{C1} = \frac{I_{C1}^{DT}\cdot D\cdot T_s}{C_1} \tag{24}$$

$$\Delta V_{Cc} = \frac{I_{Cc}^{DT}\cdot D\cdot T_s}{C_c}. \tag{25}$$

Combined (24) and (25) into (19), the input current ripple of the converter yields

$$\Delta\, I_{\text{in}} = \frac{D\left(\frac{n}{C_1}+\frac{1+n}{C_c}\right)}{4f_s^2 L_{\text{in}}}\,\frac{V_o}{R}. \tag{26}$$

By comparing (1) and (26), it is clear that the capacitor C_2 can be used for more precise tuning of the resonance frequency. Fig. 7 shows the input current ripple of the proposed circuit versus the input inductance (per μH) value at several values of the clamp capacitor. This figure is obtained at $V_o = 400$ V, $R = 533\ \Omega$, $n = 5.1$, $D = 0.55$, and $f_s = 60$ kHz. From this figure, increasing the value of C_1 can play an effective role in decreasing the input current ripple in different conditions.

C. Voltage and Current Stresses of the Semiconductors

According to the proposed topology operation, the voltage stress on the power switch (S_w) is derived as follows:

$$V_{\text{Sw(Peak)}} = \frac{V_{\text{in}}}{1-D} = \frac{V_o}{2+n}. \tag{27}$$

Moreover, the voltage stresses across the converter diodes are obtained as follows:

$$V_{\text{Dc(Peak)}} = \frac{V_o}{2+n} \tag{28}$$

$$V_{D1} = V_{Do} = \frac{1+n}{2+n}\,V_o. \tag{29}$$

Based on (27)–(29), voltage stresses across the switching components of the proposed converter are significantly less than the dc voltage of the output.

Regarding Fig. 2, and by considering the sinusoidal form of peak and rms currents passing through the diode D_1, they can be estimated as follows:

$$i_{D1_{\text{peak}}} = \frac{\pi}{2D}\,I_o \tag{30}$$

$$I_{D1(\text{RMS})} = I_o\sqrt{\frac{(\pi)^2}{8D}} \tag{31}$$

where I_o is the output load current. Also, the peak and rms currents of the output D_o can be approximated as follows:

$$i_{Do(\text{peak})} \approx \frac{I_o}{1-D} \tag{32}$$

$$I_{Do(\text{RMS})} = I_o\sqrt{\frac{1}{1-D}}. \tag{33}$$

Based on the operating mode-2 of the suggested topology, the switch current and its rms value are given as follows:

$$i_{\text{Sw}(t)} \approx \left(M + \frac{(1+n)\,\pi}{2D}\sin(\omega_r t)\right) I_o \tag{34}$$

$$I_{\text{Sw(RMS)}} = I_o\sqrt{DM^2 + \frac{DH^2}{2} + \frac{4DHM}{\pi}}. \tag{35}$$

Here, H is defined as follows:

$$H = \frac{(1+n)\,\pi}{2D}. \tag{36}$$

According to operating mode-3 of the converter, the current magnitude of the switch at the turn-OFF instant is given as follows:

$$i_{\text{SW}}^{t=\text{ off}} = i_{\text{Sw}}^{t=t_3} = MI_o. \tag{37}$$

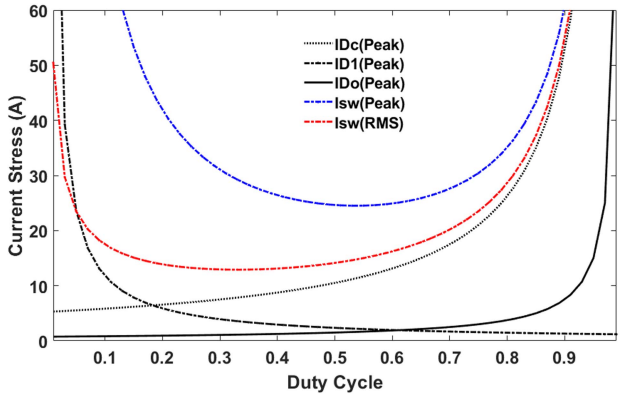


Fig. 8. Peak and rms curves of the switching components current versus duty cycle.

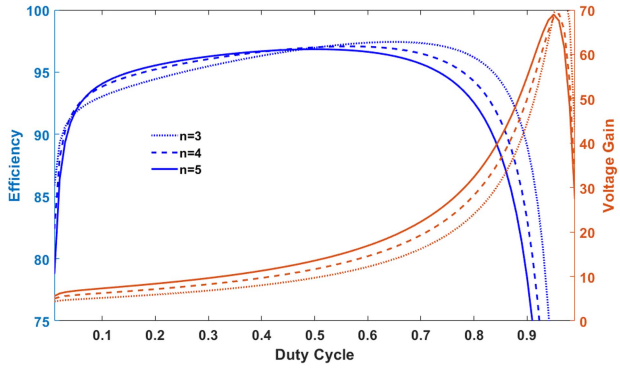


Fig. 9. Nonideal voltage gain and theoretical efficiency of the proposed converter as a function of the duty cycle.

TABLE I
PARASITIC PARAMETERS OF THE CONVERTER

Parameter	Description
$r_{DS(ON)}$	ON-state resistance of the active switch (MOSFET)
t_{on} , t_{off}	Turn-on and turn-off times of the switch
T_s	The switching cycle time of the single switch
ESR_i	Equivalent Series Resistance of the converter capacitors
V_{FDi}	Threshold voltage of the converter diodes
r_{Lin}, r_{Ni}	Parasitic resistances of the magnetic components (L_{in} and CI)

Furthermore, the maximum current value of D_c at $t = t_3$ is expressed as follows:

$$i_{Dc(\text{peak})} = i_{\text{SW}}^{t=\text{off}} = MI_o \tag{38}$$

$$I_{D1(\text{RMS})} = MI_o \sqrt{\frac{D_{34}}{3}}. \tag{39}$$

Here, D_{34} is the time duration of operating mode-4 of the proposed converter that is obtained as follows:

$$D_{34} = \frac{2}{M}. \tag{40}$$

Fig. 8 depicts the peak and the rms curves of the switching components' currents versus the duty cycle. Regarding this figure, a proper duty cycle range to achieve minimum current stress for power components is about $0.38 < D < 0.75$.

D. Efficiency Analysis

In this part, the power dissipation mechanism of the proposed circuit is evaluated. The main parasitic components of the presented converter are listed in Table I.

Regarding the ZCS performance at the turning-ON time of the switch of the proposed converter, the power loss of the power switch in the suggested topology can be estimated as follows:

$$P_{\text{Sw}} = \frac{1}{2T_s} \cdot V_{DS} \left(i_S^{t=\text{off}} \cdot t_{\text{off}}\right) + r_{DS(\text{on})} \cdot I_{\text{Sw(RMS)}}^2 \tag{41}$$

where $i_{\text{Sw}}^{t=\text{off}}$ and $I_{\text{Sw(RMS)}}$ depict the power switch currents at turn-OFF instant and rms values, respectively [(35) and (38)]. Furthermore, the quasi-resonant performance of the converter during operating mode-2 reduces the value of the $i_{\text{Sw}}^{t=\text{off}}$, which alleviates the switch power loss. The conduction loss of the diode can be achieved as follows:

$$P_{Di} = V_{FDi} \cdot I_{D(\text{AVG})}. \tag{42}$$

Here, $I_{D(\text{AVG})}$ denotes the average value of the diode current. Moreover, the capacitor loss is given as follows:

$$P_{\text{Cap}\cdot i} = \text{ESR}_i \cdot I_{C(\text{RMS})}^2. \tag{43}$$

Finally, the magnetic component's loss dissipations can be determined by

$$P_{\text{Mag.}} = r_{L_{\text{in}}} \cdot I_{L_{\text{in}}(\text{RMS})}^2 + r_{N1} \cdot I_{lk1(\text{RMS})}^2 + r_{N2} \cdot I_{N2(\text{RMS})}^2 + P_{\text{Core}(L\text{in, CI})}. \tag{44}$$

Fig. 9 expressed the effect of the parasitic components of the circuit under several turn ratios of the CI on the converter voltage-gain ratio and the theoretical efficiency. This curve is drawn at $V_{\text{in}} = 25$ V, $R_L = 533\ \Omega$, and $f_s = 60$ kHz. Moreover, the other parasitic components of the circuit are $r_{DS} = 6.7$ mΩ, $t_{\text{off}} = 4$ ns, $\text{ESR}_{Cc} = \text{ESR}_{C1} = \text{ESR}_{C2} = 8$ mΩ, $\text{ESR}_{Co} = 80$ mΩ, $V_{FDc} = 0.55$ V, $V_{FD1} = V_{FDo} = 0.7$ V, $r_{Dc} = r_{D1} = r_{Do} = 7$ mΩ, $r_{Lin} = 10$ mΩ, and $r_{N1} = 7$ mΩ. According to this figure, the proposed converter with a high voltage gain along with soft-switching performance is able to provide high power-handling capacities.

IV. PERFORMANCE COMPARISON

Table II compares the main key performance indicators of the dc–dc converters, including components counts, voltage-gain ratio, component voltage stresses, and soft-switching performance of the presented topology with some other zero input current ripple converters mentioned in the literature.

Regarding Table II, the proposed converter along with the converters in [10], [21], [26], and [28] perform at soft-switching conditions without reverse-recovery issue. At turn ratio $n = 5$, Fig. 10 expresses the voltage-gain comparison of converters specified in the comparison table. It should be noted that, since the converter in [26] uses three-winding CI with $n_{21} = n_{31} = n$, the turns ratio $n = 5/2$ ($n = 2.5$) is considered. From this figure, the proposed converter along with the converters in [19] and [28] are able to provide higher output voltages than the

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER WITH OTHER COUNTERPARTS

Converter Topology	No. of Components S/D/C/CI+L/T	Voltage Gain	Z.I.C.R	Voltage Stress on Main Switch (V_s/V_o)	Maximum Voltage Stress on Diodes (V_D/V_o)	Soft-Switching (Main Switch)	Reverse Recovery Loss
[10]	2/1/3/1^{2w} +1/8	$\frac{1+D}{(1-D)}$	Yes	$\frac{V_o}{1+D}$	$\frac{2V_o}{(1+D)}$	ZVS	Very Low
[19]	1/4/5/2^{2w} +1/13	$\frac{1+D+nD}{(1-D)^2}$	Yes	$\frac{V_o}{1+D+nD}$	$\frac{(1+n)V_o}{1+D+nD}$	-	Low
[21]	2/2/5/2^{2w} +0/11	$\frac{1+n}{(1-D)}$	Yes	$\frac{V_o}{1+n}$	$\frac{nV_o}{1+n}$	ZVS	Very Low
[22]	1/3/5/2^{2w} +0/11	$\frac{1+n+D}{(1-D)}$	Yes	$\frac{V_o}{1+n+D}$	$\frac{(1+n)(n-2D)V_o}{(2+n)(1+n+D)}$	QR	Low
[23]	1/1/4/0 +2/8	$\frac{1}{(1-D)}$	Yes	V_o	V_o	ZVS	Very Low
[24]	1/4/2/0 +3/10	$\frac{1+D}{(1-D)}$	Yes	V_o	$\frac{DV_o}{1+D}$	-	High
[25]	2/3/3/0 +3/11	$\frac{3}{(1-D)}$	Yes	$\frac{V_o}{3}$	$\frac{2V_o}{3}$	-	High
[26]	2/3/5/1^{3w}+1/12	$\frac{1+2n}{(1-D)}$	Yes	$\frac{V_o}{1+2n}$	$\frac{nV_o}{1+2n}$	ZVS	Very Low
[27]	1/2/4/1^{4w}+2/10	$\frac{n_3-n_2+(n_3+n_2)D}{(n_3-n_2)(1-D)}$	Yes	$\frac{(n_3-n_2)V_o}{n_3-n_2+(n_3+n_2)D}$	$\frac{(n_3+n_2)V_o}{n_3-n_2+(n_3+n_2)D}$	-	Low
[28]	2/6/8/1^{2w} +1/18	$\frac{1+2n}{(1-D)}$	Yes	$\frac{V_o}{1+2n}$	$\frac{nV_o}{1+2n}$	ZVS	Very Low
Proposed Converter	1/3/4/1^{2w} +1/10	$\frac{2+n}{(1-D)}$	Yes	$\frac{V_o}{2+n}$	$\frac{(1+n)V_o}{2+n}$	ZCS+QR	Very Low

S = Switch, **D** = Diode, **C** = Capacitor, **CI** = Coupled-Inductor, **L** = Inductor, **T** = Total Device Count, **Z.I.C.R** = Zero Input Current Ripple

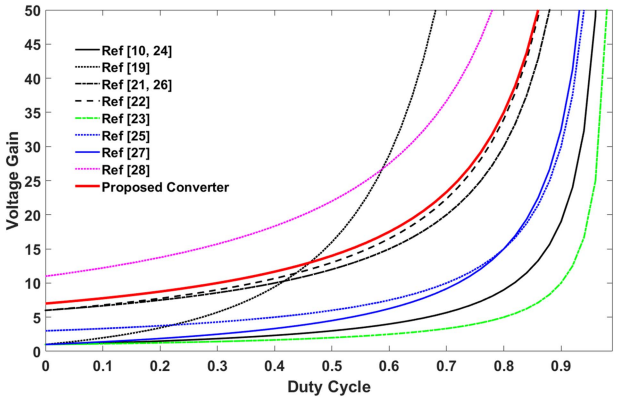


Fig. 10. Total voltage-gain comparison.

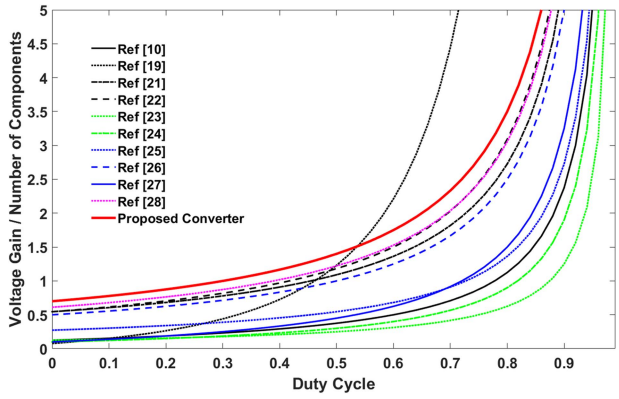


Fig. 11. Voltage gain per number of components comparison.

others. However, the converters in [19] and [28] suffer from hard-switching performance and large component counts. Moreover, Fig. 11 depicts the voltage-gain ratio per number of components. Regarding this figure, only the introduced converter along with the converter in [19] with hard-switching performance has a higher voltage-gain ratio per number of components.

Furthermore, the normalized switch voltage stress of converters mentioned in Table II is plotted in Fig. 12. As shown in this figure, the introduced topology along with the converter in [28] (with 18 component counts) have the lowest voltage stress than the competitors. From Fig. 13, the normalized maximum diode voltage stress of the suggested circuit is at a low level. Therefore, switching devices with lower voltage rates can be selected for the proposed converter.

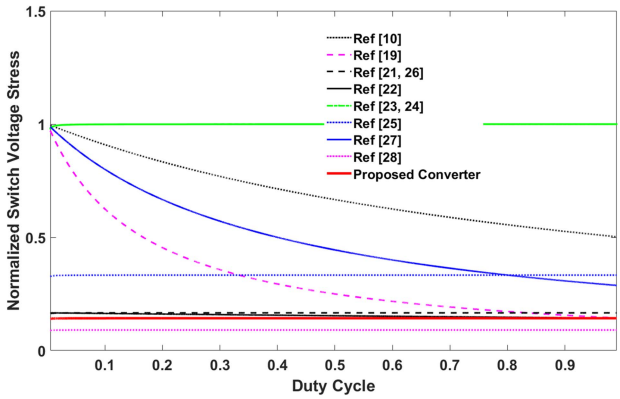


Fig. 12. Comparison of normalized voltage stress of the power switch.

TABLE III
THEORETICAL EFFICIENCY OF THE CONVERTERS

Converter	[10]	[19]	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	Proposed
Duty Cycle	D=0.88	D=0.5	D=0.63	D=0.59	D=0.93	D=0.88	D=0.82	D=0.63	D=0.81	D=0.33	D=0.57
Efficiency %	93.6%	93.3%	95.3%	96.4%	92.8%	91.0%	96.1%	95.8%	94.7%	93.9%	96.7%

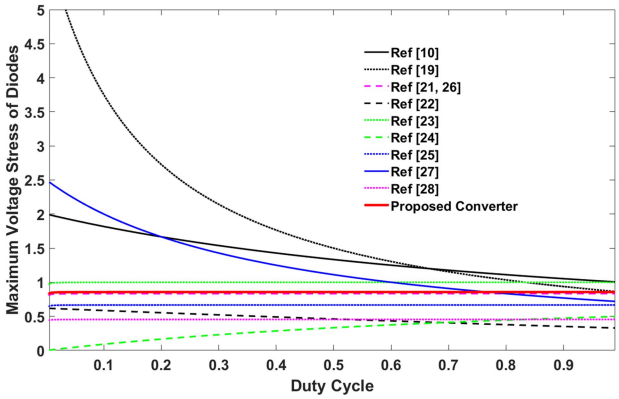


Fig. 13. Comparison of normalized maximum voltage stress of the diodes of the converters in Table II.

Moreover, a comparison of the theoretical efficiency of the converters referred in the comparison table at the same conditions (25 V/400 V, 300 W, 60 kHz, $n = 5$) is provided and summarized in Table III. The parasitic components are chosen based on the voltage and current stress values and selected from the related datasheets. Due to full soft-switching performance and very LRR problem, the proposed topology demonstrates the high efficiency against other converters.

The comparison indicates that the introduced topology in this article has better performance than the others.

V. PARAMETERS DESIGN

The parameters design of the proposed circuit, including the magnetic components, resonant tank, and capacitors, is provided in this section.

A. Magnetic Components

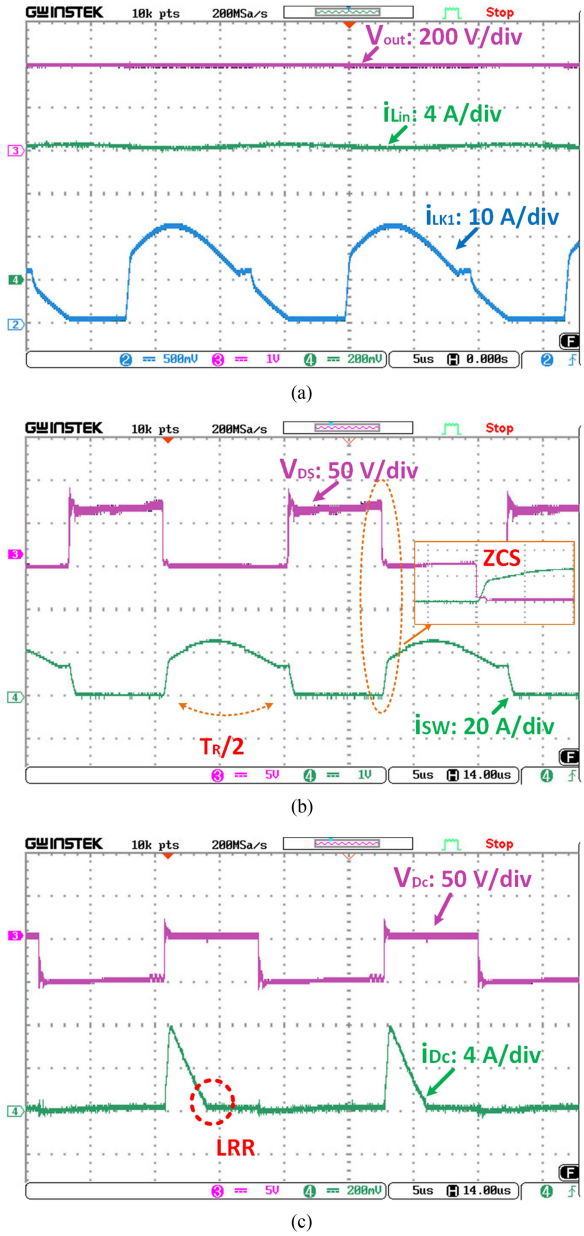
Using (26), the minimum value of the input inductance of the proposed converter is designed as follows:

$$L_{\text{in}} > \frac{2D\left(\frac{n}{C_1}+\frac{1+n}{C_c}\right)}{8f_s^2\Delta I_{\text{in}}}\frac{V_o}{R_L}. \tag{45}$$

From (45), the parameters design of input inductance depends on the desired input current ripple (ΔI_{in}), output voltage (V_o), the load resistor (R_L), turns ratio of the CI, and the switching frequency f_s. Furthermore, the range of the magnetizing inductance of the CI can be determined as follows:

$$L_M = \frac{V_{Lm}\cdot D}{\Delta I_{LM}\cdot f_s} = \frac{V_{\text{in}}\cdot D}{\Delta I_{L\text{in}}\cdot f_s} \tag{46}$$

where ΔI_{LM} is the current ripple rate of the magnetizing inductance.



(a)

(b)

(c)

Fig. 14. Experimental results. (a) Output voltage, input current, and the leakage inductor current. (b) Power MOSFET. (c) Diode D_c.

To estimate the optimal design of the magnetic cores of the input inductor and CI, the parameter product of window winding area cross-sectional area (A_P) can be used [1]. A_P is defined as follows:

$$A_p = \left[\frac{K_i\cdot L\cdot \hat{I}^2\cdot\sqrt{1+\gamma}}{B_{\max}\cdot K_t\cdot\sqrt{K_u\Delta T}}\right]^{\frac{8}{7}}. \tag{47}$$

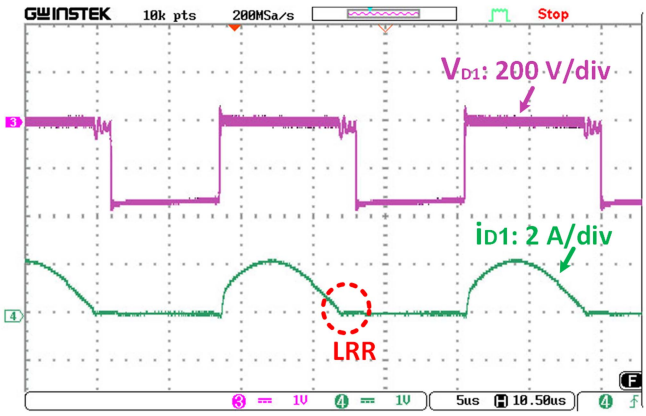


Fig. 15. Experimental results of the diodes D_1.

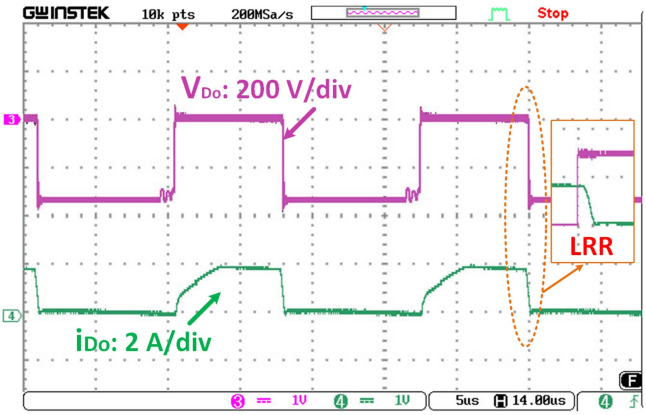


Fig. 16. Experimental results of the diode D_o (**LRR** = Low reverse recovery).

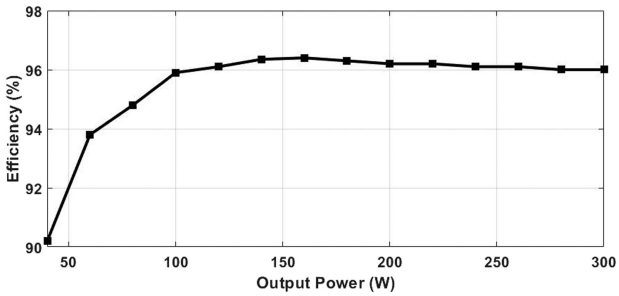


Fig. 17. Measured efficiency versus output power.

Here, K_i is the current waveform factor, L is the inductance value, $\hat{I}$ is the peak current, γ is the ratio of iron loss to copper loss, $B_{\max}$ is the maximum flux density, K_t is a constant value 48 200, K_u is the window utilization factor, and ΔT is the allowable temperature rise. Then, using (48), the turns ratio of the input inductor and the primary side of the CI is given

$$n = \sqrt{\frac{L}{A_L}} \tag{48}$$

where A_L denotes the inductance per turn that can be extracted from the desired core datasheet.

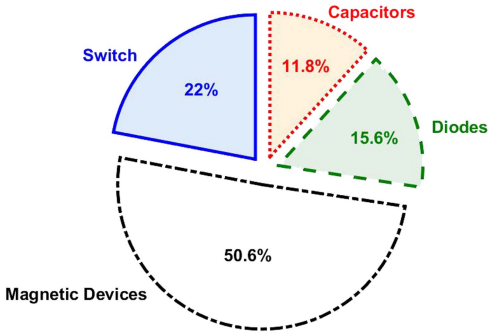


Fig. 18. Estimated loss distribution profile of the proposed converter at full-load condition (25 V/400 V)/300 W).

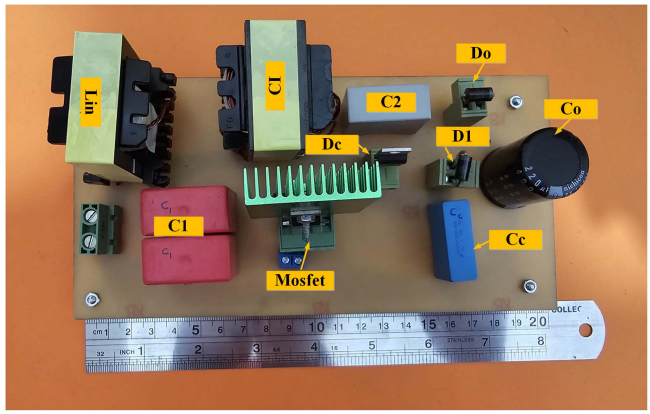


Fig. 19. Photograph of the proposed converter prototype.

B. Capacitors

To reduce the output voltage ripple (typically less than 1%), the output capacitance C_o can be calculated as follows:

$$C_{o1} = \frac{D}{\Delta V_{co} \cdot f_s} \left(\frac{V_o}{R_L}\right). \tag{49}$$

Moreover, the suitable values of the middle capacitors, including C_1, C_2, and C_3, can be given as follows:

$$C_1 = \frac{(n+1)\, V_o}{\Delta V_{C1} \cdot f_s R_L} \tag{50}$$

$$C_2 = \frac{V_o}{\Delta V_{C2} \cdot R_L f_s} \tag{51}$$

$$C_c = \frac{(n+1)}{\Delta V_{C_c} \cdot f_s} \left(\frac{V_o}{R_L}\right) \tag{52}$$

where $\Delta V_{C1,2,Cc}$ are the allowable voltage ripple rates of the capacitors. However, according to (1), calculating the capacitors C_1, C_2, and C_c needs extra consideration as follows:

$$\pi \sqrt{L_k \left(C_1 \| n^2 C_2 \| \left(\frac{n}{1+n}\right)^2 C_c\right)} = DT_S. \tag{53}$$

TABLE IV
KEY PARAMETERS OF PROTOTYPE SETUP

Parameter	Values
Output Power (P_{out})	300 W
Input Voltage (V_{in})	25 V
Output Voltage (V_o)	400 V
Switching Frequency (f_s)	60 kHz
Capacitor C_1	2.*MKS 15 µF/100 V
Capacitor C_c	MKT 10 µF/100 V
Capacitor C_2	MKT 2.2 µF/250 V
Capacitor C_o	220 µF/450 V
Power Switch S	IPP076N15N5/ $R_{DS(on)}$=7.6 mΩ
Input Inductor L_{in}	70 µH / EE42/21/15
Magnetizing Inductor of the CL (L_m)	90 µH
Turns Ratio of the TWCI *(n)*	(1:5.2) / 42/21/20
The leakage inductance (L_K)	0.9 µH
Diodes D_1 and D_o	MUR440
Diode D_c	MBR10100

VI. EXPERIMENTAL VALIDATION

A 300-W sample prototype with an input voltage of 25 V and output voltage of 400 V (voltage gain $M = 16$) is provided to validate the effectiveness of the proposed converter. The specifications of this prototype are the same, as listed in Table IV. Thanks to the low-voltage stress, a MOSFET (*IPP076N15N5*) with a very low $R_{DS(\text{on})}$ is used. To improve the circuit efficiency, the middle capacitors C_1, C_2, and C_c are selected as film capacitors (types metallized polyester capacitors (MKS) and metallized polyester film capacitors (MKT)) with a very low equivalent series resistance (ESR).

A high-frequency current probe PA-667 with division coefficients of 500 and 50 mV/A and a differential voltage probe GDP-025 with division coefficients of ×20, ×50, and ×200 are also employed to extract the current and voltage waveforms.

When the output power of the proposed converter is 300 W at $V_{\text{in}} = 25$ V and $V_o = 400$ V, the input inductor current $i_{L\text{in}}$ is shown in Fig. 10. Regarding Fig. 14(a), the input current ripple is almost zero ($\Delta I_{L\text{in}} < 0.4$ A). Furthermore, due to the soft-switching performance of the suggested topology, the output voltage is constant without noises and switching spikes.

Moreover, the current that passes through the leakage inductor of the CI is also shown in Fig. 14(a). Moreover, Fig. 14(b) illustrates the experimental current and voltage results of the power MOSFET. It is evident that the switch performs at ZCS at turning ON time. Furthermore, the voltage across the power MOSFET is clamped at about $V_{DS} \approx 60$ V. Also, thanks to the quasi-resonant tank, the current value of the power MOSFET is decreased at the turn-OFF instants, which alleviates the power dissipations. According to Figs. 14(c), 15, and 16, the converter diodes are turned OFF with a light slope without a reverse-recovery problem. According to Figs. 14 and 15, the experimental results are close to the theoretical values.

The experimental efficiency of the presented converter versus the output power at $V_o = 400$ V is obtained, which is shown in Fig. 17. For the full-load conditions (25–400 V, 300 W), the efficiency of the converter is obtained about 96%. Moreover, Fig. 18 depicts the loss distribution profile of the introduced topology. A photograph of the proposed converter prototype is shown in Fig. 19. In addition, the power loss distribution of the suggested circuit components at full-load condition 300 W ($V_{\text{in}} = 25$ V/$V_o = 400$ V) is provided in Table V.

TABLE V
LOSS DISTRIBUTIONS OF THE PROPOSED TOPOLOGY

Components	Power loss relations	Loss value (w)	Percent (%)
Input inductor r_{lin}	$P_{ohmic}^{loss} + P_{core}^{loss}$	1.68	16.47
CI loss		3.58	35.0
Turn-off loss (MOS.T)	$\frac{1}{2T_s}(I_{switch(\max)} \cdot V_{DS} \cdot t_{off})$	0.1	0.98
Conduction loss (MOSFET)	$I_{S(RMS)}^2 \cdot R_{DS(on)}$	2.05	20.09
Capacitive turn-on loss (MOSFET)	$\frac{1}{2T_s}(C_{oss} \cdot V_{DS}^2)$	0.1	0.98
D_1	$V_F \cdot I_{D(AVG)}$	0.6	5.8
D_c		0.4	3.9
D_o		0.6	5.8
C_1	$I_{C(RMS)}^2 \cdot ESR$	0.3	2.9
C_2		0.03	0.29
C_c		0.75	7.3
C_o		0.1	0.98

VII. CONCLUSION

In this article, a new ripple-free input current high step-up dc–dc converter with soft-switching performance for all components has been suggested. In this topology, high voltage gains are achieved with the help of a CI along with a VM. A regenerative passive clamp circuit limits voltage spikes across the power switch. In this topology, to further increase the efficiency, a resonant circuit is designed without adding auxiliary components. High voltage gain under a low component count along with soft-switching performance and LRR problem lead to efficiency improvement. The experimental results from a sample prototype of 300 W ($V_{\text{in}} = 25$ V/$V_o = 400$ V) have justified the feasibility of the introduced converter design. Thus, the proposed topology is well suited for high step-up RES applications.

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