High Step-Up DC-DC Converter by Integration of Active Switched Inductors, Built in Transformer, and Multipliers

Rezvan Fani, Zahra Akhlaghi, and Ehsan Adib, *Member, IEEE*

***Abstract*—This article presents a novel high step-up dc/dc converter by integrating active switched inductors, built-in transformers (BITs), and multipliers. The turn ratio of the BIT provides an extra degree of freedom. Hence, ultrahigh voltage gain is achievable by proper duty cycle and adjusting turn ratio. Multipliers are used to reach high voltage gain even with the unity turn ratio of the transformer. This feature is an effective factor to improve the efficiency. Further, the voltage stress of switches is reduced. It causes the reduction of conduction losses of switches due to the lower resistance of low voltage power MOSFETs. An efficient passive clamp circuit is used to cancel the voltage oscillation of the switches caused by the mismatch of inductors. Regarding these specifications, power losses decrease, and the efficiency is improved. The proposed converter is analyzed theoretically, and the validity of theoretical analysis is verified by constructing a 40–400 V, 200 W prototype.**

***Index Terms*—Built in transformer (BIT), dc–dc converter, high step up, multiplier cell, switched inductor (SL).**

I. Introduction

TODAYS, there is a public concern about environmental pollution and global warming created by fossil fuels. Therefore, much research has been focused on the development of renewable energy systems such as photovoltaic systems, fuel cells, etc. High step-up dc–dc converter is one of the unavoidable parts of these systems, which increases the low dc voltage level of renewable energy sources (about 20–50 V) to the desirable dc voltage level (about 400–750 V). Practically, the conventional dc–dc boost converter cannot realize this high conversion ratio. The required duty cycle for this conversion ratio is too large, which causes significant conduction losses and control problems. Further, it suffers from enormous voltage stress of semiconductor devices and reverse recovery problems of diodes. Therefore, presenting new topologies with high conversion ratio, low voltage stress, high efficiency, and low reverse recovery of diodes is noticed [1], [2], [3].

Employing switched capacitors (SC) or switched inductors (SL), coupled inductors (CL)/built-in transformers (BIT), and their combinations are some techniques to increase voltage gain [4]. In [5], an SC cell with two capacitors and three diodes has been introduced and combined with basic step-up converters to increase the voltage gain. In [6], SC cells have been employed to lift the voltage gain by charging and discharging capacitors. In [7], SCs have been used as voltage multiplier cells and integrated with traditional dc–dc boost converter to increase the conversion ratio. However, in order to reach high voltage gain by these converters, several SC cells are required, which increases the number of elements and losses. Using CLs is the other technique to increase voltage gain. In [8], CLs have been integrated with traditional boost converter, and a passive clamp circuit has been used to limit the voltage spikes of switches. A high voltage ratio is achievable at a large turn ratio of the CLs. However, a high turn ratio results in large leakage inductance and low efficiency. In [9], [10], [11], [12], [13], [14], [15], and [16], CL/BIT and SC techniques have been employed. So, high voltage gain with a low turn ratio of CLs has been achieved.

In [17], [18], and [19], SL cells have been used to increase the voltage gain of traditional boost converter. However, a large number of SL cells must be employed to reach the required voltage gain. In [20], an active switched inductor (ASL) has been used to increase the voltage gain with the low number of elements. However, the achieved voltage gain is not sufficient for the mentioned application. Further, voltage oscillation has appeared on the switches due to the inductors mismatch. The other drawback is that the load is floating and the control circuit is complicated. In [21], the ASL has been integrated with the passive SC network, and the voltage gain has been increased. Nevertheless, the control circuit is complicated. In addition, there is still voltage oscillation on switches. In [22], SC cells and an efficient clamp circuit have been applied to the ASL converter, which has increased the voltage gain and canceled the voltage oscillation of switches. However, this converter has floating ground like [20], [21] and needs a complicated control circuit. In [23], a quasi-active switched inductor (QASL) has been presented, which uses CLs to increase the voltage gain. The drawbacks are as follows.

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1) Efficiency is reduced due to the more inductor losses.
2) Load is floating, and the control unit is complicated.

In [24] and [25], SC cells are applied to QASL. So, higher voltage gain has been achieved with lower duty cycles and turn ratios. However, they still suffer from complicated control units, larger inductor losses, and voltage oscillation on switches. As a result, the main drawbacks of previous ASL-based converters can be organized as follows.

1) Voltage oscillation on switches due to the mismatch of inductors.
2) Floating load.
3) Large inductor loss in CL-based ASL converters.

In order to solve these problems, a new high step-up converter is proposed, which integrates SC multipliers and BIT with the conventional ASL-based converter. The proposed converter possessed grounded load. For this reason, the control circuit is not complicated. This new configuration provides a high voltage gain with a unity turn ratio of the transformer and proper duty cycle. Further, the voltage stress of switches is reduced. In addition, two efficient passive clamp circuits are employed to omit the voltage oscillation of switches caused by inductor mismatches. The BIT is placed at the low current side of the converter. Therefore, the transformer core size and copper length decrease efficiently, which reduces total circuit size, cost, and loss. The leakage inductance of the BIT reduces the reverse recovery losses of diodes, and improves efficiency. The advantages of the proposed converter are summarized as follows.

1) No voltage oscillation on switches.
2) Grounded load.
3) Low inductor loss despite the use of a transformer.
4) High voltage gain with low turn ratio and proper duty cycle.
5) Low reverse recovery of diodes.
6) High efficiency.
7) Low voltage stress.

The rest of this article is organized as follows. In Section II, the proposed converter is introduced, and its operation modes are studied. In Section III, the steady-state operation is analyzed theoretically. Section IV is related to the comparison of the proposed converter with other ASL-based high step-up converters. A 200 W laboratory prototype converting 40V to 400V is implemented, and the experimental results are studied in Section V. Finally, Section VI concludes this article.

II. Operating Principle of the Proposed Converter

Fig. 1(a) indicates the schematic of the main idea of the proposed converter. An ASL cell is integrated with a BIT. This integration increases the voltage gain of the proposed converter by an additional degree of freedom, i.e., the turn ratio of the BIT. However, because of the absence of a proper clamp circuit, voltage oscillation appears on the switches due to the mismatch of the inductors, which increases the real voltage stress of the switches. Hence, a proper clamp circuit is employed, and the main idea is developed. Then, a multiplier cell is added to the proposed converter, and the voltage ratio is improved. Fig. 1(b)

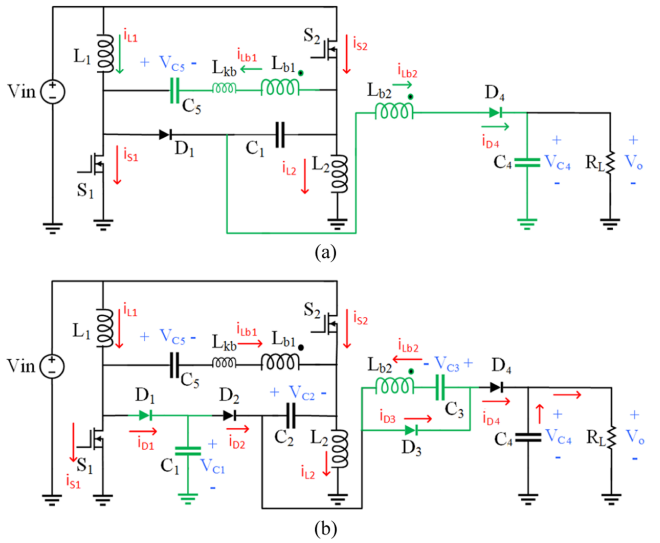

Fig. 1. Proposed converter schematic (a) *Main Idea*: Integration of BIT and conventional ASL converter. (b) *Developed Idea*: Integration of the main idea with multiplier cell and clamp circuit.

demonstrates the final circuit of the proposed converter. The ASL cell contains two inductors $L_{1,2}$ and two switches $S_{1,2}$ with synchronous switching. When the switches are ON, the inductors are placed in parallel. While at the OFF state, they are connected in series, and the current of L_1 flows to L_2 through the clamp circuit and built in transformer. The BIT is modeled by a leakage inductance L_{kb}, and an ideal transformer with two windings: L_{b1} introduces the primary winding and L_{b2} denotes the secondary one.

In order to provide volt-second balance for the BIT, its primary side is placed in series with the capacitor C_5 in a resonant tank. A clamp circuit including two diodes $D_{1,2}$ and two capacitors $C_{1,2}$ helps to absorb the energy of inductors and limit the voltage spikes of switches. The secondary winding of the BIT L_{b2}, diode D_3, and capacitor C_3 provide a multiplier cell to increase the voltage gain. The output diode D_4 makes a route for storing energy into the output capacitor C_4.

In order to study the circuit operation of proposed converter, continues-conduction-mode (CCM) analysis is investigated. The operation of the proposed converter in one switching cycle is divided into six time intervals. Fig. 2 demonstrates the key waveforms of the proposed converter. Fig. 3 shows the equivalent circuit of this converter in each time interval. For simplification, all components are assumed ideal, and the inductors' currents and capacitors' voltages are considered constant during each switching period.

1) Mode I [t_0, t_1]: At this mode, both switches $S_{1,2}$ are just turned ON, and all diodes except D_3 are OFF. The parasitic capacitor of each switch discharges, and the voltage polarity of each inductor and BIT is changed. The inductors $L_{1,2}$, start to store energy. Meanwhile, the leakage inductance of the BIT L_{kb}, releases its energy into C_3, and its current is reduced linearly. At t_1, this current reaches zero, and D_3 turns OFF under zero current situation. Hence, the reverse recovery problem is reduced. See Fig. 3(a).

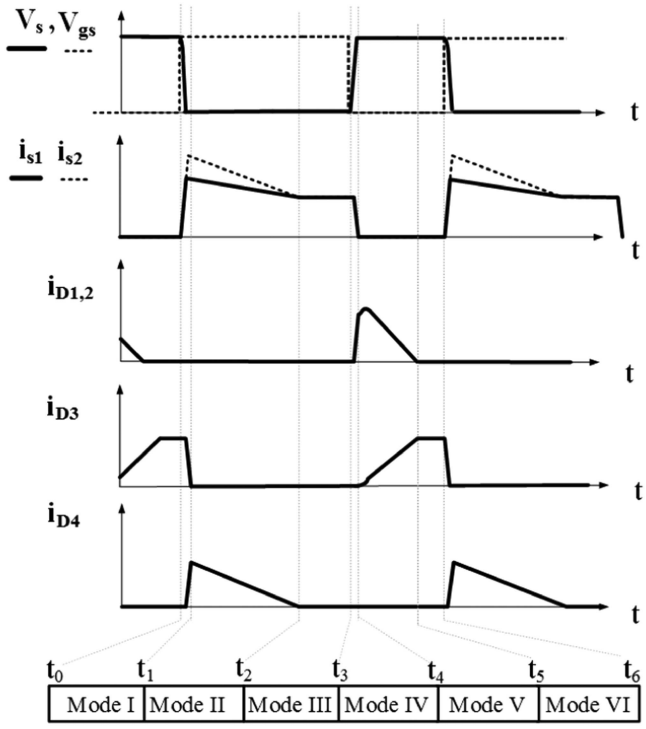

Fig. 2. Key waveforms of the proposed converter.

2) Mode II [t_1, t_2]: During this mode, $S_{1,2}$ are at ON-state, and the inductors $L_{1,2}$, keep storing energy. The winding current direction of the built in transformer is reversed and makes D_4 to conduct. Therefore, C_2 and C_3 transfer their energy to the load through the secondary winding of BIT L_{b2}, and their currents decrease. At t_2, the winding current reaches zero, and the conduction of D_4 is stopped under zero current situation. See Fig. 3(b).

The resonance period of the resonance tank, including L_{kb} and C_5, determines the time range of this mode. In order to realize zero turn OFF situation for D_4, the half of the resonance period, t_r should be adjusted to lower than DT_s, and it is better to have a proper margin to this boundary time. However, a lower resonance period results in a higher resonance peak current. So, the proper choice for t_r can be considered about $T_s/2$.

3) Mode III [t_2, t_3]: During this interval, $S_{1,2}$ are ON, the inductors still store energy while all diodes are OFF, and the power transfer through the BIT is stopped. Simultanusely, C_4 transfers its energy to the load. At t_3, $S_{1,2}$ are turned OFF and this mode ends. See Fig. 3(c).

4) Mode IV [t_3, t_4]: This mode starts when the switches are turned OFF. The parasitic capacitors of switches are charged rapidly, and their drain-source voltages increase to their steady-state amount. See Fig. 3(d).

5) Mode V [t_4, t_5]: Now, switches $S_{1,2}$ are at OFF-state, and the clamp diodes $D_{1,2}$ conduct to limit the voltage spikes ON $S_{1,2}$. The inductors are placed in series, and their currents flow through $D_{1,2}$. So, C_2 is charged by the currents of inductors. The voltage polarity of the primary winding of the BIT is changed, and its current increases linearly in the reverse direction. The current direction of the secondary winding of the BIT leads

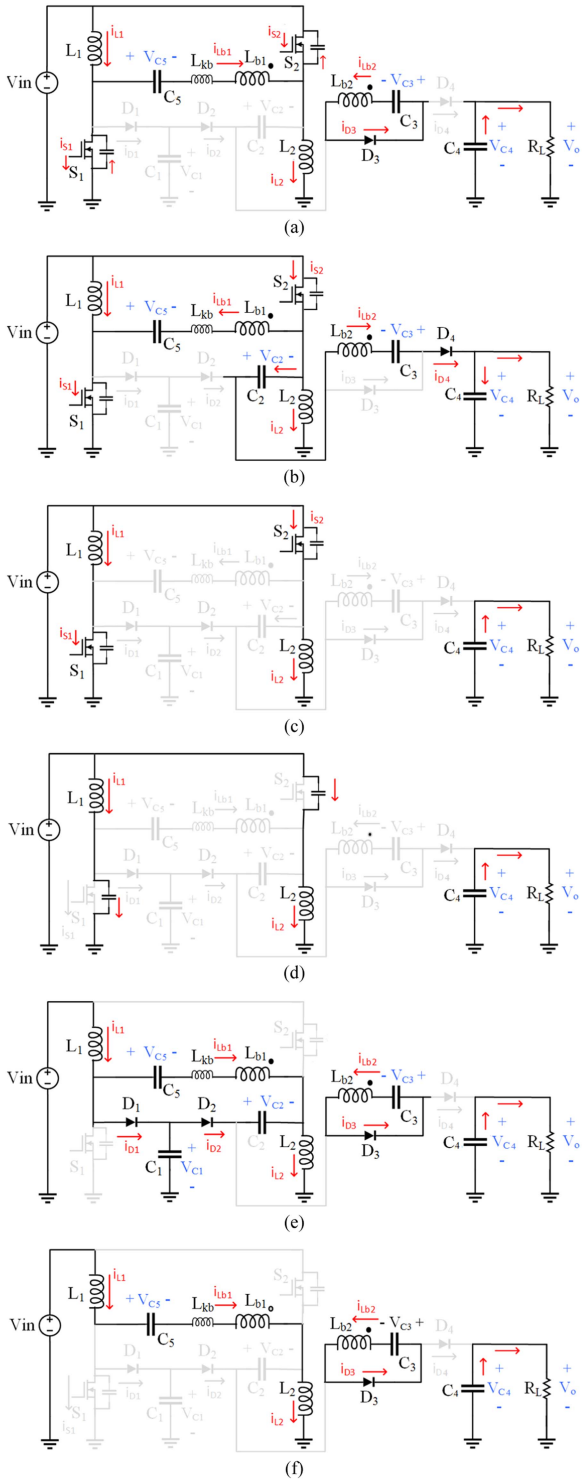

Fig. 3. Equivalent circuit of each operating mode. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI.

D_3 to conduct, and C_3 is charged. While the clamp capacitors absorb the energy of leakage inductance, the currents of $D_{1,2}$ are reduced. At t_5, their currents reach zero, and the mentioned diodes turn OFF at zero current situation. Simultaneously, C_4 transfers its energy to the load. See Fig. 3(e).

6) Mode VI [t_5, t_6]: During this mode, switches are still OFF. Likewise, $D_{1,2}$ and D_4 are OFF. The input current goes through the primary winding of the BIT. It is transferred to the secondary winding and charges C_3. At t_6, switches are turned ON, and this mode ends. See Fig. 3(f).

III. Steady-State Analysis

A. Voltage Gain Analysis

In this section, the CCM operation of the proposed circuit is analyzed in steady-state condition. The inductors store energy when the switches are on, i.e., in modes I, II, and III, which is determined by indices $^{(1)}$ in the following equations. Their energy release occurs when the switches are OFF, i.e., during mode IV, which is determined by indices $^{(2)}$ in the following equations. According to the volt-second balance principle for the inductors and BIT, the following equations are obtained:

$$\int_0^{DT_s} V_{L_{1,2}}^{(1)} dt + \int_{DT_s}^{T_s} V_{L_{1,2}}^{(2)} dt = 0 \tag{1}$$

$$\int_0^{DT_s} V_{L_{b1}}^{(1)} dt + \int_{DT_s}^{T_s} V_{L_{b1}}^{(2)} dt = 0 \tag{2}$$

where $V_{L_{1,2}}^{(1)} = V_{\text{in}}$. So, $V_{L_{1,2}}^{(2)}$ is computed as following:

$$V_{L_{1,2}}^{(2)} = -\frac{DV_{\text{in}}}{1-D}. \tag{3}$$

By applying the KVL rule to the resonant tank, the following equations are obtained:

$$V_{\text{in}} - V_{L_1}^{(1)} - V_{C5} + V_{L_{b1}}^{(1)} - V_{L_2}^{(1)} = 0 \tag{4}$$

$$V_{\text{in}} - V_{L_1}^{(2)} - V_{C5} + V_{L_{b1}}^{(2)} - V_{L_2}^{(2)} = 0. \tag{5}$$

By solving (2), (4), and (5), it yields

$$V_{C5} = V_{\text{in}} \tag{6}$$

$$V_{L_{b1}}^{(1)} = 2V_{\text{in}} \tag{7}$$

$$V_{L_{b1}}^{(2)} = \frac{-2DV_{\text{in}}}{(1-D)}. \tag{8}$$

According to Fig. 3(d) and (3) and (8), the voltage across C_{1-3} is derived as follows:

$$V_{C1} = \frac{V_{\text{in}}}{(1-D)} \tag{9}$$

$$V_{C2} = \frac{(1+D)\,V_{\text{in}}}{(1-D)} \tag{10}$$

$$V_{C3} = \frac{2nDV_{\text{in}}}{(1-D)} \tag{11}$$

where n is the turn ratio of the BIT.

Finally, the output voltage is obtained from (7)–(11) and Fig. 3(b) and (c)

$$V_o = V_{\text{in}} + V_{C2} + V_{C3} + V_{L_{b2}}^{(2)} = \frac{(2n+2)\,V_{\text{in}}}{(1-D)}. \tag{12}$$

Therefore, the voltage gain is

$$M = \frac{V_o}{V_{\text{in}}} = \frac{2n+2}{(1-D)}. \tag{13}$$

B. Voltage and Current Stress Analysis

Considering the previous equations and Fig. 3, the voltage stress of semiconductor devices can be computed as follows:

$$V_{S1,2} = V_{D1,2} = \left(\frac{1}{1-D}\right)\ V_{\text{in}} = \frac{V_o}{2n+2} \tag{14}$$

$$V_{D3} = \left(\frac{2n}{1-D}\right)\ V_{\text{in}} = \frac{nV_o}{n+1} \tag{15}$$

$$V_{D4} = \left(\frac{2n+1}{1-D}\right)\ V_{\text{in}} = \frac{(2n+1)\,V_o}{2n+2}\ . \tag{16}$$

Due to the ampere-second balance principle for capacitors, the average current of diodes is equal to the output current I_o

$$\langle i_{D1-4} \rangle = I_o\ . \tag{17}$$

According to Fig. 3(b)–(d), it yields

$$i_{D3(\text{peak})} = I_{L_{b2(\text{peak})}}^{(2)} = \frac{2I_o}{(1-D)} \tag{18}$$

$$i_{D4(\text{peak})} = I_{L_{b2(\text{peak})}}^{(1)} = \frac{2I_oT_s}{t_r} = 4I_o \tag{19}$$

where t_r determines the time interval of mode II, which is considered $T_s/2$, here.

The switches' peak currents can be written as follows:

$$i_{S1(\text{peak})} = I_{L1} + I_{L_{b1(\text{peak})}}^{(1)} \tag{20}$$

$$i_{S2(\text{peak})} = I_{L2} + I_{L_{b1(\text{peak})}}^{(1)} + I_{L_{b2(\text{peak})}}^{(1)}. \tag{21}$$

From Fig. 3, I_{L1} and I_{L2} can be expressed as follows:

$$I_{L1} + I_{L2} + \langle I_{C2} \rangle + \langle I_{C5} \rangle = I_{\text{in}} \tag{22}$$

where $I_{L1,2}$ and I_{in} denote the average of the inductors and input currents, respectively. So,

$$I_{L1} = I_{L2} = \frac{I_{\text{in}}}{2} = \frac{(n+1)\,I_o}{(1-D)}\ . \tag{23}$$

Substituting (18), (19), and (23) into (20) and (21), gives the switches' peak currents

$$i_{S1(\text{peak})} = \frac{[n+1+4n\,(1-D)]I_o}{(1-D)} \tag{24}$$

$$i_{S1,2(\text{peak})} = \frac{[n+1+(4n+4)\,(1-D)]\,I_o}{(1-D)}\ . \tag{25}$$

C. Design Procedure of Converter Elements

In this section, converter elements are designed for CCM operation. So, following equation should be realized:

$$I_{L1,2} \geq \frac{\Delta i_{L1,2}}{2} \tag{26}$$

where

$$\Delta i_{L1,2} = \frac{DV_{\text{in}}}{L_{1,2} f_s}. \tag{27}$$

Combining (23), (26) and (27), and some simplification gives the minimum value of inductors

$$L_{1,2} \geq \frac{D(1-D)^2 R_{l(\text{BCM})}}{(2n+2)^2 f_s} \tag{28}$$

where $R_{L(\text{BCM})}$ denotes the boundary condition mode (BCM) load.

The primary winding turns of BIT, N_{b1}, is computed as follows:

$$N_{b1} = \frac{2V_{\text{in}} D}{A_C \Delta B f_s} \tag{29}$$

where A_C denotes the core area and ΔB is the flux density.

The minimum value of capacitors is derived from the current-second balance of capacitors

$$C_4 \geq \frac{DV_o}{R_l f_s \Delta V_{C_4}} \tag{30}$$

$$C_{1-3} \geq \frac{V_o}{R_l f_s \Delta V_{C_{1-3}}} \tag{31}$$

$$C_5 \geq \frac{V_o}{R_l f_s \Delta V_{C5}}. \tag{32}$$

On the other hand, From Fig. 3(d), the capacitors C_5 and C_2 and the leakage inductance of the BIT L_{kb}, make a resonant tank with the resonant frequency f_r, which is expressed as

$$f_r = \frac{1}{2\pi} \sqrt{\frac{C_5 + C_2}{L_{kb} \cdot (C_5 C_2)}}. \tag{33}$$

As explained in Section II, the proper choice for the resonance period is about $T_s/2$. So, the value of L_{kb} must fulfill

$$L_{kb} \cong \frac{T_s^2 (C_5 + C_2)}{4\pi^2 C_5 C_2}. \tag{34}$$

D. Control Module

This converter benefits from common ground between input and output. For this reason, the control module is not complex and does not need an optocoupler to provide isolation. On the other hand, although there are two switches, they both operate synchronously. Therefore, its control unit is as simple as the control circuit of common ground single switch converters. The output voltage is regulated by a simple voltage mode PWM control technique. The system block diagram is demonstrated in Fig. 4. The output voltage V_o is compared with the reference voltage V_{ref} by an error amplifier. Then the differential voltage is compared with a sawtooth waveform by a pulsewidth modulation generator to provide the pulse signal for the gate drivers. As a result, the pulse width of gate signal is determined by the help of the control unit to regulate the output voltage V_o.

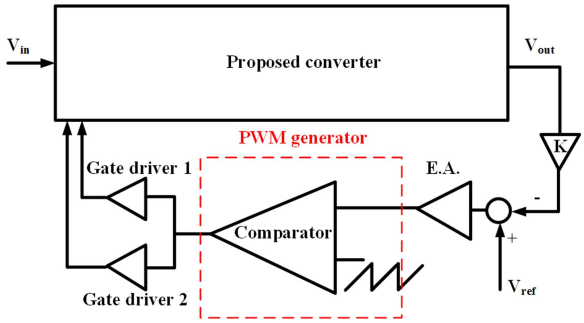

Fig. 4. Block diagram of control strategy.

IV. Performance Comparison

The specification of the proposed converter and the converters of [20] and [22], [23], [24], [25] are compared in Table I. All compared circuits, [20] and [22], [23], [24], [25], use the ASL technique. The terms of voltage gain, voltage stress of semiconductors, number of elements, core loss, winding loss, output ground, and the ability of voltage oscillation cancelation are given in Table I.

In order to have a better adjudication of the proposed converter performance, the voltage gain and voltage stress of the proposed converter and its counterparts are plotted in Figs. 5 and 6, respectively. As can be seen, the proposed coverter has higher voltage gain and lower voltage stress in comparison to [20] and [22], [23] but lower voltage gain and higher voltage stress than [24] and [25]. However, Luo et al. [24] and Liang et al. [25] employ two CL, and each CL has significant loss, which reduces their efficiency. The proposed converter employs two inductors and one BIT. The inductor core loss is slight because of its low current ripple, and its winding loss is lower than CL due to its shorter winding length.

On the other hand, the BIT is placed at the low current side. As a result, it requires a smaller core volume and smaller winding length in comparison with the CLs of [24] and [25]. So, the proposed converter's total inductor loss is improved. Hence, using BIT is a more efficient approach to increase the voltage gain against employing CLs instead of the inductors in ASL-based converters. In addition, although [24] and [25], have achieved a higher gain, they suffer from oscillation on their switches. Therefore, they require some extra diodes and capacitors for switch oscillation cancelling, which increases the number of their elements, whereas the proposed converter provides switch oscillation cancelling without extra components. On the other hand, in [24] and [25], the common ground feature is sacrificed for higher voltage gain, which makes the control module complicated, while the proposed converter shares the input and output grounds and its control is capable by a simple structure.

V. Discussion on Simulation and Experimental Results

A 200 W, 40 to 400 V prototype circuit is simulated by ORCAD PSPICE and fabricated to verify the truth of theoretical analysis. In order to reach this conversion ratio, the BIT is implemented by unity turn ratio, and the duty ratio of switches is

TABLE I
COMPARISON OF THE PROPOSED CONVERTER WITH PERVIOUS NONISOLATED CONVERTERS

Non-isolated topologies	Yang et al. [20]	Cui et al. [22]	Liu and Li [23]	Luo et al. [24]	Liang et al. [25]	Proposed converter
Technique	ASL	ASL + SC	ASL + CI	ASL + CI + SC	ASL+CI + SC	ASL + BIT + SC
Voltage gain	$\frac{1+D}{1-D}$	$\frac{3+D}{1-D}$	$\frac{1+D(2n+1)}{1-D}$	$\frac{1+2n+3D}{1-D}$	$\frac{3+n+D}{1-D}$	$\frac{2+2n}{1-D}$
Voltage stress of switch	$\frac{V_o}{1+D}$	$\frac{V_o}{3+D}$	$\frac{V_o}{1+D(2n+1)}$	$\frac{V_o}{1+2n+3D}$	$\frac{V_o}{3+n+D}$	$\frac{V_o}{2+2n}$
Maximum Voltage stress of diodes	$\frac{2V_o}{1+D}$	$\frac{V_o}{3+D}$	$\frac{2nV_o}{1+D(2n+1)}$	$\frac{(2+2n)V_o}{1+2n+3D}$	$\frac{(2+n)V_o}{3+n+D}$	$\frac{(1+2n)V_o}{2+2n}$
Number of elements Switches/diodes/ capacitors/Inductors/BIT/CI	2/1/1/2/0/0	2/4//4/2/0/0	2/3/3/0/0/2	2/3/4/0/0/2	2/3/3/0/0/2	2/4/5/2/1/0
Core loss	small	small	large	large	large	moderate
Winding loss	small	small	large	large	large	moderate
Common ground	No	No	No	No	No	Yes
Voltage oscillation on switches	Yes	No	No	Yes	Yes	No

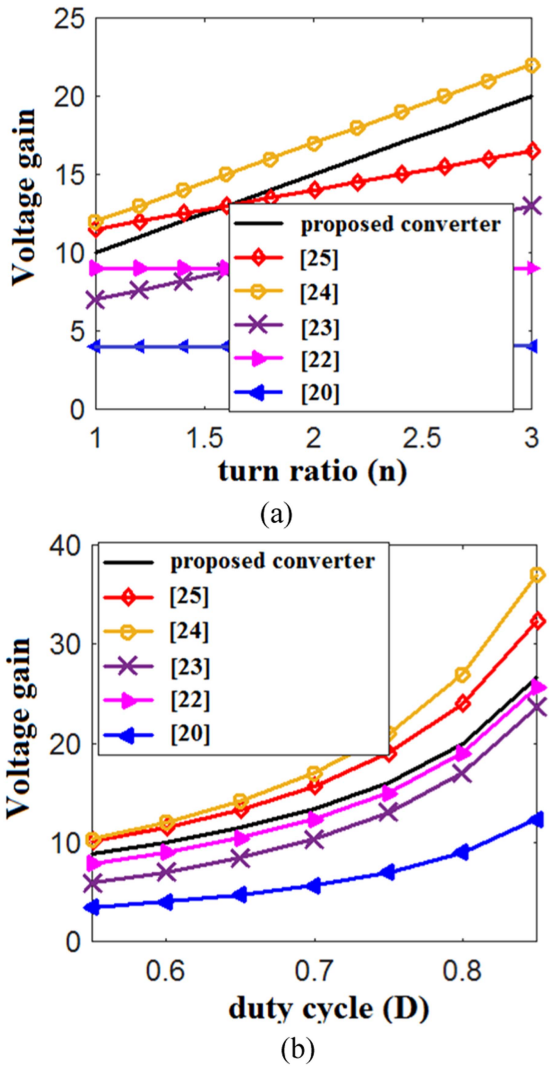

Fig. 5. Voltage gain. (a) Versus turn ratio at $D = 0.6$. (b) Versus duty cycle at $n = 1$.

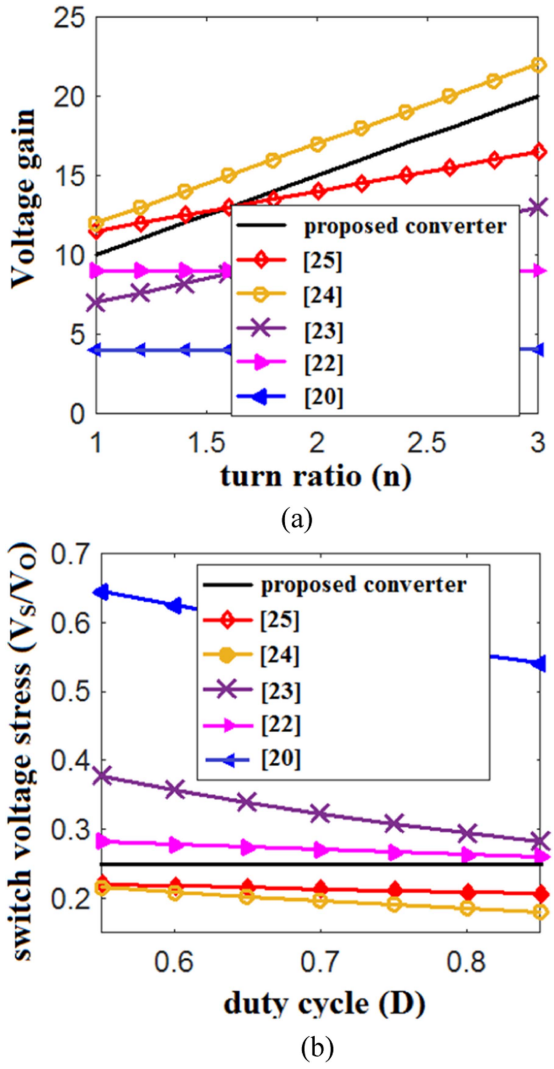

Fig. 6. Voltage stress of switches normalized by V_o. (a) Versus turn ratio at $D = 0.6$. (b) Versus duty cycle at $n = 1$.

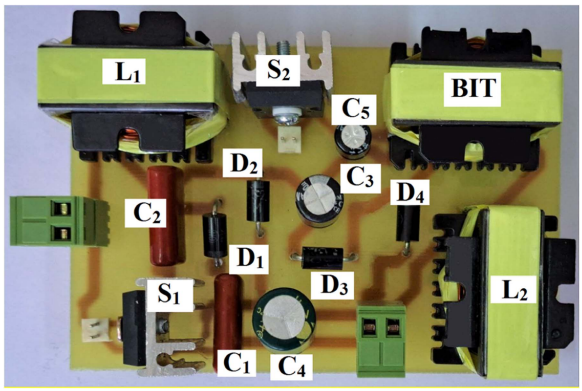

Fig. 7. Laboratory prototype of the proposed converter.

TABLE II
SPECIFICATIONS OF THE IMPLEMENTED PROTOTYPE CIRCUIT

symbol	Parameter	value
V_{in}	Input DC voltage	40 V
V_o	Output DC voltage	400 V
P_o	Maximum output power	200 W
f_s	Switching frequency	50 kHz
$C_{1\text{-}2}$	Capacitors	2.2 µF
C_3		6.8 µF
C_4	Output capacitor	22 µF
C_5	Resonant capacitor	10 µF
$D_{1\text{-}2}$	Clamp diodes	SR5200
$D_{3\text{-}4}$	Output diodes	MUR460
S	Power switch	IRFP260
	inductor	
---	Core type	EI33/29
$L_{1,2}$	Inductors	2 mH
	Built-in transformer	
---	Core type	EI33/29
n	Turn ratio	1
L_{kb}	Leakage inductance	2 µH

about 0.6. Fig. 7 demonstrates the photograph of the fabricated prototype circuit. In order to design inductors, (28) is used, and the BIT is designed by (29) and (34). The maximum ripple of the output capacitor is considered 0.1%, and other capacitors are designed for 2–3% voltage ripple. The specification of the prototype circuit is given in Table II.

Fig. 8 shows the simulated current and voltage waveforms of switches and diodes, which confirm theoretical analysis. The voltage and current waveforms of the switches are indicated in Fig. 9(a)–(b) and realize (14), (24), and (25). The voltage and current waveforms of diodes are shown in Fig. 9(c)–(f). These waveforms confirm (14)–(19) and zero current turn-OFF of diodes. So, the reverse recovery of diodes is alleviated. As can be seen, experimental results are matched with the simulation results, which were shown in Fig. 8.

Current waveforms of the inductors and BIT are shown in Fig. 10. As expected, the inductor current is half of the input current. The inductor current has a ripple value of 0.5 A. From this figure, it is evident that the BIT RMS current is lower than the inductor's current, which verifies core cost and volume reduction compared to CL-based converters. Because, with similar design criteria, CL-based ASL converters require more winding windows and so a larger core volume and cost to provide enough space for their two winding in comparison to the input inductors of the proposed converter. On the other hand, since the BIT RMS current is lower than the input inductor current, its winding window requirement is not as large as CLS winding window requirement in the CL-based ASL converters.

VI. Loss Analysis

To assess the effectiveness of the proposed converter, the power loss of each component must be calculated. This section analyzes the different types of losses in the converter, including conduction, switching, capacitive turn-ON, diode, capacitor, and inductor losses.

A. Conduction Loss of Switches

Conduction losses formula of each switch is given as

$$P_{\text{Cond }S} = R_{ds} \cdot I^2_{S\text{rms}} \tag{35}$$

where $I_{S\ \text{rms}}$ represents the RMS switch current, and its value for S_1 and S_2 is 2.53 and 3.67A, respectively. The ON resistances of switches are 68 mΩ at an operating temperature denoted by R_{ds}. From (35), the total conduction losses of switches are calculated as follows:

$$P_{\text{Cond }S} = P_{\text{Cond }S1} + P_{\text{Cond }S2} = 1.369\ \text{W}. \tag{36}$$

B. Switching Loss

The switching losses of each switch are computed using

$$\begin{aligned} P_{S1(\text{sw})} &= 0.5 f_s \left(V_{S\text{off}1} I_{S\text{off}1} t_{ffs} + V_{S\text{on}1} I_{S\text{on}1} t_{rfs}\right) \\ P_{S2(\text{sw})} &= 0.5 f_s \left(V_{S\text{off}2} I_{S\text{off}2} t_{ffs} + V_{S\text{on}2} I_{S\text{on}2} t_{rfs}\right). \end{aligned} \tag{37}$$

Here, $V_{S\text{off}1,2}$ and $V_{S\text{on}1,2}$ represent the voltages across $S_{1,2}$ during turn-OFF and turn-ON, respectively, and they are equal to 100 V. $I_{S\text{off}1,2}$ is the corresponding current during turn-OFF, which is 2.7 A, while $I_{S\text{on}1}$ and $I_{S\text{on}2}$ are the currents during turn-ON, and their values are 4.5 and 6.5 A, respectively. t_{ffs} and t_{rfs} denote the fall and rise times for switches and are derived from the switch datasheet. From (37), total switching losses yield as follows:

$$P_{\text{Switching}} = P_{S1(\text{sw})} + P_{S2(\text{sw})} = 2.298\ \text{W}. \tag{38}$$

C. Capacitive Turn-On Loss of Switches

The capacitive turn-ON losses of each switch can be calculated as follows:

$$P_{\text{Cap Turn-on}} = 0.5 C_{\text{oss}} V^2_{S\text{on}} f_s. \tag{39}$$

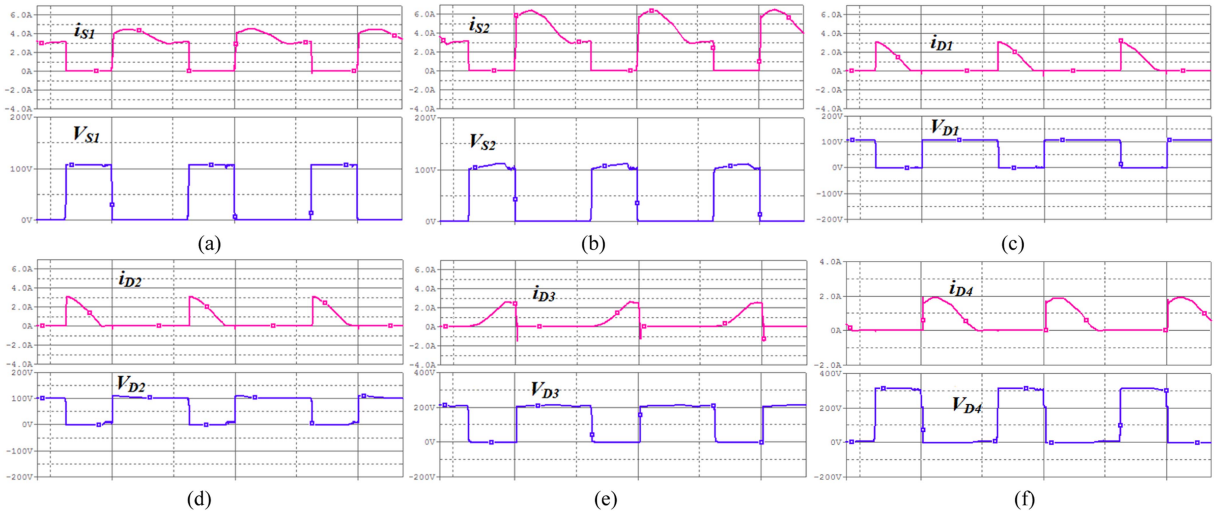

Fig. 8. Simulation current and voltage waveforms of (a) S_1, (b) S_2, (c) D_1, (d) D_2, (e) D_3, and (f) D_4.

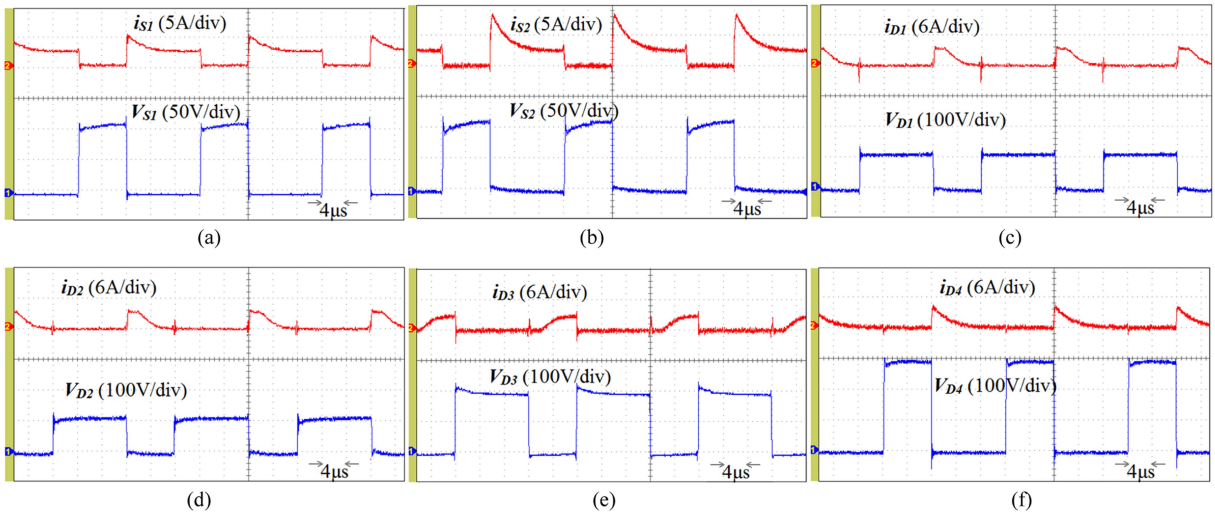

Fig. 9. Experimental current and voltage waveforms of (a) S_1, (b) S_2, (c) D_1, (d) D_2, (e) D_3, and (f) D_4.

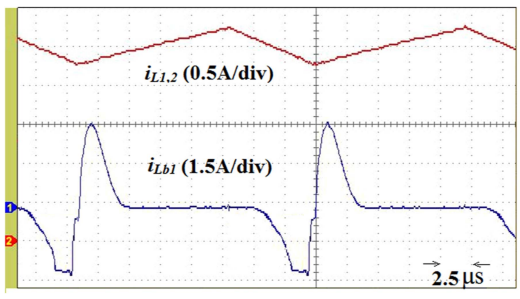

Fig. 10. Current waveform of $L_{1,2}$ and L_{b1}.

In (39), C_{oss} represents the output capacitances of switches and are derived from the switch datasheet. $V_{S\text{on}}$ is the switch voltage during turn-ON, which is equal to 100 V for both switches, and f_s represents the switching frequency.

So from (39), the total capacitive turn-on losses of switches are computed as follows:

$$P_{\text{Cap Turn-on}} = P_{\text{Cap Turn-on1}} + P_{\text{Cap Turn-on2}} = 0.3\text{W}. \tag{40}$$

D. Conduction Loss of Diodes

According to the datasheets, the assumed forward voltages for diodes D_{1-4} are $V_{\gamma 1} = V_{\gamma 2} = 0.47$ and $V_{\gamma 3} = V_{\gamma 4} = 0.9$. The average currents flowing through $D_{1\text{-}4}$ are denoted as $I_{D_i(\text{avg})}$, and each with a value of 0.5 A. So, the conduction losses of the diodes can be calculated as follows:

$$P_{\text{Cond D}} = \sum_{i=1}^{4} P_{\text{Cond}D_i} = \sum_{i=1}^{4} V_{\gamma_i} \times I_{D_i(\text{avg})} = 1.37\ \text{W}. \tag{41}$$

E. Capacitor Loss

By measuring $(\text{ESR1}) = 0.004$, $(\text{ESR2}) = 0.004$, $(\text{ESR3}) = 0.05$, $(\text{ESR4}) = 0.06$, and $(\text{ESR5}) = 0.01$, the ESR losses of the capacitors yield as follows:

$$P_{\text{ESR}} = \sum_{i=1}^{5} P_{\text{ESR}_i} = \sum_{i=1}^{5} \text{ESR}_i I_{C_{\text{irms}}}^2 = 0.137 \text{ W}. \quad (42)$$

In (40), $I_{\text{C rms}}$ denote the RMS currents flowing through the capacitor and $I_{\text{C1 rms}} = 26$ mA, $I_{\text{C2 rms}} = 1.35$A, $I_{\text{C3,5 rms}} = 1.3$ A, $I_{\text{C4 rms}} = 0.7$ A.

F. Inductor Loss

The inductor losses consist of conduction losses and core losses.

The conduction losses formula is given as

$$P_{\text{Cond } L} = R_L \cdot I_{L \text{ rms}}^2 \quad (43)$$

where R_L is the parasitic resistance of inductors and $I_{L \text{ rms}}$ is the RMS currents flowing through inductors. By measuring $R_{L1,2} = 75$ mΩ and $I_{L1,2 \text{ rms}} = 2.5$ A which denote R_L and $I_{L \text{ rms}}$ of $L_{1,2}$, respectively, and measuring $R_{Lb1,2} = 119$ mΩ and $I_{Lb1,2 \text{ rms}} = 1.25$A that are related to $L_{b1,2}$, and substituting in (43) total conduction losses is calculated as follows:

$$\begin{aligned} P_{\text{Cond } L(\text{total})} &= P_{\text{Cond } L1} + P_{\text{Cond } L2} + P_{Lb1} + P_{Lb2} \\ &= 1.315 \text{ W}. \end{aligned} \quad (44)$$

The core loss is determined using the following formulas:

$$P_{\text{Core } L} = P_{cv} \cdot V_e. \quad (45)$$

In (45), P_{Core} represents the core loss, and P_{cv} and V_e represent the core loss volume density and the effective core volume, respectively. From (45), total core losses are computed as

$$P_{\text{Core(total)}} = P_{\text{Core } L1} + P_{\text{Core } L2} + P_{\text{Core } BT} = 0.584 \text{ W}. \quad (46)$$

To evaluate the overall efficiency of the converter, each component's losses are added together. So using (36), (38), (40)–(42), (44), and (46), the total losses of the proposed converter yield

$$\begin{aligned} P_{\text{Total Loss}} = P_{\text{Cond } S} + P_{\text{Switching}} + P_{\text{Cap Turn-on}} + P_{\text{Cond D}} \\ + P_{\text{ESR C}} + P_{\text{Cond } L} + P_{\text{Core(total)}} = 7.373 \text{ W}. \end{aligned} \quad (47)$$

According to the total losses computed in (47), the efficiency (η) of the proposed converter is calculated as follows:

$$\eta = 96.44\%. \quad (48)$$

Fig. 11 indicates the efficiency curve of the proposed converter at various loads and the power distribution at full load, respectively. It can be seen that the full load efficiency is 96.4%, and the maximum efficiency yields at 150 and 200 W, which is 96.4%. In addition, the power loss distribution pie diagram shows that BIT loss has a small portion in comparison to inductors. So, a high voltage gain with three degrees of freedom is achieved, while BIT does not affect the loss increment as much as inductors. It proves the authors' claim about moderate loss of magnetizing elements.

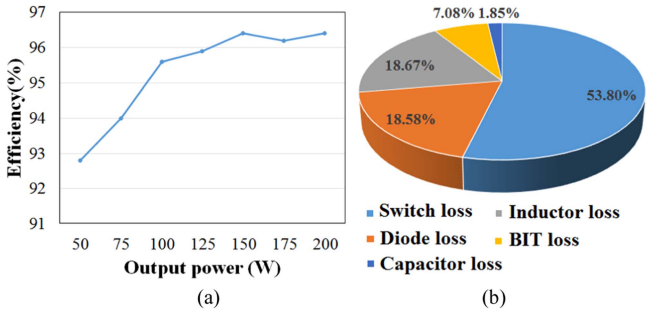

Fig. 11. Power loss analysis. (a) Efficiency curve versus output power. (b) Power loss distribution.

VII. Conclusion

This article proposes a high step-up dc–dc converter based on ASLs. It uses a BIT to increase the voltage gain. This converter achieves a high voltage gain even with the unity turn ratio of the transformer, while does not require a large duty cycle either. By this new topology, the voltage stress of switches decreases, and the use of the low-voltage switch with low conduction resistance is feasible. The leakage inductance of the BIT reduces the reverse recovery of diodes. An efficient passive clamp circuit with two diodes and two capacitors is used to cancel the voltage oscillation of switches caused by the mismatch of inductors. This clamp circuit not only limits the voltage spikes of switches, but also increases the voltage gain. From this article, it was found that using BIT is a more efficient way to raise the voltage ratio of ASL-based converters against employing CLs. The low number of elements and high efficiency are the other merits of the proposed converter. A 200 W prototype circuit was implemented and tested to convert 40 to 400 V. The experimental results verified the validity of the theoretical analysis. The maximum efficiency of 96.4% was achieved at full load condition, which is a good record in hard-switching converters.

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