Letters

Dynamic On-Resistance Characterization of GaN Power HEMTs Under Forward/Reverse Conduction Using Multigroup Double Pulse Test

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***Abstract*—In bridgeless power factor correction converters and inverters, GaN high-electron-mobility transistors (HEMTs) operate in both forward and reverse conduction modes, which may feature different dynamic ON-resistance (R_{ON}) behaviors. Despite the extensive study of dynamic R_{ON} under forward conduction, dynamic R_{ON} under reverse conduction still demands comprehensive evaluation. In this letter, the dynamic R_{ON} of two commercial p-GaN gate HEMTs with different technologies under forward/reverse conduction and hard/soft switching is characterized using the custom-designed multigroup double pulse test system, which nearly eliminates the accumulated self-heating effect in the device. First, the test was conducted at OFF-state bias voltage = 400 V, I_{DS} = 70% $I_{DS(max)}$. For the Schottky-type *p*-GaN gate HEMTs, the dynamic R_{ON} in reverse conduction is found to be more than 3%–5% higher compared to the forward conduction. However, for the hybrid-drain-embedded gate injection transistor, operating in reverse conduction mode leads to a slighter dynamic R_{ON} degradation effect, with a reduction of approximately 10% compared to the forward conduction. Next, I_{DS} was modulated to evaluate its impact on dynamic R_{ON}. For both devices, during reverse conduction it was observed that the dynamic R_{ON} initially decreases and subsequently increases with the I_{DS} increase.**

***Index Terms*—Dynamic ON-resistance, GaN high-electron-mobility transistors (HEMTs), multigroup double pulse test, reverse conduction.**

I. Introduction

OVER the past decade, due to GaN high-electron-mobility transistors' (HEMTs) unique advantages, such as low gate charge, low output capacitance, and no reverse recovery charge, it has been gradually used in consumer electronics, server power modules, and inverters [1]. However, there exists dynamic ON-resistance (R_{ON}) degradation issue in commercial GaN devices because of the electron trapping at the GaN buffer and AlGaN surface [2], [3].

In popular applications, such as bridgeless CCM or BCM (ZVS) boost power factor corrections (PFCs), the switches operate in the forward conduction and reverse conducting modes. The dynamic ON-resistance of GaN devices in forward conducting mode for hard and soft switching conditions has been extensively studied [4]. However, investigation and discussion on the degradation and behavior of dynamic R_{ON} in the reverse conduction is still rare.

A 230 s single pulse test of forward and reverse conduction modes was conducted after a 10 s full voltage stress bias for a 200 V GaN HEMTs in [5], and the reverse conduction mode induces a lower current collapse than forward conduction. However, due to the significant difference in dynamic R_{ON} changes of GaN devices under continuous pulses compared to single pulses [6], [7], the test results obtained in this article do not match the practical operating conditions. And, the forward and reverse R_{ON} of GaN HEMTs, which used the proposed trapezoidal current mode (TZCM) method, was evaluated in [8]; however, this work primarily focuses on utilizing the TZCM testing method to measure dynamic R_{ON} under constant current to enhance the testing accuracy. And it should be noted that in this circuit, the devices only operate in soft-switching mode. Therefore, it is difficult to evaluate the impact of hard-switching on the degradation of the HEMTs' dynamic R_{ON}.

An H-bridge derived circuit is presented in [9] for testing the dynamic resistance of GaN HEMTs. While this work evaluates the dynamic R_{ON} of the device in reverse conduction hard switching-OFF mode, it does not consider the soft switching-off mode of reverse conduction. Besides, this work focuses on low-voltage GaN devices and does not assess whether there are variations in dynamic R_{ON} performance in reverse conducting mode among different GaN devices, including Schottky-type p-GaN gate HEMTs and hybrid-drain-embedded gate injection transistor.

The traditional DPT may not accurately reflect actual operating conditions [10], [11]. And, the continuous pulses for dynamic R_{ON} testing leads to an increase in the junction temperature of GaN HEMTs. Consequently, the measurement results will be the combination of dynamic R_{ON} degradation effect and self-heating effect unless the junction temperature can be controlled accurately with a complex setup.

Thus, in this letter, the multigroups DPT methods [12] is adopted to evaluate the dynamic R_{ON} for avoiding self-heating effects. In contrast to previous studies on GaN device dynamic R_{ON} during reverse conduction, this letter evaluates dynamic R_{ON} in hard- and soft-switching-off conditions during reverse conduction and compares the dynamic R_{ON} during forward conduction on the same testing platform. And it analyzes how changes in I_{DS} during device conduction impact dynamic R_{ON} performance. Additionally, two types of the state-of-the-art commercial GaN devices are investigated, the key parameters of devices under test (DUTs) are presented in Table I.

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TABLE I
COMPARISON OF DEVICE UNDER TEST

Parameters	Device A	Device B
Voltage/Current Rating	600 V/12 A	650 V/15 A
Static R_{ON}	147 mΩ	100 mΩ
Gate metal/*p*-GaN contact	Ohmic contact	Schottky contact
Technology	HD-GIT	*p*-GaN Schottky gate

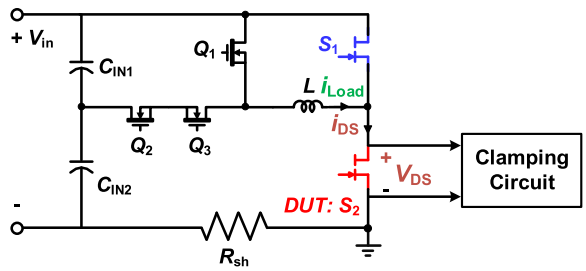

Fig. 1. Measurement circuit schematic, and the clamping circuit is analyzed in the next section.

TABLE II
COMPONENT LIST OF TEST CIRCUIT

Parameters	Value
Inductance (L)	20 μH – 400 μF
Capacitance (C_{IN1}, C_{IN2})	440 μF
S_1, S_2 (DUT)	Detailed in TABLE I
Q_1, Q_2, Q_3	IPW65R080CFD
Isolated Gate-driver	2EDF7235K

II. MEASUREMENT CIRCUIT AND METHODS FOR DYNAMIC R_{ON} UNDER DIFFERENT OPERATION MODES

A. Operating Description and Control Scheme of the Measurement Circuit

A simple and effective half-bridge configuration test circuit shown in Fig. 1 is proposed to evaluate the dynamic R_{ON} degradation of the E-mode GaN HEMTs under both forward and reverse operating modes including hard- and soft-switching conditions. The essential elements of the test circuit are detailed in Table II, and the photo of the test circuit is provided in Fig. 2.

Because dynamic R_{ON} degradation of the GaN power devices strongly relies on OFF-state stress, a set of stress switches composed of Q_1, Q_2, Q_3 is used in the circuit to control the time slots and magnitude of the OFF-state voltage stress. S_1 and S_2 form a half-bridge structure, and the operational principle of this component is akin to a synchronous rectifier buck circuit, with the task of enabling the DUT to operate in a specific mode (e.g. forward or reverse hard- and soft-switching mode). The current measurement is performed using a low inductance coaxial current shunt SSDN-10 from T&M Research Products, represented as R_{sh} in Fig. 1.

To illustrate the specific working method of the test circuit shown in Fig. 1, the hard switching-ON operation in the forward conduction mode is considered as an example. The timing diagram for this operation mode is depicted in Fig. 3(a).

Before t_0, Q_2 and Q_3 are kept in the ON-state to maintain the potential of OFF-state bias voltage of S_2 at half of V_{in}. From the perspective of controlling variables, the duration of this stage was uniformly set to 5 s in the experiment.

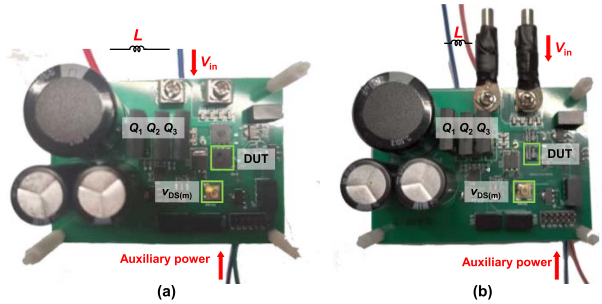

Fig. 2. Physical implementation of the proposed circuit. (a) Device A. (b) Device B.

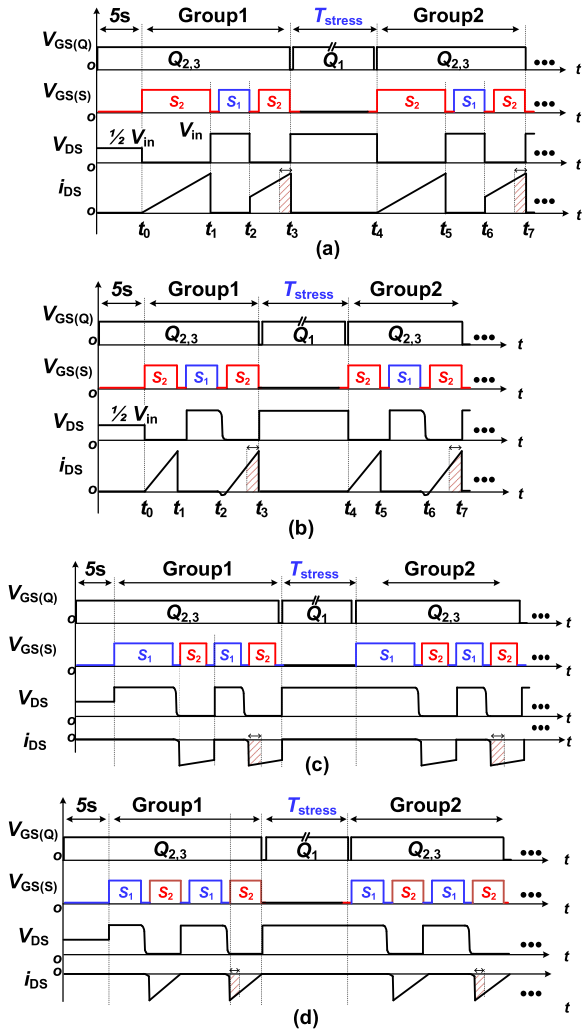

Fig. 3. Timing diagram of critical control signals to precisely control the OFF-state stress, and related voltage/current waveforms. (a) Forward hard switching ON. (b) Forward soft switching ON. (c) Reverse hard switching OFF. (d) Reverse soft switching OFF.

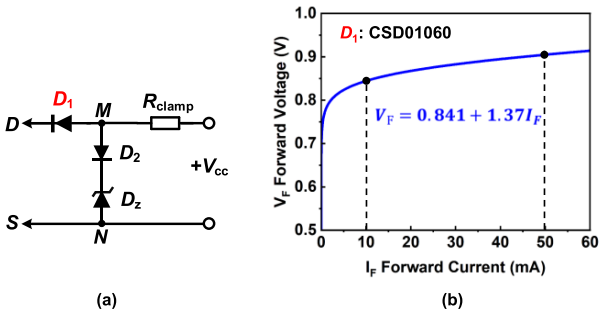

Fig. 4. (a) Clamping circuit for forward and reverse conduction mode R_{ON} testing. (b) V_{F}–I_{F} characteristics of D_1 at 25 °C, the fitted linear region is the interval with I_{F} greater than 10 mA but less than 50 mA.

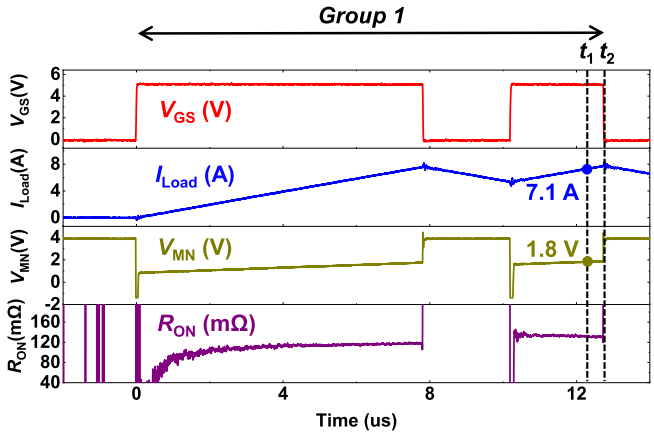

Fig. 5. Critical waveforms in the first group of DPT tests under the forward conduction hard switching mode. V_{GS} refers to gate pulse signal of DUT, I_{Load} refers to current of inductor, V_{MN} refer to voltage from *M* to *N* in Fig. 3(a).

From t_0 to t_3, the S_1 and S_2 switches are controlled to perform a dual pulse test (DPT), referred to as the "*Group1*" stage in Fig. 3(a), indicating the completion of the first group of tests. In the second pulse of DPT, the DUT conduction time is approximately 2 μs.

From t_3 to t_4, there is an interval between groups, allowing the device to fully dissipate heat. This process, represented as "T_{stress}" in Fig. 3(a), involves no switch action for S_1 and S_2. Q_2 and Q_3 are in OFF-state, while Q_1 is in ON-state. During this stage, the potential of V_{DUT} is maintained at V_{in}. In this experiment, this stage is set to 100 ms.

After time t_4, the next group of DPT is initiated, and the process from t_0 to t_4 is repeated. In this experiment, a total of 600 groups of DPT were conducted, resulting in a test duration exceeding 60 s. This approach allows for the measurement of the DUT's dynamic R_{ON} in a stable state.

Fig. 3(b) illustrates the switch waveform during forward soft switching, with the second pulse in each DPT achieving the soft switching-ON of the device. Additionally, Fig. 3(c) and (d) show switch waveforms during reverse hard and soft switching-OFF, respectively. These test pulse settings simulate key waveforms in the totem-pole PFC and inverter circuit during reverse operation.

B. Voltage Clamping Circuit and Dynamic $\mathrm{R_{ON}}$ *Extraction Method*

As depicted in Fig. 4(a), the voltage clamping circuit is designed to measure the V_{DS} of the DUT in both forward and reverse conduction mode. To prevent the conduction of diode D_{z} when the DUT operates in reverse conduction, a diode with a common cathode is connected in series in this branch to block the current flow. V_{MN} represents the sum of V_{DS} and the diode forward voltage V_{D1}. The B1505A semiconductor parameter analyzer measures the *I*–*V* characteristics of D_1 in Fig. 4(b). Since the current flowing through D_1 can be determined by *V*cc and R_{clamp}, its voltage can be calculated. Therefore, the V_{DS} of DUT can be accurately measured.

As depicted in Fig. 5, it illustrates the key waveforms (V_{GS}, I_{Load}, V_{MN}, and calculated R_{ON}) of the Device B during group 1 of multigroup DPT in forward conduction hard switching mode with OFF-state bias voltage = 400 V and I_{Load} = 6 A.

In data processing, we select the group's representative value by averaging data within a short time window around the peak current point, typically around 300 ns, between t_1 and t_2. This method is also used for data processing in other operating modes. In Fig. 3, the shaded area indicates the calculation range for dynamic R_{ON} near the peak current for each respective mode.

For the clamping circuit depicted in Fig. 4(a), there is a possibility of errors in the measurement of V_{DS} due to the presence of leakage current in the *MN* branch. This is because the current flowing through D_1 is no longer solely determined by the current passing through R_{clamp}. As a result, there may be some inaccuracies in the calculation of D_1 voltage. Therefore, the data at t_1 in Fig. 5 are taken as examples to analyze the potential magnitude of errors.

The Zener diode employed in this experiment is MMSZ6478. First, considering that the V_{MN} is 1.8 V, according to the *IV* curve of the Zener diode, it can be concluded that the current flowing through the *MN* branch, I_{MN}, is less than 50 μA. And the voltage of D_1 will experience a change depending on whether the leakage current I_{MN} is ignored or taken into account

$$V_{D1} = 0.841 + 1.37 I_{D1} \tag{1}$$

$$\Delta V_{D1} = 1.37\,\Delta I_{D1} = 1.37 I_{MN} < 68\,\mu\mathrm{V}. \tag{2}$$

According to R_{ON}'s calculation formula, we can determine whether to ignore the impact of I_{MN} on R_{ON}

$$R_{DS(\mathrm{on})} = \frac{V_{MN} - V_{D1}}{I_L} \tag{3}$$

$$\Delta R_{DS(\mathrm{on})} = \frac{\Delta V_{D1}}{I_L} < 11.5\,\mu\Omega. \tag{4}$$

$$\frac{\Delta R_{DS(\mathrm{on})}}{R_{DS(\mathrm{on})}} = \frac{\Delta V_{D1}}{V_{MN} - V_{D1}} < 0.001\%. \tag{5}$$

According to the above calculation, the impact caused by the leakage current of the *MN* branch is less than 0.001%, which is negligible. Therefore, it can be ignored in the experimental results, and it will not cause any significant errors.

III. Dynamic R_{ON}'s Experimental Results Under Four Operating Modes and Different I_{LOAD}

A. Testing Accuracy and Influencing Parameters

In order to verify the accuracy of the testing platform, the Si device without dynamic R_{ON} phenomenon was first tested. And this part of the work is detailed in our groups' previously published paper [4].

Meanwhile, considering the various factors that influence the dynamic R_{ON} of GaN devices, as delineated in [11], we maintained

TABLE III
PARAMETERS FOR EXPERIMENTATION

Parameters	Value
Stress Voltage	400 V
OFF-State Stress Time	5 s
Duty Cycle	50%
Total Pulses Numbers	1200
Total Testing Time	60 s
Gate Resistance	10 Ω
Gate Drive Voltage	Turn-ON: 5 V; turn-OFF: 0 V
Junction Temperature	25 ℃

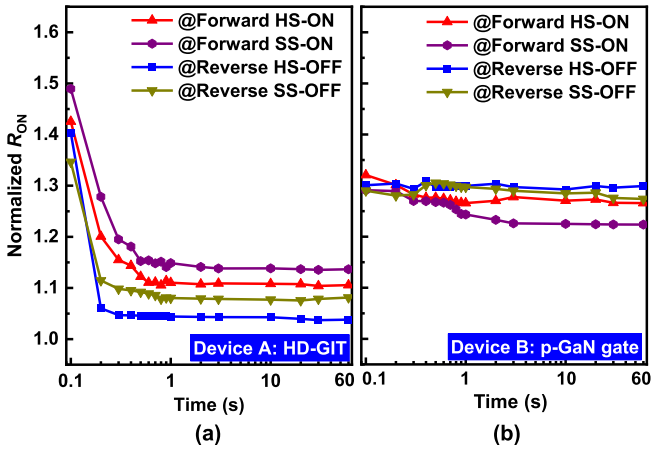

Fig. 6. Four operating modes' multigroup DPT results. (a) Device A (HD-GIT) at OFF-state bias voltage = 400 V, I_{load} = 8 A (70% $I_{D(max)}$). (b) Device B (p-GaN) at OFF-state bias voltage = 400 V, I_{load} = 10 A (70% $I_{D(max)}$).

consistent conditions across all test groups to guarantee the reliability of our results. A comprehensive list of these parameters and their respective controlled values can be found in Table III.

B. Experimental Results

As GaN devices' dynamic R_{ON} degradation is closely related to the load current (it shows a trend of increasing with the load current rises in forward hard switching conduction mode [13]), in this section, the test was initially conducted at 70% of the rated $I_{DS(max)}$ to establish a baseline measurement as shown in Fig. 6.

For Device A, the dynamic R_{ON} is significantly influenced by the prestressing stage, accounting for approximately 35% to 50% of the first segment (0.1 s) of the sequential pulse. However, once the sequential pulse exceeds 1 s, the dynamic R_{ON} in all operating modes decreases by over 30%. From that point onward, until the end of the whole pulse (60 s), the dynamic resistance exhibits minimal regenerative changes. For Device B, the dynamic R_{ON} shows a relatively consistent trend throughout the entire pulse sequence (cumulative 60 s), with the largest decrease (∼7%) observed in the forward soft switching mode. When analyzing the performance of dynamic R_{ON} in both forward and reverse conduction modes, Device A and Device B exhibit contrasting behaviors. Device A demonstrates a slighter dynamic R_{ON} degradation effect during reverse conduction compared to forward conduction, with a noticeable difference of approximately 10% observed at the 60 s. On the other hand, Device B shows a better recovery in dynamic R_{ON} during forward conduction compared to reverse conduction, with an advantage of approximately 3%–5% observed at the 60 s.

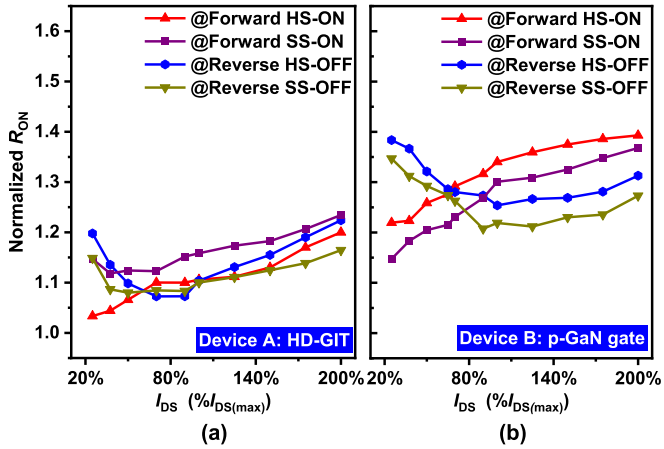

Fig. 7. Four operating modes' multigroup DPT results, at OFF-state bias voltage = 400 V, I_{load} varies within the range of 20%–200%. (a) Device A (p-GaN gate). (b) Device B (p-GaN gate).

Besides, the influence of drain current (I_{DS}) on the dynamic R_{ON} under four operating modes is characterized as shown in Fig. 7. The plotted data are extracted at the relatively stable stage (60 s after the prestress) to reveal the practical dynamic R_{ON} behavior. The two devices exhibit similar variation trends of dynamic R_{ON} with I_{DS}. Under the forward conduction mode, dynamic R_{ON} mainly increases with higher I_{DS}. Differently, under the reverse conduction mode, dynamic R_{ON} first decreases and then increases with higher I_{DS}.

IV. CONCLUSION

In this letter, the dynamic R_{ON} behaviors of two types of state-of-the-art commercial GaN devices are measured (HD-GIT and Schottky-type *p*-GaN) and compared under forward and reverse conducting conditions using multigroups double pulse testing methods.

Two different GaN devices show distinct dynamic R_{ON} behavior under multigroups DPT. The experimental results in Fig. 6 reveal that the dynamic R_{ON} in HD-GIT structured devices gradually recovers as pulse numbers increase, while the Schottky *p*-GaN gate device does not exhibit significant recovery.

Moreover, concerning the current scale, it is noticeable that when the device operates in reverse conduction mode, dynamic R_{ON} first decreases and then increases with an increase in I_{DS}, forming a "valley," as depicted in Fig. 7. Conversely, during forward conduction mode, there is a positive correlation with the increase in I_{DS}.

It is crucial to consider the significant difference in ON-resistance between forward and reverse hard switching operation modes. This difference can lead to inconsistent losses between the upper and lower switches of the bridge arm in a hard switching inverter circuit, as evidenced by the experimental results in Fig. 6, when Device A operates at 80% I_{DS}, the switch operating in forward mode experiences losses approximately 10% higher than that of the switch operating in reverse conduction mode. Such disparity may introduce potential thermal reliability concerns. Considering the dramatic increasing of GaN power HEMTs in PFC and inverter applications, it is important to take into account the dependence between dynamic R_{ON} and the conducting modes. By understanding the relationship between dynamic R_{ON} and the conduction mode, engineers may evaluate the conduction losses of GaN devices for different applications. And, the contradiction behaviors of the two types GaN HEMTs may help people to understand and investigate the performance and reliability of GaN HEMTs.

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